Record I_{on} (0.50 mA/μm at V_{DD} = 0.5 V and I_{off} = 100 nA/μm) 25 nm-Gate-Length ZrO_2/InAs/InAlAs MOSFETs

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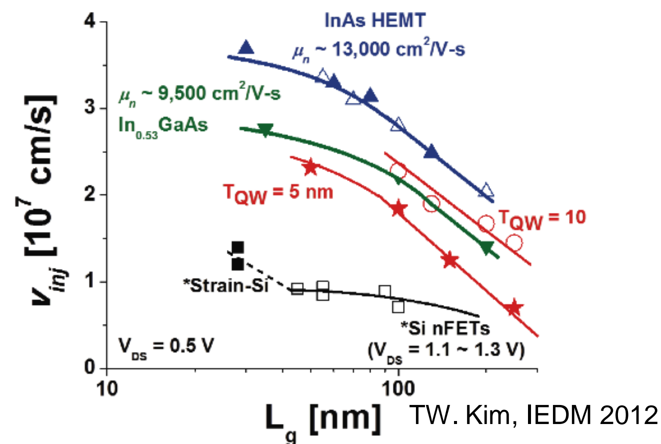
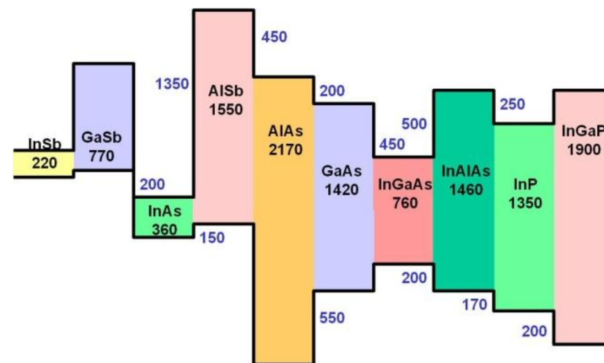
Why III-V MOSFETs in VLSI applications?

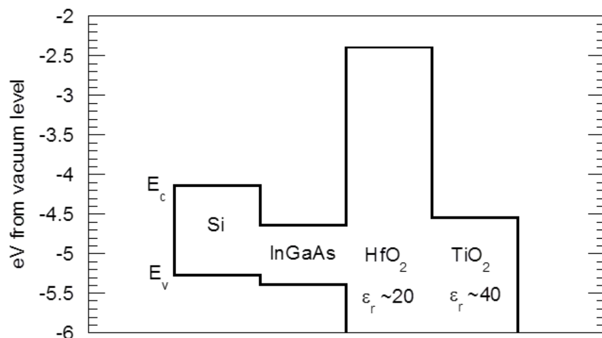
Low m* in III-V material ➔ high v_{inj}
➔ high transconductance

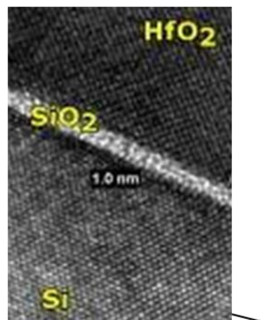


More transconductance per gate width
more current ➔ lower intrinsic delay
-or- reduced V_{DD} ➔ less power consumption
-or- small FETs ➔ reduced IC size

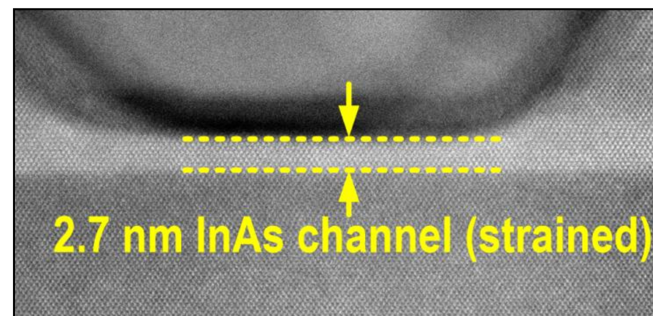


Other advantages
Wide range of available materials
nm-precise growth ➔ 1-2 nm thick channel
Larger ΔE_c ➔ Better confinement, Small EOT





http://nano.boisestate.edu/research-areas/gate-oxide-studies/



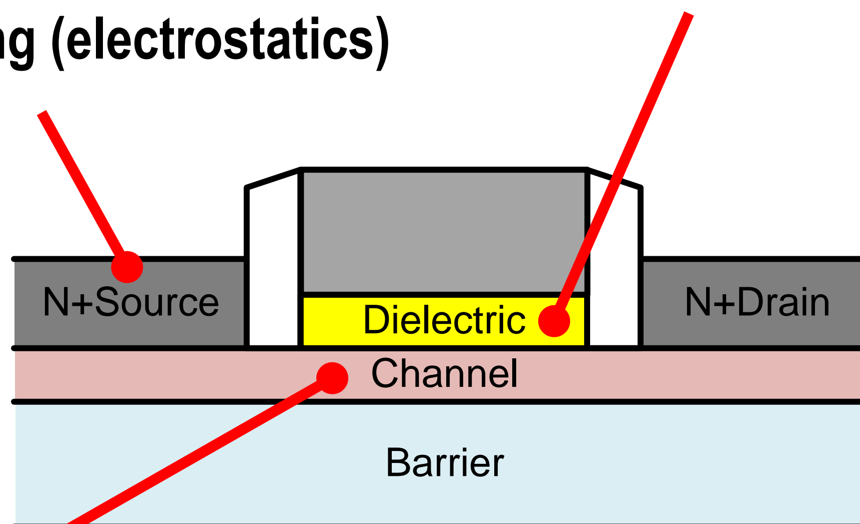
Key Design Considerations

Source/Drain:

- Low ρ_c ➔ Small contact size
- Self-aligned ➔ Small contact pitch
- Shallow ➔ Scaling (electrostatics)

Dielectric:

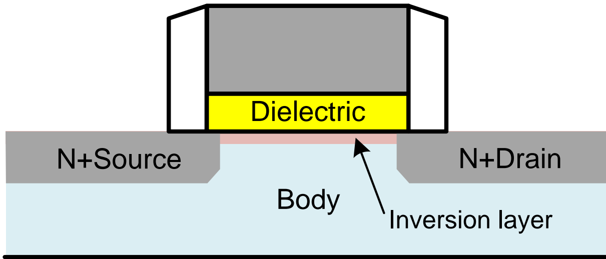
- Thin ➔ high I_{on}, better SS and DIBL
- Low D_{it} ➔ Better SS

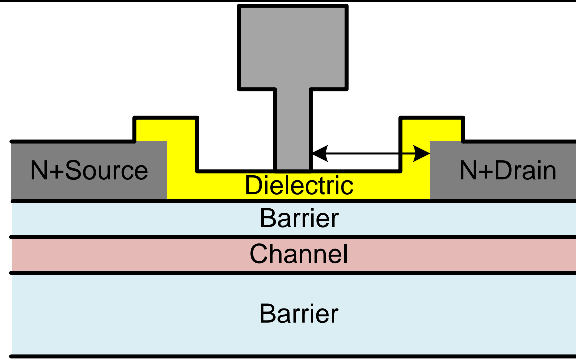


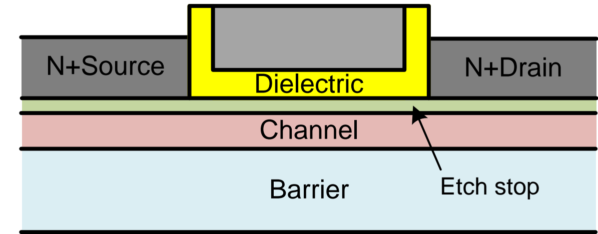
Channel:

- Thin ➔ Electrostatics
- Thin and wide bandgap ➔ Small band-band tunneling
- Thick and narrow bandgap ➔ higher injection velocity

FET Structures







Inversion mode MOSFETs

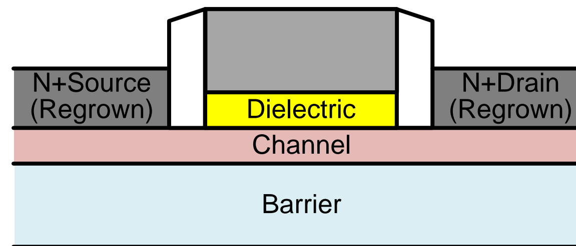
- Self-aligned ✓
- Implant damage ✗
- Large R_{access} (limited doping) ✗

MOS-HEMT

- Good short channel effect ✓
- Large device footprint ✗
- Large R_{access} (Barrier) ✗

Trench-etch

- Small footprint ✓
- Small R_{access} ✓
- Limited L_g scaling (wet etch) ✗



Regrown S/D with gate-first

Regrown S/D with gate-Last

- Small footprint and L_g ✓
- Small R_{access} ✓
- Abrupt junction ✓

- High damage (gate-stack etch) ✗

- Low damage (No dry etch) ✓

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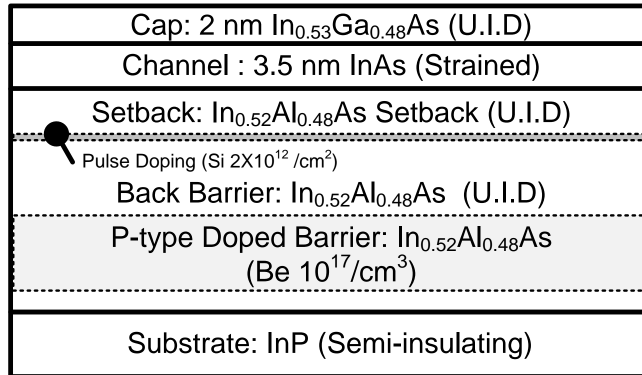
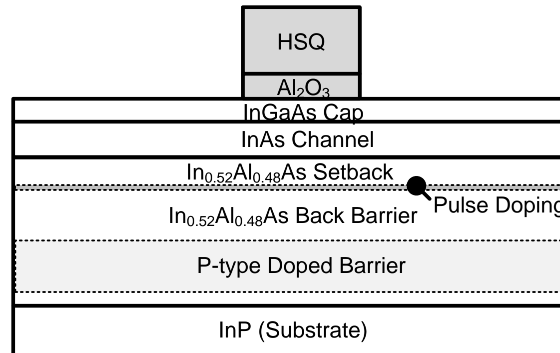
Gate-Last Process (Simplified for Development)

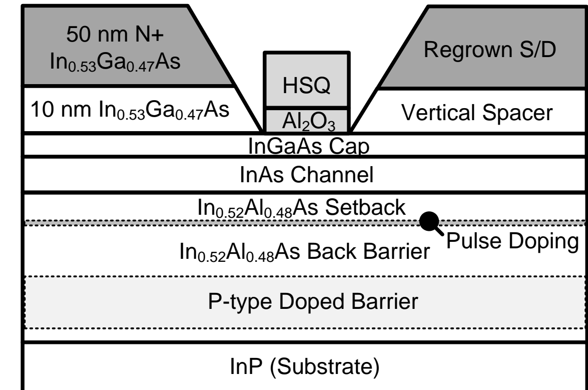
Channel growth By MBE



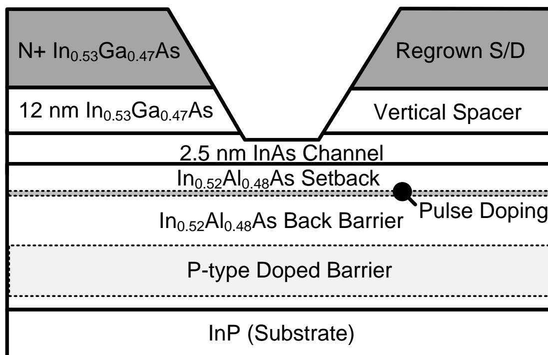
Dummy gate formation e-beam lithography



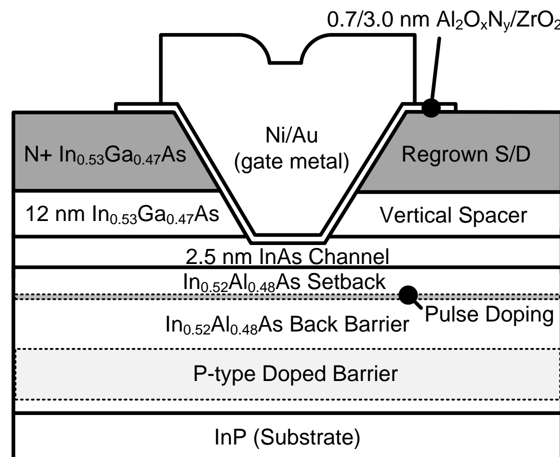
Vertical spacer and N+ S/D regrowth in MOCVD



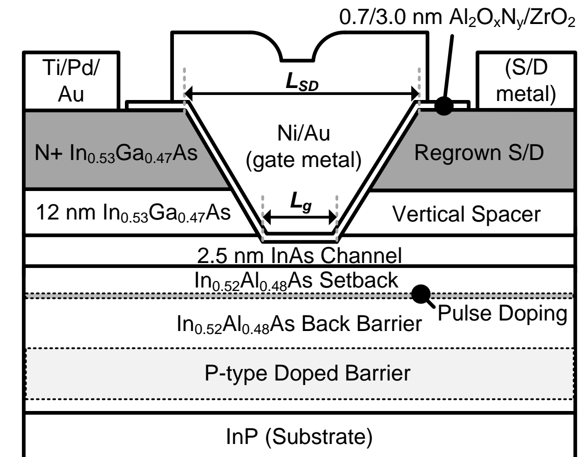
Mesa-isolation Surface digital etching



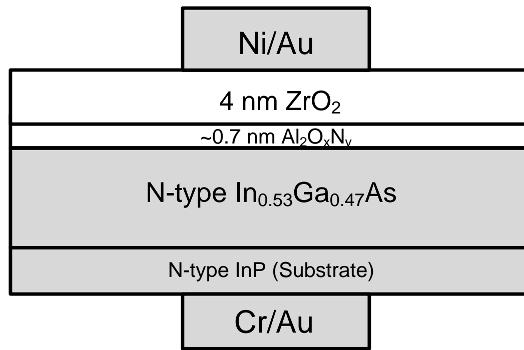
Gate stack formation



S/D metal contact formation

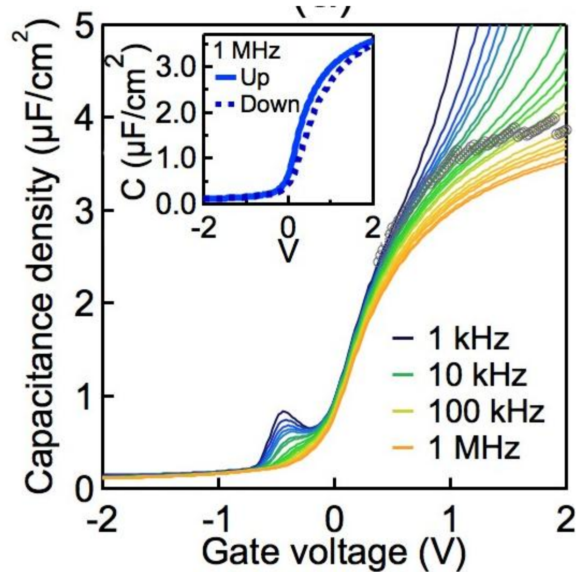


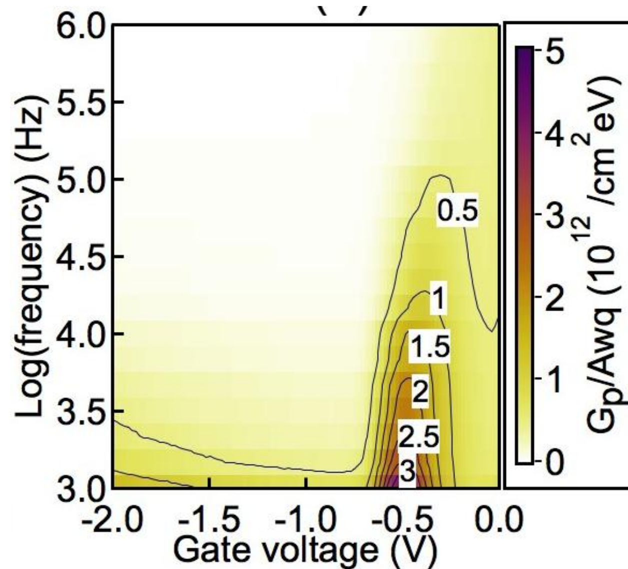
High-k : MOSCAP with 0.7/5.0 nm $Al_2O_xN_y/ZrO_2$

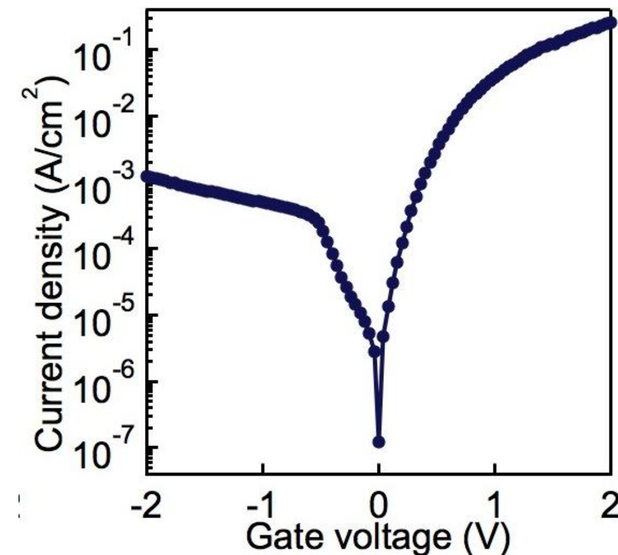


MOSCAP structure

- dielectric constant for ZrO_2 is 23; EOT is ~1 nm
- 3.5 $\mu F/cm^2$ accumulation capacitance at 1MHz
- ~$1X10^{12}$ $/cm^2$-eV D_{it} near midgap.
- Gate leakage < 1 A/cm^2 up V_G=2 V

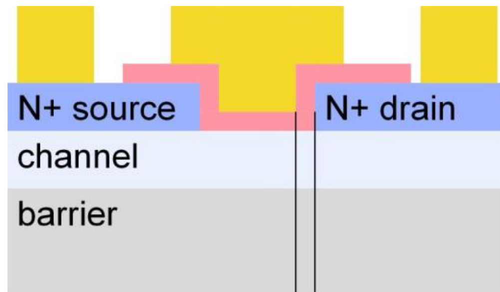


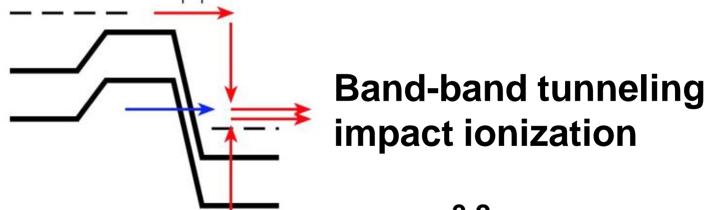


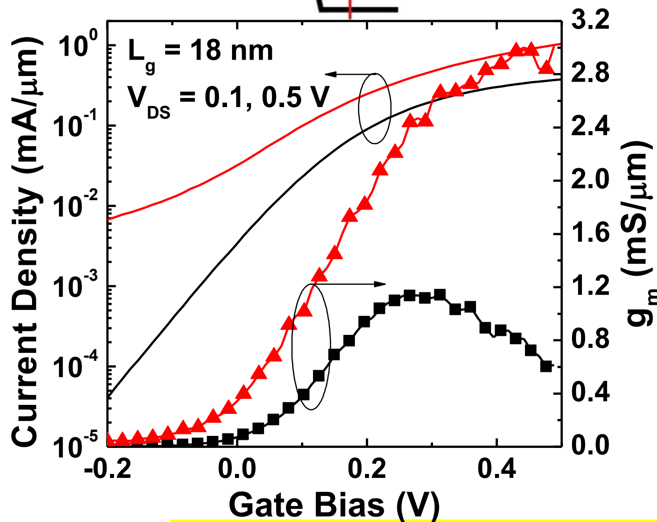


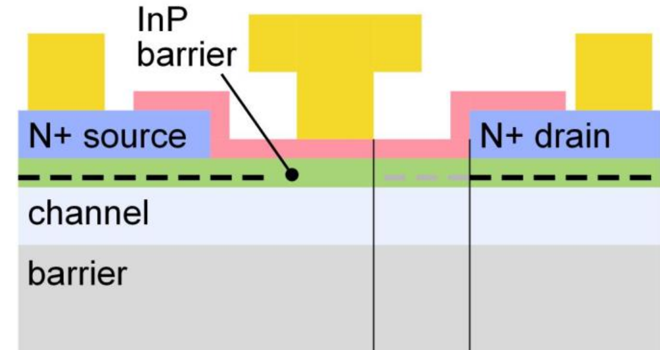
(V. Chobpattana, et al., ‘Scaled ZrO2 dielectrics for InGaAs gate stack with low interface trap densities’, APL 2014)

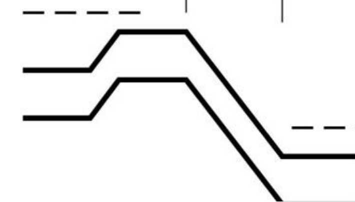
Off-state leakage and S/D spacers

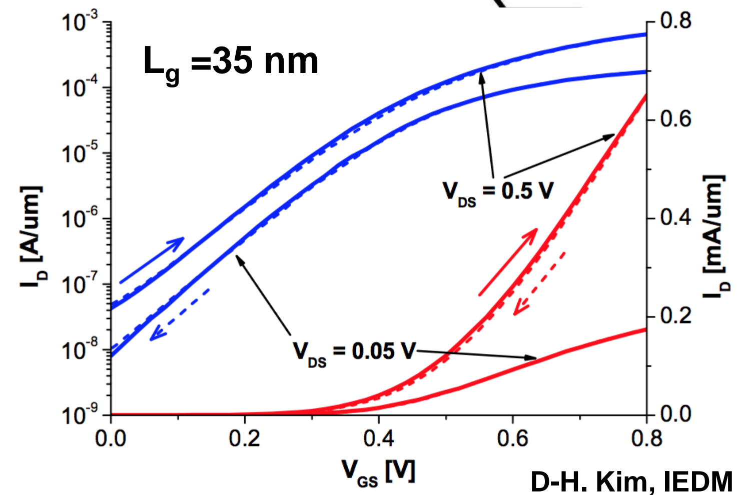








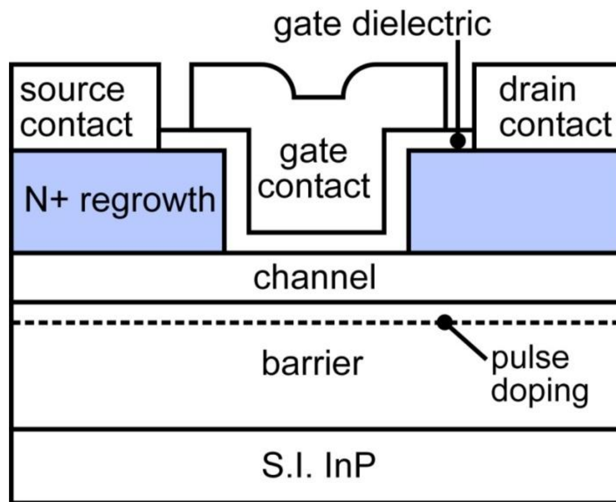


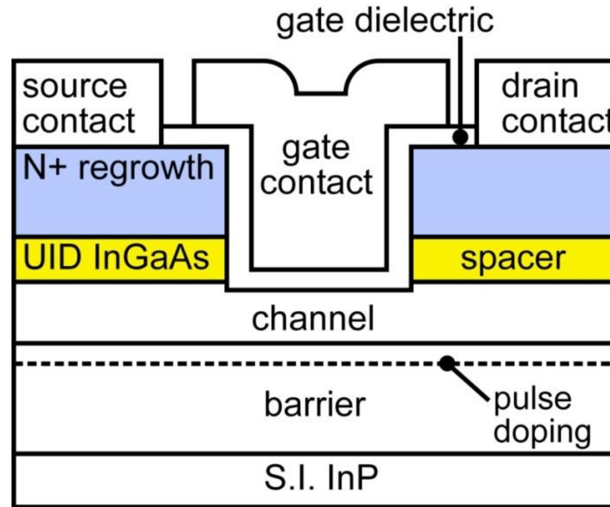


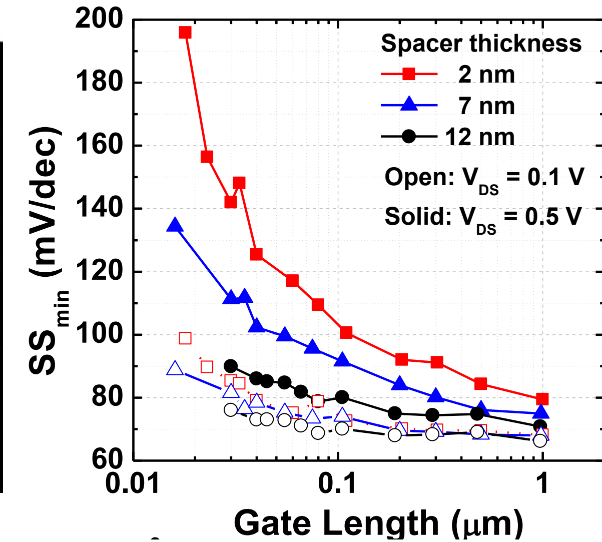
D-H. Kim, IEDM 2012

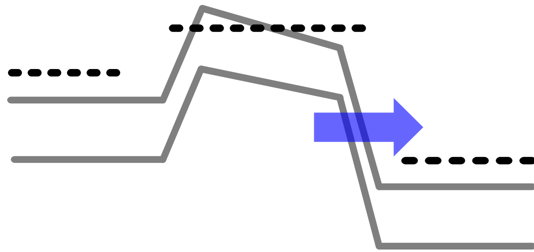
Large lateral spacer → low leakage, good short channel immunity
Large lateral spacer → large S/D pitch

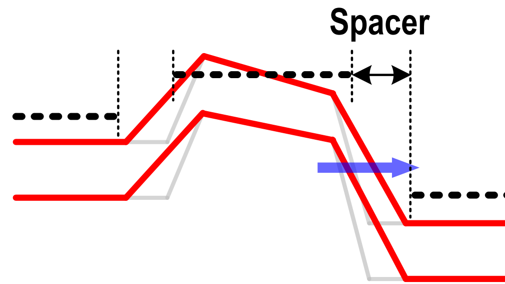
Vertical Spacers → reduced off-state leakage

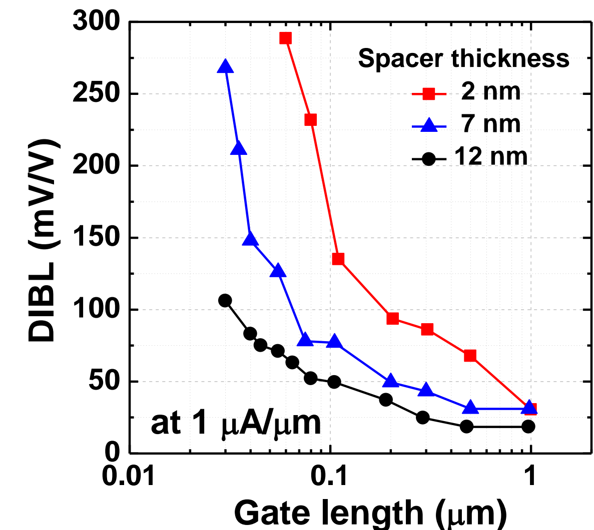








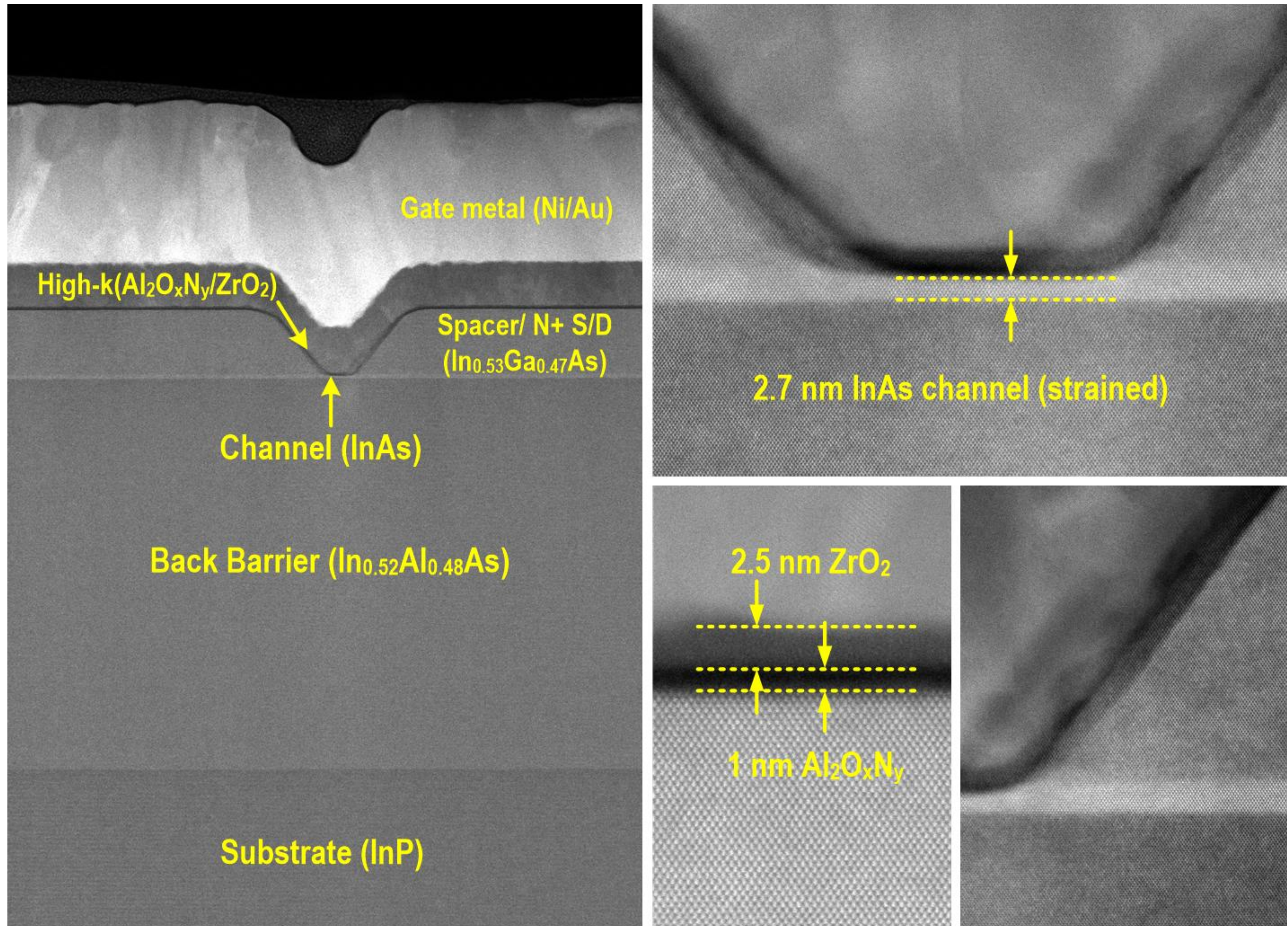




- **Larger spacer**
  → **better short channel effect at short and long channels**

(S. Lee, et al., EDL, June 2014)

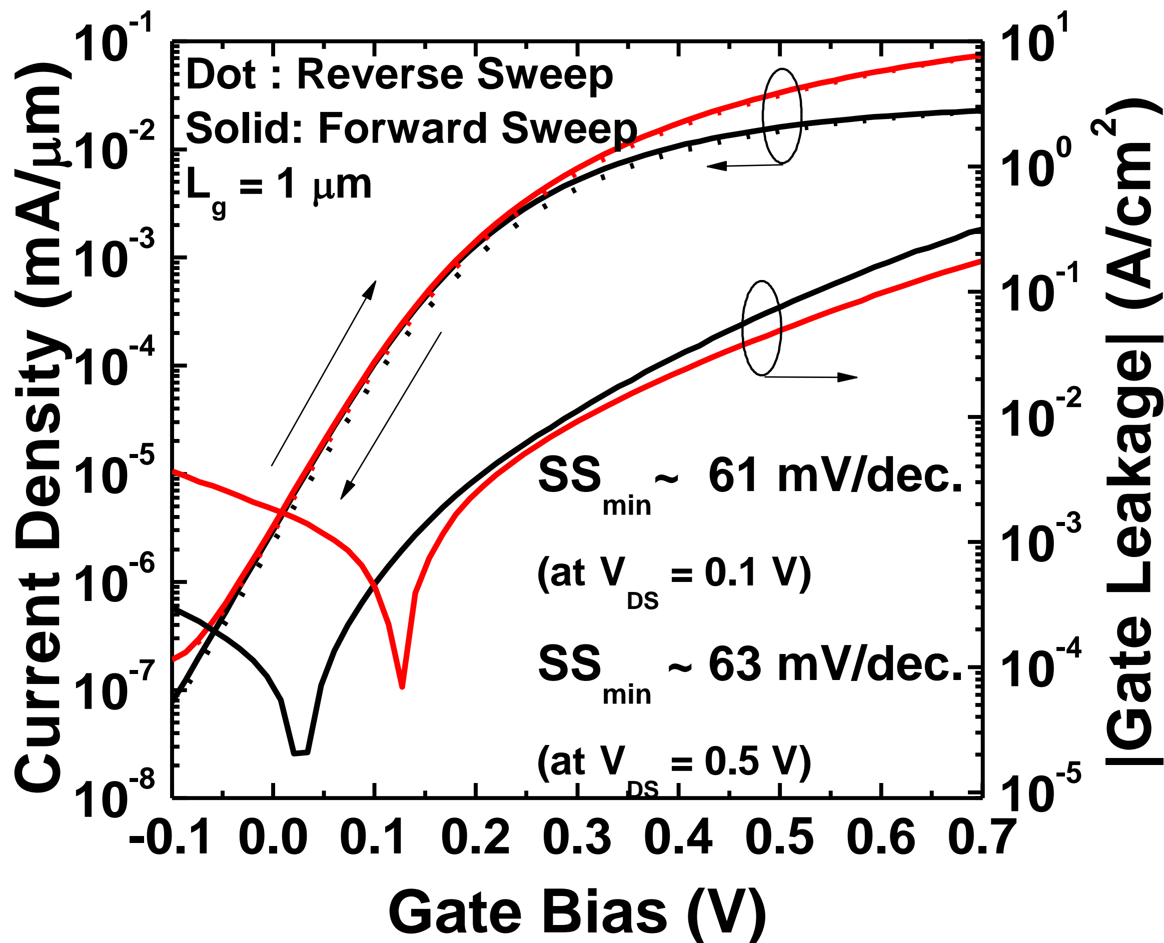
Cross-sectional STEM image



Courtesy of S. Kraemer (UCSB)

*Heavy elements look brighter

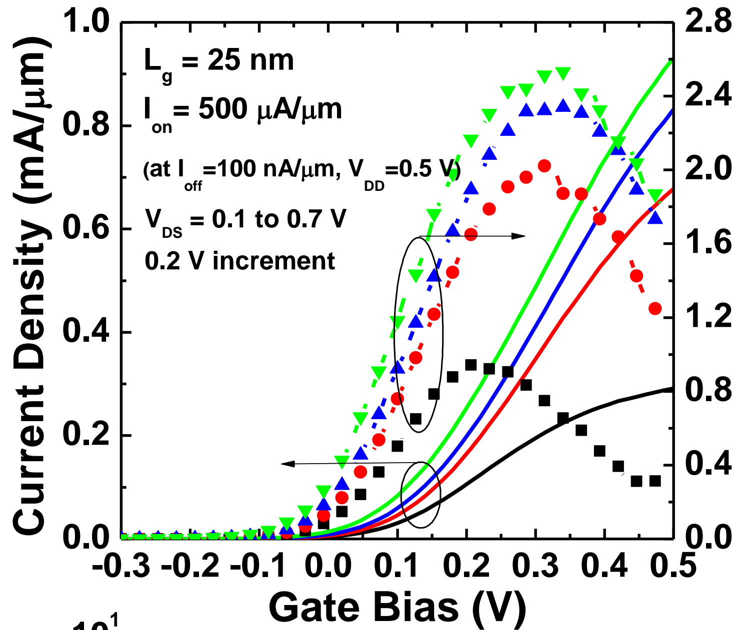
I-V characteristics for long channel device (L_g = 1 μm)

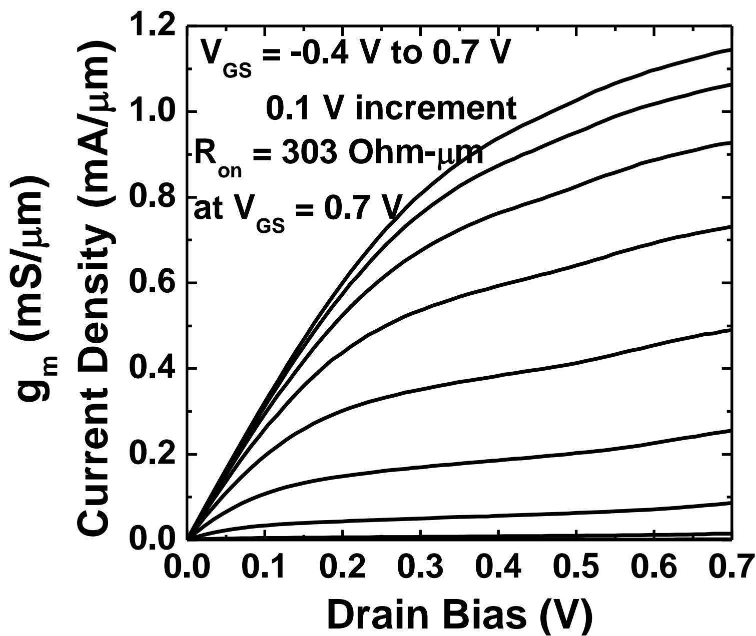


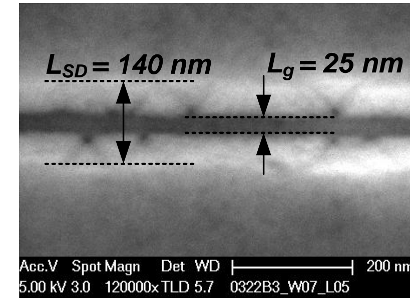
- 61 mV/dec Subthreshold swing at V_{DS}=0.1 V
- Negligible hysteresis
- <1 A/cm^2 gate leakage at measured bias range

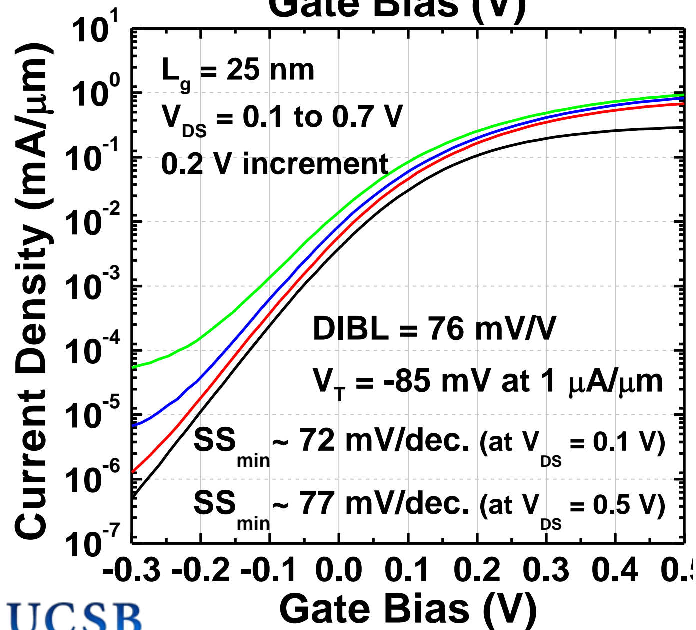
UCSB

I-V characteristics for short channel devices (L_g = 25 nm)



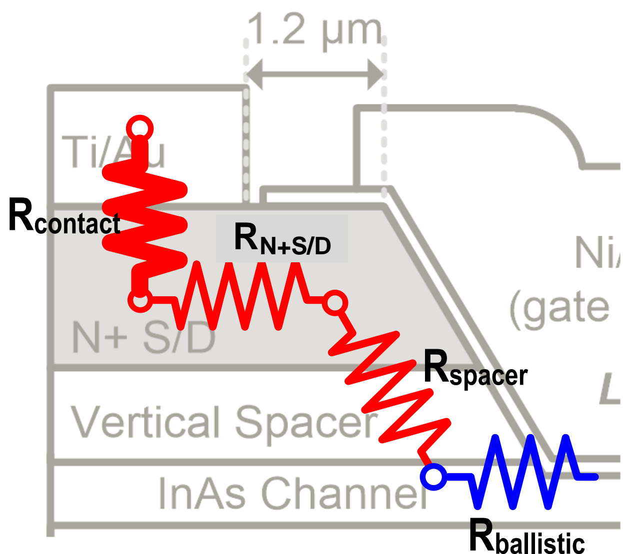


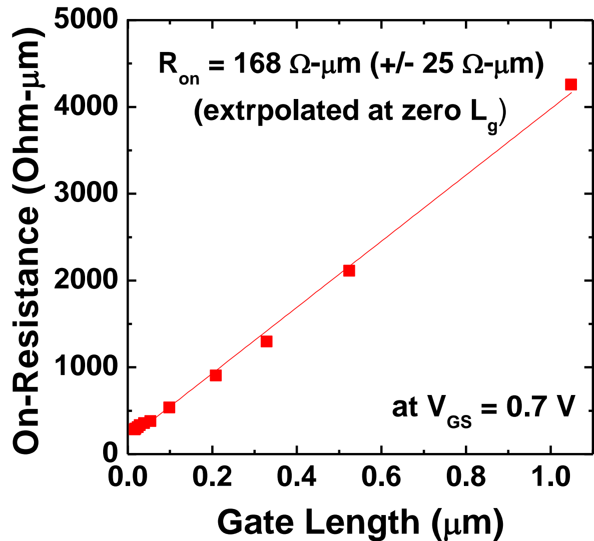


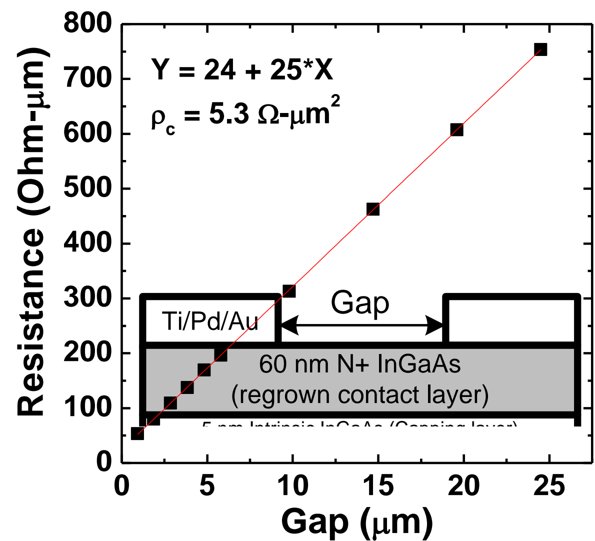


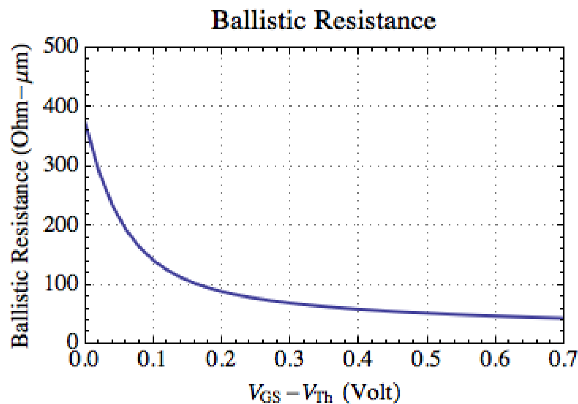
- ~2.4 mS/μm Peak g_m at V_{DS}=0.5 V
- ~300 Ohm-μm on-resistance at V_{GS}=0.7 V
- 77 mV/dec Subthreshold Swing at V_{DS}=0.5 V, 76 mV/V DIBL at 1 μA/μm
- 0.5 mA/μm I_{on} at I_{off}=100 nA/μm and V_{DD}=0.5 V

Source/drain series resistance







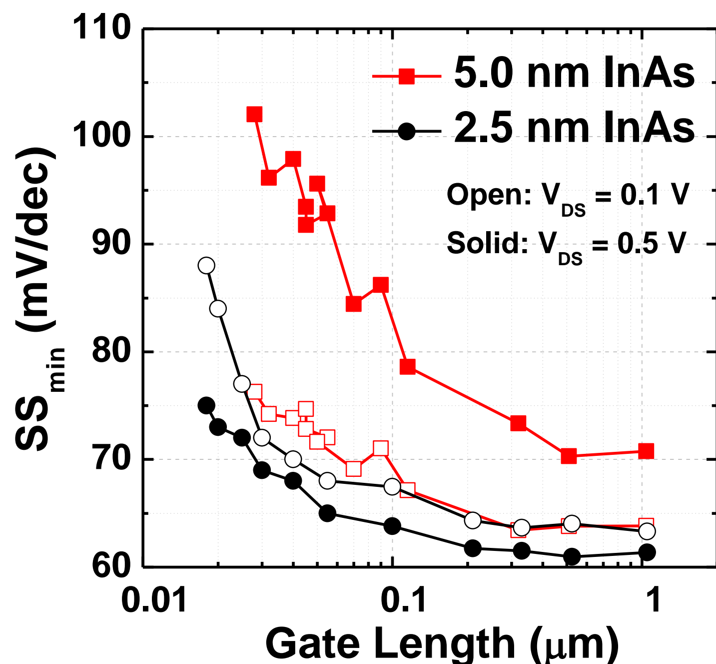


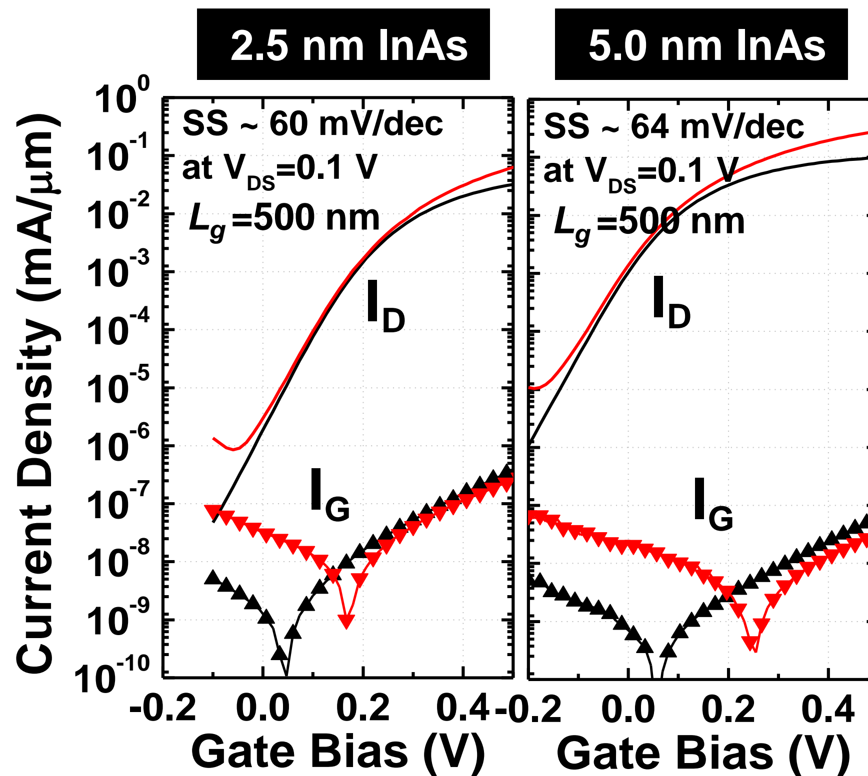
$R_{contact}$ [Ohm-µm]	$R_{N+ S/D}$ [Ohm-µm]	R_{spacer} [Ohm-µm]	$R_{ballistic}$ [Ohm-µm]	R_{on} at zero L_g[Ohm-µm]
25	60	35	50	170

for both source and drain sides

- **From TLM measurement for N+S/D, $R_{N+S/D\ sheet}$ = 25 ohm/sq, ρ_c= ~5.3 ohm-µm²**
- **R_{spacer} is estimated to be ~35 ohm-µm for both sides**

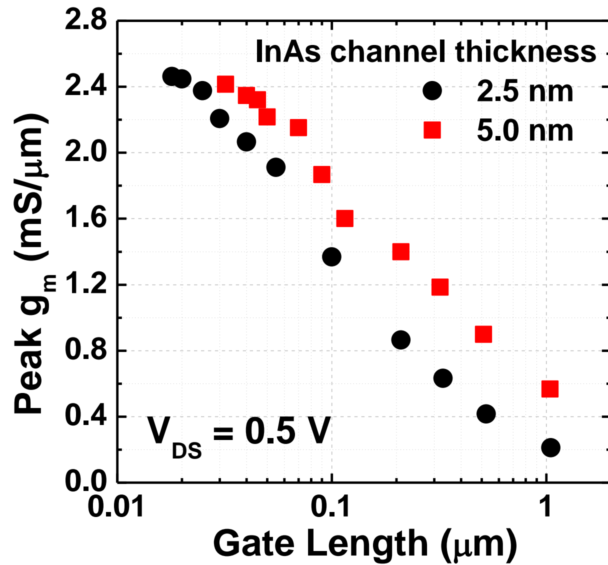
Performance comparison: 2.5 nm VS 5.0 nm-thick channel

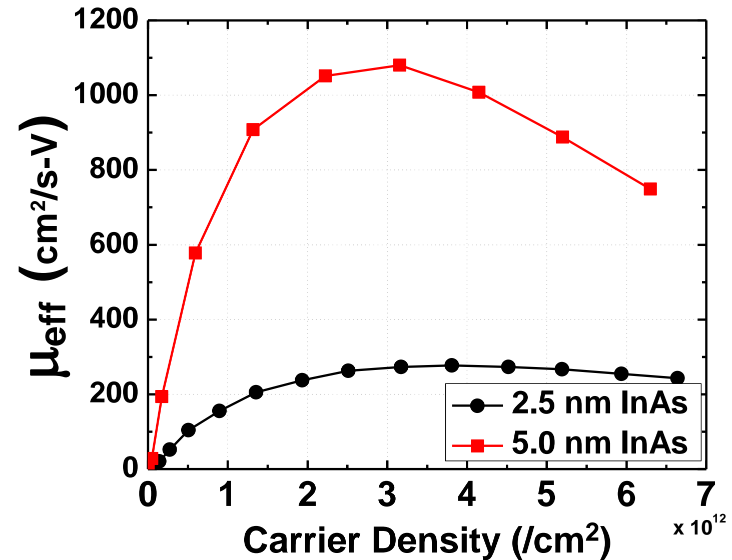


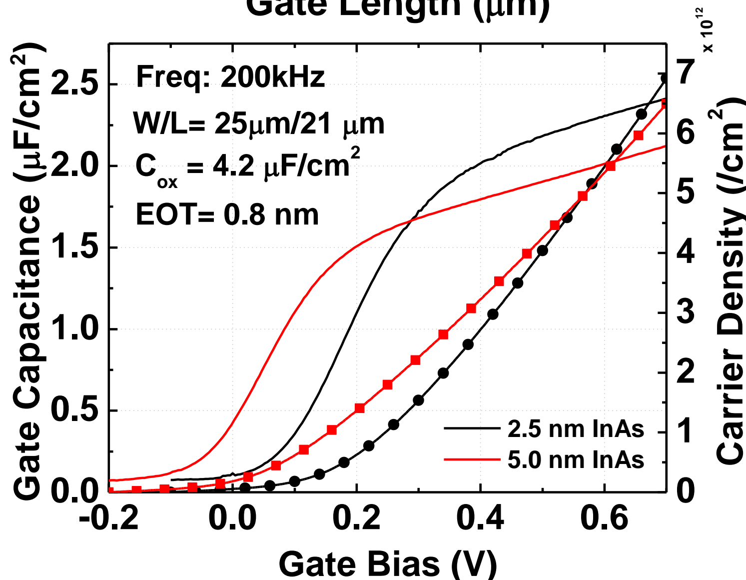


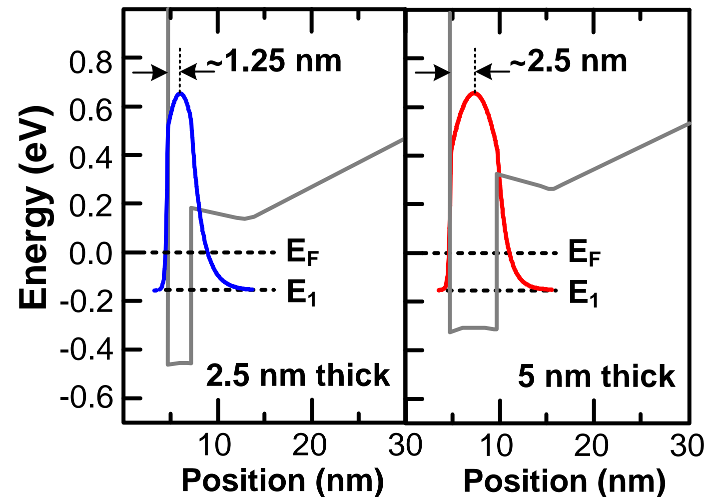
- Better SS at all gate length scale:
  🡐 Better electrostatics, reduced BTBT
- ~1:10 reduction in minimum off-state leakage
- ~5:1 increase in gate leakage 🡐 increased eigenstate

Performance comparison: 2.5 nm VS 5.0 nm-thick channel



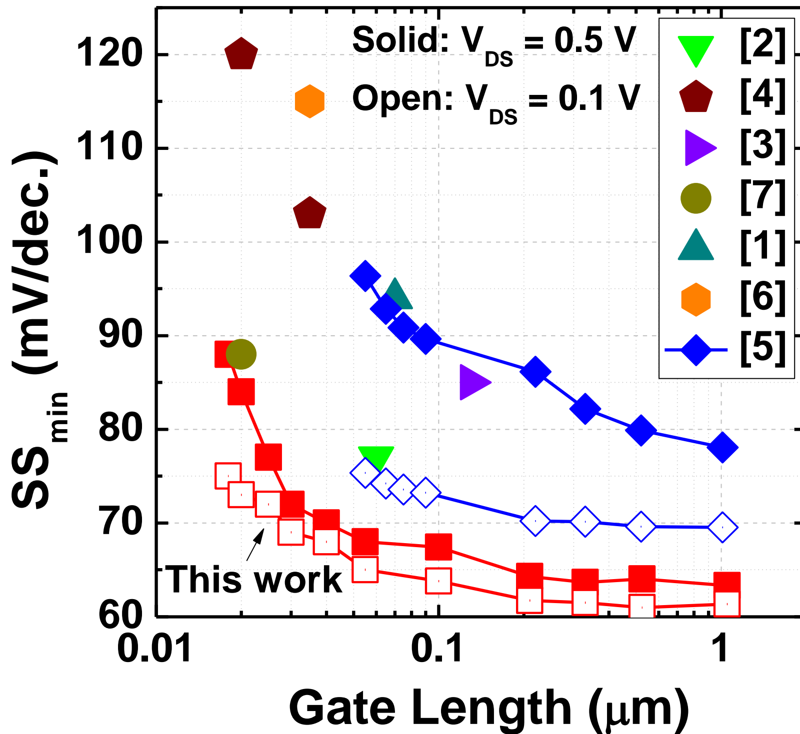


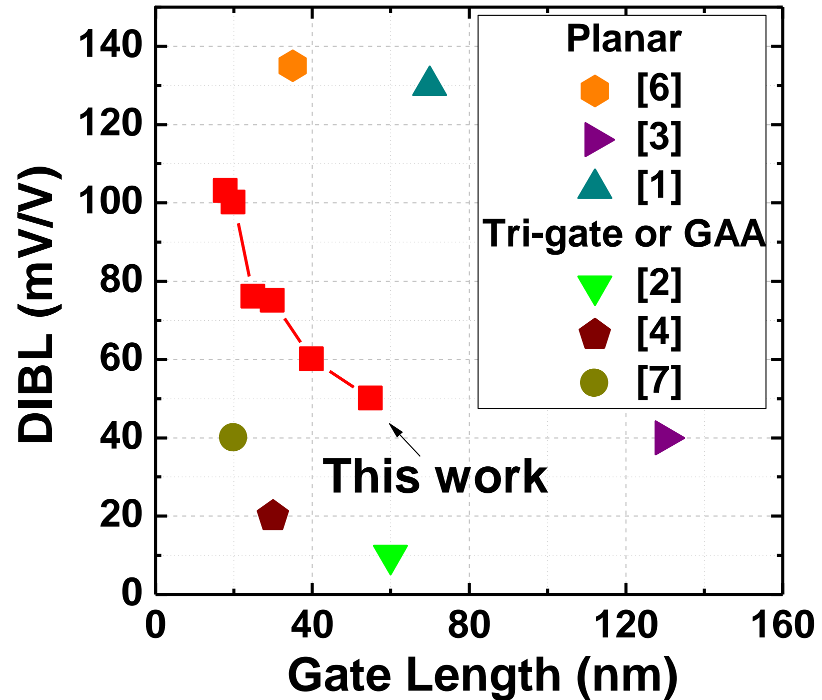




1D-Possion Schrodinger solver
(coded by W. Frensley, UT Dallas)

SS and DIBL vs. L_g (Benchmarking)

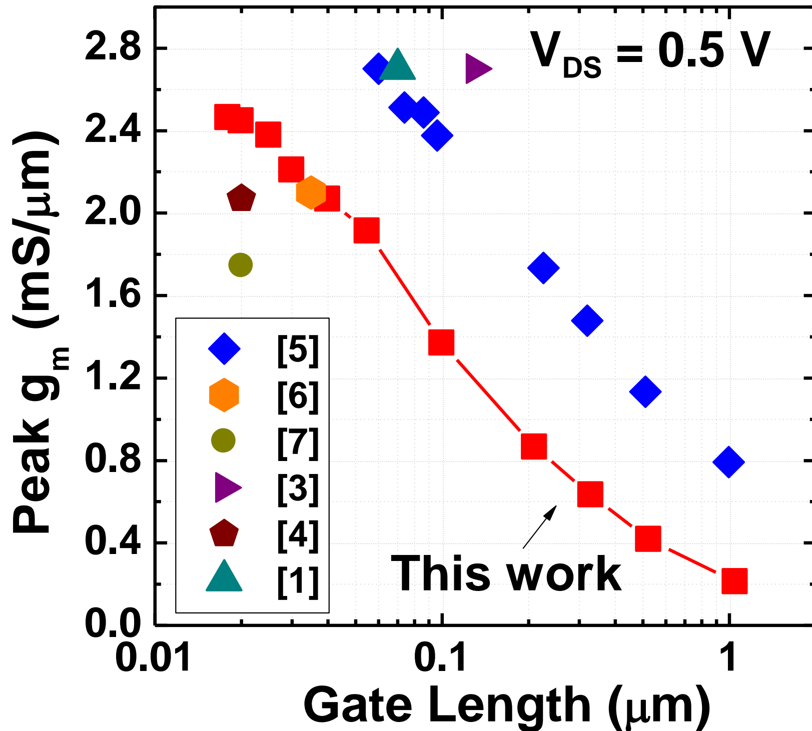


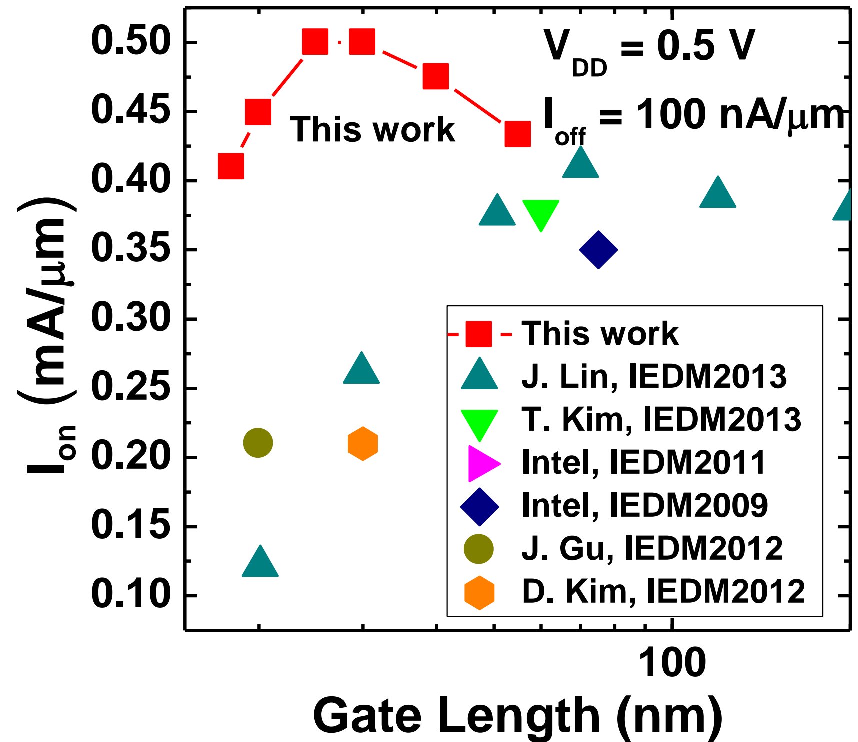


[1] Lin IEDM 2013,[2] T.-W. Kim IEDM 2013,[3] Chang IEDM 2013,[4] Kim IEDM 2013
[5] Lee APL 2013 (UCSB), [6] D. H. Kim IEDM 2012,[7] Gu IEDM 2012,[8] Radosavljevic IEDM 2009

- <80 mV/dec at sub-30 nm L_g and V_{DS}=0.5 V
- Record low subtheshold swing among any reported III-V FETs.
- Lowest DIBL among planar-type III-V FETs.

Peak g_m and I_{on} at fixed I_{off} vs. L_g (Benchmarking)





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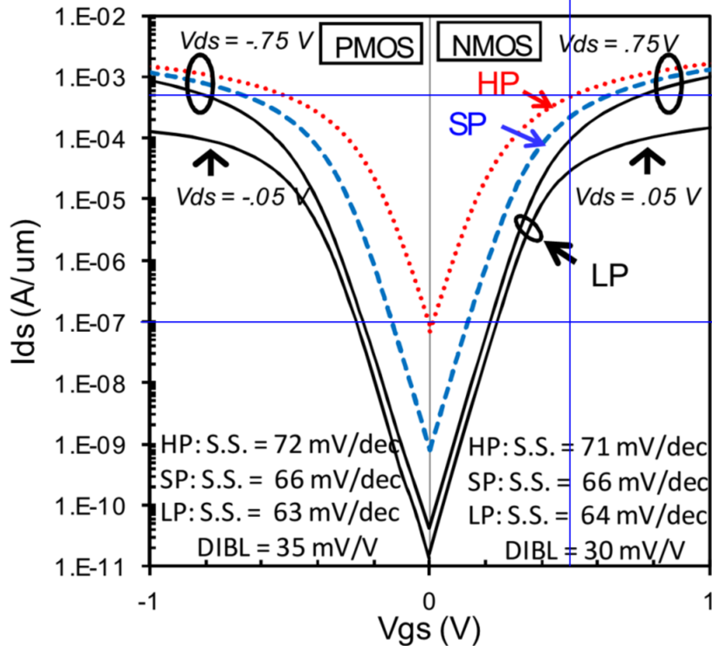
[5] Lee APL 2013 (UCSB), [6] D. H. Kim IEDM 2012,[7] Gu IEDM 2012,[8] Radosavljevic IEDM 2009

- >2.4 mS/μm peak g_m at V_{DS}=0.5 V and sub-30 nm L_g.
- Highest I_{on} at I_{off}=100 nA/μm and V_{DD}=0.5 V
- 0.5 mA/μm I_{on} at sub-30 nm L_g

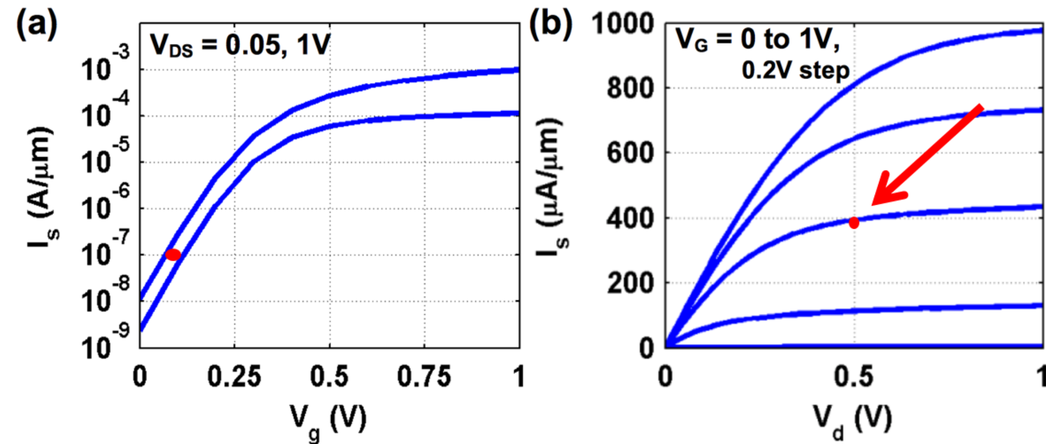
Benchmark with 22 nm node Si Fin- and nanowire FET

Intel 22 nm Si FinFET



Jan, IEDM 2012

IBM 22 nm nanowire FET



S. Bangsaruntip et al., IEDM 2013

- Intel 22 nm FinFETs (HP) : ~0.5 mA/μm (?) @ V_{GS}=0.5 V, V_{DS}=0.75 V
- IBM 22 nm nanowire : ~0.4 mA/μm @ V_{GS}=0.5 V, V_{DS}=0.5 V
- Comparable performance with state-of-the-art Si-FinFETs (nanowire).

Conclusion

- Developed vertical spacer to reduce off-state leakage and to improve short channel effect.
- Integrated sub-1 nm EOT ZrO_2 high-k with low D_{it}
- Obtained 61 mV/dec at V_{DS} =0.1 V and 1 μm-L_g.
- Obtained 0.5 mA/μm at I_{off} =100 nA/μm and V_{DD} =0.5 V (best reported I_{on} among any reported III-V MOSFETs)
- Achieved comparable I_{on} to state-of-art multi-gate Si-FETs

Acknowledgment

Thanks for your attention!
Questions?

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