Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp658-659

High Performance III-V MOS Technologies.

M. J. W. Rodwell[1], S. Lee[1], C.-Y. Huang[1] , D. Elias[1] , V. Chobpattana[2], B. J. Thibeault[1], W. Mitchell[1], S. Stemmer[2], A. C. Gossard[2]

[1]ECE Department, [2]Materials Department, University of California, Santa Barbara, CA 93106 USA,

Abstract

We review recent development of In(Ga)As-channel MOSFETs. Planar UTB devices with raised regrown source and drain scale readily to sub-20nmgate lengths. Low-effective mass InAs and InGaAs channels, combined with thin gate dielectrics, provide high transconductance, but off-state leakage can be high due to band-band and source-drain tunneling currents. Leakage is reduced through thin 2.5-3nmchannels, and through InGaAs or wide-bandgap InP vertical field spacers in the regrown S/D. Growing the FET channel by atomic layer epitaxy on the sidewall of a sacrificial ridged template will enable InGaAs/InAs finFETs of few-nm channel thicknesses.

Overview

InAs and InGaAs have been recently and extensively studied for potential application in VLSI [1]-[9]. Interest is motivated by the high mobilities and high carrier injection velocities associated with these materials, parameters providing high transconductance and consequently the potential for high on-currents at low power supply voltages. Yet, impact ionization, band-band tunneling, and source/drain (S/D) tunneling leakage currents can be high because of low bandgaps and low electron effective mass; until recently [10], I_{on} (at specified low I_{off} and V_{DD}), had not approached or surpassed Si.

If III-V MOSFETs are to supplant silicon MOSFETs in VLSI, their leakage currents will have to be greatly reduced, to levels varying from 100nA/μm for high-performance (HP) logic to 30pA/μm for low-power (LP) logic. Such low leakage currents must be obtained at device dimensions consistent with the next few scaling generations of VLSI; implying gate lengths approach 7-15nm and source/drain contact pitches approaching 20-40nm. Given such tight dimension, reduction of leakage through use of large lateral gate-drain spacers has little relevance to VLSI.

Here we describe device designs for low-leakage III-V MOSFETs. In addition to benefiting FET electrostatics, extreme thinning the epitaxial InAs or InGaAs channel to 2-3nm increases the channel quantized bandgap, thereby also decreasing off-state leakage arising from BTBT. Inserting undoped vertical spacers within the raised regrowth source/drain (S/D) reduces the otherwise extreme electric field in the gate-drain region, reducing band-to-band tunneling (BTBT) leakage currents. InP, with its wider bandgap, is less prone to BTBT, but, with its higher electron effective mass, its extensive use within the FET channel will decrease the transconductance and on-current; by judicious insertion of InP only in the regions of highest field concentration, leakage can be greatly reduced while minimizing the sacrifice in on-current.

III-V MOSFET scaling limitations extend beyond leakage currents. Because of the low effective mass, collapse of mobility from surface roughness scattering in nm-thick channels is a more serious challenge with In(Ga)As than with Si. FinFETs, necessary for scaling to very small L_g, demand very thin bodies of precisely-controlled thickness, yet III-V materials are prone to extreme damage when dry-etched. By forming the III-V fin by atomic-layer epitaxial growth on the sidewall of a sacrificial ridged growth template, high-damage dry-etch processes are avoided, and fin thicknesses can be controlled by the number of ALE growth cycles.

Results

Figure 1 shows a schematic cross-section of a recent device, and Figure 2 a TEM cross-section of the channel. The FET has a 2.5-2.7nm thick InAs channel, a 1.0nm Al_2O_3/2.5nm ZrO_2 gate dielectric [11] and 12nm undoped InGaAs vertical spacers in the raised regrown S/D. Transconductance (Figure 3) is high because of low InAs effective mass and thin channel and dielectric; off-state leakage is moderately low (Figure 4) because of the vertical spacers and the strong quantization in the thin channel. Long-channel FETs show 61 mV/dec. subthreshold swing *S.S.*(Figure 6) , on-current at 500mV V_{DD} and 100nA/μm I_{off} (Figure 7) is 0.5mA/μm, comparable to, or surpassing, leading [12]-[13] Si fin- and nanowire FETs.

Because of residual BTBT at negative V_{gs}, off-current (Figure 4) in the FETs of Figure 1 meets the HP but not GP/LP/UPL ITRS requirements. Inserting (Figure 8) [14] raised-plus-recessed InP S/D spacers reduces off-current (Figure 9) more than 10:1 at a given (V_{gs}-V_{th}); our current efforts seek to minimize the sacrifice in on-current through use of InP only in the regions of greatest electric field.

Figure 10 illustrates finFET fabrication by atomic layer epitaxy [15], while Figure 11 is a TEM cross section of a 180nm height, 8nm thick InGaAs fin formed by this process.

References

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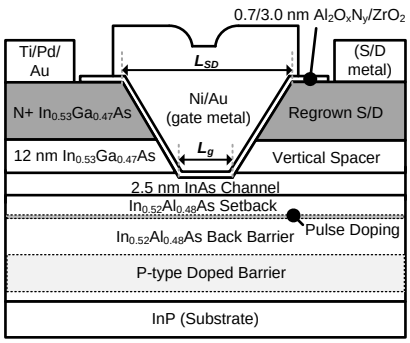

Figure 1: Schematic cross-section of III-V MOSFET with 2.5 nm InAs channel.

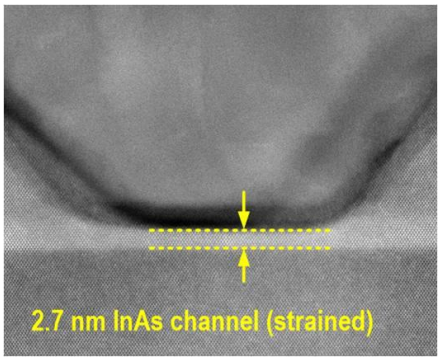

Figure 2: TEM cross-section of InAs MOSFET with 2.7nmInAs channel.

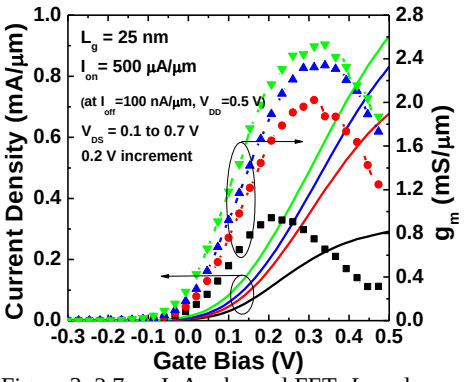

Figure 3: 2.7nm InAs channel FET: I_D and g_m, versus V_{GS}, at 25 nm L_g.

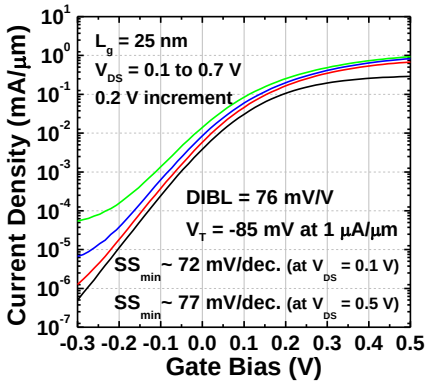

Figure 4: 2.7nm InAs channel FET: subthreshold characteristics at 25 nm L_g.

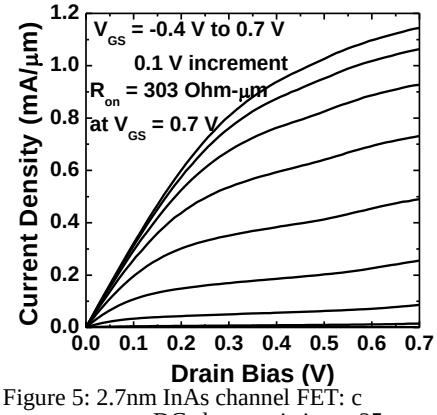

Figure 5: 2.7nm InAs channel FET: c ommon-source DC characteristics at 25 nm L_a.

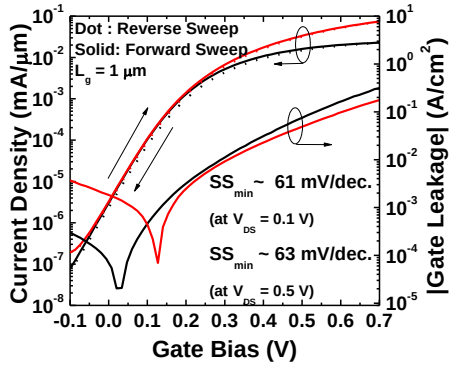

Figure 6: 2.7nm InAs channel FET: log(I_D) and log(I_G) versus V_{GS}, at 1µm L_g, at V_{DS} = 0.1 V and 0.5 V.

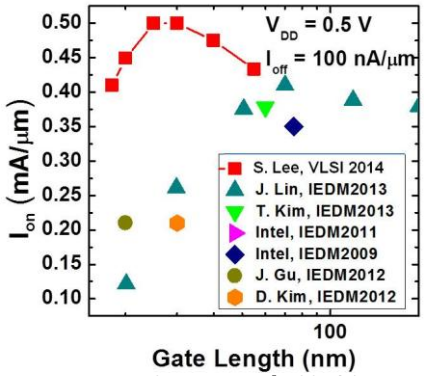

Figure 7: I_{on}, at 0.5V V_{DS} and 100nA/µm I_{off}, versus L_a, compared to the literature

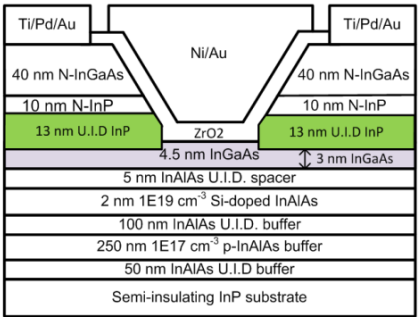

Figure 8: InGaAs MOSFET with recessed undoped InP S/D field spacers

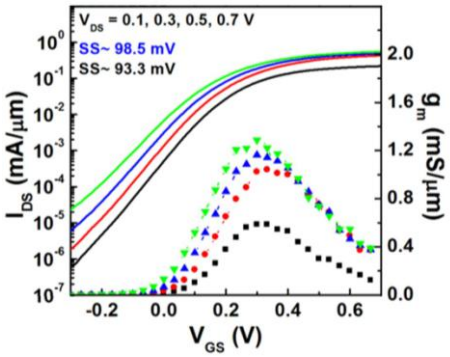

Figure 9:Subthreshold characteristics of the FET of fig. 8. Note the reduced leakage.

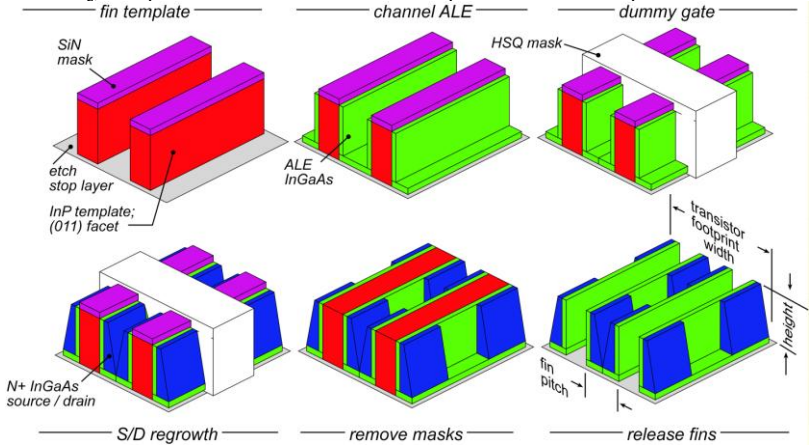

Figure 10: Process flow for high aspect ratio finFETs. The InP template is defined by an wet etch selective to the vertical (011) facet. ALE growth can provide monolayer control of the channel thickness. Not shown: ALD gate dielectric, gate & S/D metals

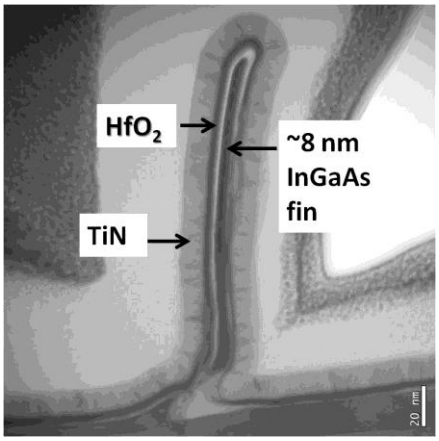

Figure 11: TEM image of a single fin of ~180nm height