Influence of InP Source/Drain Layers upon the DC Characteristics of InAs/InGaAs MOSFETs

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Because of the low effective mass, MOSFETs using In-rich (x>53%) $In_xGa_{1-x}As$ channels [1-5] exhibit high on-state current I_{on} at low drain bias (V_{DS}=0.5 V). However, the small bandgap of high-indium $In_xGa_{1-x}As$ channels can lead to high off-state leakage I_{off} due to band-to-band tunneling (BTBT) and impact ionization (I.I.). Earlier we had reported [1] that adding an unintentionally-doped (UID) InGaAs vertical spacer within the raised source/drain (S/D) of an InAs/InGaAs channel MOSFET substantially reduced I_{off}. Here we compare the characteristics of FETs using a wide-bandgap UID InP vertical spacer to earlier results [1] using an InGaAs spacer, and to control devices using only a very thin spacer. We find that FETs using InP spacers have I_{off} comparable to FETs using narrower-bandgap InGaAs spacers of similar thickness, suggesting that with the spacer, the observed I_{off} at high V_{DS} arises from BTBT or I.I. within the channel, and not within the high-field gate-drain spacer layer. Further, the wide-gap UID InP source spacer does not increase the threshold voltage V_{th}, suggesting that the gated potential barrier remains in the channel and not in the source spacer region. We also compare the on-state characteristics of FETs using InAs/InGaAs channels and an N+ InP S/D. Unlike the findings of [6], we do not observe improved I_{on} with the use of a wider-bandgap N+ source.

Fig 1. shows device structures. The epitaxial structures consist of a semi-insulating InP substrate, a 50 nm U.I.D InAlAs layer, a 250 nm 1×10^{17} cm^{-3} Be-doped InAlAs layer, a 100 nm U.I.D InAlAs layer, a 2 nm 1×10^{19} cm^{-3} Si-doped InAlAs modulation-doped layer, a 5 nm U.I.D InAlAs setback layer, a 3 nm InGaAs sub-channel, a 6 nm InAs channel, and a 4 nm InGaAs cap. HSQ dummy gates were patterned by e-beam lithography. Before S/D regrowth, ~2 nm of the InGaAs cap at the S/D region was digitally etched using UV ozone and dilute HCl. The samples were then transferred to an MOCVD reactor for InP spacer and InGaAs S/D regrowth. Sample A has a 50 nm N+ InGaAs regrowth. Sample B and sample C incorporate a 10 nm N+ InP spacer and a 10 nm U.I.D InP spacer between the channel and the N+ InGaAs S/D, respectively. The devices were then isolated and a three cycle digital etch removed the 4 nm InGaAs cap in the channel region. After transferring to an ALD, the surface was prepared by TMA/nitrogen plasma cycles, and 2.9 nm HfO_2 was deposited [7]. Nickel gates and Ti/Pd/Au S/D contacts were defined using liftoff.

Fig. 2 shows the transfer characteristics and output characteristics of L_g-65 nm devices for sample A, B and C. Sample B with a N+ InP spacer shows comparable on-state and off-state performance to Sample A, featuring a record transconductance of 2.95 mS/um at V_{DS}=0.5 V. The subthreshold swing (SS) of L_g=65 nm devices for both sample A and B is ~ 150 mV/dec at V_{DS}=0.5 V. In contrast to [6], no significant improvement in on-state current is observed after incorporating the N+ InP spacer. Note however that even sample A has a conduction-band offset between the N+ source and the channel.

Adding a 10 nm U.I.D InP spacer (sample C), significantly improves the subthreshold swing (*SS*=114 mV/dec at V_{DS}=0.5 V) and I_{off} of an a L_g=65 nm device. Transconductance remains high (g_m~2.6 mS/um at V_{DS}=0.5 V). The minimum off-state leakage of sample C (10nm InP spacer) is significantly smaller than that of sample A (2nm InGaAs spacer), but is similar to that reported in [1] for a FET of similar channel design and an 8 nm InGaAs spacer. We observe that it is the spacer thickness, and not its bandgap, which determines I_{off}. This indicates that the spacer reduces I_{off} through decreased electric field at the drain end of the channel. Examining sample C's output characteristics (fig. 2), under large positive gate bias (V_{GS}>0.5 V) I_{on} is reduced; the band offset at the interface between the N+ InGaAs and the UID InP spacer limits the source electron supply to the InAs/InGaAs channel, reducing the maximum I_{on}. Fig. 3 shows transconductance g_m versus L_g for samples A, B, and C. All the samples show high g_m, with a slight degradation (~10%) for sub-100 nm-L_g devices on Sample C. Fig. 4 shows *SS* versus L_g for Sample A, B, and C. The insertion of the UID InP spacer significantly improves *SS* at short gate lengths. Fig. 5 compares the g_m and *SS* of this work to recently reported III-V MOSFETs. The UID InP vertical spacer shows performance similar to the UID InGaAs vertical spacer [1]. In contrast to FETs using lateral gate-drain spacers to reduce I_{off} [4,5], the vertical spacer allows continuous scaling of the S/D contact pitch, as is necessary in VLSI.

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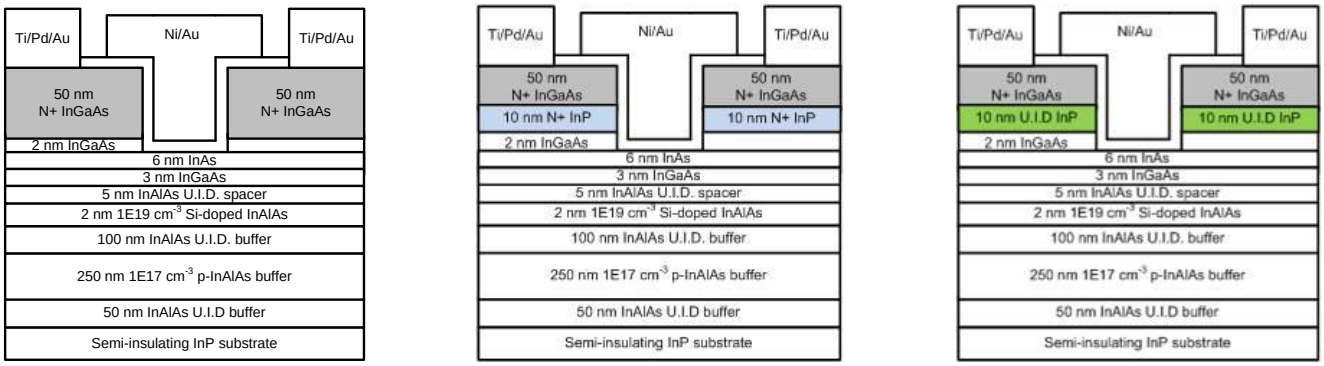

(a) (b) (c)

Fig. 1. Device cross-sections: (a) 2 nm U.I.D. InGaAs spacer, N+ InGaAs source/drain (b) 2nm U.I.D. InGaAs spacer, N+ InP/InGaAs source/drain and (c) 2/10 nm U.I.D. InGaAs/InP spacer, N+ InGaAs source/drain.

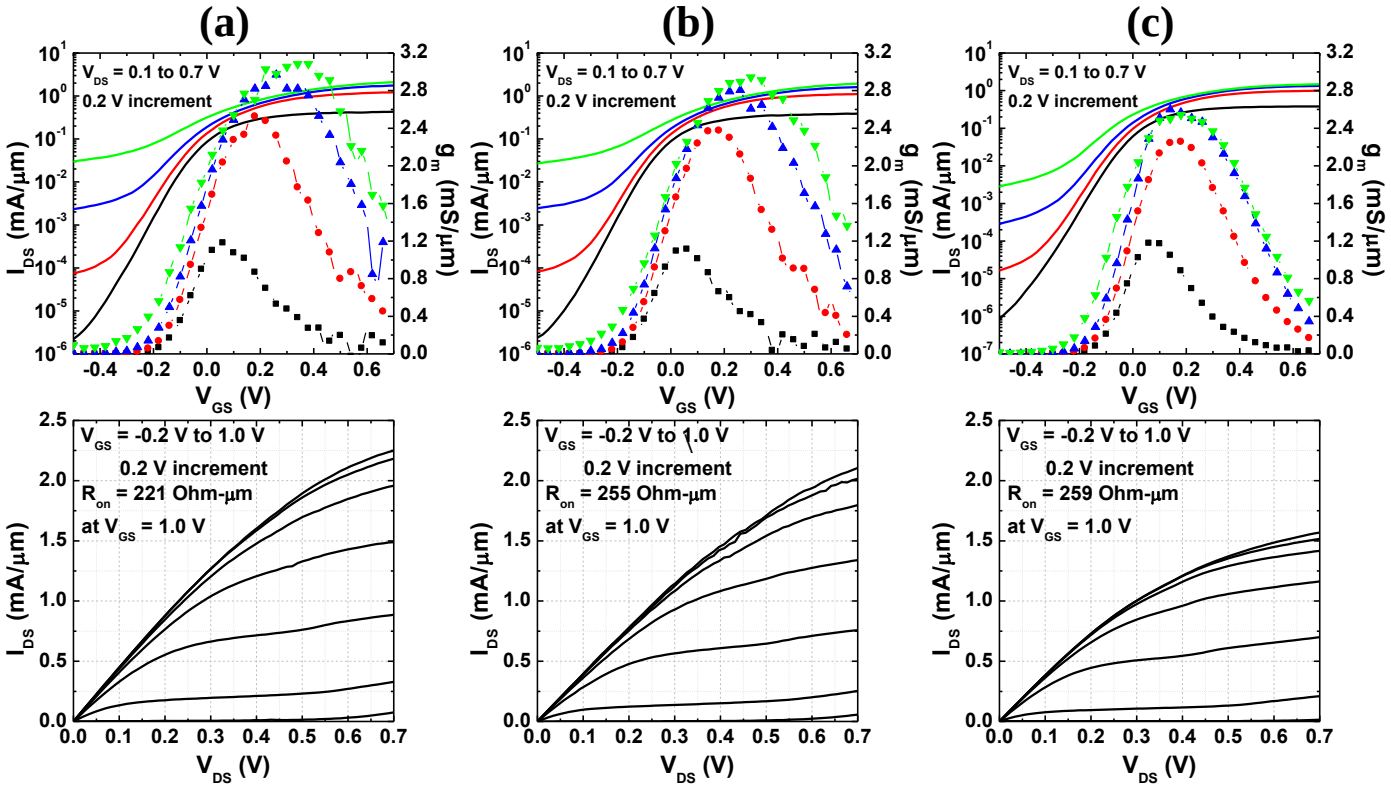

Fig. 2. Transfer and output characteristics of L_g=65 nm devices for (a) sample A, (b) sample B, and (c) sample C.

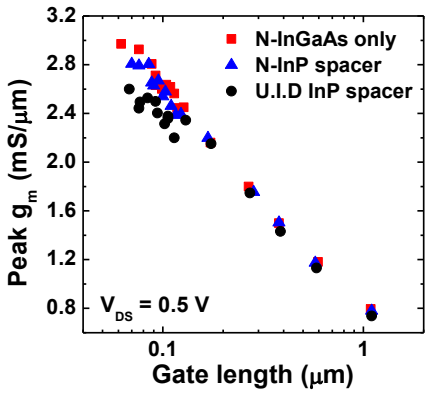

Fig. 3. Comparison of g_m versus L_g for samples A, B, and C.

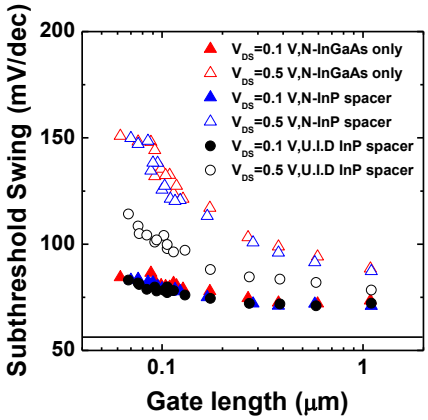

Fig. 4. Comparison of *SS* versus L_g for samples A, B, and C.

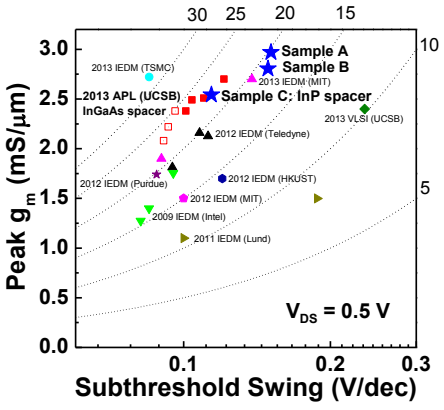

Fig. 5. Benchmark of peak g_m versus *SS* for this work and the recent reported III-V MOSFETs.