

# 50-500GHz Wireless Technologies: Transistors, ICs, and Systems

***Mark Rodwell, UCSB***

*J. Rode\*, P. Choudhary, B. Thibeault, W. Mitchell,  
J. Buckwalter, U. Madhow, A.C. Gossard : **UCSB***

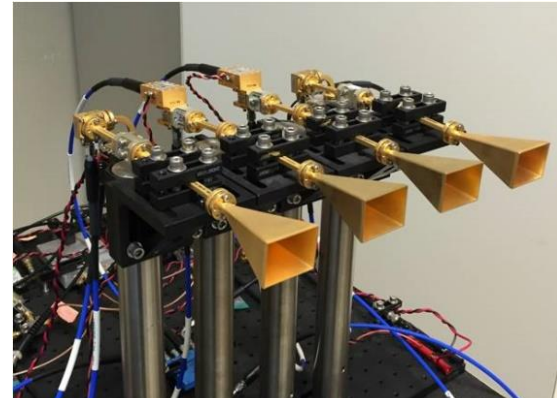
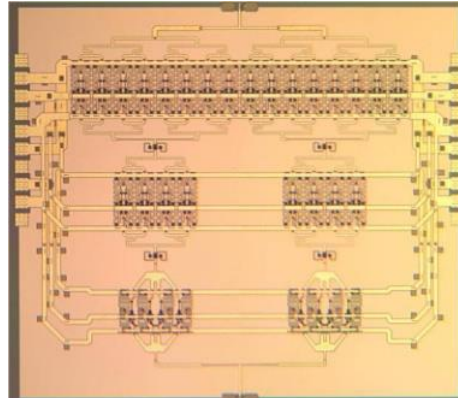
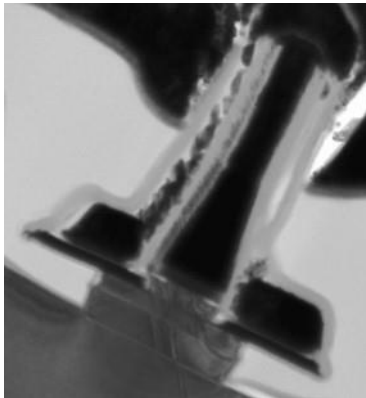
*M. Urteaga, J. Hacker, Z. Griffith, B. Brar: **Teledyne Scientific and Imaging***

*M. Seo: **Sungkyunkwan University***

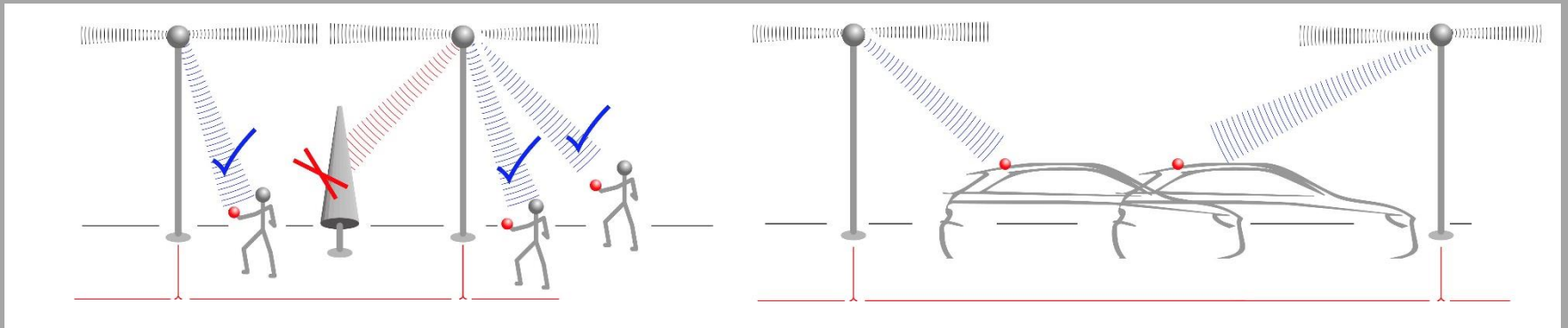
*\* Now with Intel*

# Why mm-wave wireless ?

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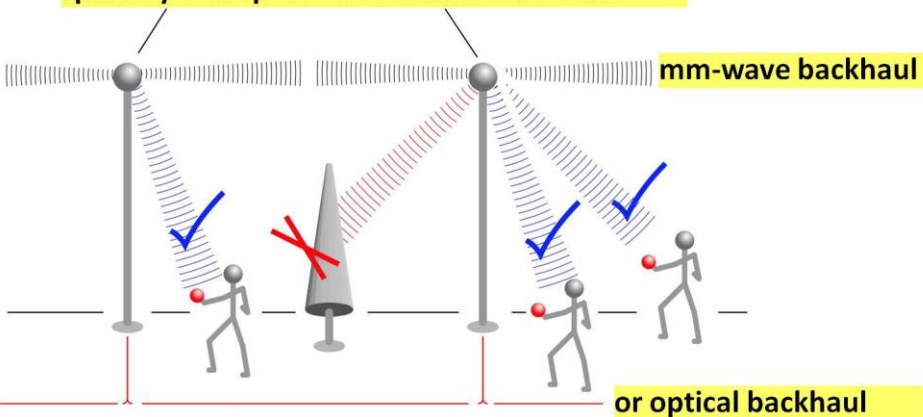


# Links

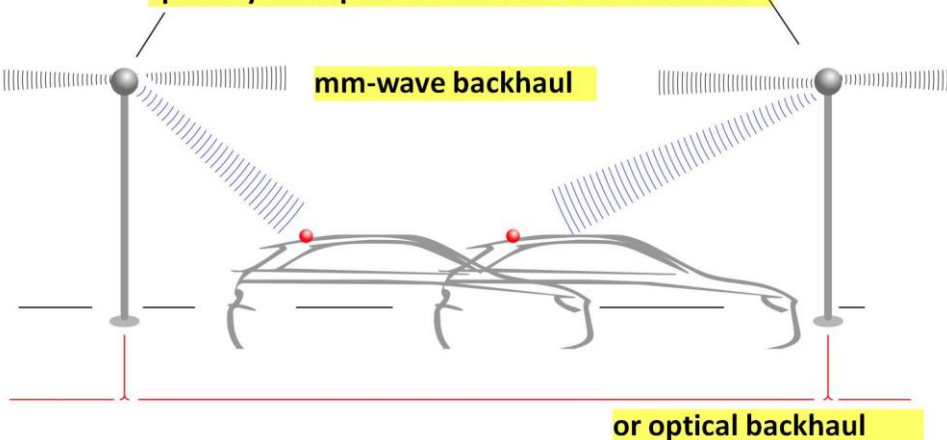


# mm-Waves: high-capacity mobile communications

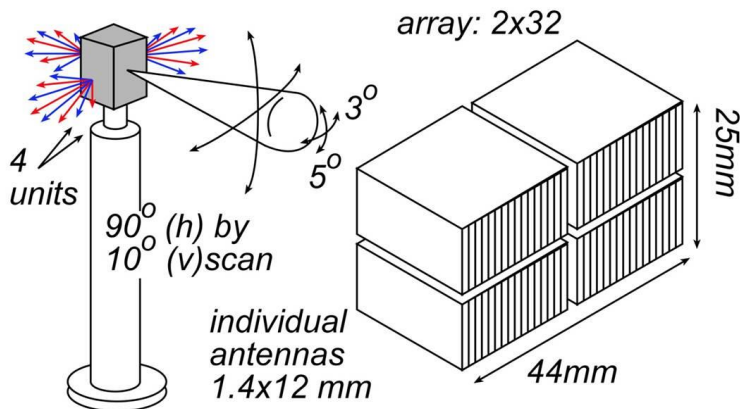
spatially-multiplexed mm-wave base stations



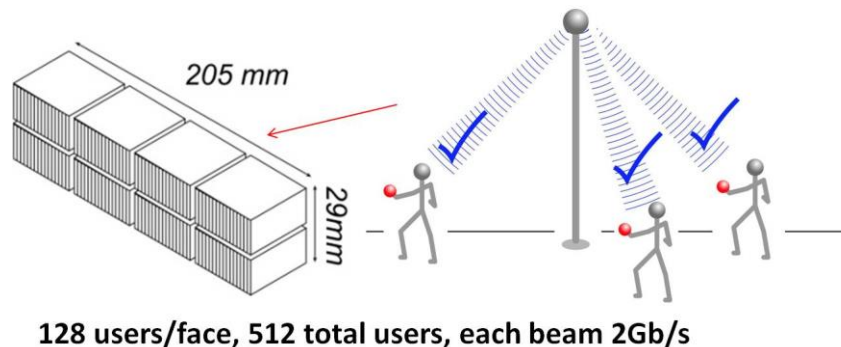
spatially-multiplexed mm-wave base stations



140 GHz, 10 Gb/s Adaptive Picocell Backhaul



60 GHz, 1 Tb/s Spatially-Multiplexed Base Station



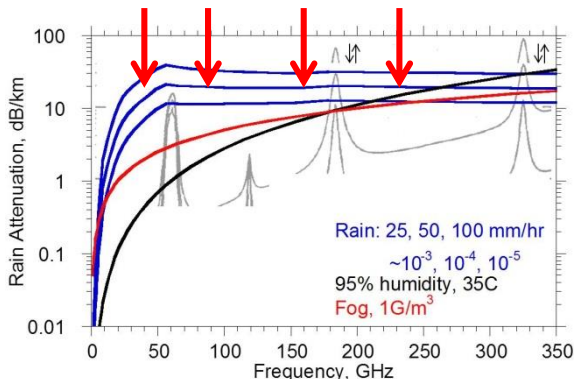
## Needs → research:

RF front end: phased array ICs, high-power transmitters, low-noise receivers

IF/baseband: ICs for multi-beam beamforming, for ISI/multipath suppression, ...

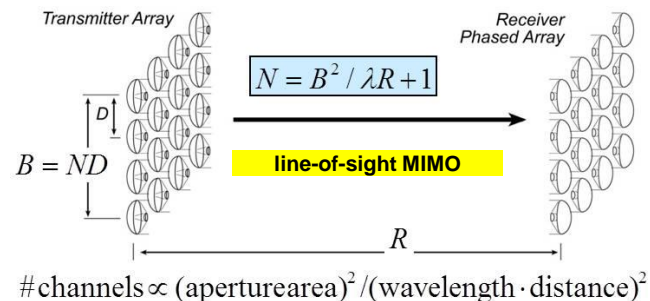
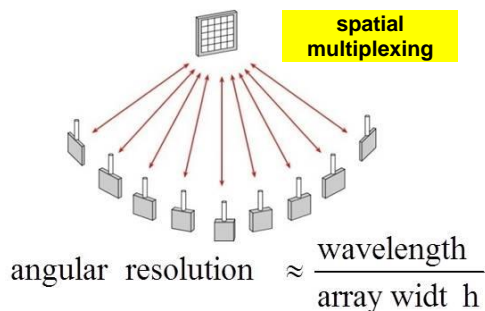
# mm-Waves: benefits & challenges

## Large available spectrum

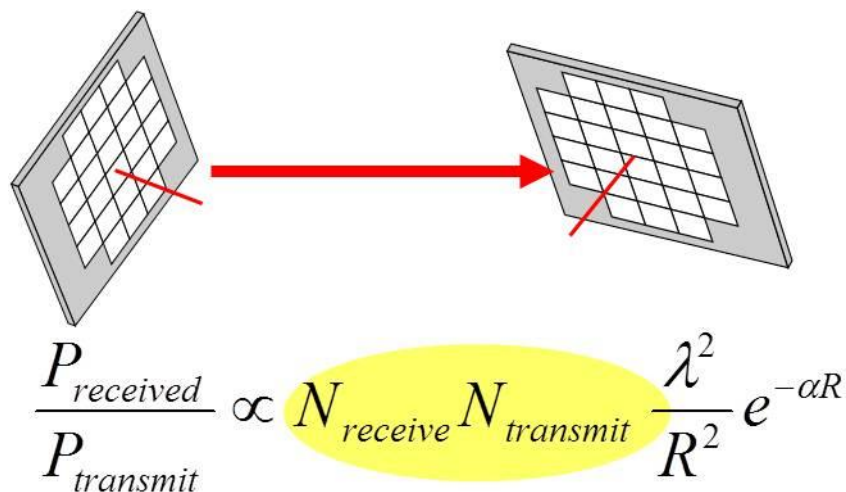


(note high attenuation in foul weather)

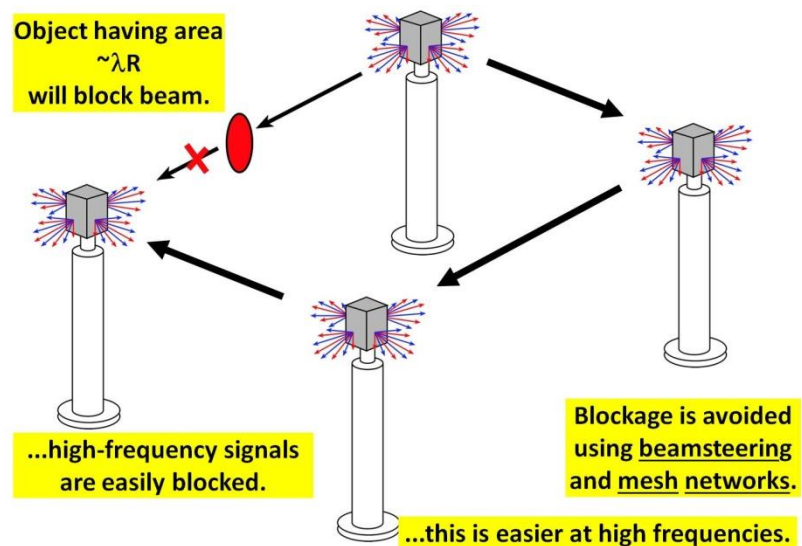
## Massive # parallel channels



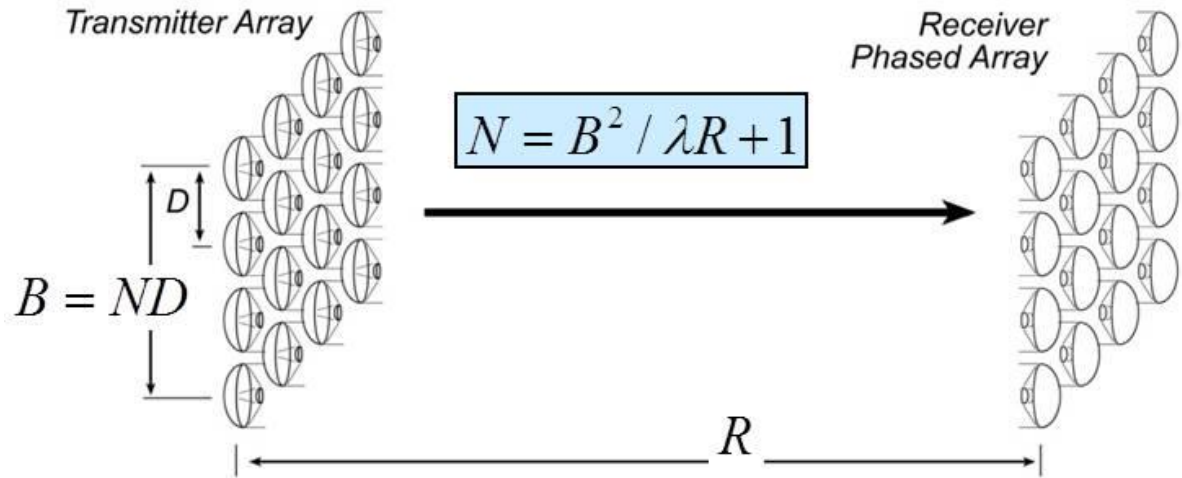
## Need phased arrays (overcome high attenuation)



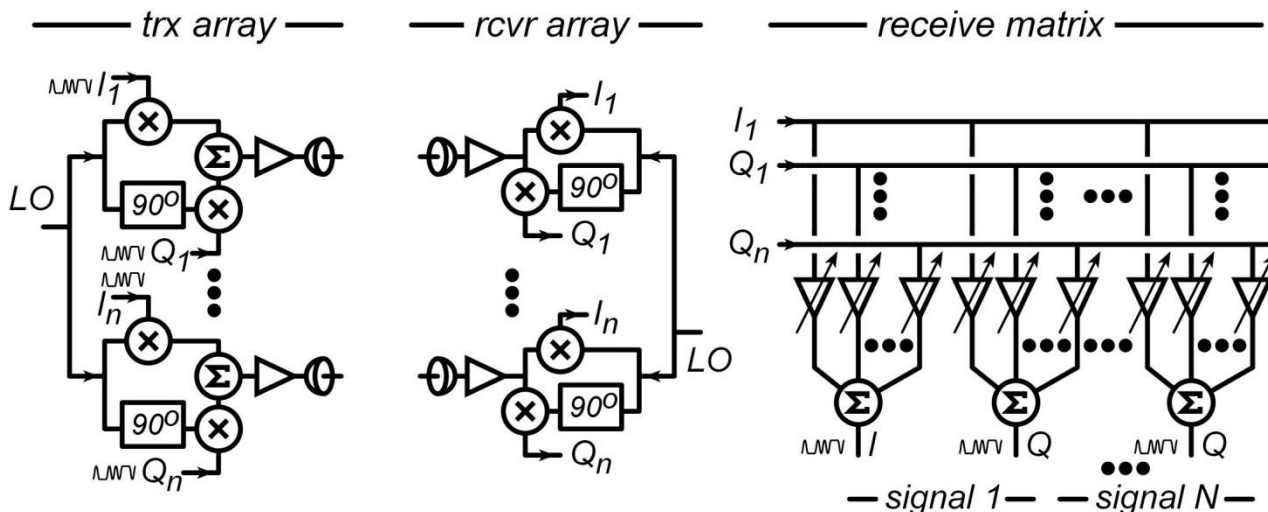
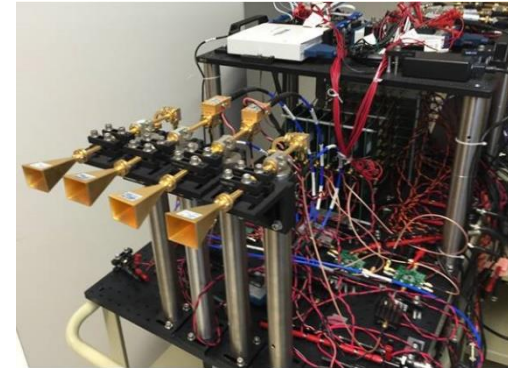
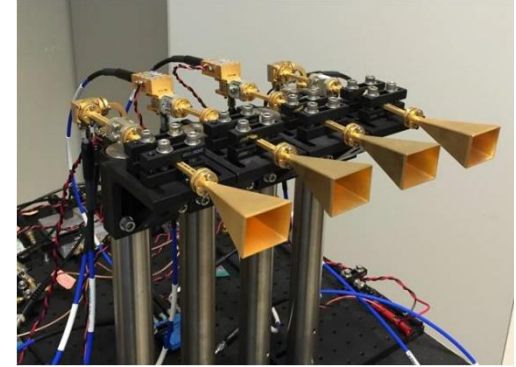
## Need mesh networks



# mm-Wave LOS MIMO: multi-channel for high capacity



#channels  $\propto$  (aperture area)<sup>2</sup> / (wavelength · distance)<sup>2</sup>



Torklinson : 2006 Allerton Conference  
 Sheldon : 2010 IEEE APS-URSI  
 Torklinson : 2011 IEEE Trans Wireless Comm.

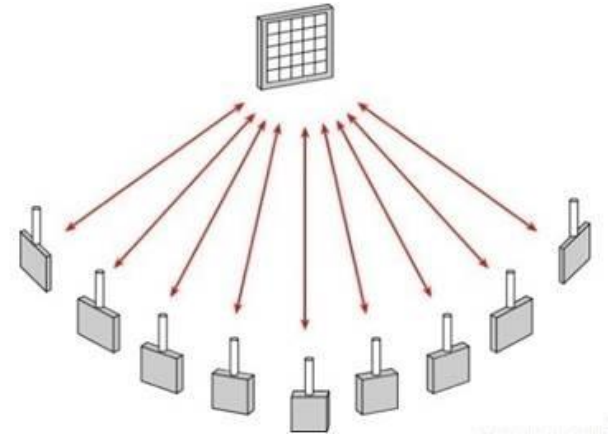
# Spatial Multiplexing: massive capacity RF networks

## multiple independent beams

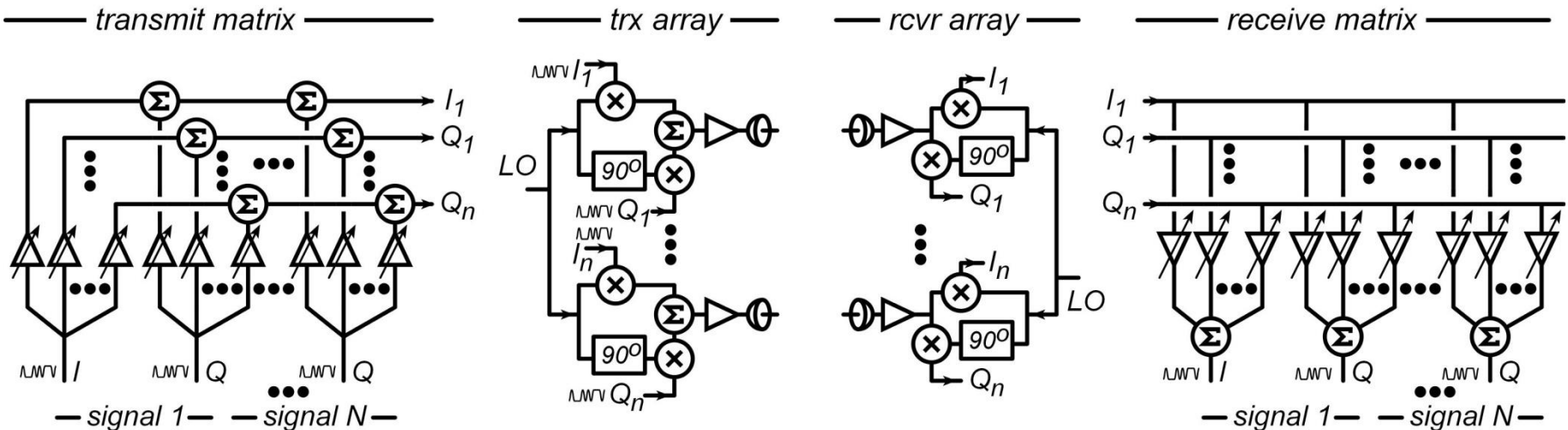
each carrying different data

each independently aimed

# beams = # array elements

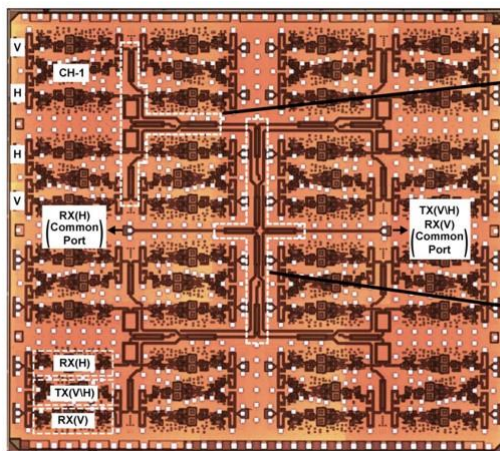
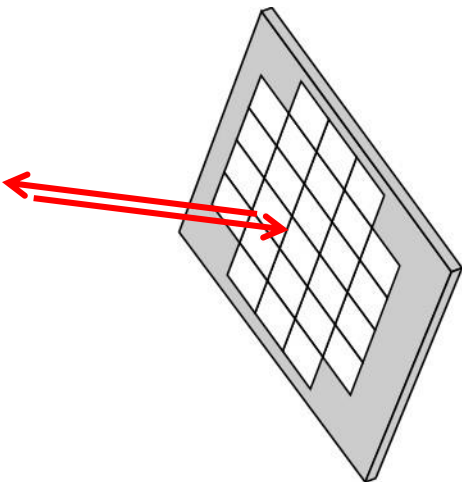


## Hardware: multi-beam phased array ICs



# Millimeter-wave imaging

**10,000-pixel, 94GHz imaging array → 10,000 elements**

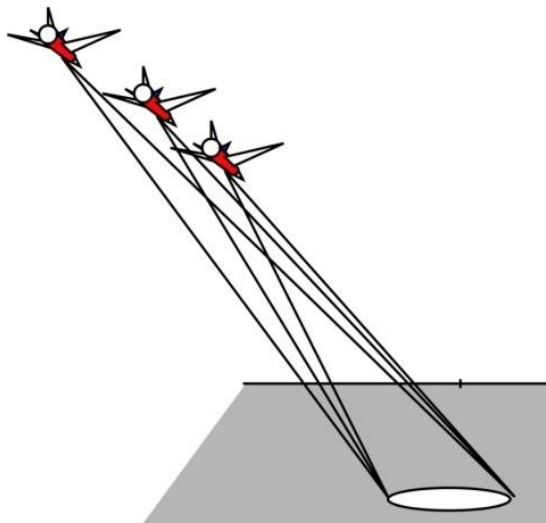


Golcuk: Trans MTT, Aug 2014

**Demonstrated:**  
SiGe, 1.3 kW (UCSD/Rebeiz)

**Lower-power designs:**  
InP, CMOS, SiGe  
(UCSB, UCSD, Virginia Poly.)

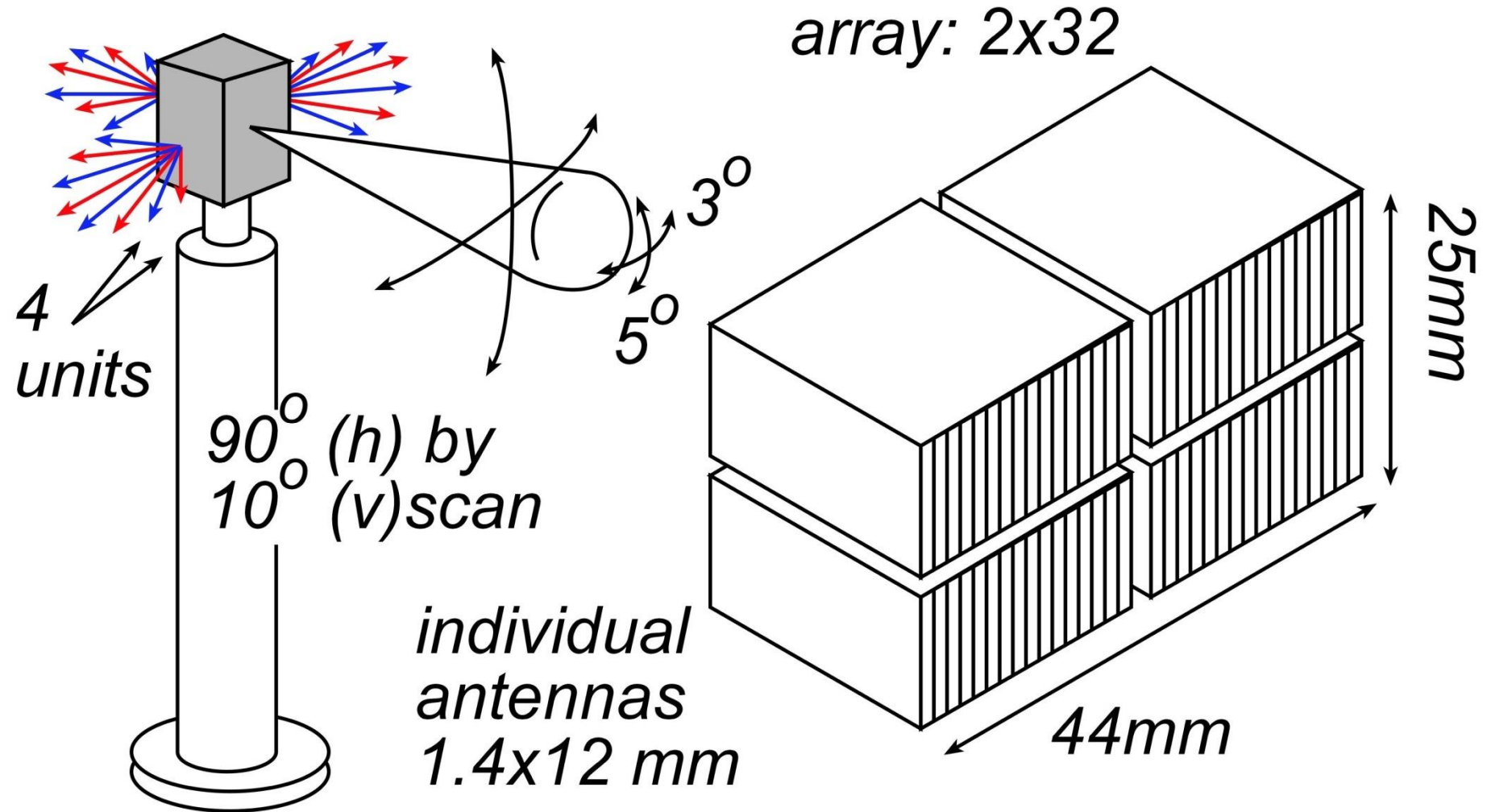
**235 GHz video-rate synthetic aperture radar**



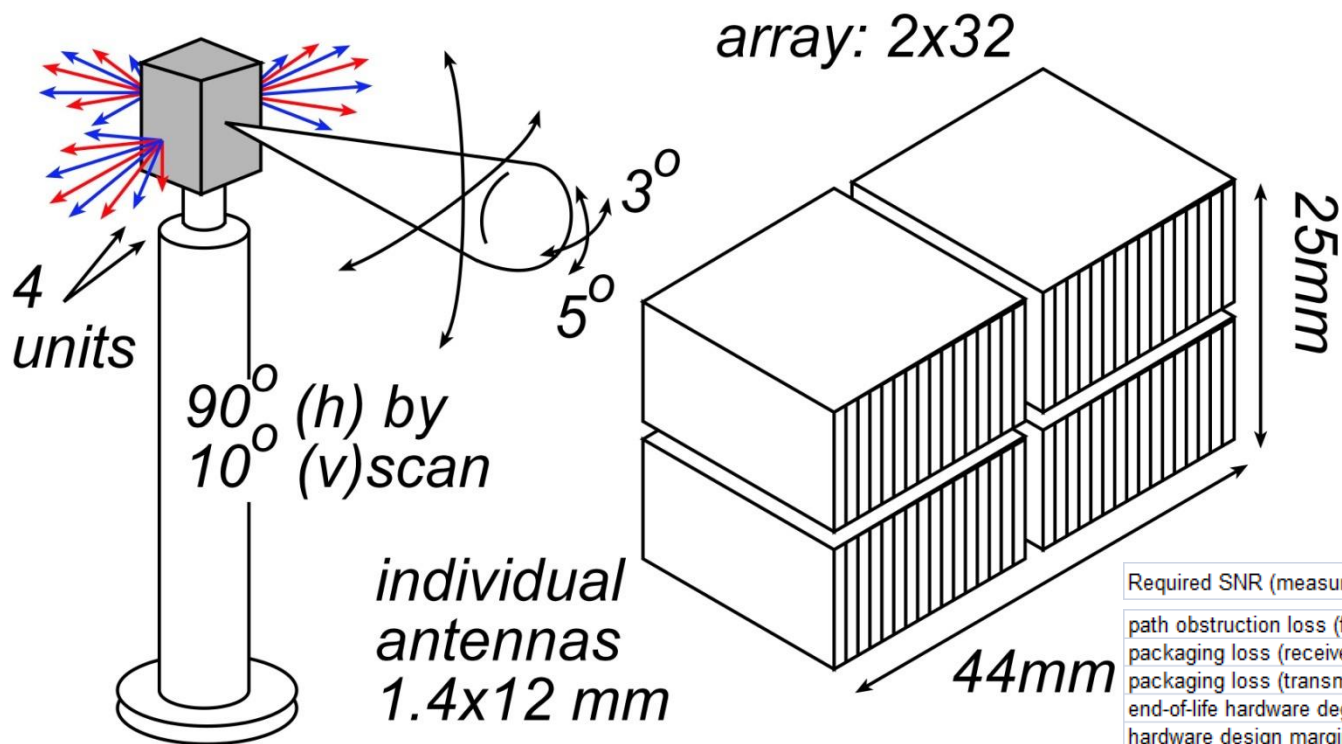
1 transmitter, 1 receiver  
100,000 pixels  
20 Hz refresh rate  
5 cm resolution @ 1km  
50 Watt transmitter  
(tube, solid-state driver)



# 140 GHz, 10 Gb/s Adaptive Picocell Backhaul



# 140 GHz, 10 Gb/s Adaptive Picocell Backhaul



Required SNR (measured as Eb/No)	6.8	dB
path obstruction loss (foliage, glass)	5.00	dB
packaging loss (receiver)	3	dB
packaging loss (transmitter)	3	dB
end-of-life hardware degradation	3	dB
hardware design margin	3	dB
beam aiming loss (edge of beam)	3	dB
systems operating margin	10	dB
PA backoff for OFDM	7.00E+00	dB

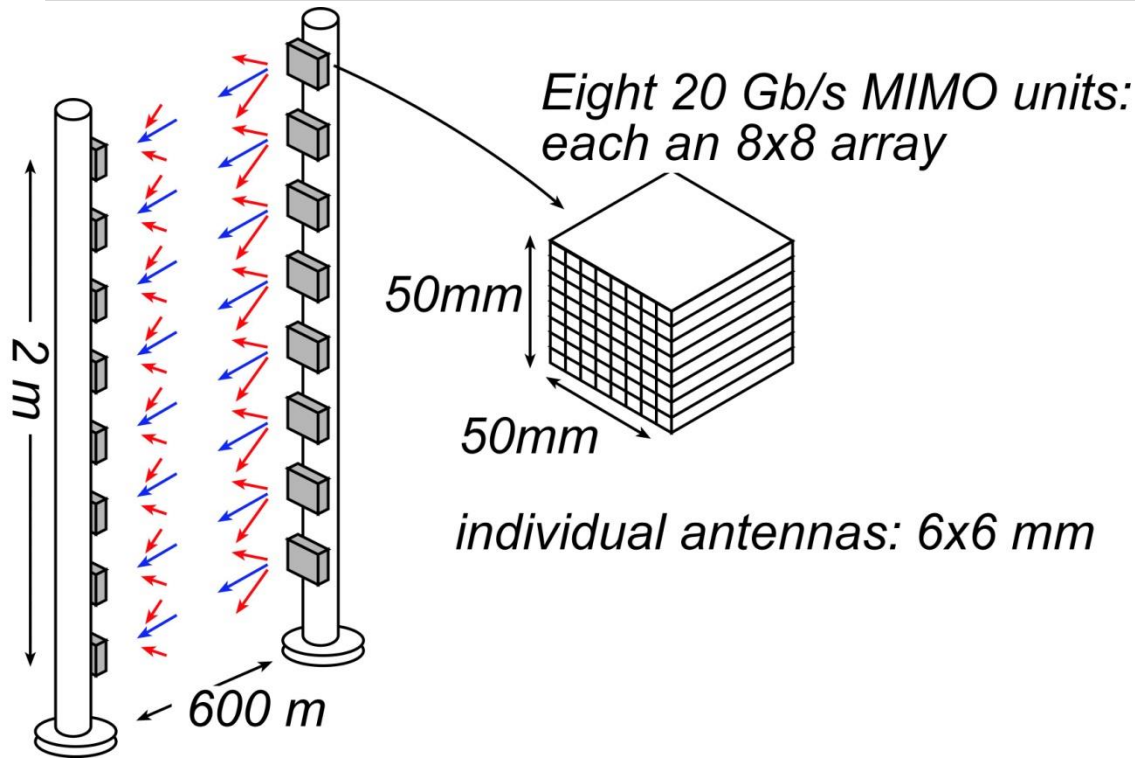
**350 meters range in 50mm/hr rain**

**Realistic packaging loss, operating & design margins**

**PAs: 24 dBm  $P_{\text{sat}}$  (per element) → GaN or InP**

**LNAs: 4 dB noise figure → InP HEMT**

# 340GHz, 160Gb/s spatially multiplexed backhaul



**1° beamwidth; 8° beamsteering**

**600 meters range in 50 mm/hr rain**

**Realistic packaging loss, operating & design margins**

**PAs: 14 dBm  $P_{\text{sat}}$  (per element) → InP**

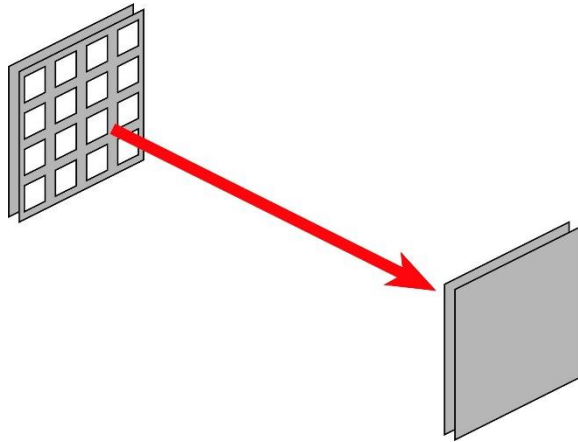
**LNAs: 7 dB noise figure → InP HEMT**

# Optimum array size for low system power

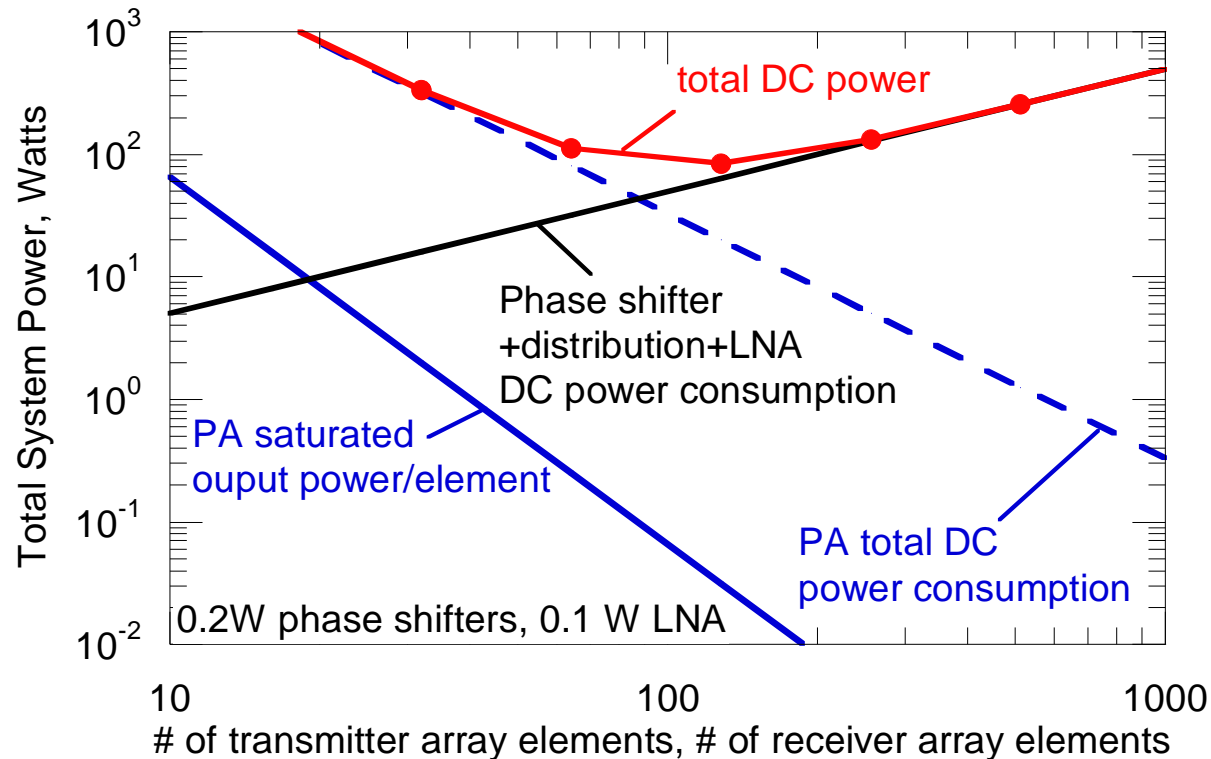
$$\frac{P_{receive}}{P_{transmit}} \propto N^2 \frac{\lambda^2}{R^2} \longrightarrow P_{transmit} \propto \frac{1}{N^2}$$

Do large arrays save power?

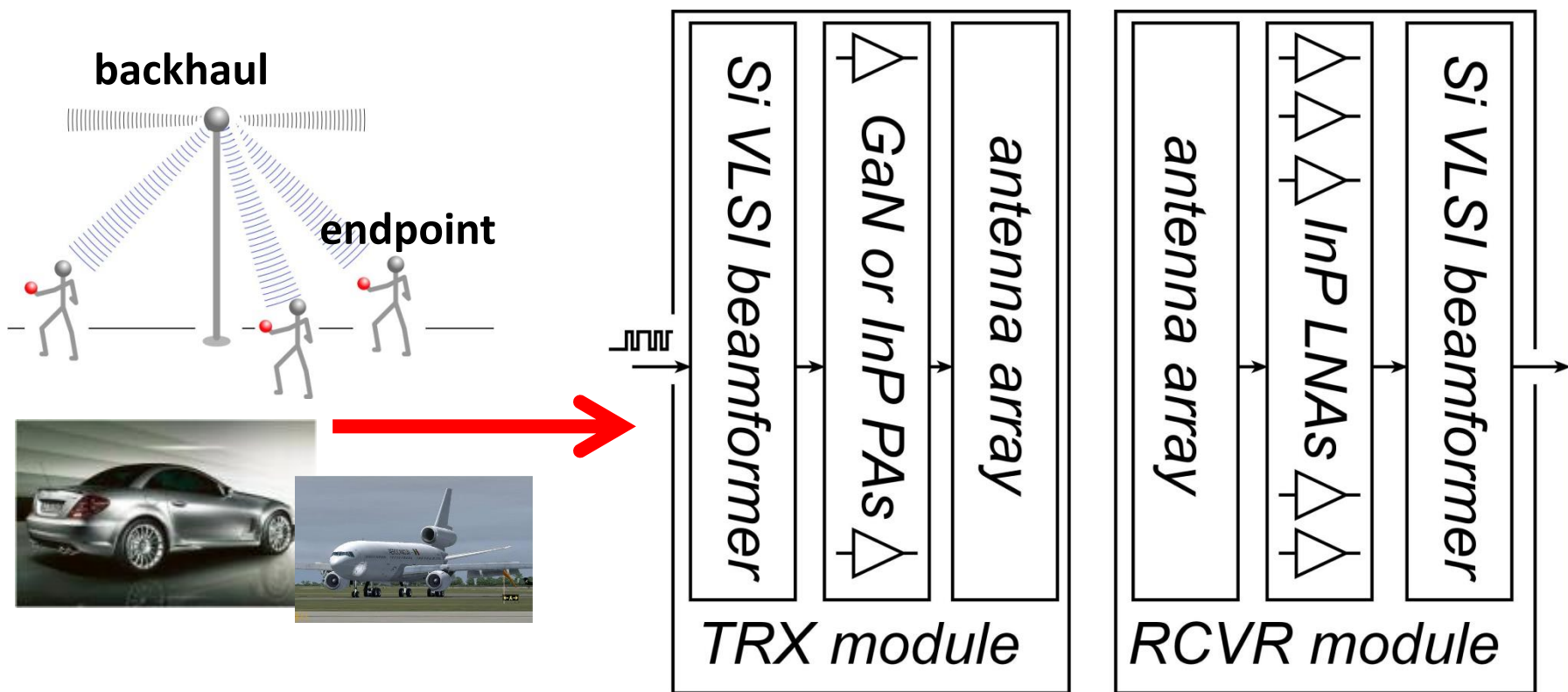
$$\text{Total system power} = \frac{P_{transmit}}{\text{efficiency}} + N(\text{power of LNA, phase shifters...})$$



**At optimum-size array, target PA output power is typically 10-200 mW**



# 50-500 GHz Wireless Transceiver Architecture

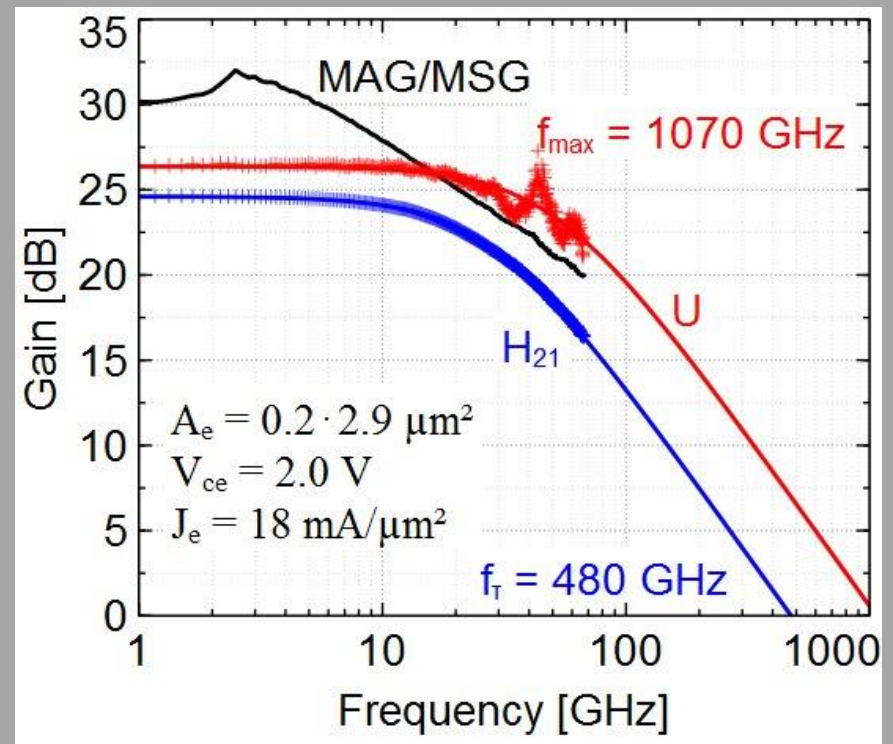
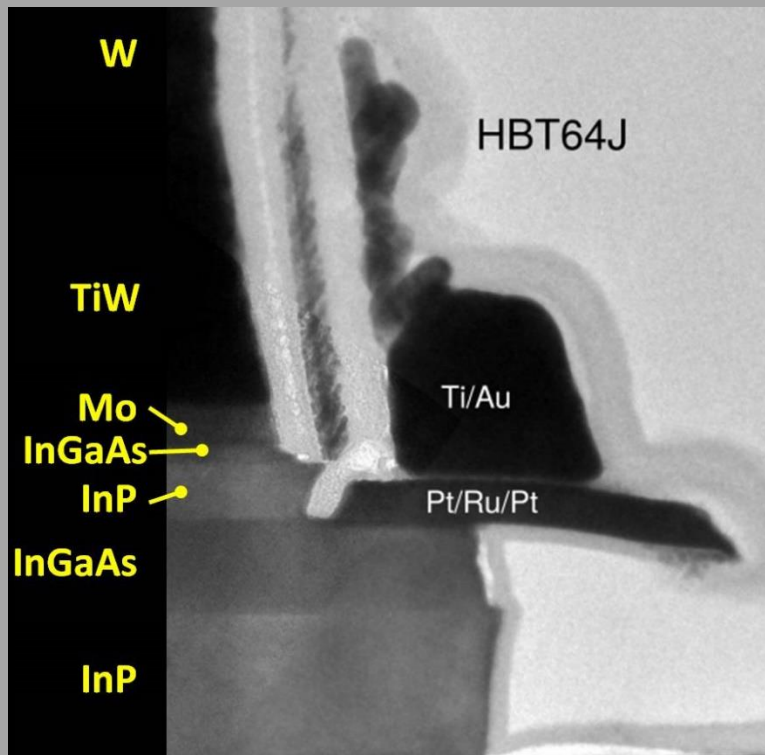


**III-V LNAs, III-V PAs → power, efficiency, noise**  
**Si CMOS beamformer → integration scale**

**...similar to today's cell phones.**

**High-gain antenna → large area**  
**→ much too big for monolithic integration**

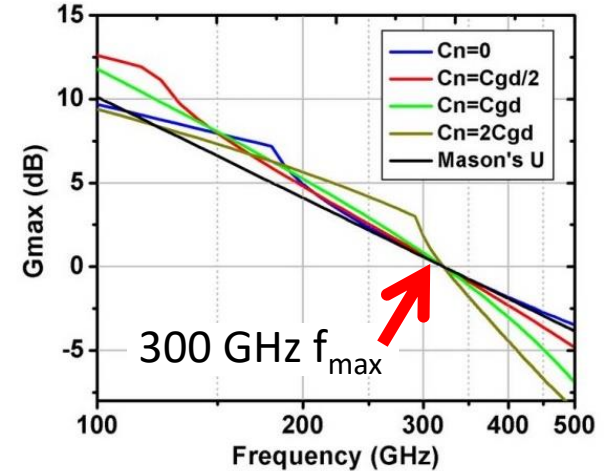
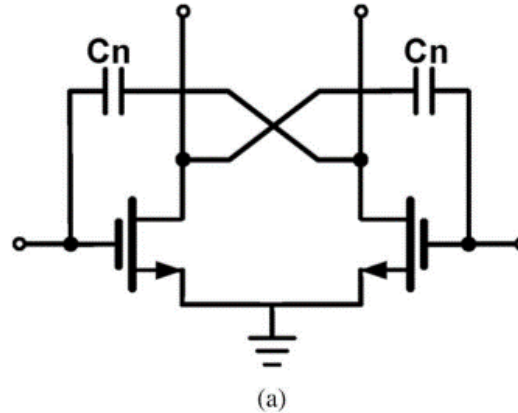
# Transistors



# mm-wave CMOS (examples)

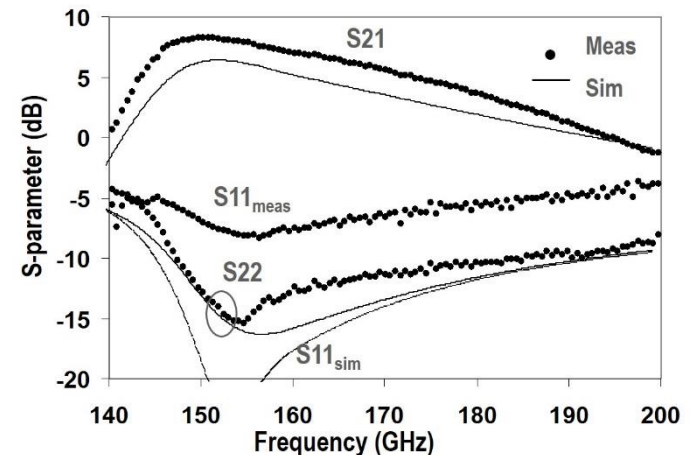
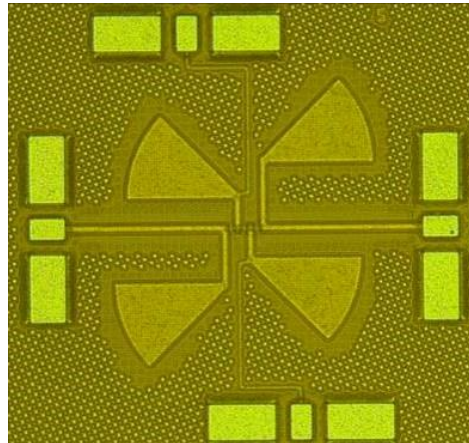
## 210 GHz amplifier: 32 nm SOI, positive feedback, 15 dB, 3 stages

Wang et al. (Heydari), JSSC, March 2014



## 150 GHz amplifier: 65 nm bulk CMOS, 8.2 dB, 3 stages (250GHz $f_{max}$ )

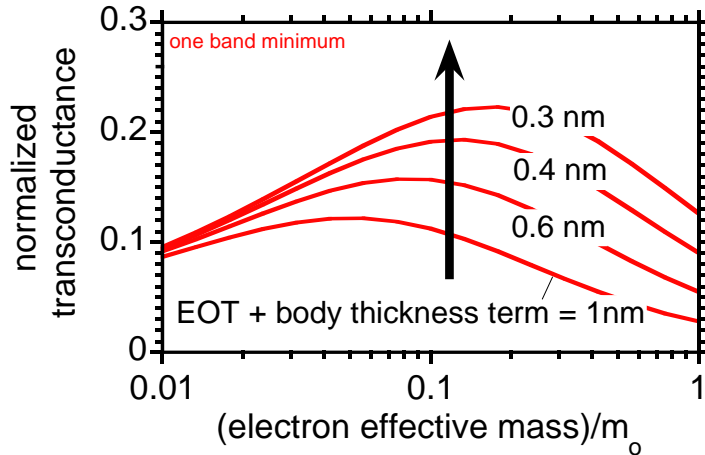
Seo et al. (UCSB), JSSC, December 2009



# mm-Wave CMOS won't scale much further

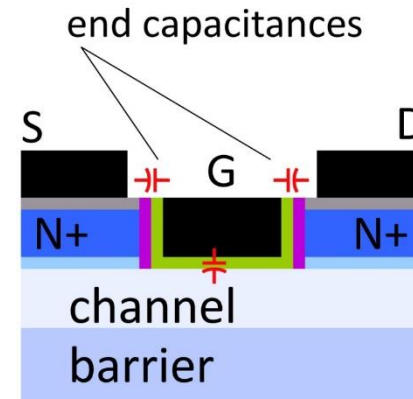
## Gate dielectric can't be thinned

→ on-current,  $g_m$  can't increase



## Shorter gates give no less capacitance

dominated by ends;  $\sim 1\text{fF}/\mu\text{m}$  total

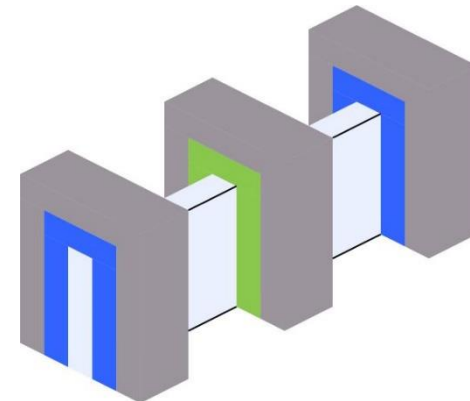


**Maximum  $g_m$ , minimum  $C \rightarrow$  upper limit on  $f_T$**   
about 350-400 GHz.

## Tungsten via resistances reduce the gain

Inac et al, CSICS 2011

Present finFETs have yet larger end capacitances



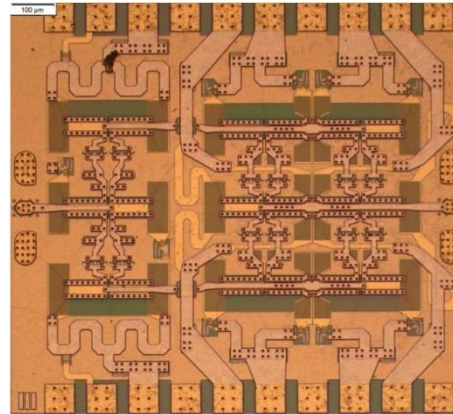


# III-V high-power transmitters, low-noise receivers

**Cell phones & WiFi:**  
GaAs PAs, LNAs

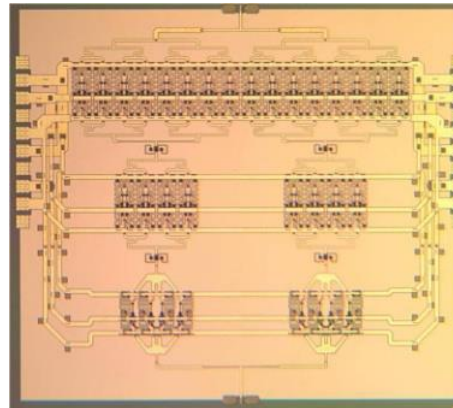


**mm-wave links need**  
high transmit power,  
low receiver noise



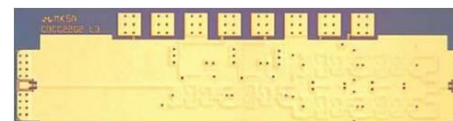
**0.47 W @86GHz**

H Park, UCSB, IMS 2014



**0.18 W @220GHz**

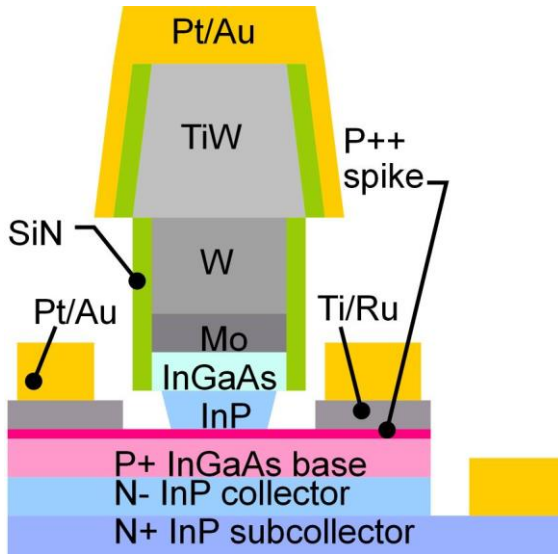
T Reed, UCSB, CSICS 2013



**1.9mW @585GHz**

M Seo, TSC, IMS 2013

# Making faster bipolar transistors



to double the bandwidth:	change
emitter & collector junction widths	decrease 4:1
current density ( $\text{mA}/\mu\text{m}^2$ )	increase 4:1
current density ( $\text{mA}/\mu\text{m}$ )	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1

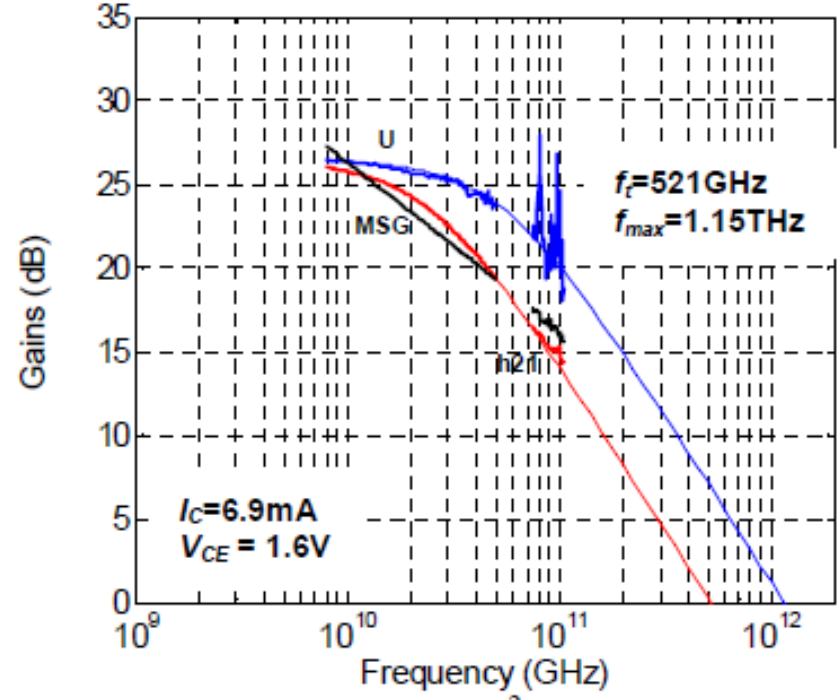
Narrow junctions.

Thin layers

High current density

Ultra low resistivity contacts

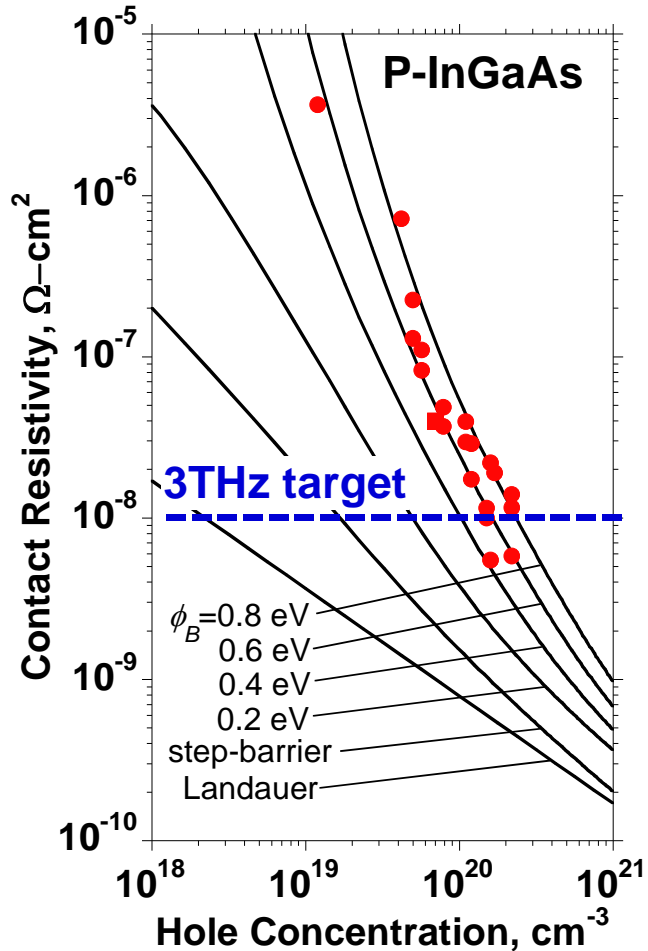
Teledyne: M. Urteaga *et al*: 2011 DRC



# THz HBTs: The key challenges

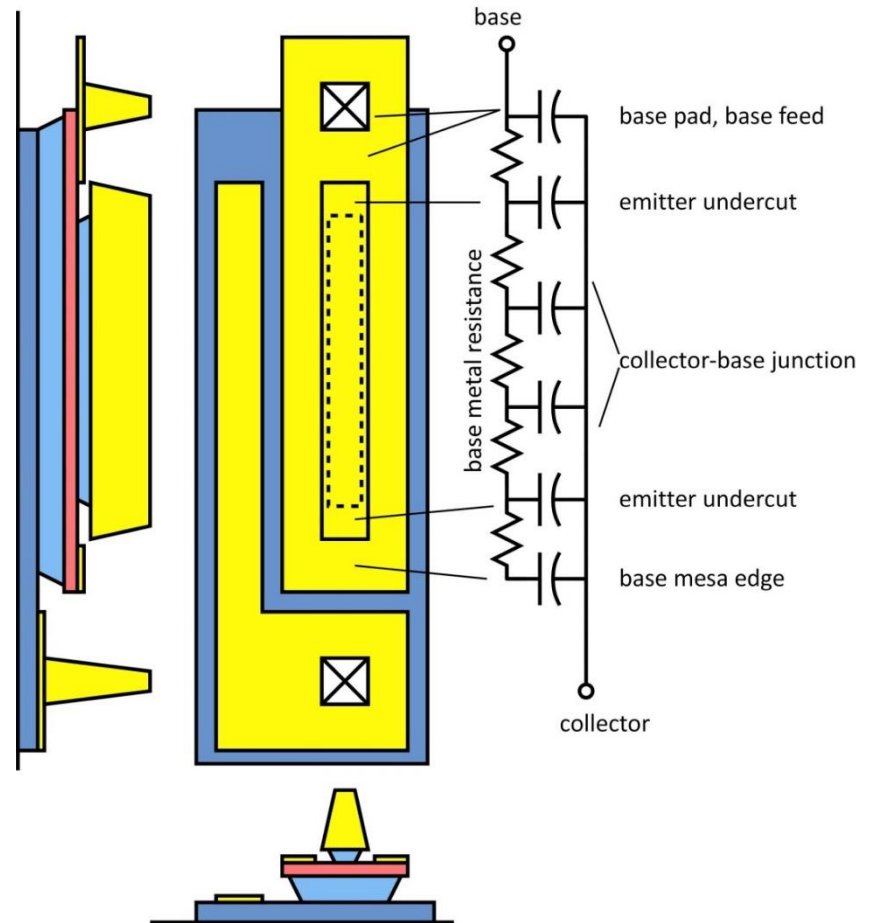
## Obtaining good base contacts

*in HBT vs. in contact test structure*  
(emitter contacts are fine)

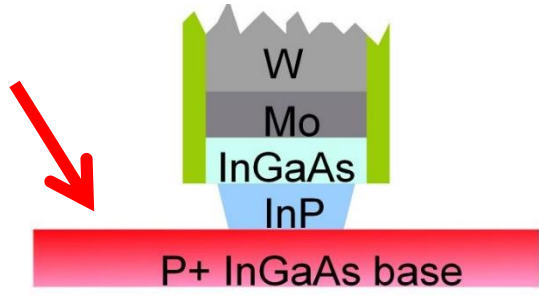


## RC parasitics along finger length

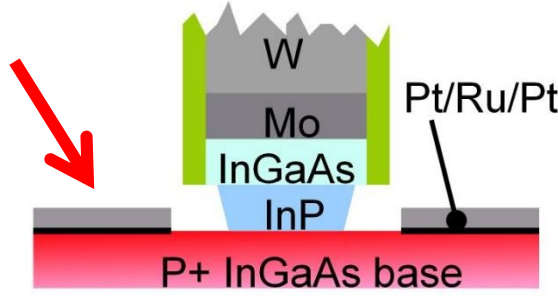
metal resistance, excess junction areas



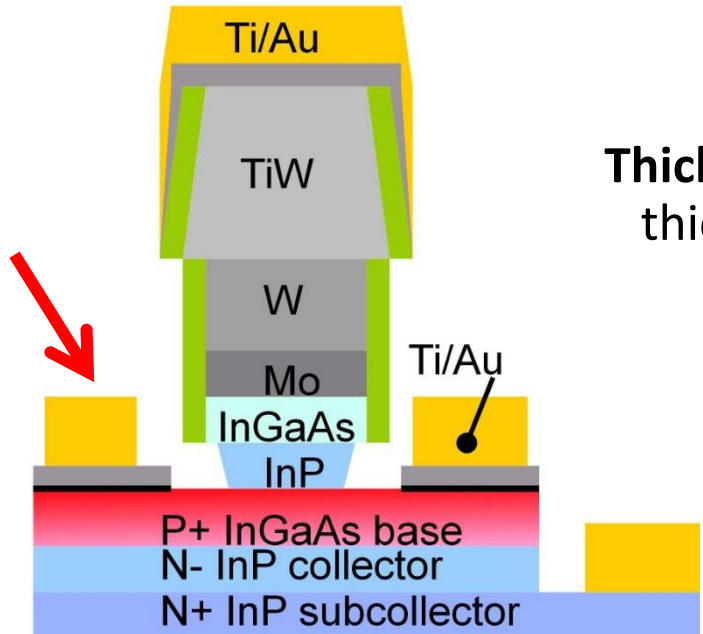
# THz HBTs: double base metal process



**Blanket surface clean (UV O<sub>3</sub> / HCl)**  
strips organics, process residues, surface oxides



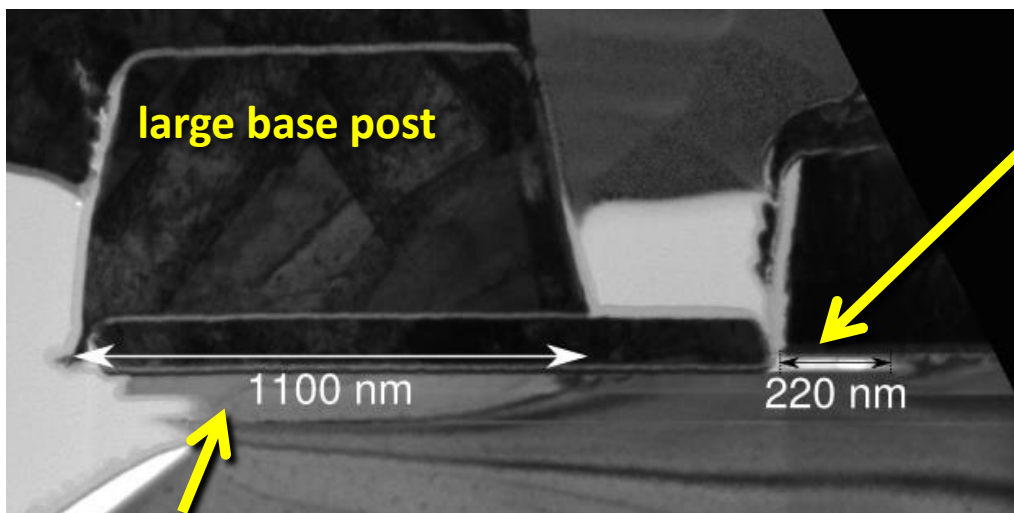
**Blanket base metal**  
no photoresist; no organic residues  
Ru refractory diffusion barrier  
2 nm Pt : penetrates residual oxides



**Thick Ti/Au base pad metal liftoff**  
thick metal → low resistivity

# Reducing Emitter Length Effects

before



large base post

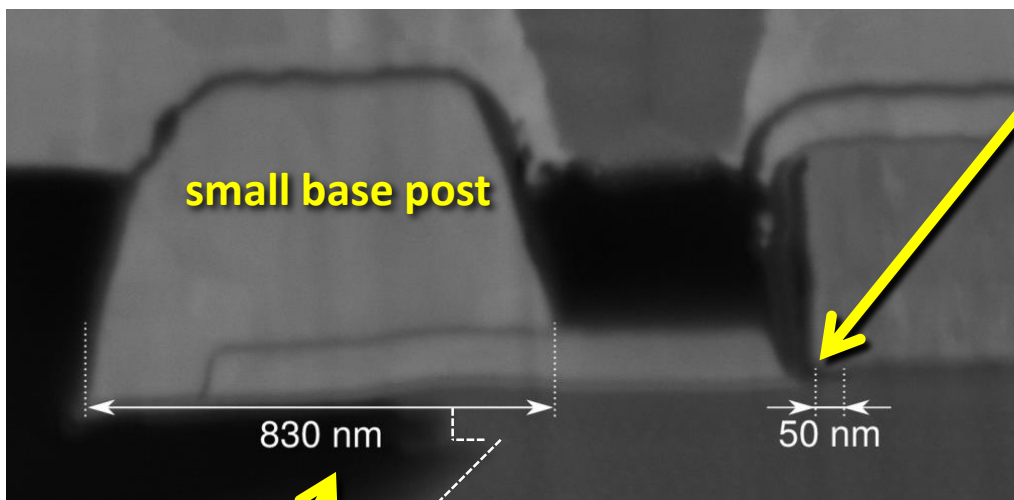
large emitter end undercut

1100 nm

220 nm

small base post undercut

after



small base post

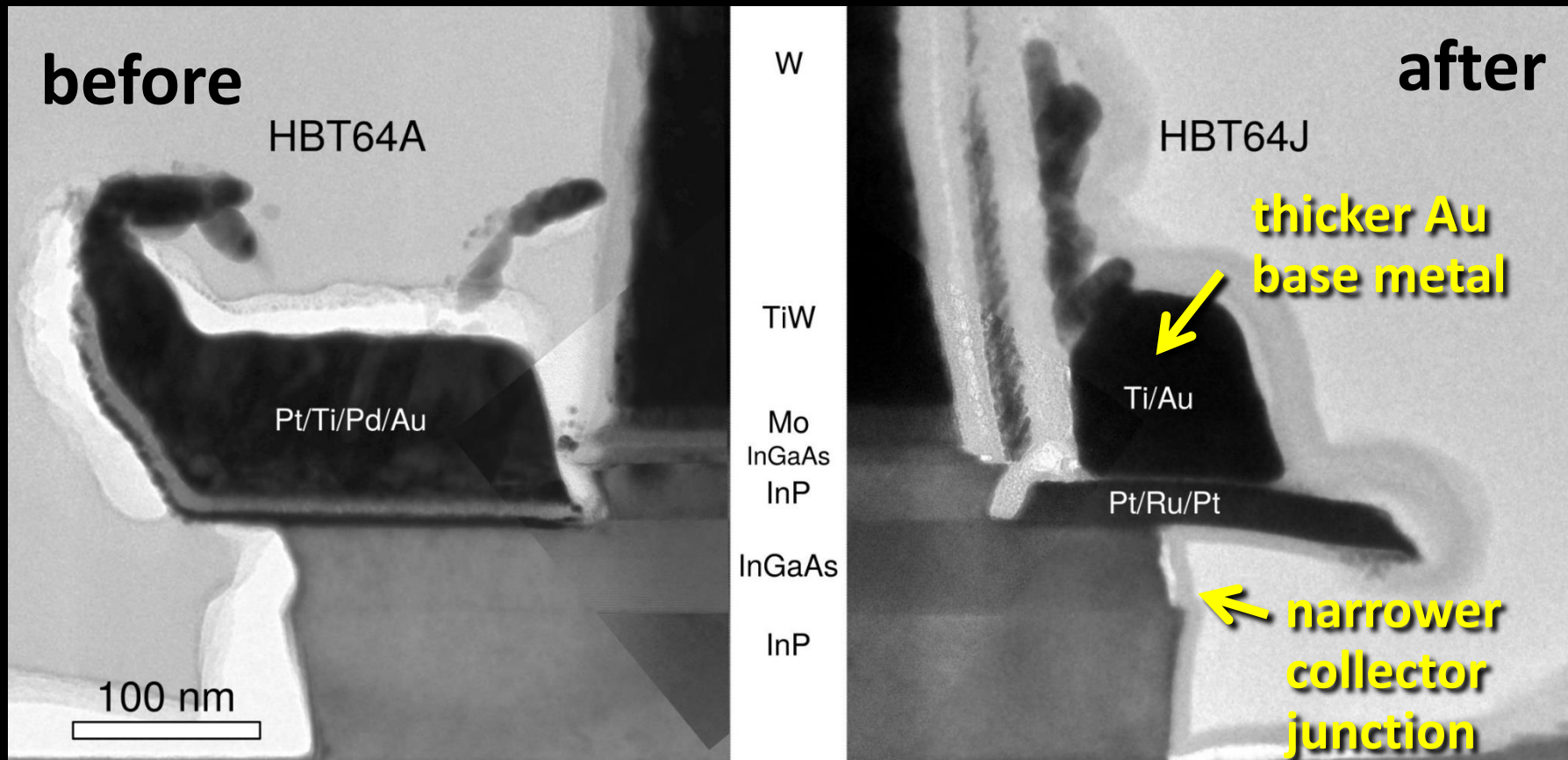
small emitter end undercut

830 nm

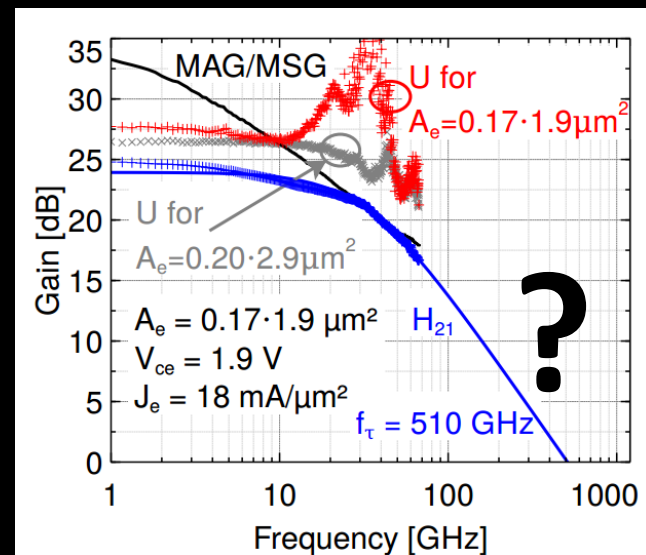
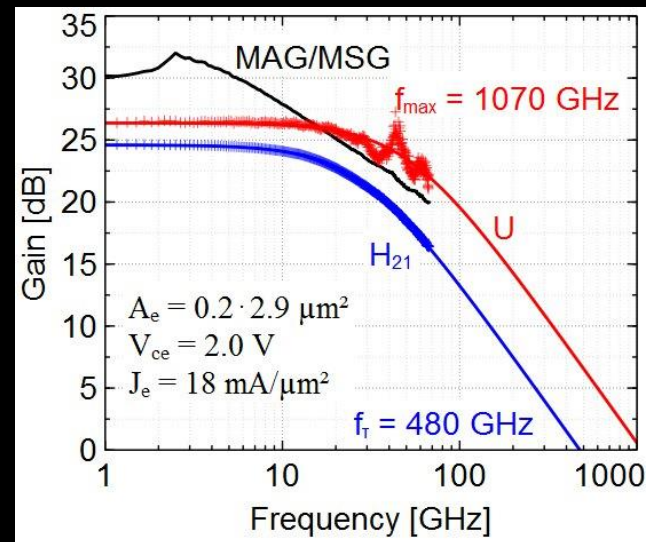
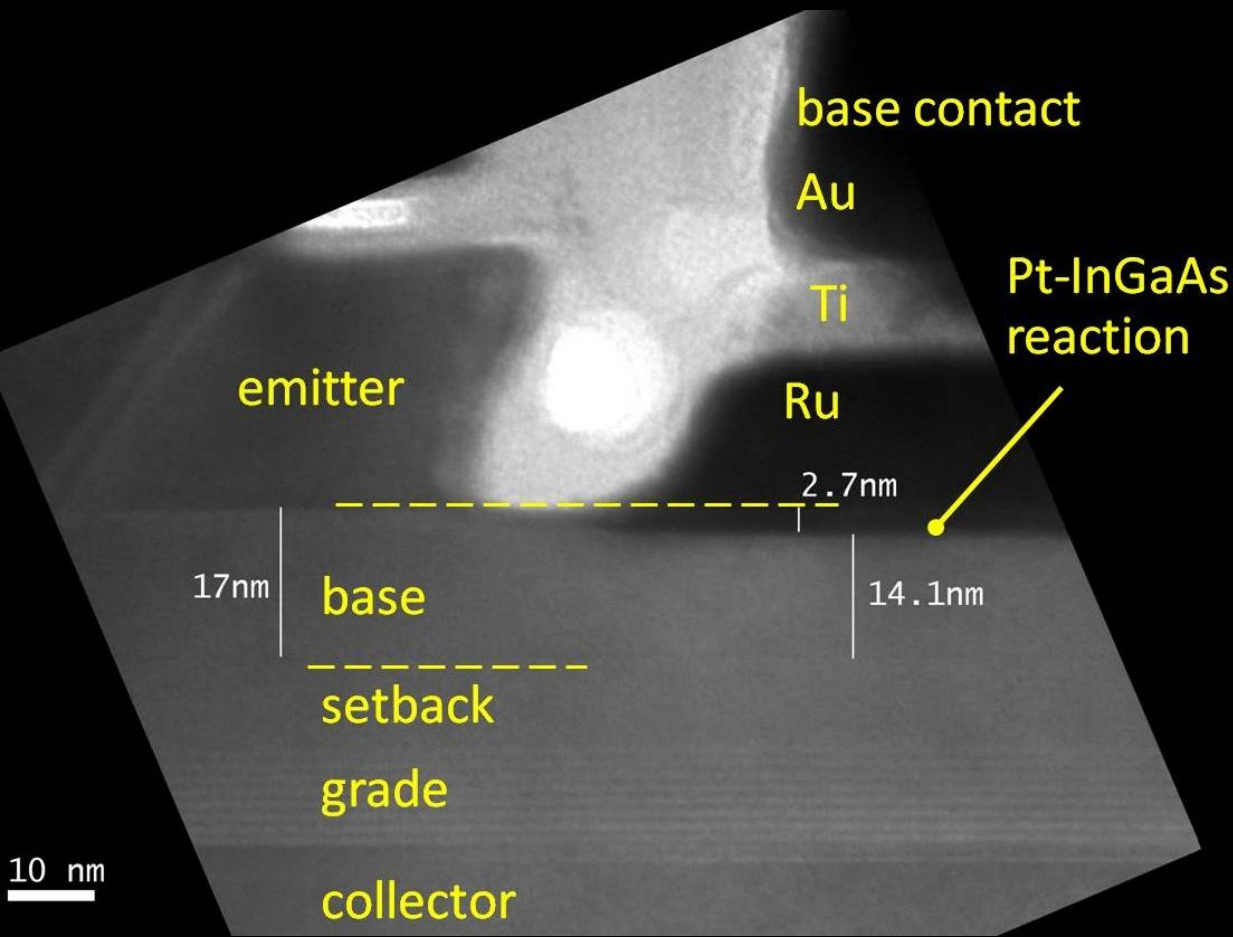
50 nm

large base post undercut

# Reducing Emitter Length Effects

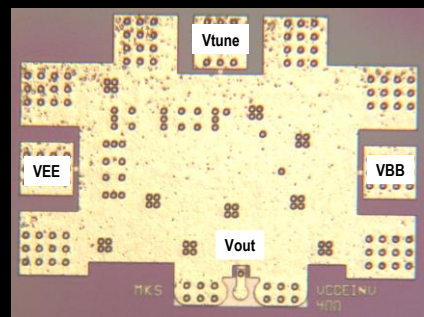


# InP HBTs: 1.07 THz @200nm, ?? @ 130nm

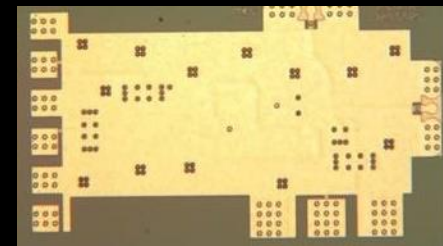


# 130nm / 1.1 THz InP HBT: ICs to 670 GHz

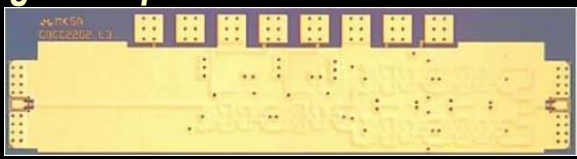
**614 GHz  
fundamental  
VCO**  
M. Seo, TSC / UCSB



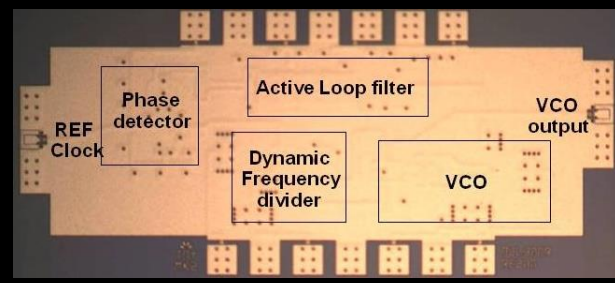
**340 GHz  
dynamic  
frequency  
divider**  
M. Seo, UCSB/TSC  
IMS 2010



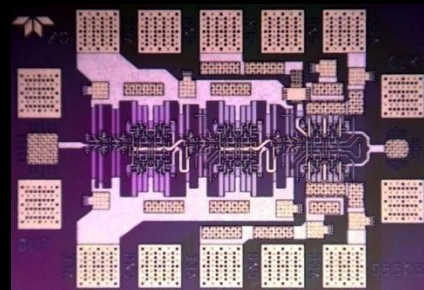
**620 GHz, 20 dB gain amplifier**  
M Seo, TSC  
IMS 2013  
also: 670GHz amplifier  
J. Hacker, TSC  
IMS 2013 (not shown)



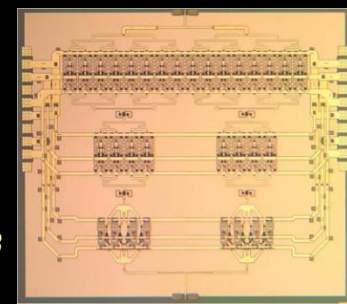
**300 GHz  
fundamental  
PLL**  
M. Seo, TSC  
IMS 2011



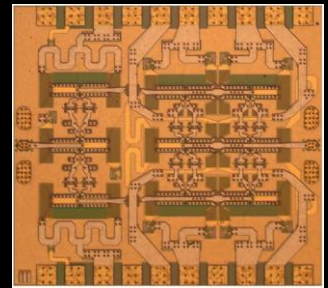
**204 GHz static  
frequency divider  
(ECL master-slave  
latch)**  
Z. Griffith, TSC  
CSIC 2010



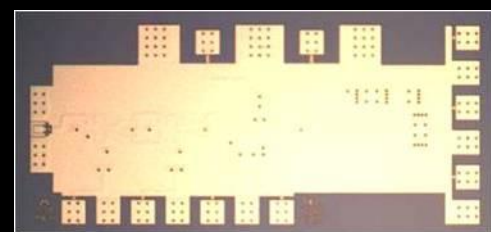
**220 GHz  
180 mW  
power  
amplifier**  
T. Reed, UCSB  
CSICS 2013



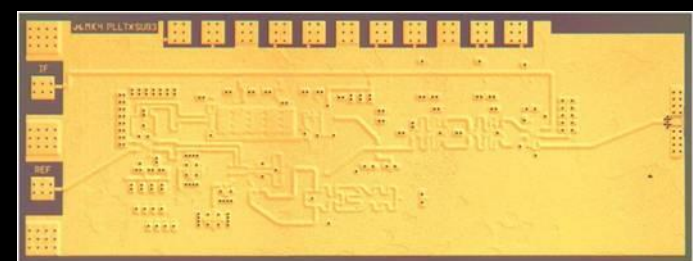
**81 GHz  
470 mW  
power  
amplifier**  
H-C Park UCSB  
IMS 2014



**Integrated  
300/350GHz  
Receivers:  
LNA/Mixer/VCO**  
M. Seo TSC

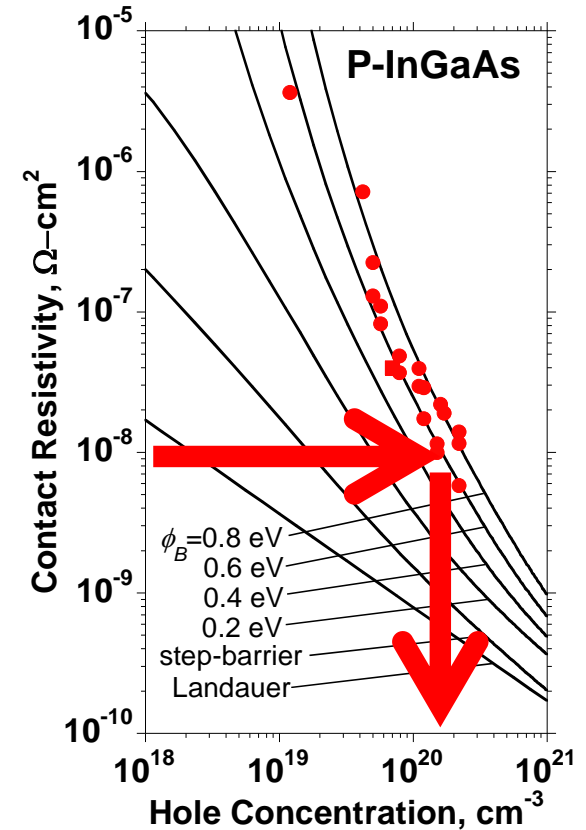
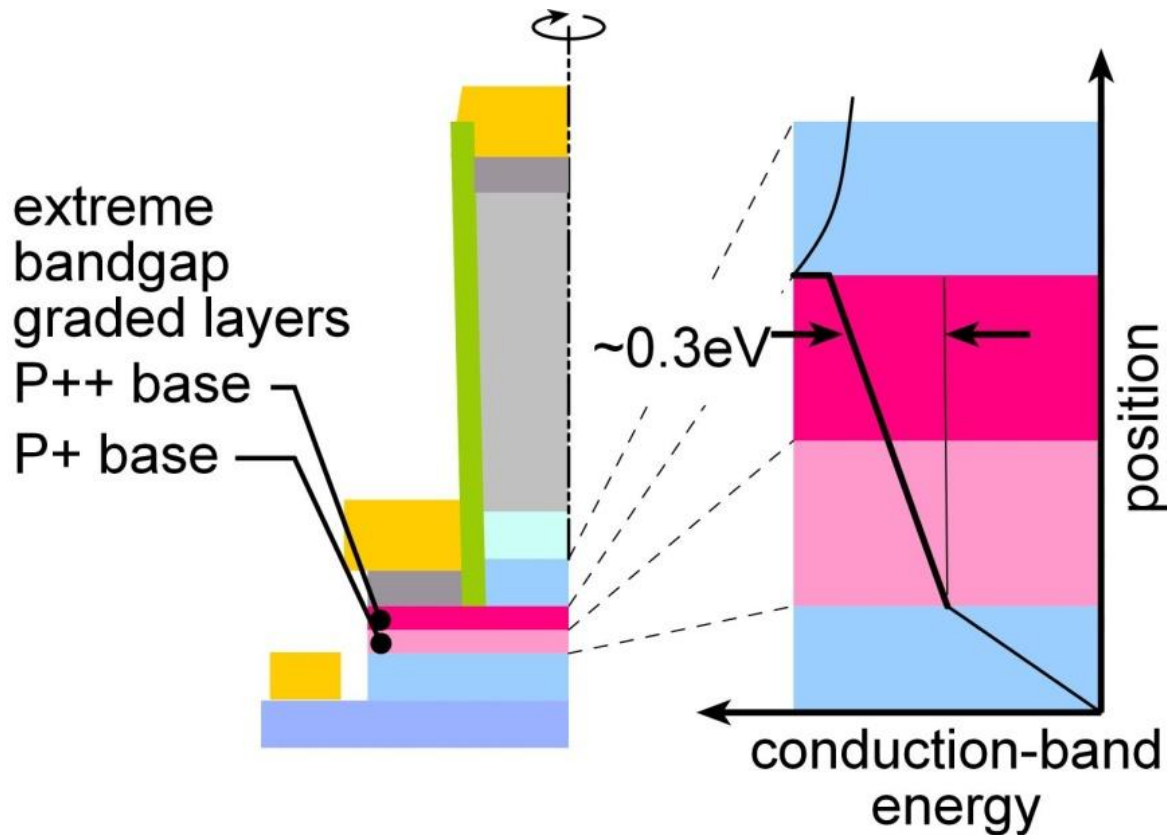


**600 GHz  
Integrated  
Transmitter  
PLL + Mixer**  
M. Seo TSC





# Towards a 3 THz InP Bipolar Transistor



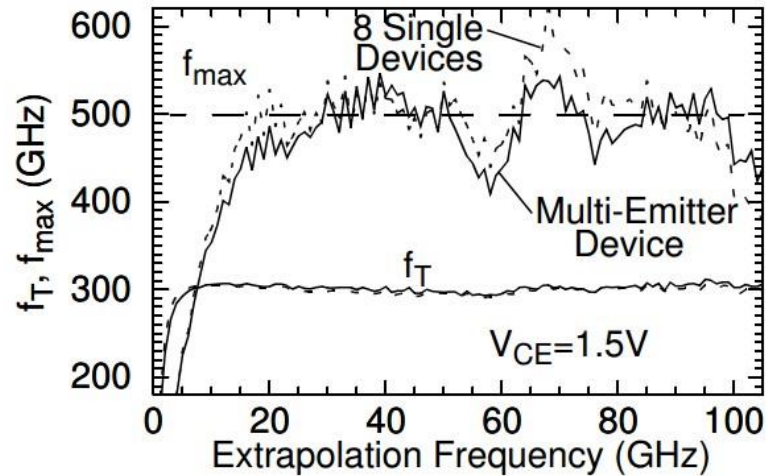
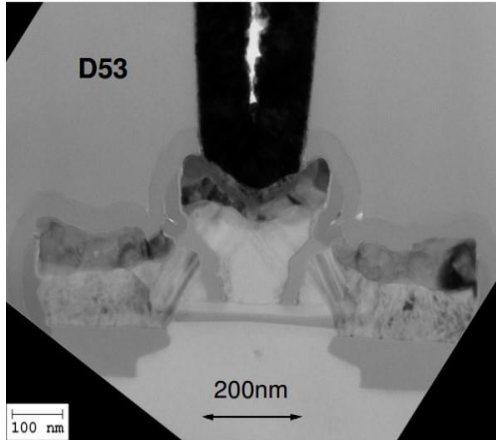
***Extreme base doping  $\rightarrow$  low-resistivity contacts  $\rightarrow$  high  $f_{max}$***

***Extreme base doping  $\rightarrow$  fast Auger ( $N\text{P}^2$ ) recombination  $\rightarrow$  low  $\beta$ .***

***Solution: very strong base compositional grading  $\rightarrow$  high  $\beta$***

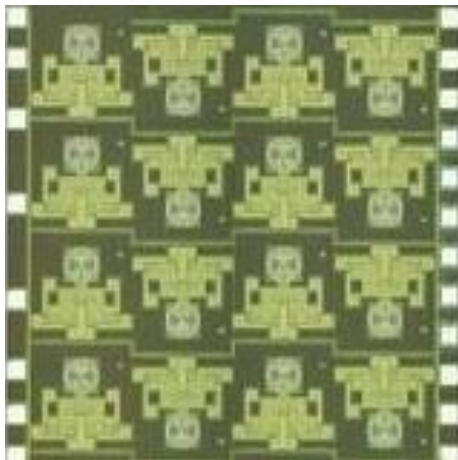
# 1/2-THz SiGe HBTs

## 500 GHz $f_{\max}$ SiGe HBTs Heinemann et al. (IHP), 2010 IEDM



## 16-element multiplier array @ 500GHz (1 mW total output)

U. Pfeiffer et. al. (Wuppertal / IHP), 2014 ISSCC



# Towards a 2 THz SiGe Bipolar Transistor

## Similar scaling

InP: 3:1 higher collector velocity

SiGe: good contacts, buried oxides

## Key distinction: Breakdown

InP has:

thicker collector at same  $f_{\tau}$ ,  
wider collector bandgap

## Key requirements:

low resistivity Ohmic contacts

note the high current densities

	InP	SiGe	
<b>emitter</b>			
junction width	64	<b>18</b>	nm
access resistivity	2	<b>0.6</b>	$\Omega\text{-}\mu\text{m}^2$
<b>base</b>			
contact width	64	18	nm
contact resistivity	2.5	<b>0.7</b>	$\Omega\text{-}\mu\text{m}^2$
<b>collector</b>			
thickness	53	15	nm
current density	36	<b>125</b>	$\text{mA}/\mu\text{m}^2$
breakdown	2.75	1.3?	V
$f_{\tau}$	1000	1000	GHz
$f_{\text{max}}$	2000	2000	GHz

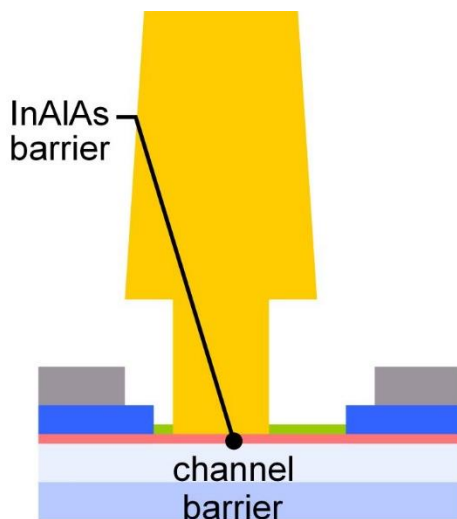
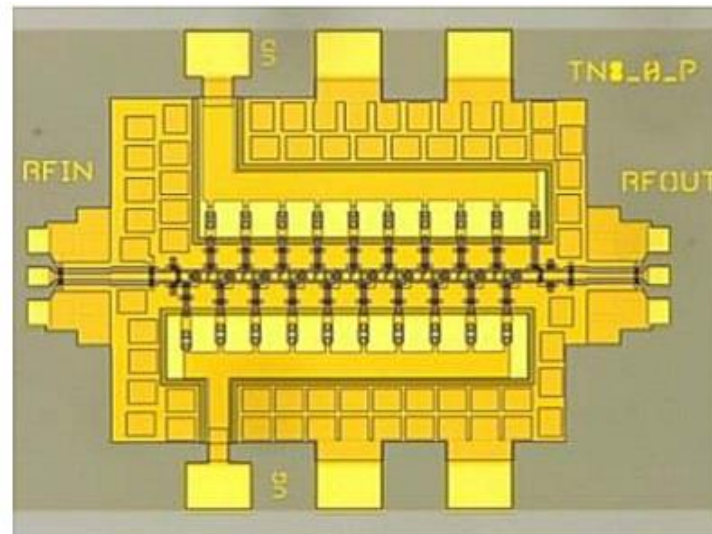
Assumes collector junction 3:1 wider than emitter.

Assumes SiGe contacts no wider than junctions

# Towards at 2.5 THz HEMT

## First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process

Xiaobing Mei, et al, IEEE EDL, April 2015 (Northrop-Grumman)

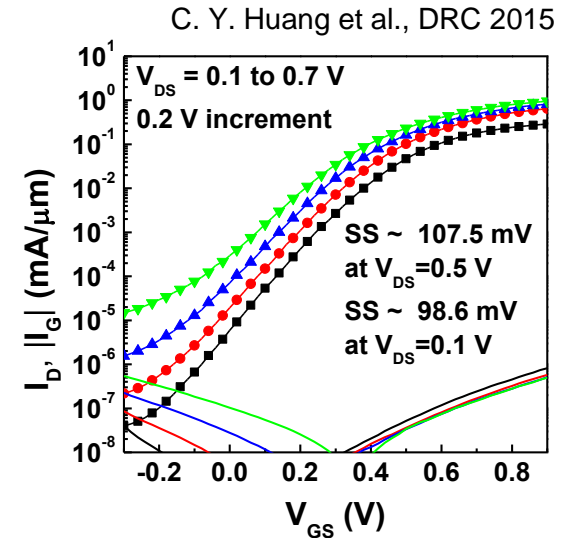
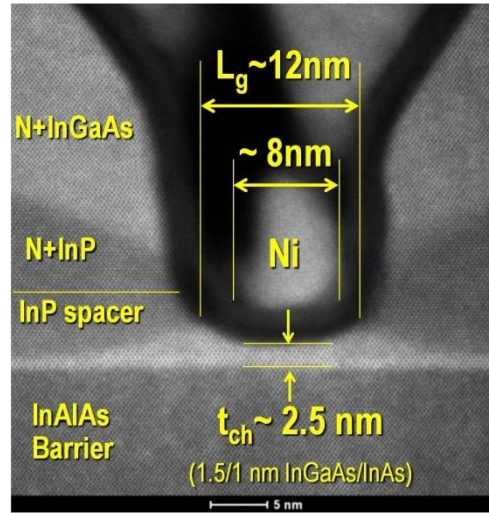
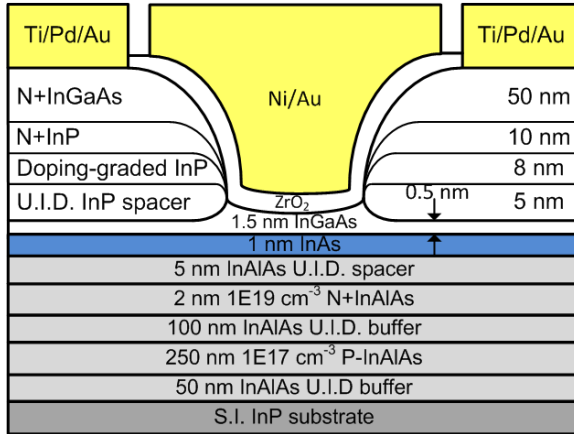


FET scaling laws; 2:1 higher bandwidth	change
gate length	decrease 2:1
current density (mA/mm), $g_m$ (mS/mm)	increase 2:1
transport mass	constant
gate-channel capacitance density	increase 2:1
contact resistivities	decrease 4:1

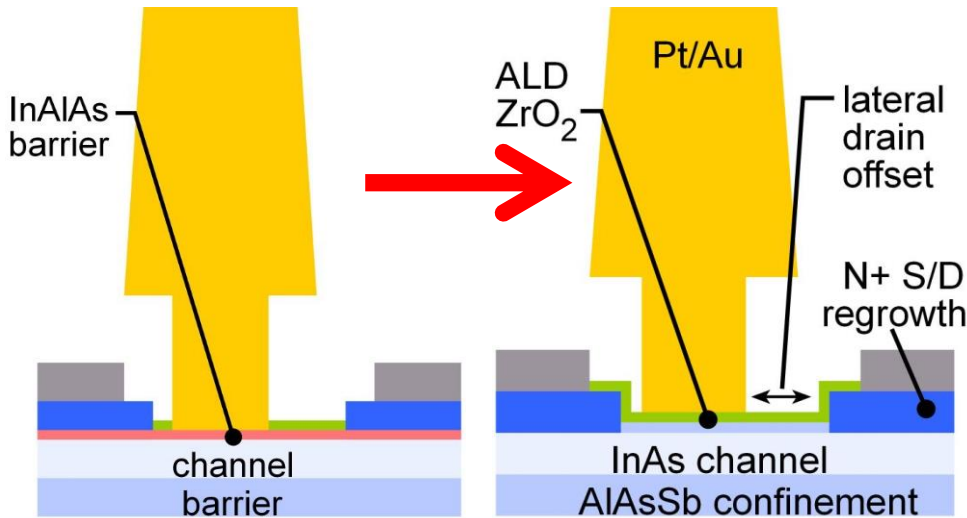
*Need thinner dielectrics, better contacts*

# Towards at 2.5 THz HEMT

## VLSI III-V MOS

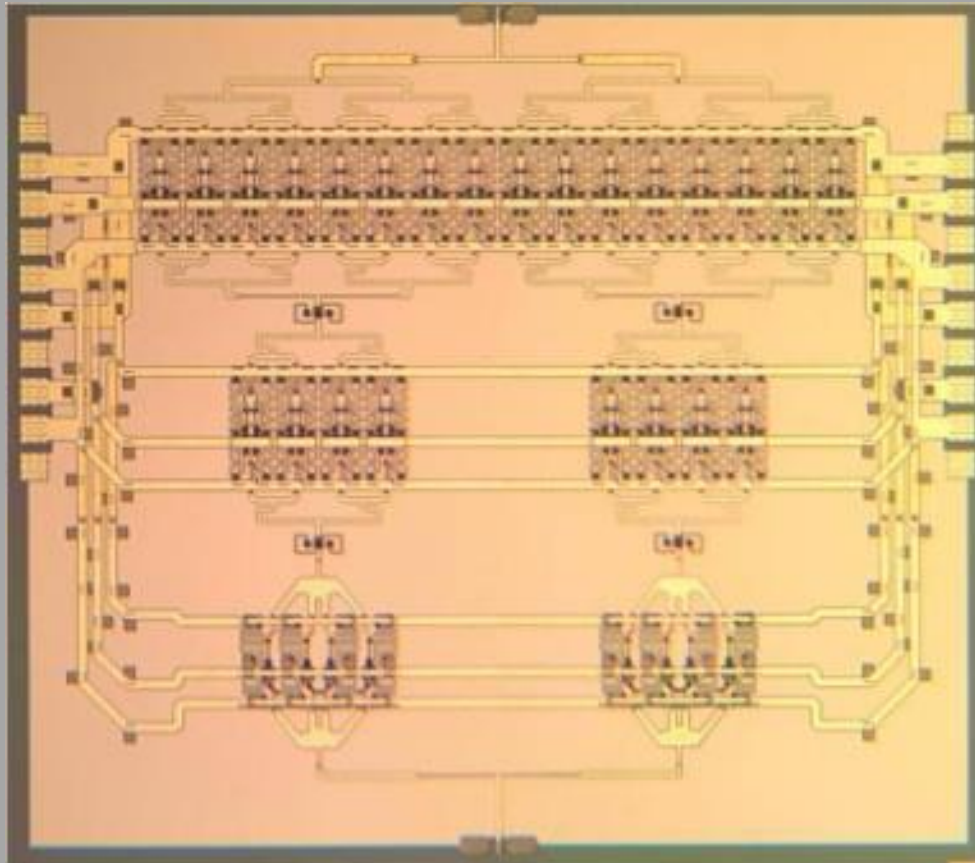


## THz III-V MOS



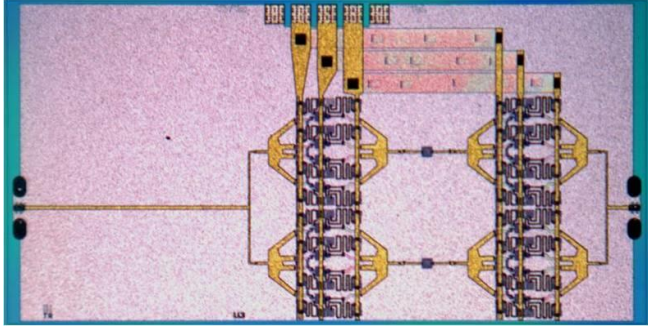
gate length	36	18	9	nm
EOT	0.8	0.4	0.2	nm
well thickness	5.6	2.8	1.4	nm
effective mass	0.05	0.08	0.08	times $m_0$
# bands	1	1	1	--
S/D resistivity	150	74	37	$\Omega\text{-}\mu\text{m}$
extrinsic $g_m$	2.5	4.2	6.4	$\text{mS}/\mu\text{m}$
on-current	0.55	0.8	1.1	$\text{mA}/\mu\text{m}$
$f_T$	0.70	1.2	2.0	THz
$f_{\text{max}}$	0.81	1.4	2.7	THz

# Power Amplifiers

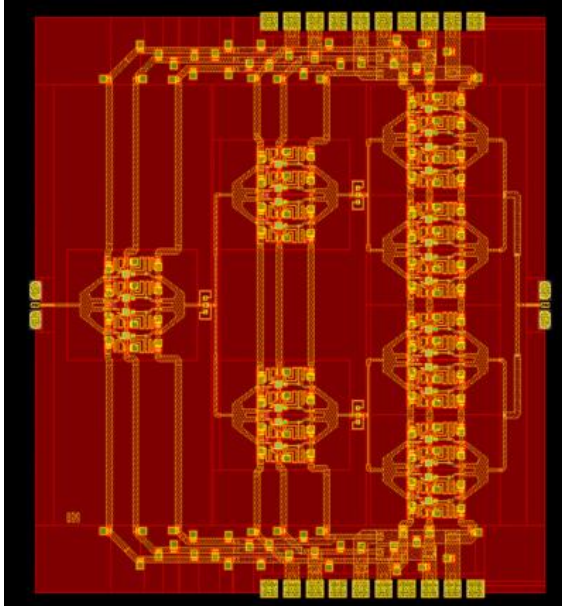


# 220 GHz power amplifiers; 256nm InP HBT

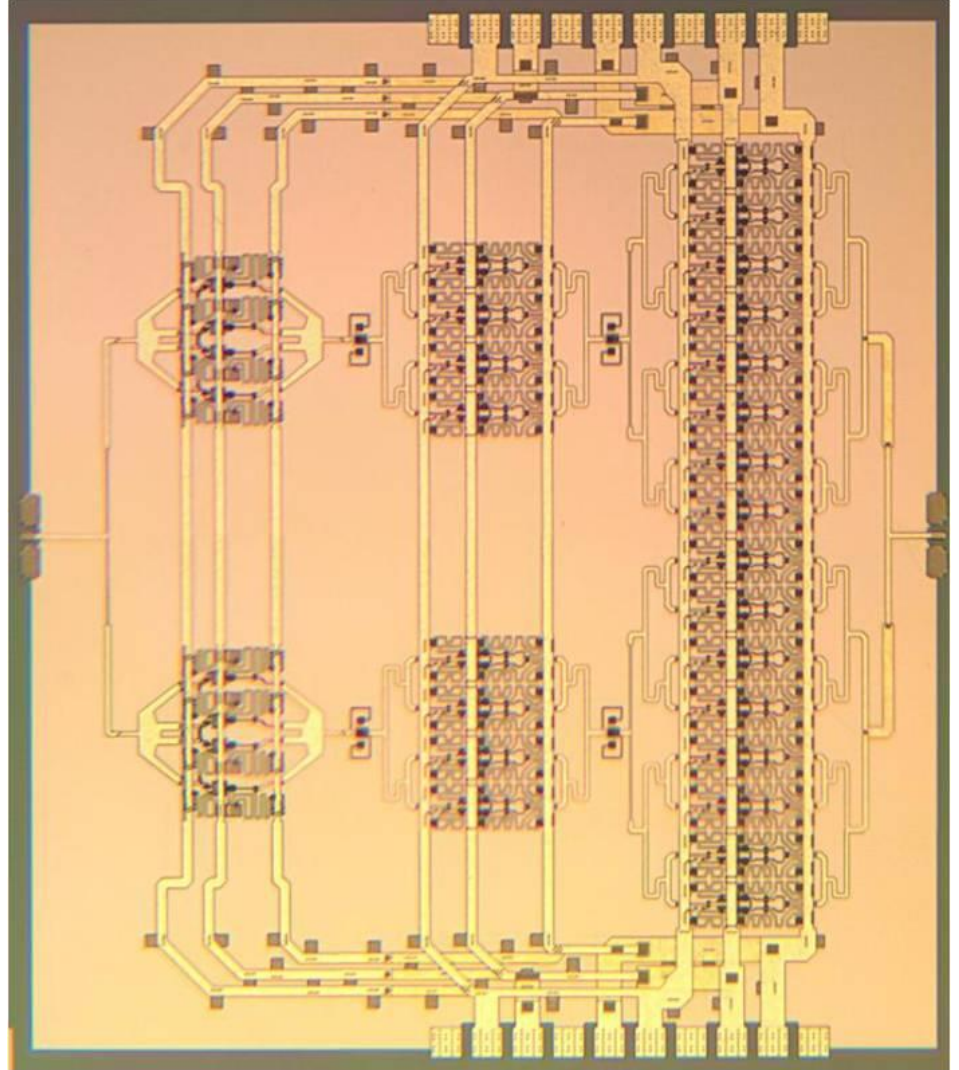
90 mW



164 mW, 0.43 W/mm, 2.4% PAE



180 mW (330 mW design; thermally limited)



# mm-Wave Power Amplifier: Challenges

**needed:** High power / High efficiency / Small die area ( low cost)

**Extensive power combining**

**Compact power-combining**

$$\text{PAE} = \eta_{\text{drain/collector}} \left( 1 - \frac{1}{\text{Gain}} \right) \cdot \eta_{\text{power-combiner}}$$

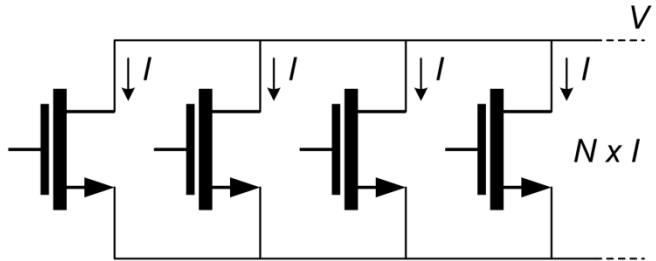
**Class E/D/F are poor @ mm-wave**  
insufficient  $f_{\text{max}}$ ,  
high losses in harmonic terminations

**Efficient power-combining**

***Goal: efficient, compact mm-wave power-combiners***



# Parallel Power-Combining

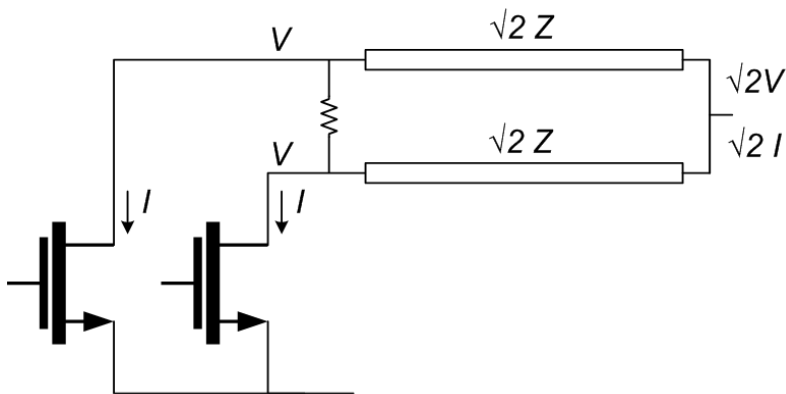


Output power:  $P_{OUT} = N \times V \times I$

Parallel connection increases  $P_{OUT}$  ✓

Load Impedance:  $Z_{OPT} = V / (N \times I)$

Parallel connection decreases  $Z_{opt}$  ✗



High  $P_{OUT} \rightarrow$  Low  $Z_{opt}$

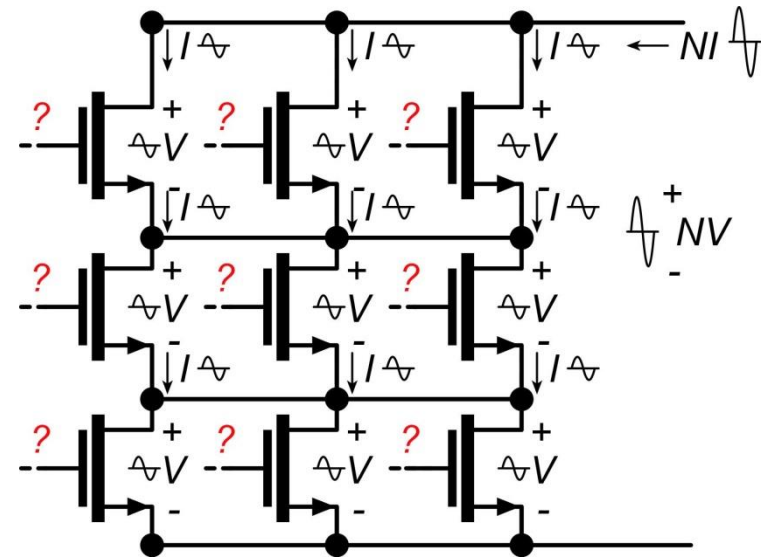
Needs impedance transformation:  
lumped lines, Wilkinson, ...

**High insertion loss** ✗

**Small bandwidth**

**Large die area**

# Series Power-Combining & Stacks



**Parallel** connections:  $I_{out} = N \times I$

**Series** connections:  $V_{out} = N \times V$

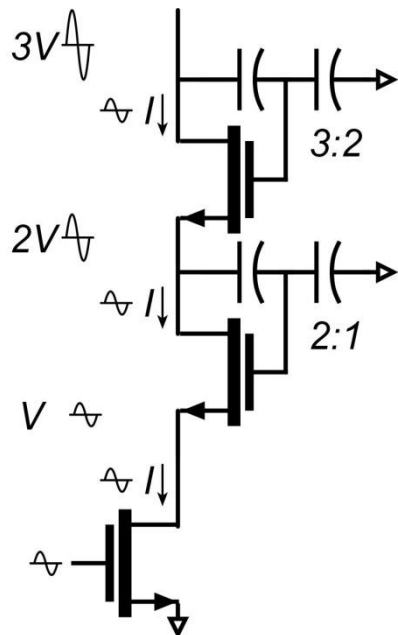
Output power:  $P_{out} = N^2 \times V \times I$

Load impedance:  $Z_{opt} = V/I$  ✓

Small or zero power-combining losses ✓

Small die area ✓

How do we drive the gates ?



Local voltage feedback:  
drives gates, sets voltage distribution

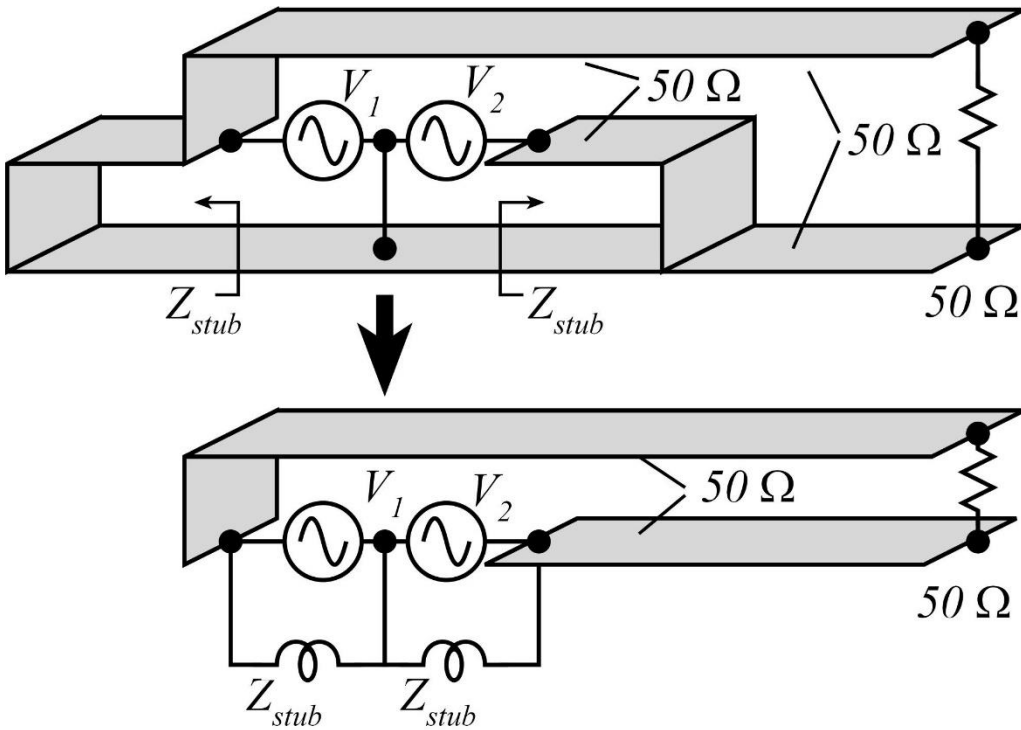
**Design challenge:**

need uniform RF voltage distribution

need ~unity RF current gain per element

...needed for simultaneous compression of all FETs.

# Sub- $\lambda/4$ Baluns for **Series** Combining



**Balun combiner:**

**2:1 series connection** ✓

each source sees  $25\ \Omega$

→ 4:1 increased  $P_{out}$  ✓

**Standard  $\lambda/4$  balun :**

long lines

→ high losses ✗

→ large die ✗

**Sub- $\lambda/4$  balun :**

stub → inductive

tunes transistor  $C_{out}$  ! ✓

short lines → low losses ✓

short lines → small die ✓

# 2:1 series-connected 86GHz power amplifier

20 dB Gain

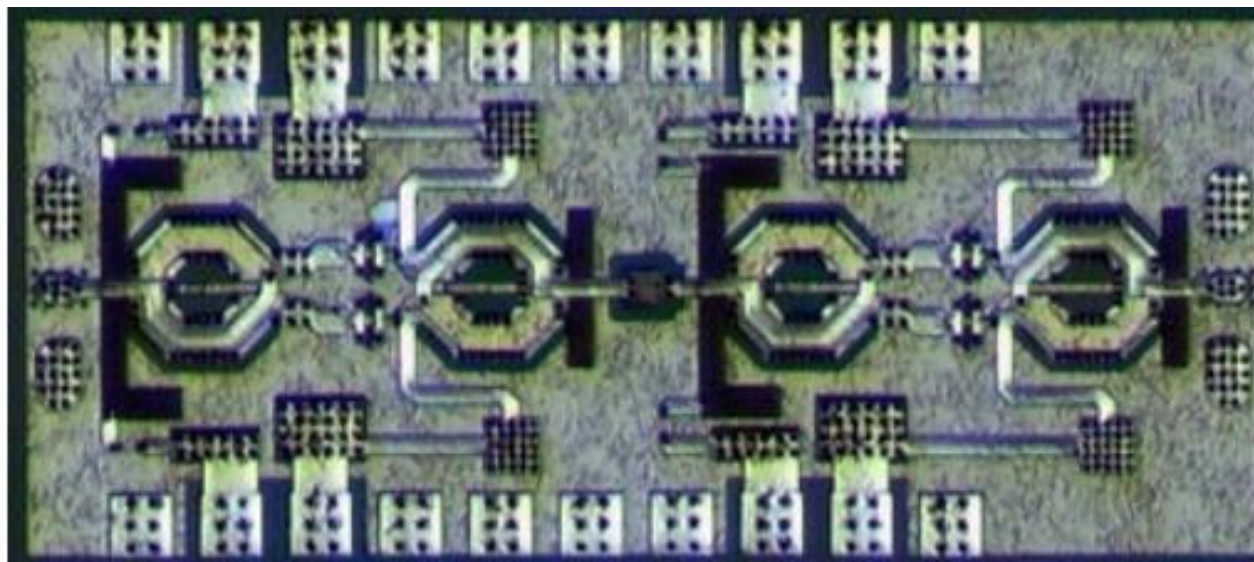
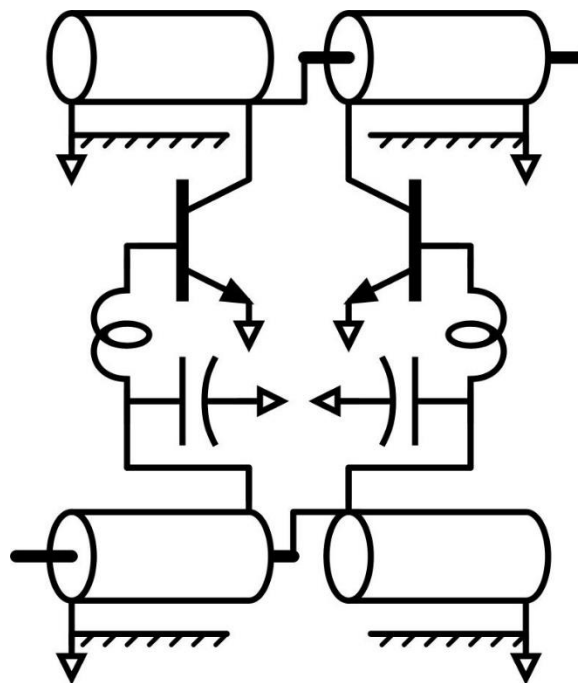
188mW  $P_{\text{sat}}$

1.96 W/mm

32.8% PAE

Teledyne 250 nm InP HBT

2 stages, 1.0 mm<sup>2</sup>



# 4:1 series-connected 81GHz power amplifier

Park et al., 2014 IEEE-IMS

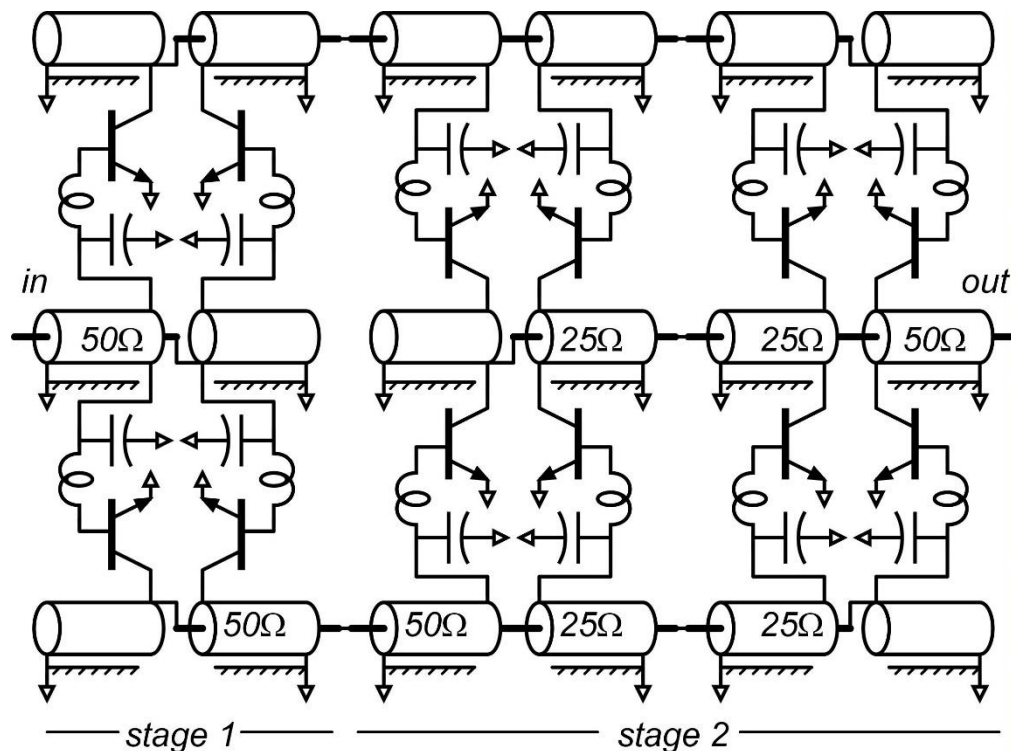
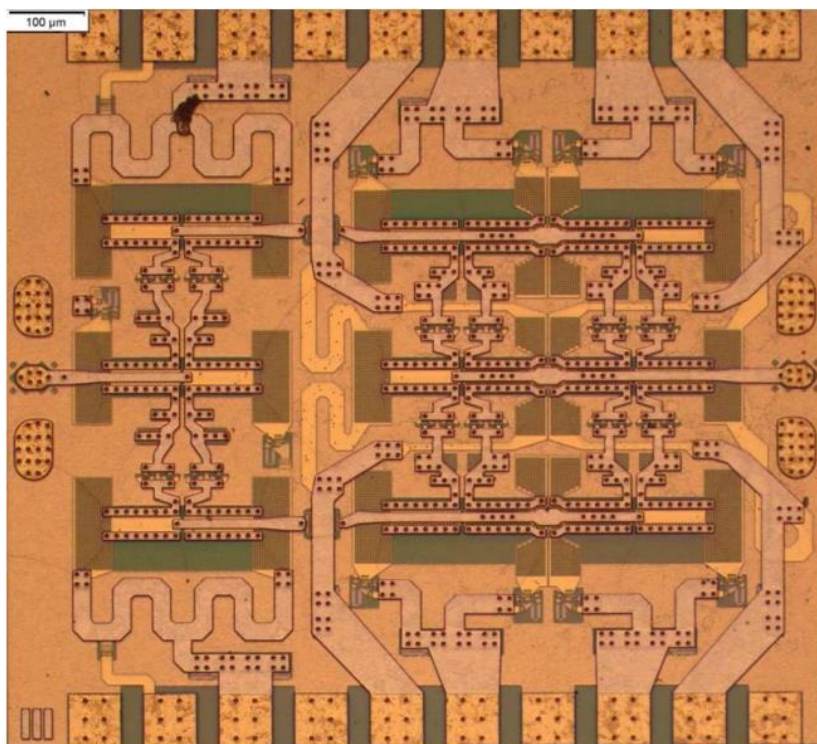
17 dB Gain

470 mW  $P_{\text{sat}}$

23% PAE

Teledyne 250 nm InP HBT

2 stages, 1.0 mm<sup>2</sup>(incl pads)

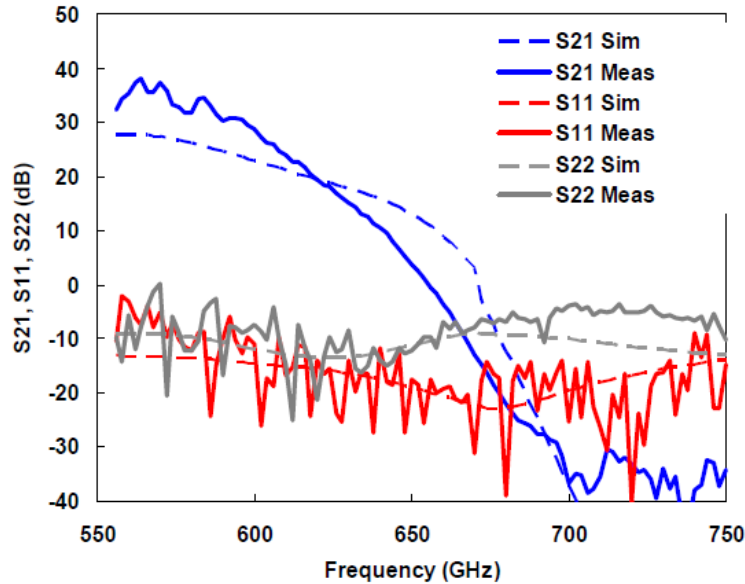


# Teledyne: 1.9 mW, 585 GHz Power Amplifier

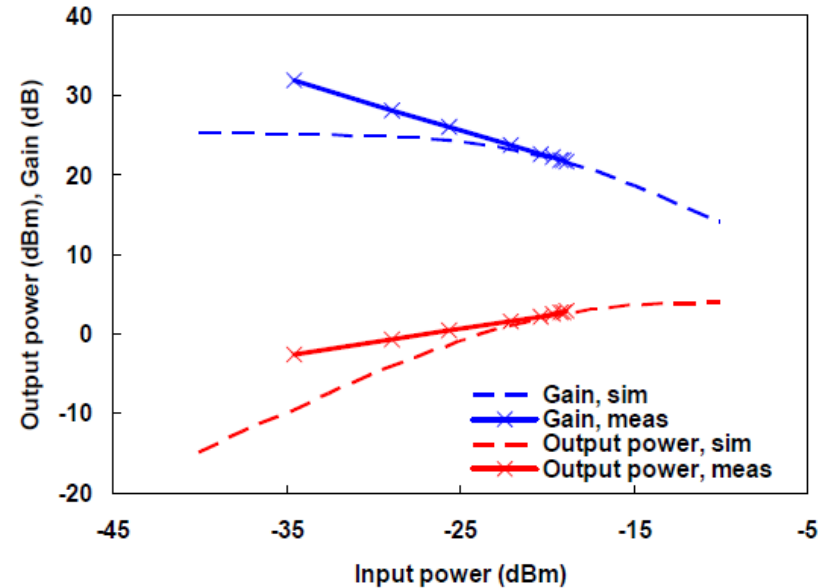
M. Seo *et al.*, Teledyne Scientific: IMS2013

Chart 38

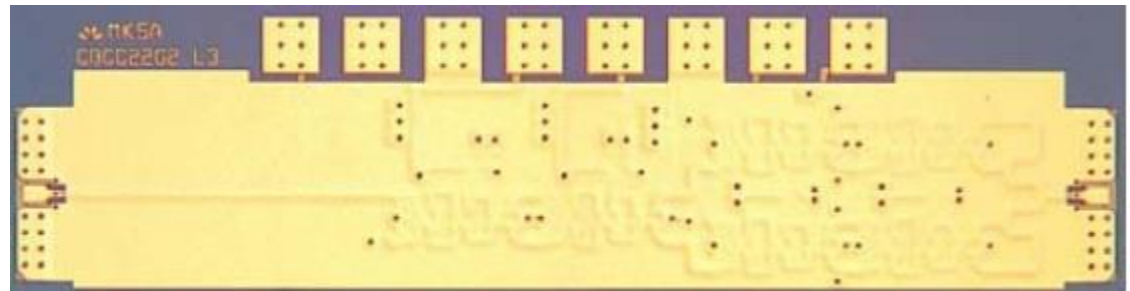
### S-parameters



### Output Power



- 12-Stage Common-base
- 2.8 dBm  $P_{sat}$
- >20 dB gain up to 620 GHz



**What limits output power in sub-mm-wave amplifiers ?**

# Sub-mm-wave PAs: need more current !

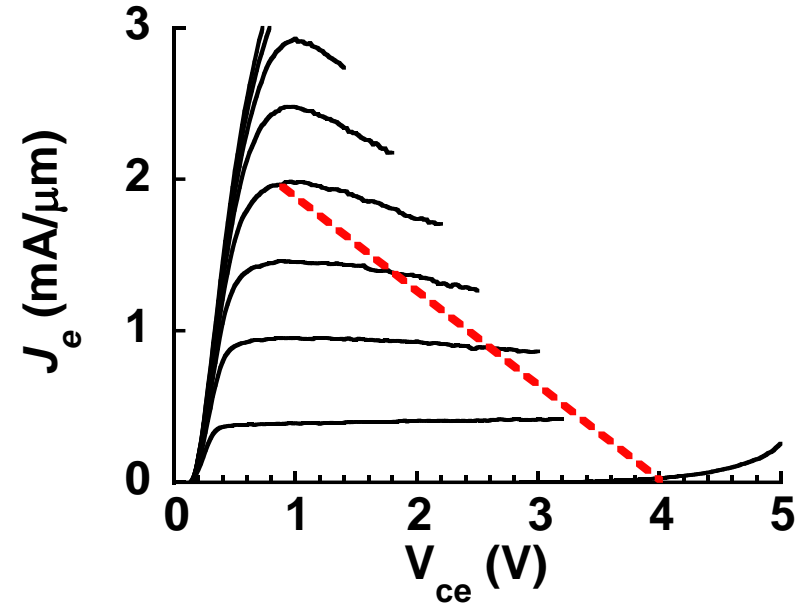
3  $\mu\text{m}$  max emitter length ( $> 1 \text{ THz } f_{\text{max}}$ )

2 mA/ $\mu\text{m}$  max current density

$$I_{\text{max}} = 6 \text{ mA}$$

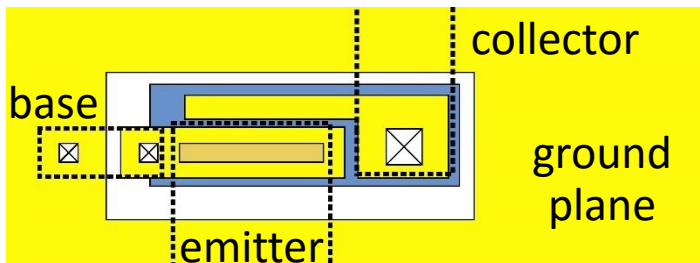
Maximum 3 Volt p-p output

$$\text{Load: } 3\text{V}/6\text{mA} = 500 \Omega$$

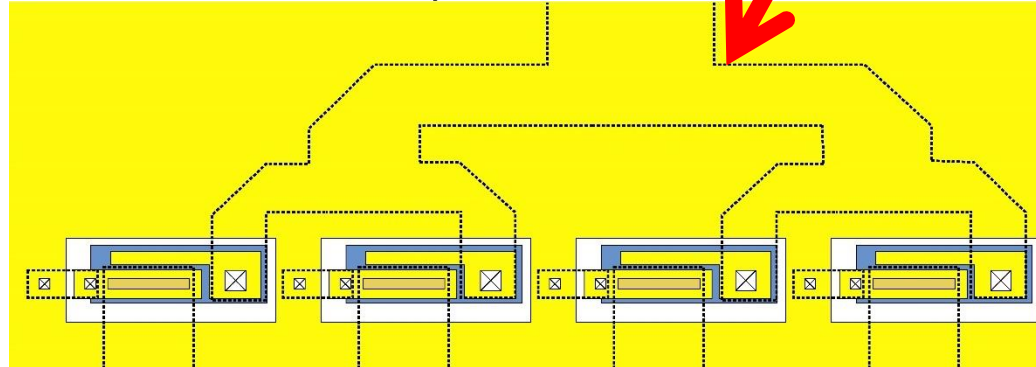


***Combiner cannot provide 500  $\Omega$  loading***

common-base HBT



HBTs with microstrip combiner



# Multi-finger HBTs: more current, lower $f_{\max}$

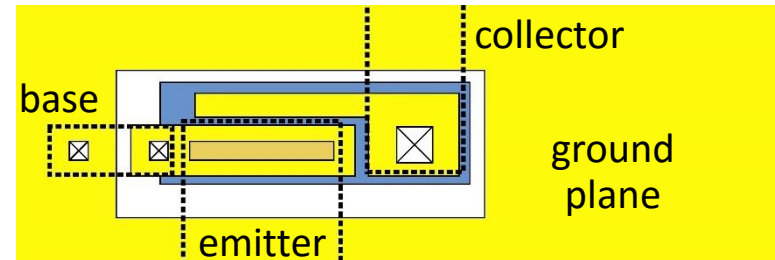
More current

→ lower cell load resistance

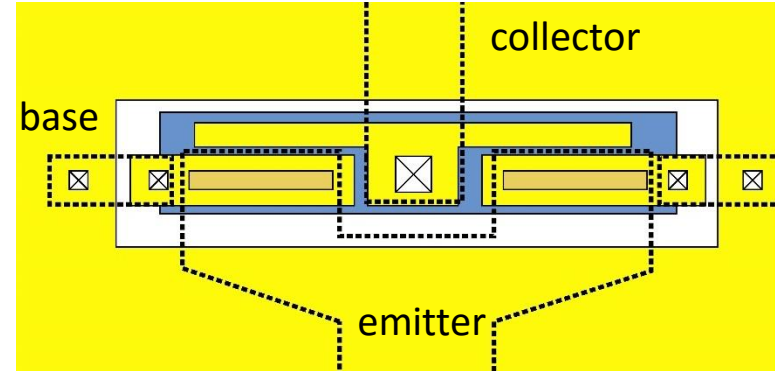
**Reduced  $f_{\max}$ , reduced RF gain:**  
common-lead inductance →  $Z_{12}$   
feedback capacitance →  $Y_{12}$   
phase imbalance between fingers.

**Worse at higher frequencies:**  
less tolerant of cell parasitics  
less current per cell  
higher required load resistance  
Can optimum load be reached ?

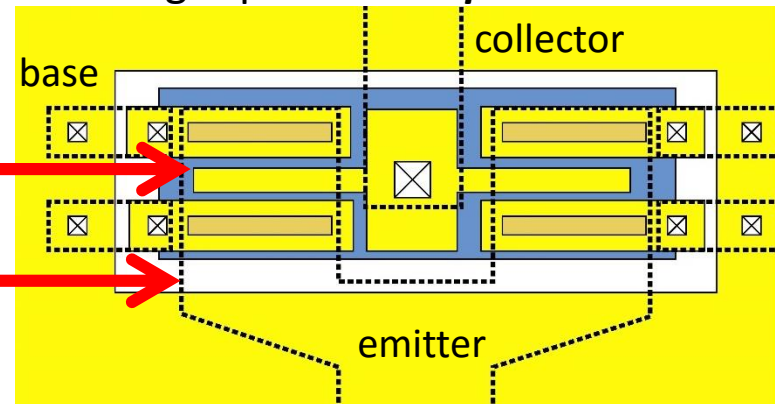
one-finger common-base HBT



two-finger power cell



four-finger power cell: *parasitics*





# Sub-mm-wave transistors: need more current

## InP HBTs:

thinner collector → more current  
hotter → improve heat-sinking  
or: longer emitters → thicker base metal

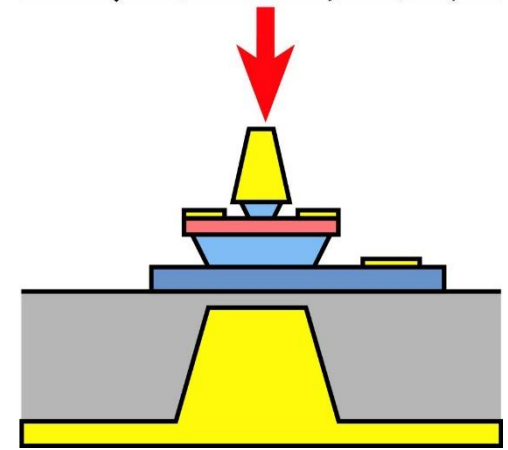
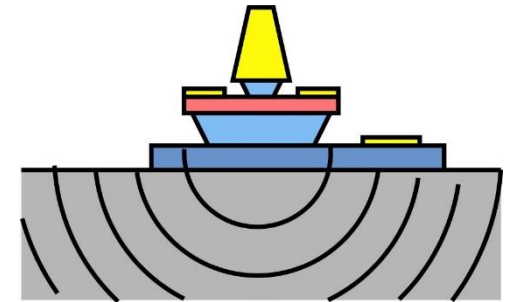
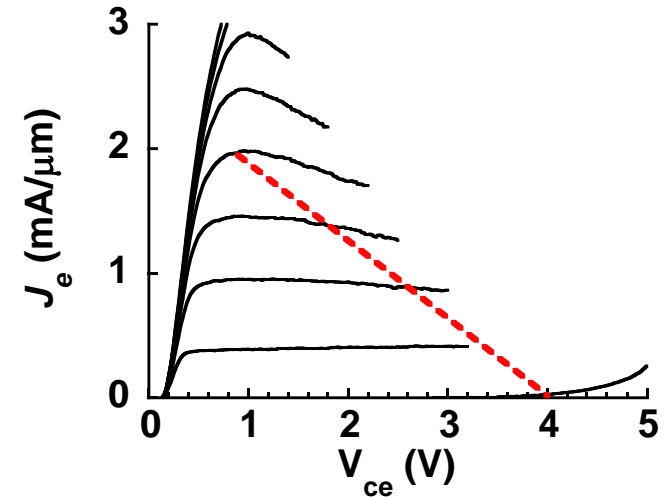
## GaN HEMTs:

much higher voltage  
100+ GHz: large multi-finger FETs not feasible  
***Need high current to exploit high voltage.***

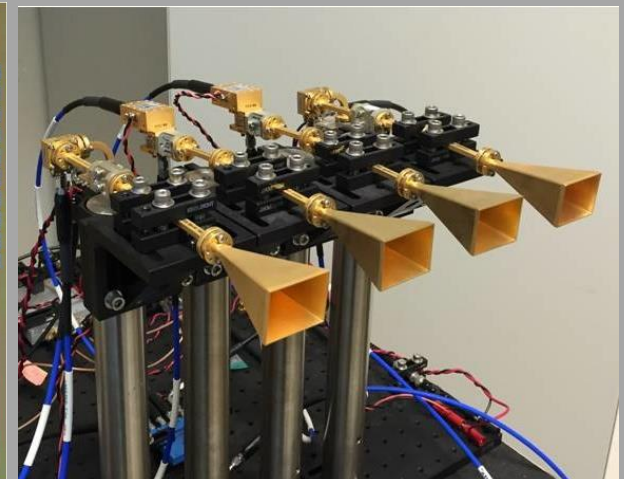
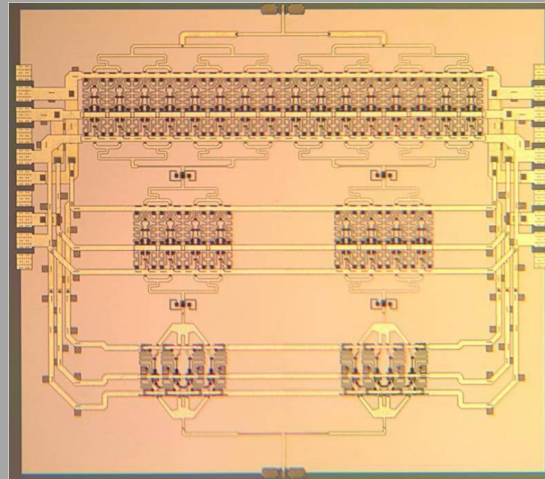
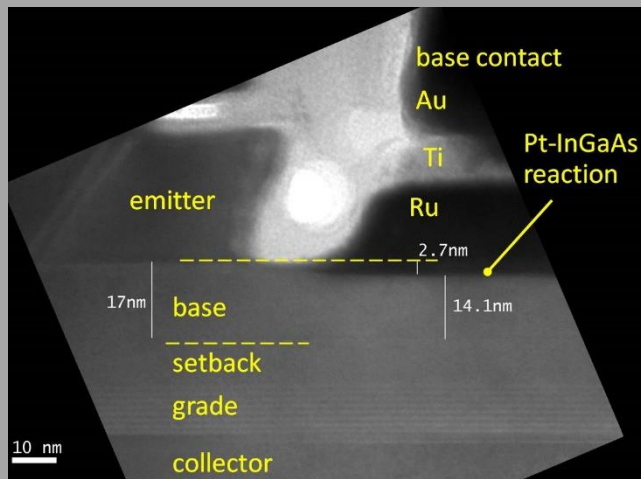
## Example:

2mA/μm, 100 μm max gate width, 50 Volts  
200mA maximum current  
50 Volts/200mA = 250 Ω load → unrealizable.

***Need more mA/μm or longer fingers***

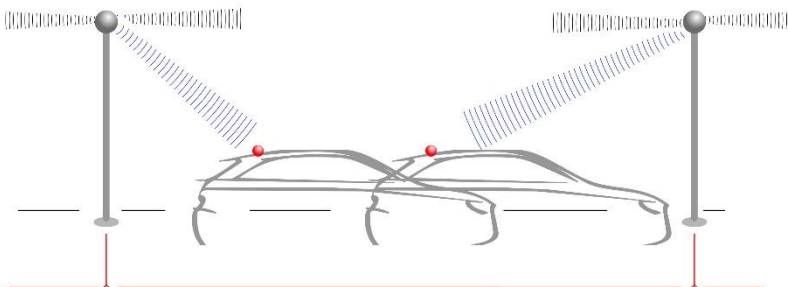
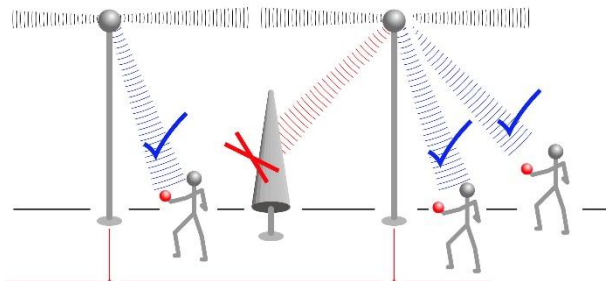


# 50-500GHz Wireless

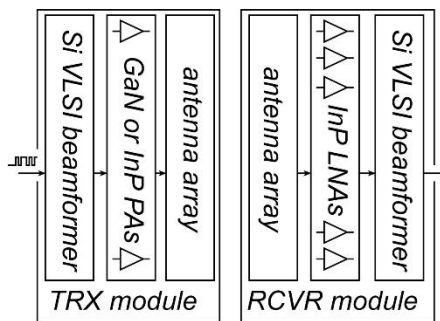
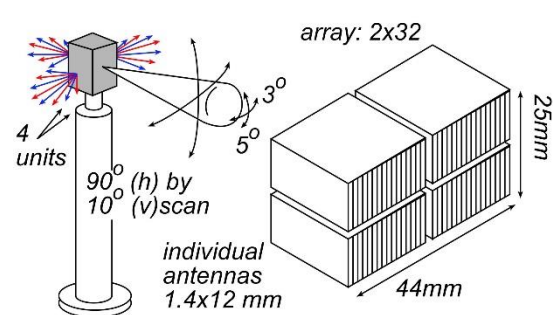


# 50-500 GHz Wireless Electronics

**Mobile communication @ 2Gb/s per user, 1 Tb/s per base station**

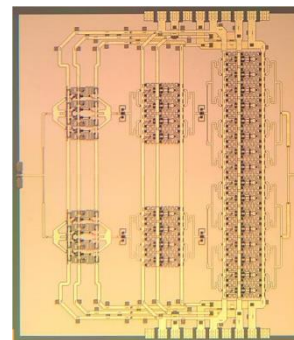
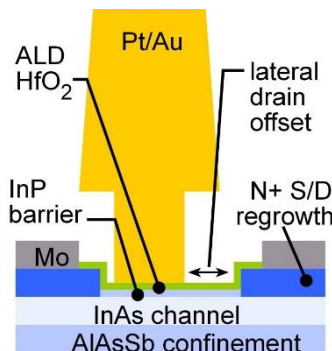
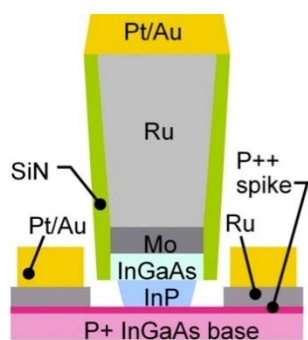
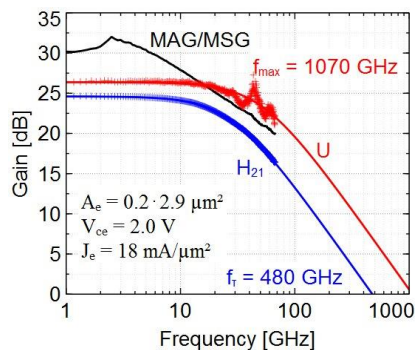


**Requires: large arrays, complex signal processing, high  $P_{out}$ , low  $F_{min}$**



**VLSI beamformers  
VLSI equalizers  
III-V LNAs & PAs**

**III-V Transistors may perform well enough even for 1 THz systems.**



**(backup slides follow)**

# asdfsadfasdfadsf

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asdfsadfasdf

**Talk is 40 min  
plus 10 min for  
questions...  
35-40 slides**

# Sub-mm-wave PAs: need more current !

<3  $\mu\text{m}$  emitter length for > 1 THz  $f_{\text{max}}$

2 mA/ $\mu\text{m}$  max current density

$I_{\text{max}} = 6 \text{ mA}$

Maximum 3 Volt p-p output

Load: 3V/6mA = 500  $\Omega$

**Combiner cannot provide 500  $\Omega$  loading**

