Ultrathin InAs-Channel MOSFETs on Si substrates

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ABSTRACT

Planar ultrathin InAs-channel MOSFETs were demonstrated on Si substrates with gate lengths (L_g) as small as 20 nm. The III-V epitaxial buffer layers were grown on 300 mm Si substrates by metal-organic chemical vapor deposition (MOCVD) and the subsequent InAlAs bottom barriers and InAs channel were grown by molecular beam epitaxy (MBE). The devices at 20 nm L_g show high transconductance, ~2.0 mS/μm at V_{DS}=0.5V.

INTRODUCTION

MOSFETs with InGaAs/InAs channels have recently shown rapid improvement, with high on-state current and high transconductance. [1-7]. Because of the low electron effective mass and the resulting high electron injection velocity, high on-state current can be achieved at low V_{DD} and V_{GS}. This offers the potential of reduced switching power consumption. To date, only few results have been reported for InGaAs/InAs MOSFETs on Si substrates [2,6-8]. If InGaAs/InAs channels are to be viable as a replacement for Si FET channels in VLSI, it must be established that high performance and high yield can be obtained. Here we fabricate planar InAs channel MOSFETs on Si, with a thin 3.5 nm InAs/0.5 nm InGaAs channel, comparing their performance to that of recent record InAs-channel devices [1] fabricated on InP substrates.

MATERIAL GROWTH AND DEVICE FABRICATION

Fig. 1 shows the device epitaxial layers. The III-V buffer layers on Si were grown by Applied Materials 300 mm III-V MOCVD system. The buffer layers grown over the entire on-axis (100) Si substrates, 400 nm unintentionally doped (UID) GaAs, 300 nm UID InP, 20 nm p-doped InGaAs, 50 nm UID InAlAs and a 10 nm UID InP cap. The samples were then shipped to UC Santa Barbara, cleaved, cleaned by dilute HCl, and immediately loaded into a Veeco GENII solid source MBE system. The cap, channel and barrier epitaxial layers reported in [1] were then grown. **Fig. 2** shows the roughness of the buffer and MBE layers, measured by AFM, and shows a device TEM image. The root-mean-square roughness (R_q) is degraded from ~3.1 nm for the III-V buffer to ~6.9 nm after MBE growth. No obvious anisotropic growth was observed on the surface. Note that the same epitaxial structure, when grown on InP substrates [1] has typically R_q~0.2 nm. The TEM image (**Fig. 2**) shows a high defect density in the epitaxial layers.

Device fabrication, similar to [1], began with dummy gate formation by e-beam lithography. Hydrogen silsesquioxane (HSQ) dummy gates were fabricated with 20-1000 nm L_g. The samples were then cleaned and loaded into the MOCVD reactor for source/drain (S/D) regrowth, comprising a 12 nm UID InGaAs vertical spacer and a heavily N+ doped InGaAs S/D. After mesa isolation, the HSQ dummy gate was removed in BHF, 1.5 nm of the InGaAs cap removed by a surface digital etch, and ~10Å AlON and ~25Å ZrO_2 deposited by ALD. The Ni gate and Ti/Pd/Au S/D contacts were defined by photoresist liftoff processes. The samples grown on the Si substrates have ~35:1 larger surface roughness than the control samples [1] grown on InP. A thicker channel (~3.5 nm InAs, ~0.5 nm InGaAs), as compared to the 2.5 nm InAs in [1], was adopted to avoid severe mobility degradation in the thin channel arising from interface roughness scattering [9].

DEVICE RESULTS AND DISCUSSIONS

Fig. 3 and **Fig. 4** show the I_D-V_{GS} and I_D-V_{DS} characteristics of 20 nm L_g devices on Si substrates. The device shows 2.0 mS/μm extrinsic transconductance (g_m) and 142 mV/dec. subthreshold swing (SS). The maximum on-state saturation current (**Fig. 4**) is ~1.5 mA/μm. **Fig. 5** compares g_m vs. L_g for devices on Si and InP [1]. The long-channel devices on Si show slightly higher g_m than in [1], implying that the mobility of the 3.5 nm InAs channel on Si is higher than that of 2.5 nm InAs channel on InP. Interface roughness scattering (IRS) varies as the sixth power of channel thickness ($\mu \sim T_{ch}^6$) [9]. Although the channel grown on Si is ~35:1 rougher than in [1], high mobility is maintained by using a thicker channel.

At small gate lengths, the transconductance of the MOSFETs on Si is inferior to those of [1]. **Fig. 6** shows R_{on} vs. L_g. The R_{on} extrapolated to zero L_g is ~247 Ω·μm, higher than ~168 Ω·μm reported in [1]. Further, from TLM measurements (**Fig. 6**) on the samples grown on Si, the regrown S/D shows 20-25% larger sheet resistance and specific contact resistivity than samples grown on InP [1]. We therefore ascribe the poorer of g_m at short L_g for the devices fabricated on Si to both increased parasitic S/D resistance (R_{SD}) and reduced gate-channel capacitance. Because of lattice mismatch and anti-phase domains, III-V heteroepitaxial layers grown on Si contain a high density of dislocations and planar defects. These defects easily propagate to the surface through the MBE channel growth and the MOCVD S/D regrowth (**Fig. 3**). These defects may cause the increased sheet resistance of the regrown S/D layers on Si, and consequently reduce the MOSFET g_m.

Fig. 7 and **Fig. 8** show *SS* and DIBL as a function of L_g. Higher *SS* and *DIBL* for the 3.5 nm InAs channel devices may be ascribed to the thicker channel, this reducing the electrostatic control of the channel by the gate. The degraded *SS* may also arise from higher interface trap density because of the rough channel surface [10]. **Fig. 9** shows I_{on} at fixed I_{off}=100 nA/μm for recent III-V FETs on Si. The devices in this work show peak I_{on}=240 μA/μm at 100 nm L_g. All the devices on Si show smaller I_{on} than in [1] due to larger *SS* and smaller g_m. **Fig. 10** shows g_m and *SS* maps of 45 nm-L_g devices. All devices show g_m=1.82±0.10 mS/μm, while 14 of 15 devices show g_m >1.7 mS/μm. The *SS* is 123±11 mV/dec.; the variation may arise from either variations in channel surface roughness or gate length. Further improve surface roughness might improve *SS* as well as I_{on}, and allow the channel to be further thinned without losing on-state performance.

CONCLUSION

We have demonstrated ultrathin InAs-channel MOSFETs on Si, showing 2.0 mS/μm extrinsic transconductance at V_{DS}=0.5V. Increasing the channel thickness reduces scattering in the rough channel, but degrades SS and I_{on}. Further improved channel growth and surface roughness might improve *SS* as well as I_{on}, and improve S/D regrowth could reduce R_{SD} and increases G_m for short L_g devices.

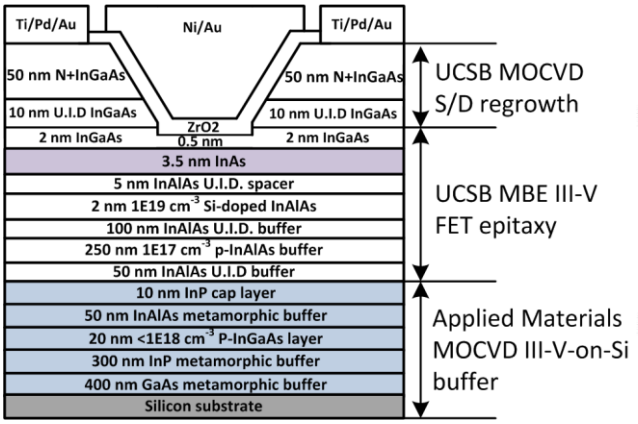

Fig. 1: Device structure of ultrathin InAs channel MOSFETs on Si substrates.

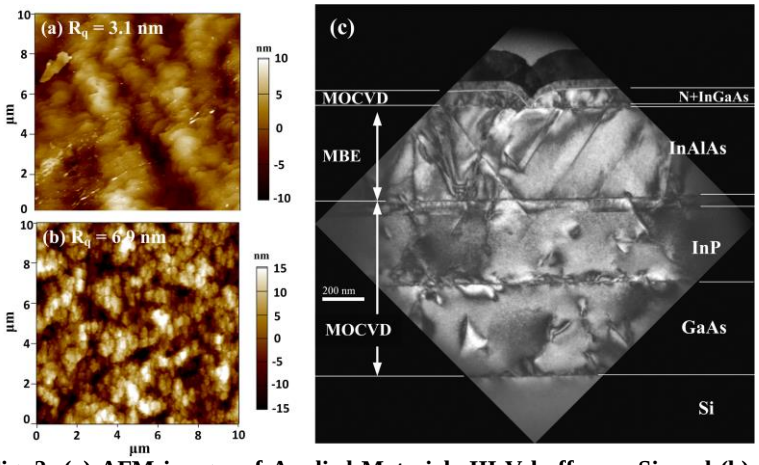

Fig. 2: (a) AFM images of Applied Materials III-V buffer on Si, and (b) the channel surface after MBE III-V FET epitaxy. (c) TEM images of the devices.

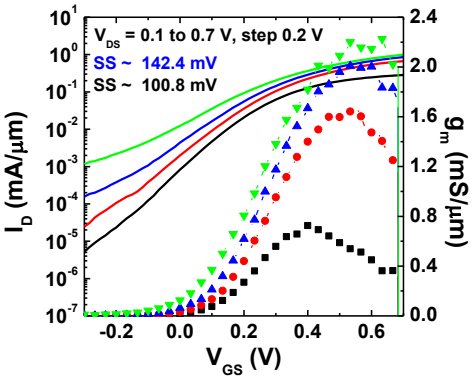

Fig. 3: I_D-V_{GS} of 20 nm-L_g devices.

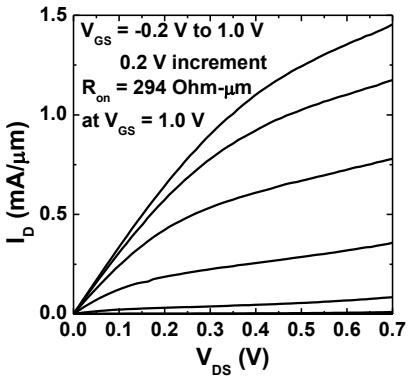

Fig. 4: I_D-V_{DS} of 20 nm-L_g devices.

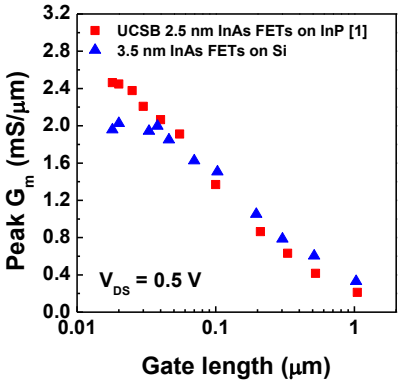

Fig. 5: Comparison of g_m vs. L_g for this work and [1].

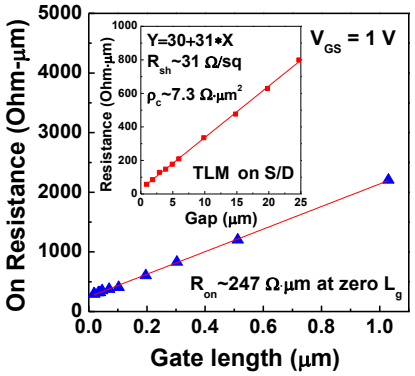

Fig.6: FET R_{on} vs. L_g. The inset is TLM data for a regrown S/D.

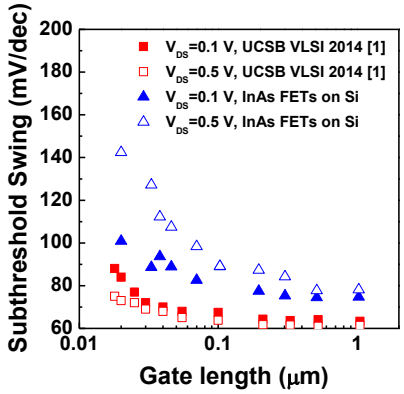

Fig.7: Comparison of *SS* vs. L_g between this work and [1].

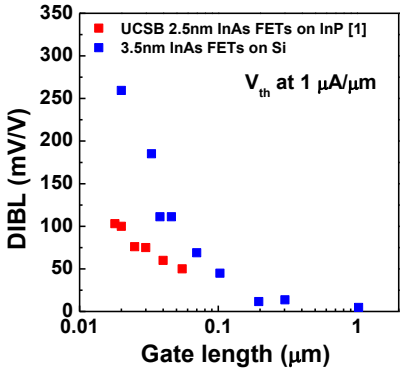

Fig.8: Comparison of *DIBL* vs. L_g between this work and [1].

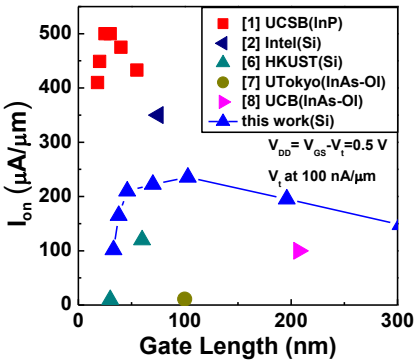

Fig. 9: I_{on} at fixed I_{off}=100 nA/μm for recently reported planar III-V FETs on Si, compared to results on InP.

G_m map (mS/μm) @ V_{DS}=0.5V

20 mm

	1	2	3	4	5
A	1.90	1.73	1.74	1.90	1.93
B	1.85	1.88	1.81	1.76	1.88
C	1.80	1.55	1.86	1.86	1.91

12 mm

SS map (mV/dec) @ V_{DS}=0.5V

20 mm

	1	2	3	4	5
A	115.7	128.3	106.9	130.6	140.2
B	107.4	117.5	107.5	141.6	120.9
C	132.1	116.4	135.2	124.4	127.4

12 mm

Fig. 10: g_m and *SS* map of 45 nm-L_g devices on the Si samples.

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ACKNOWLEDGEMENT

This work was done in UCSB Nanofabrication facility, part of the NSF funded NNIN network and MRL Central Facilities supported by the MRSEC Program of the NSF under award No. DMR 1121053.