Ultrathin InAs-Channel MOSFETs on Si Substrates

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HsinChu, Taiwan

Why InGaAs/InAs FETs?

- **III-V channel: low electron effective mass, high velocity, high mobility→ higher current at lower V_{DD}**
- **Problems:**

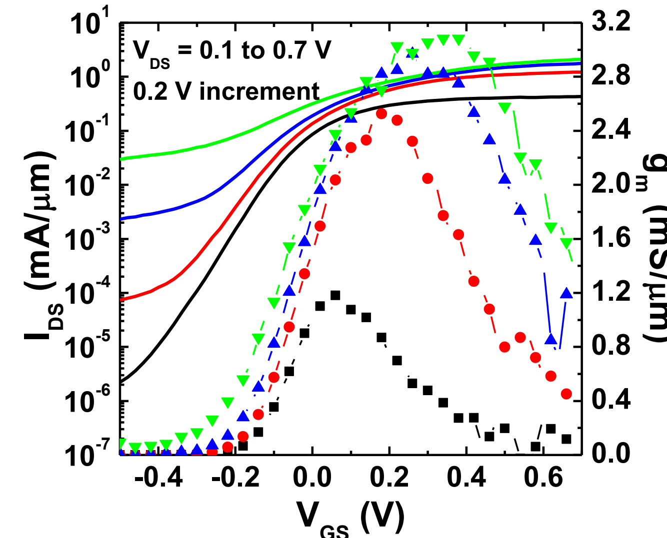
\- **Devices: low bandgap → high BTBT leakage**

high permittivity → worse electrostatics, large SS and DIBL

\- **Materials: Integration of III-V on Si, High-K dielectrics on III-V**

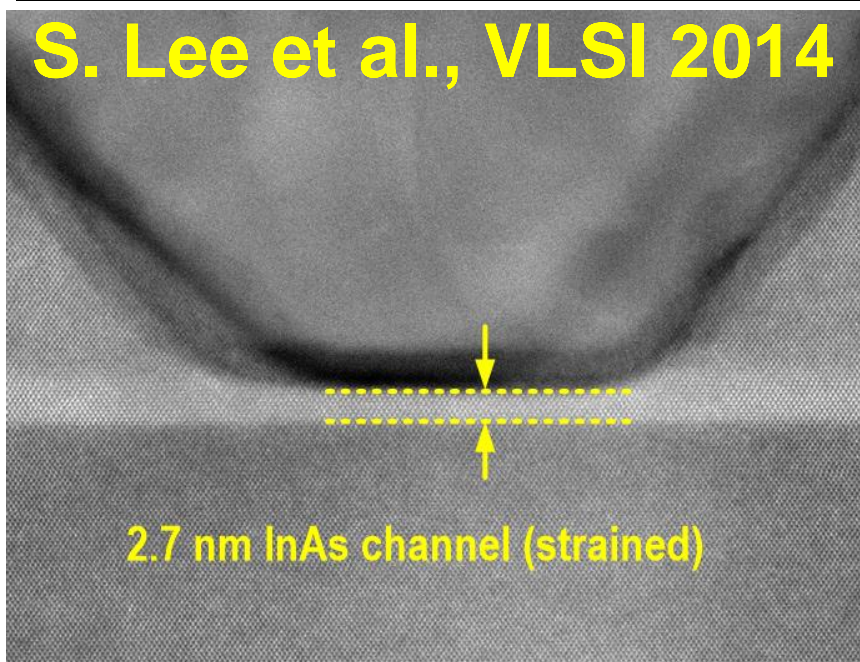
- **Goal: Fabricate ultrathin channel III-V FETs on Si**

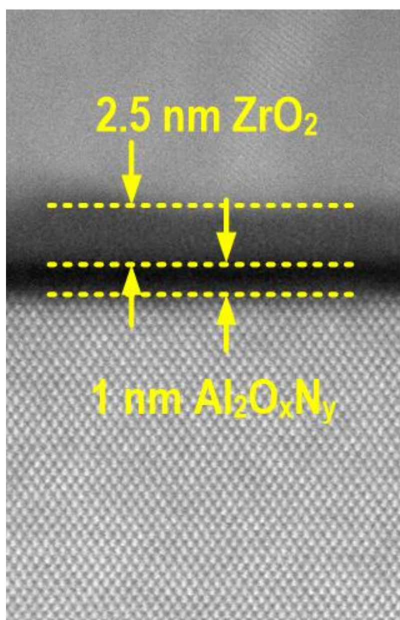
300K	Si	Ge	GaAs	InAs	$In_{0.53}Ga_{0.47}As$
m_e*	0.19	0.08	0.063	0.023	0.041
μ_e(cm²/V·s)	1450	3900	9200	33000	12000
μ_h(cm²/V·s)	370	1800	400	450	<300
Eg(eV)	1.12	0.664	1.424	0.354	0.75
ε_r	11.7	16.2	12.9	15.2	13.9
a(Å)	5.43	5.66	5.65	6.06	(InP)

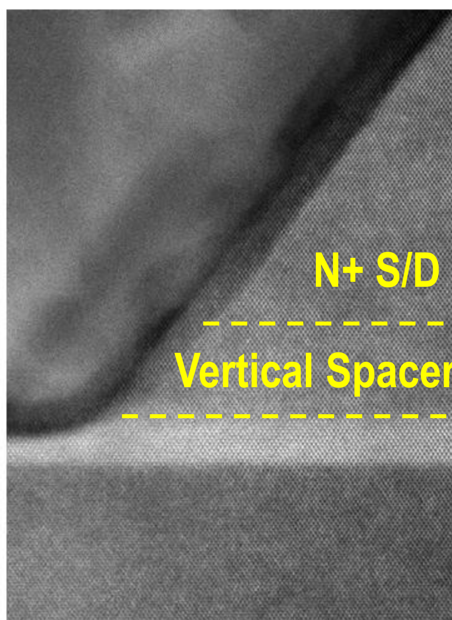


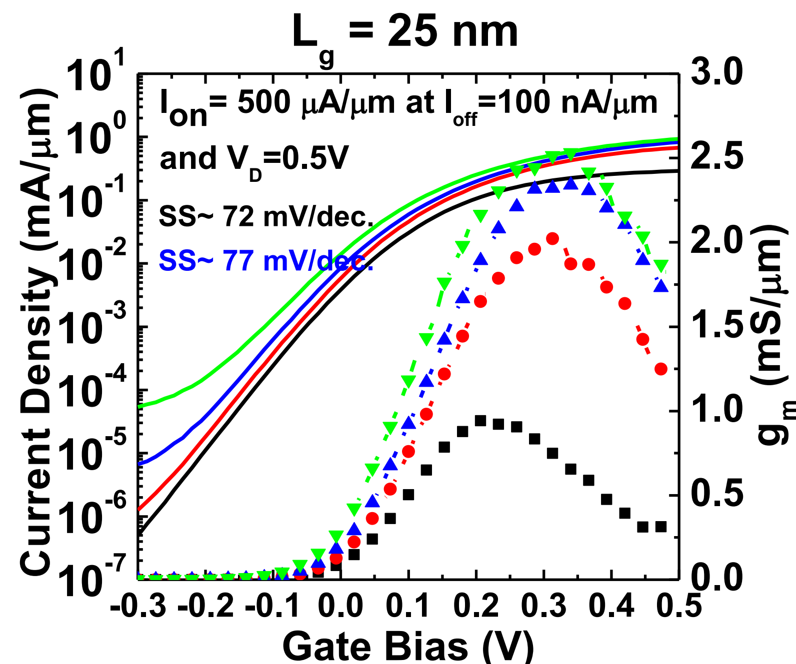
C. Huang et al., DRC 2014

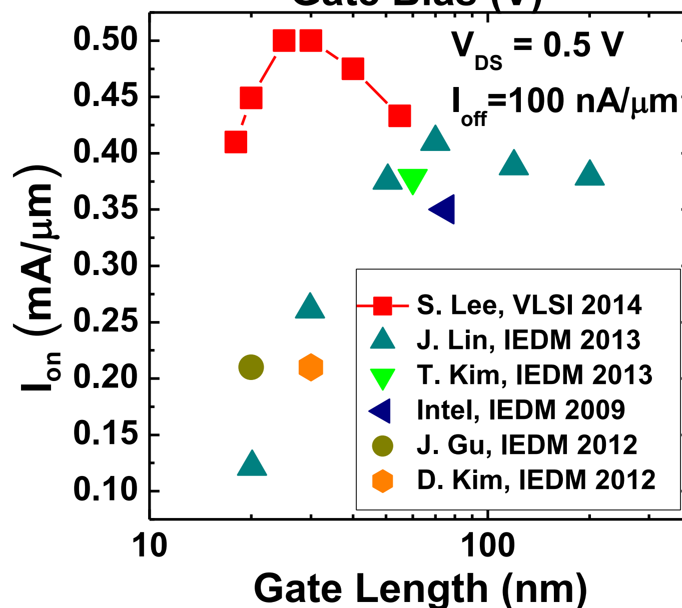
Record III-V FETs on InP substrates



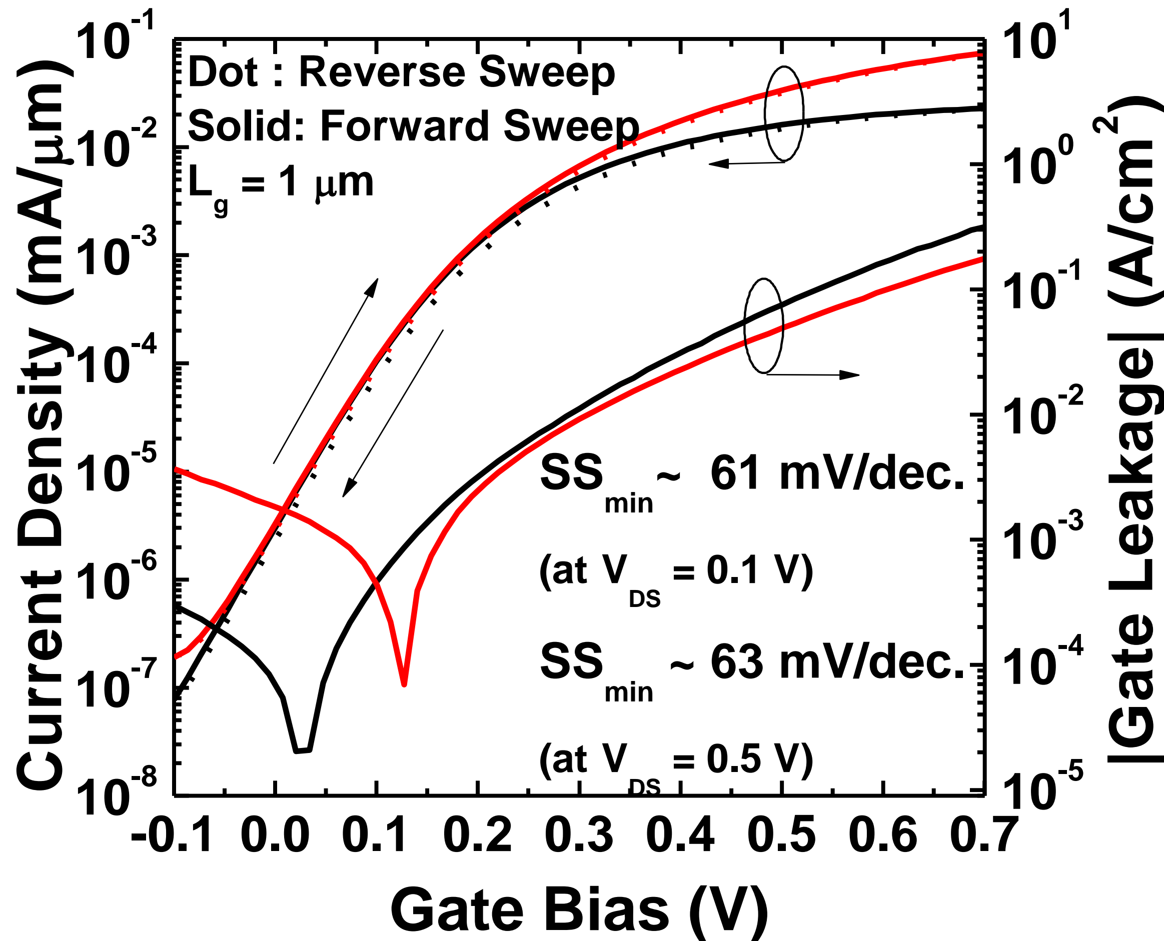








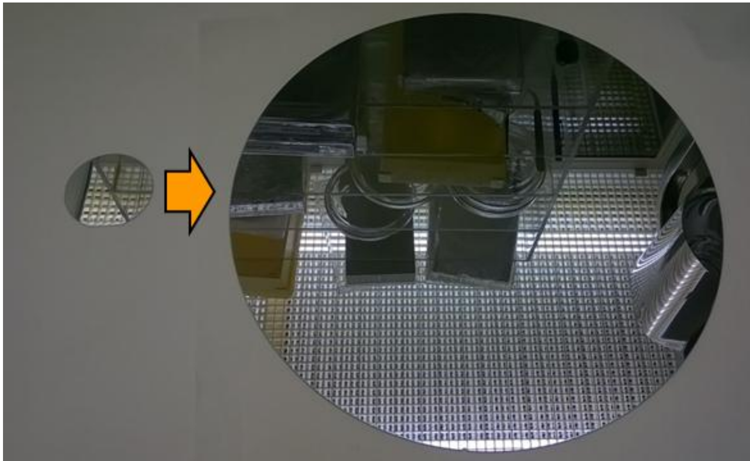
MOSFET: 2.5nm ZrO_2/ 1nm Al_2O_3 / 2.5nm InAs

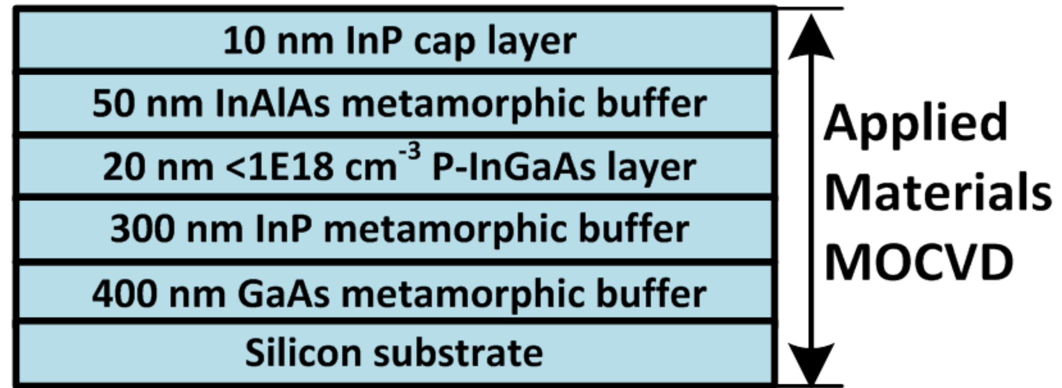


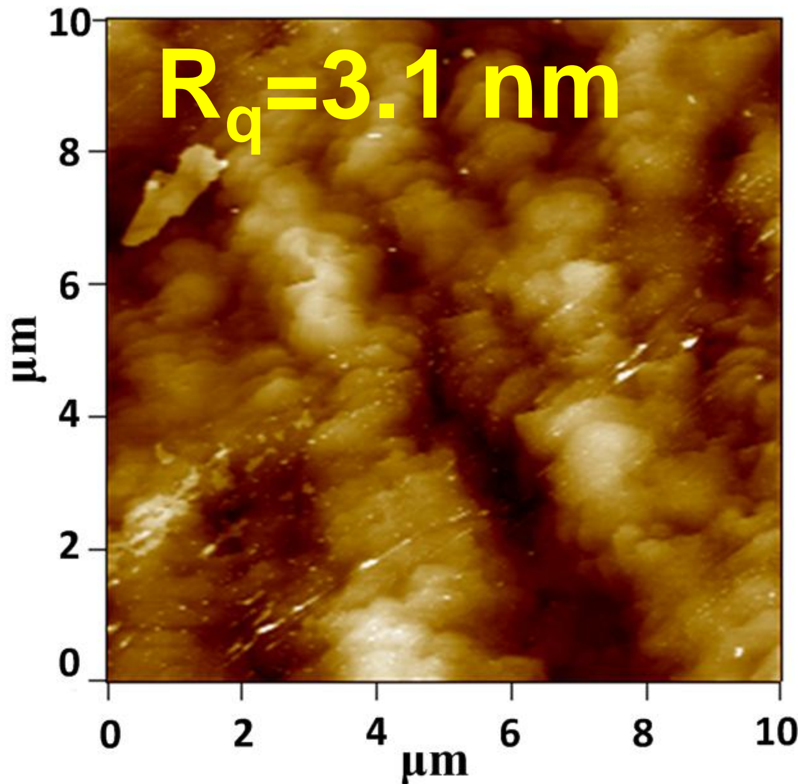
61 mV/dec Subthreshold swing at V_{DS}=0.1 V

Negligible hysteresis

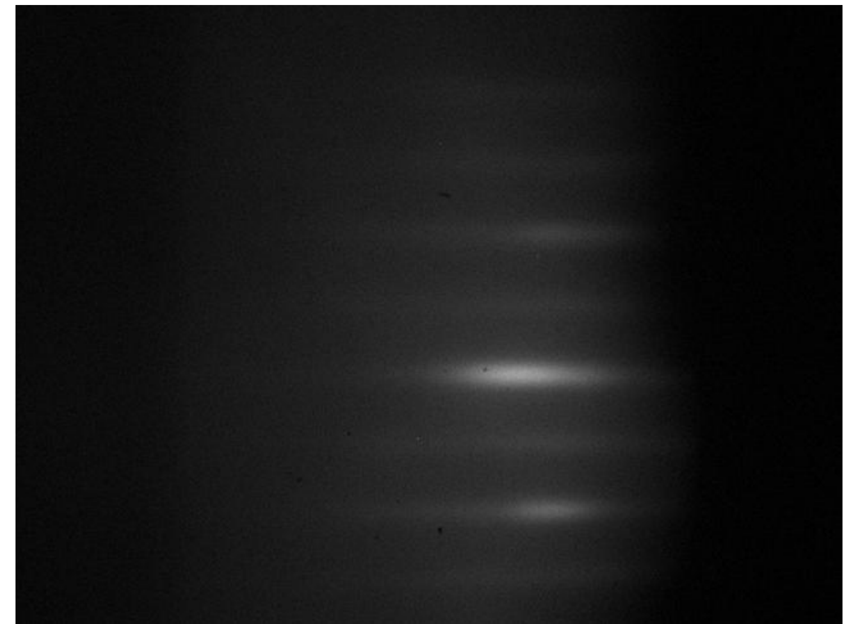
Applied Materials III-V buffer on Si





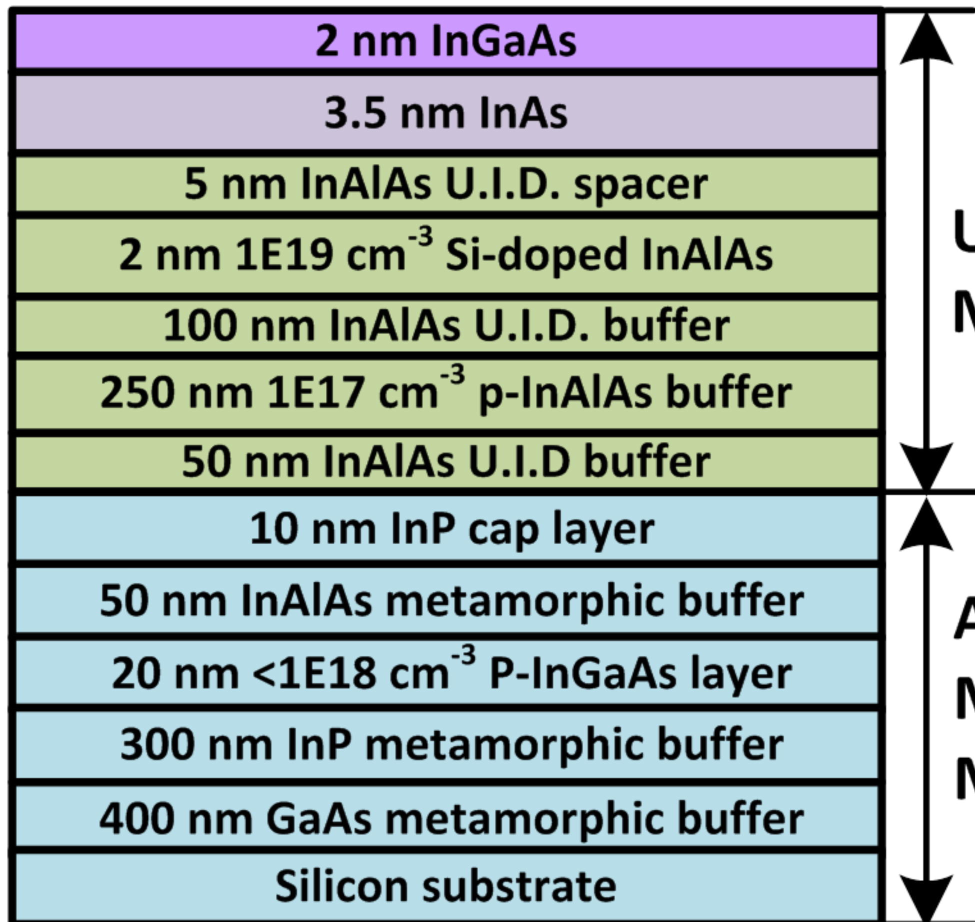


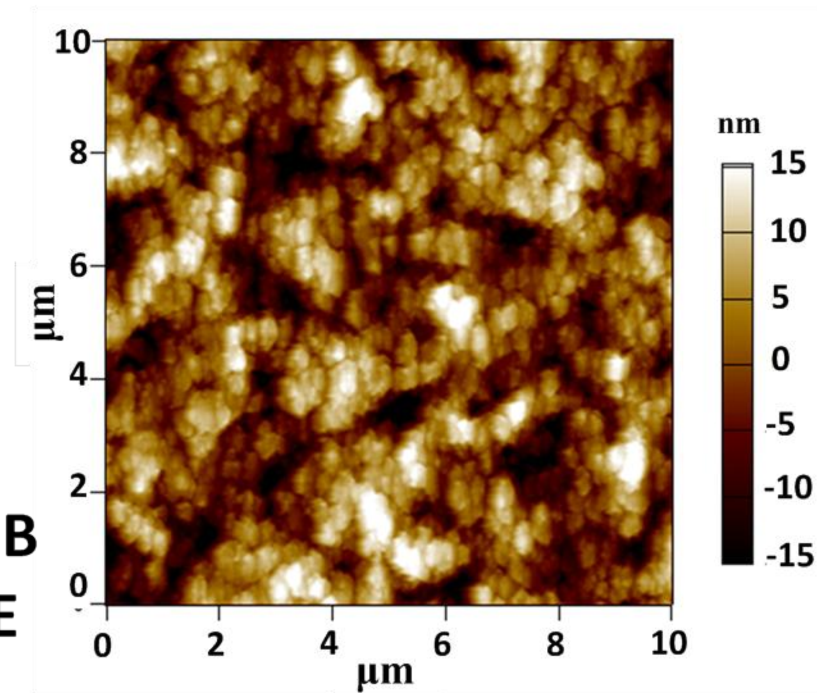
RHEED in MBE



UCSB III-V FET epitaxy

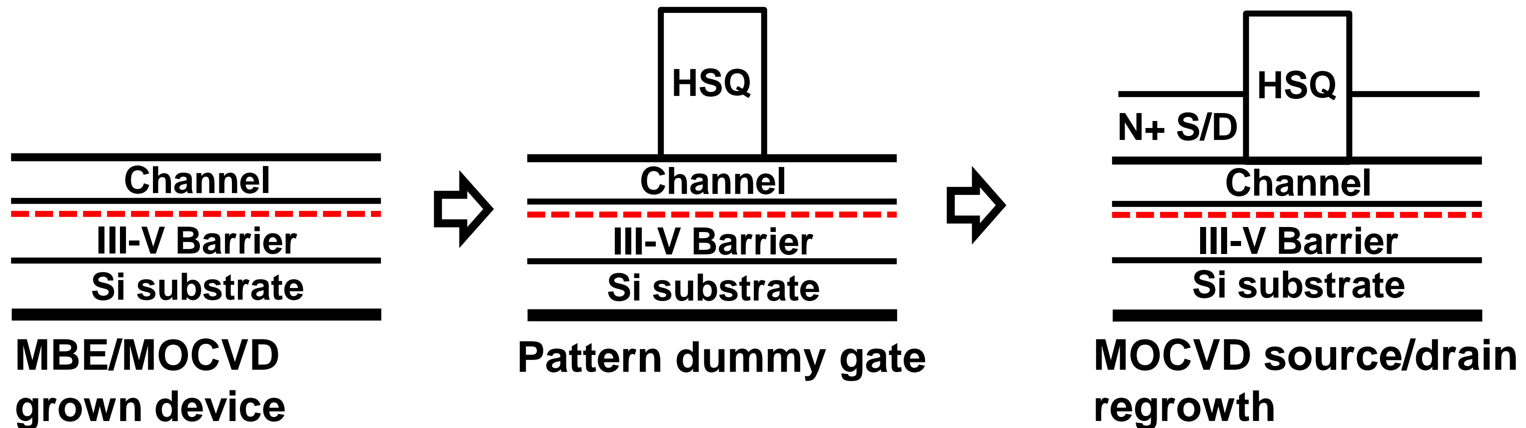
Surface roughness is degraded after FET epitaxy.

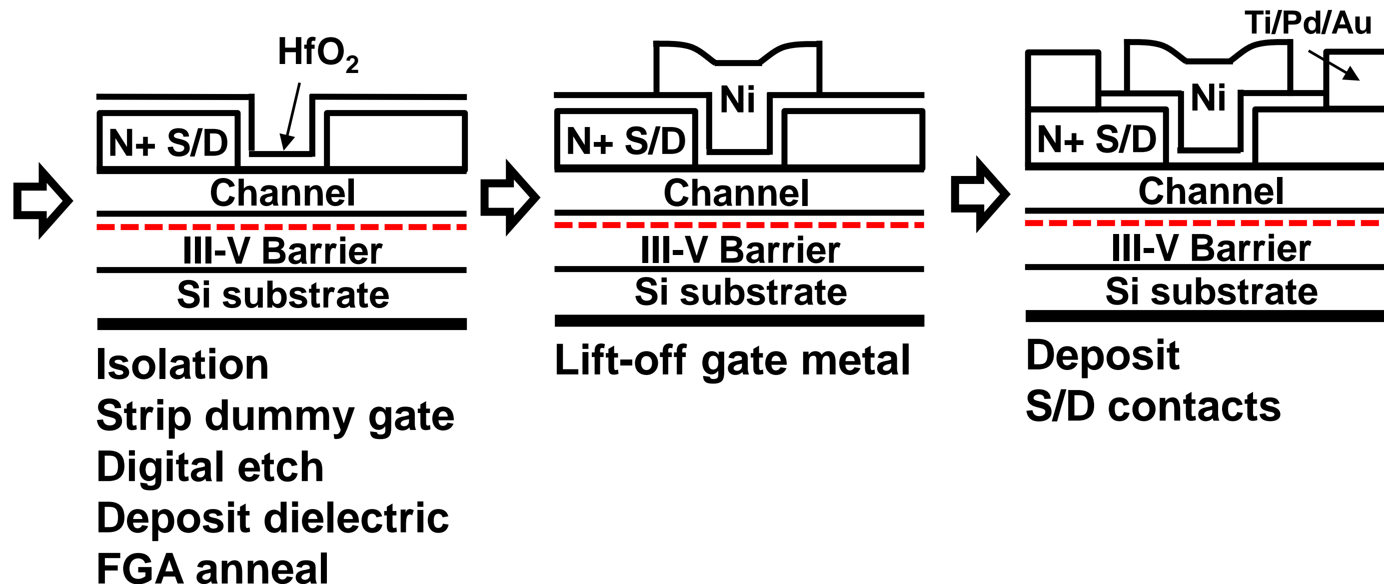




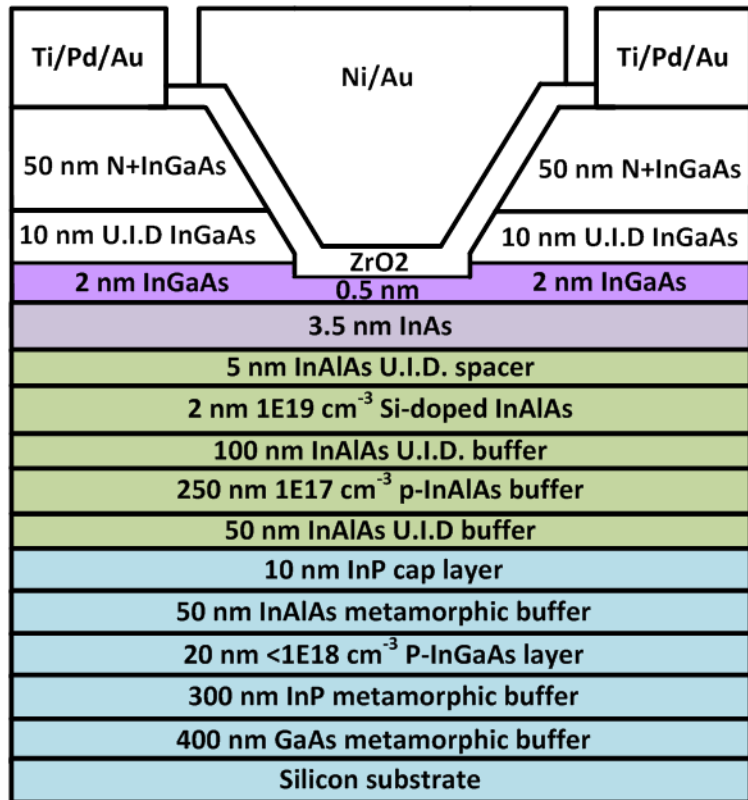
$R_q = 6.9$ nm

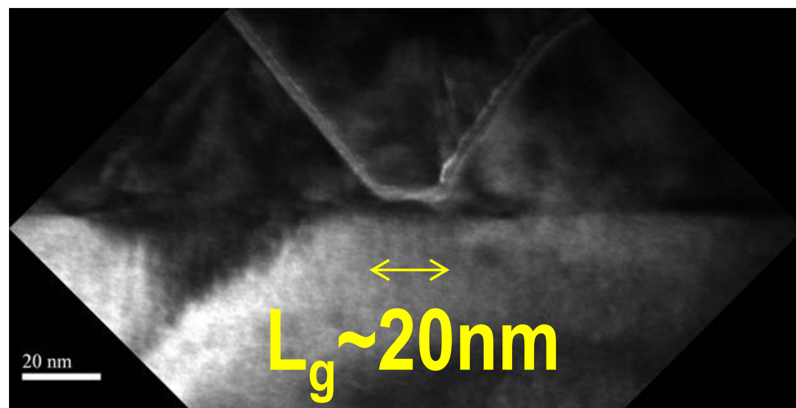
UCSB Gate Last Process Flow





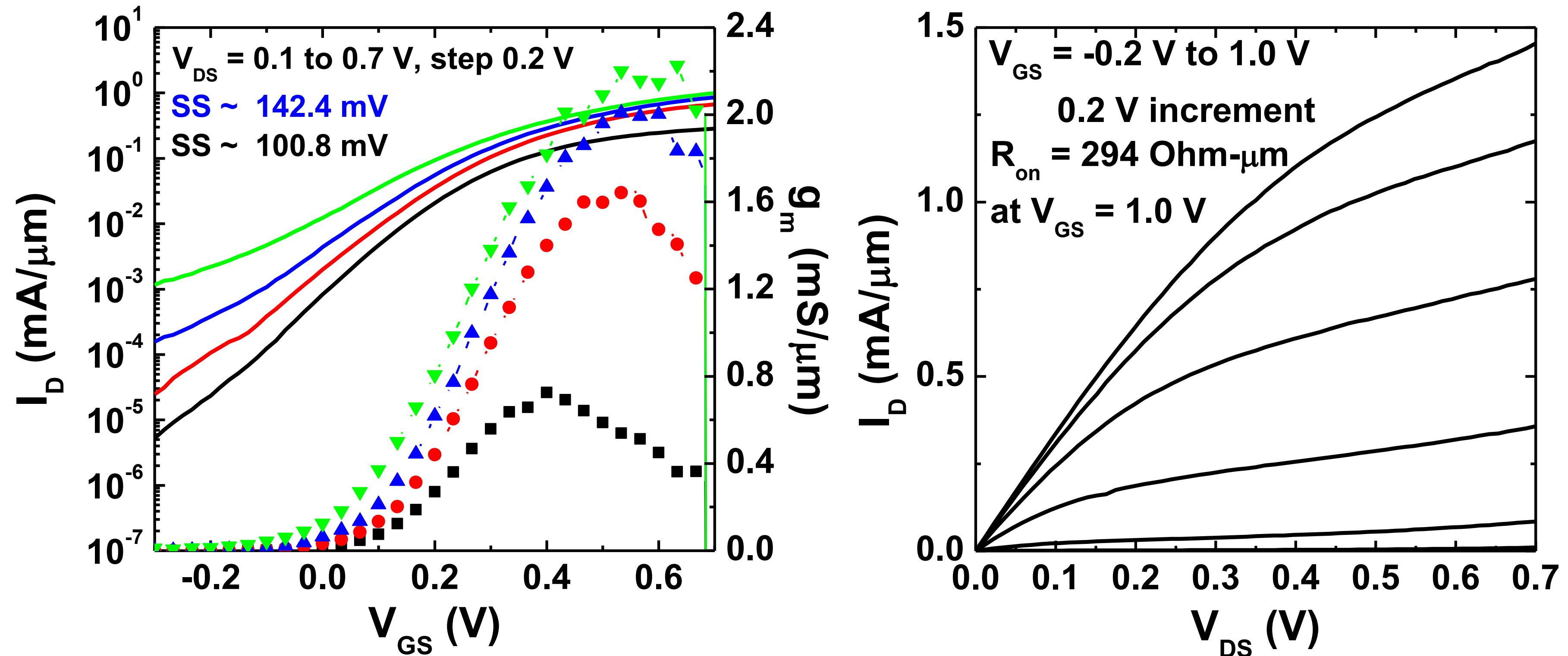
TEM images of III-V FET on Si





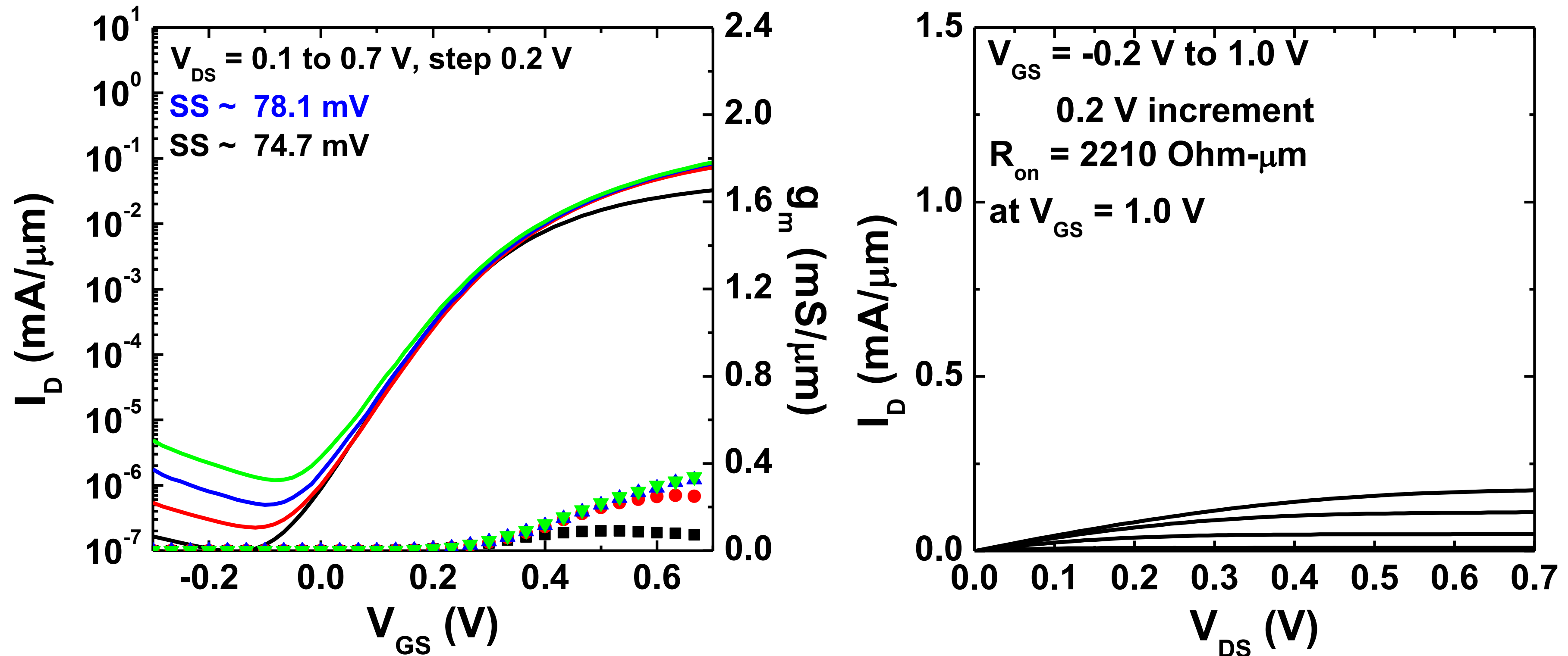
UCSB MOCVD
N+InGaAs
UCSB MBE
InAlAs
InP
200 nm
AMAT MOCVD
GaAs
Si

Short gate length: L_g-20 nm



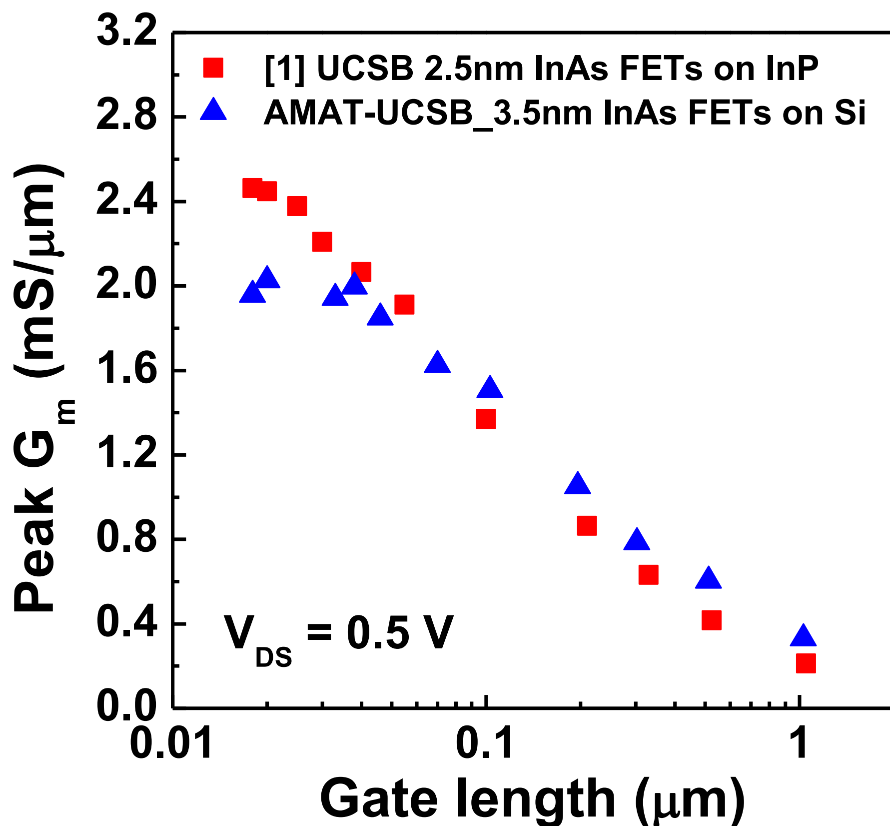
- High G_m~2.0 mS/μm at V_D=0.5 V.
- SS~140 mV/dec. at V_D=0.5 V and 101 mV/dec. at V_D=0.1 V
- High I_{on} >1.4 mA/um at V_{GS}=1V.

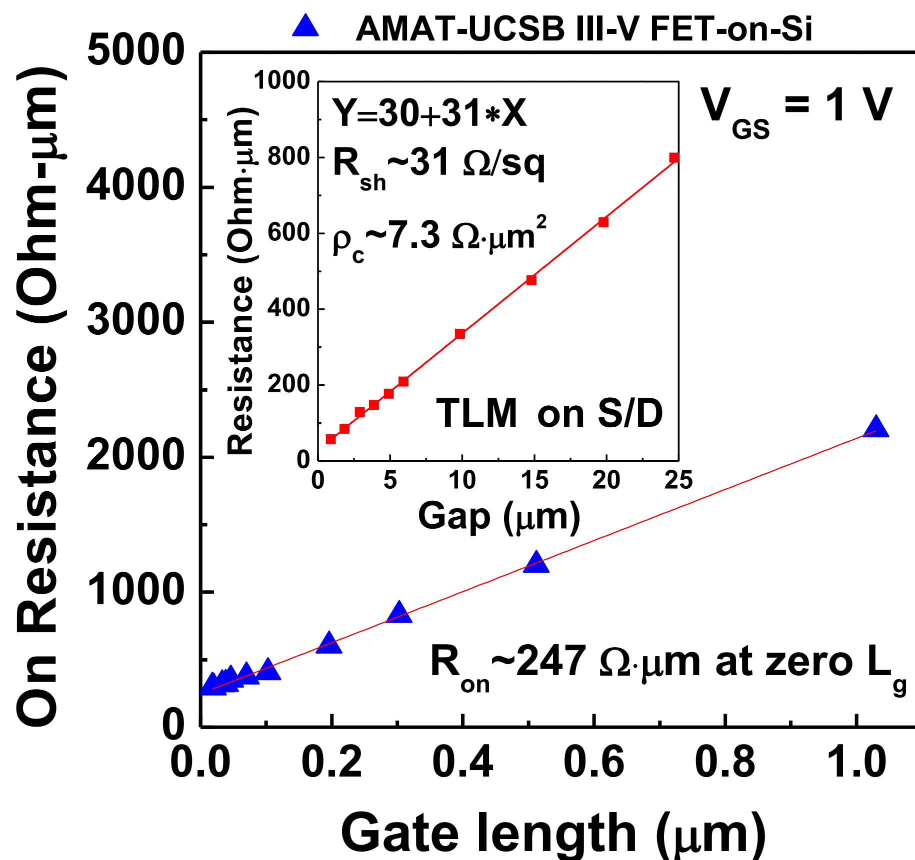
Long gate length: L_g-1 μm



- SS~74 mV/dec. for L_g-1 μm devices.
- Off-state leakage dominated by band-to-band tunneling.
- Negligible buffer leakage.

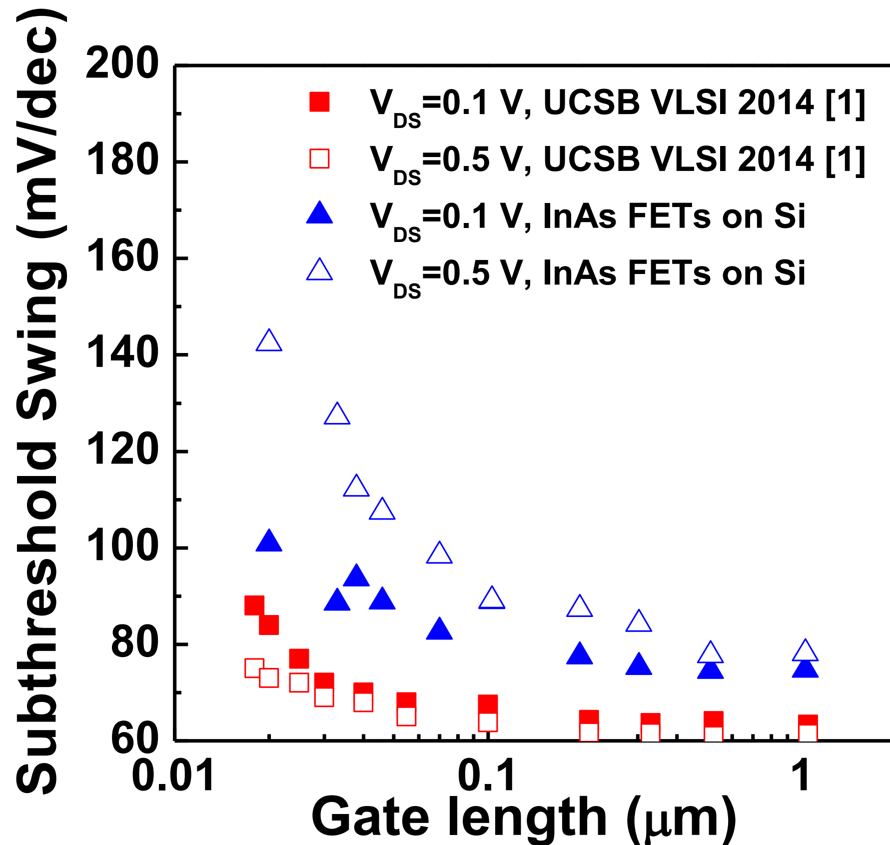
On-state characteristics

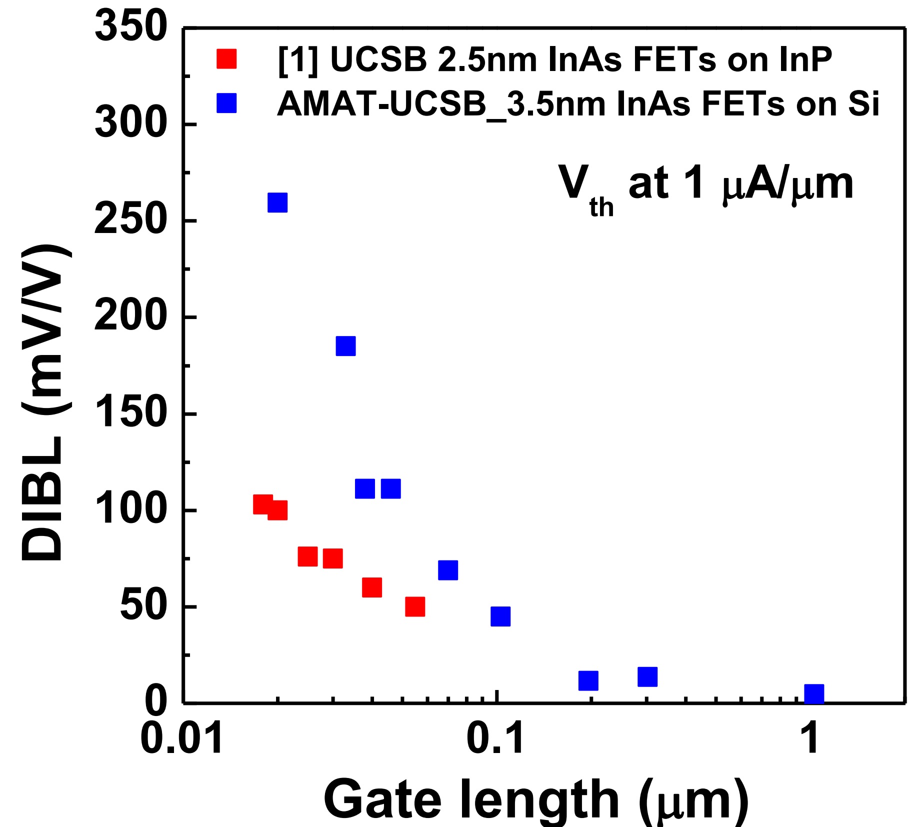




- Long L_g devices show similar G_m to record FETs→ comparable mobility to 2.5 nm InAs on InP.
- ~25% degradation on S/D sheet resistance and contact resistance.
- Thicker channel and degraded $R_{S/D}$ decrease G_m at short L_g.

Subthreshold Characteristics





- SS and DIBL are degraded due to thicker channel.
- Higher SS at long L_g: higher interface trap density.

Within-wafer uniformity: L_g-45nm devices

G_m map (mS/μm) @ V_{DS}=0.5V (20 mm × 12 mm)

	1	2	3	4	5
A	1.90	1.73	1.74	1.90	1.93
B	1.85	1.88	1.81	1.76	1.88
C	1.80	1.55	1.86	1.86	1.91

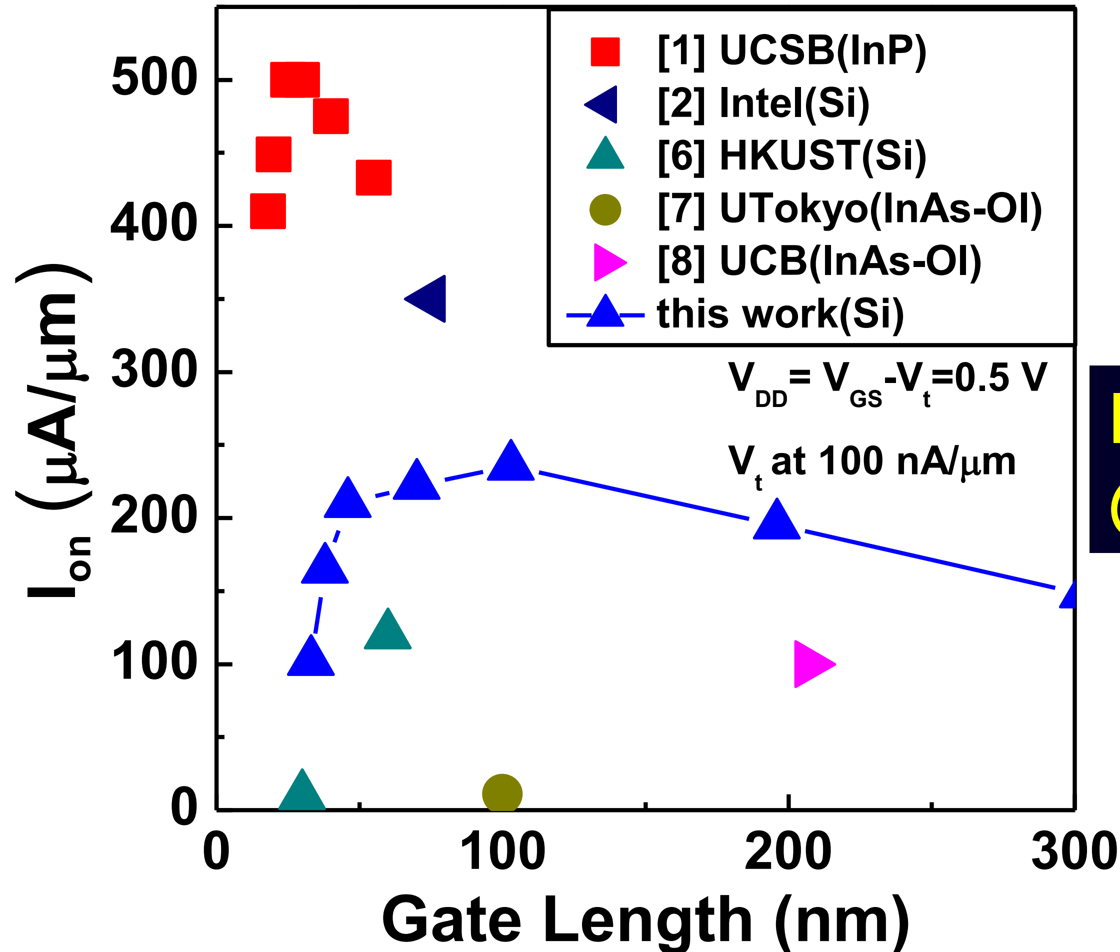
G_m~1.82 mS/μm

SS map (mV/dec) @ V_{DS}=0.5V (20 mm × 12 mm)

	1	2	3	4	5
A	115.7	128.3	106.9	130.6	140.2
B	107.4	117.5	107.5	141.6	120.9
C	132.1	116.4	135.2	124.4	127.4

SS~123 mV/dec

Benchmark of III-V FETs on Si



I_{on}~235µA/µm @100nA/µm I_{off}

Further improved material quality reduces R_{on} and increases I_{on}. Further improved surface roughness allows further thinning the channel, and improves C_g, SS and I_{on}.

Summary

- **Demonstrated high performance, and high yield III-V UTB-FETs on Si substrates using the combination of MOCVD and MBE growth, featuring 3.5~4 nm ultrathin channel and L_g~20 nm.**
- **Achieved high G_m ~ 2.0 mS/µm at V_D =0.5V and high I_{on}~1.4 mA/m at V_{GS}=1V and L_g~20 nm.**
- **Improving channel surface roughness will allow further channel thickness scaling, and improve SS and I_{on}.**
- **Improving material quality will reduce R_{on} and increase G_m and I_{on}.**

Thank you! Question?

(backup slides follow)

Within-wafer uniformity: V_{th} of Lg-45 nm devices

$V_{t,\,lin}$ (V) @ 1 μA/μm, V_{DS}=0.1V

20 mm (columns) × 12 mm (rows)

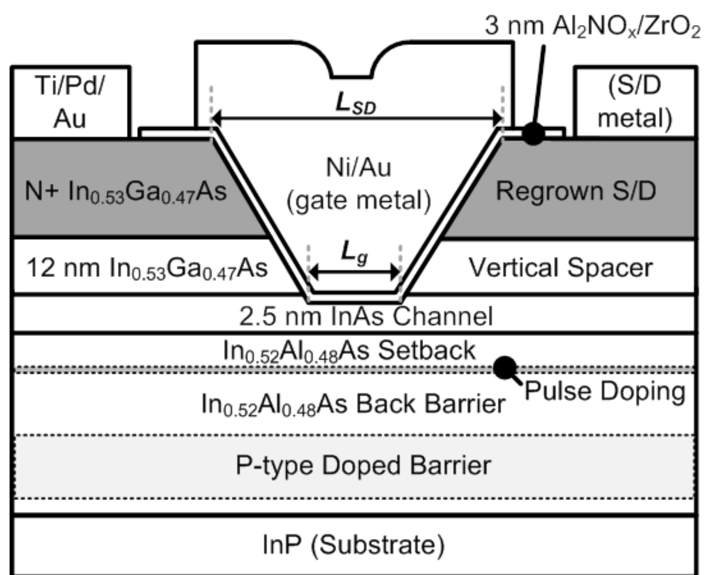
	1	2	3	4	5
A	0.070	0.045	0.074	0.043	0.020
B	0.085	0.054	0.063	0.044	0.054
C	0.041	0.102	0.047	0.056	0.055

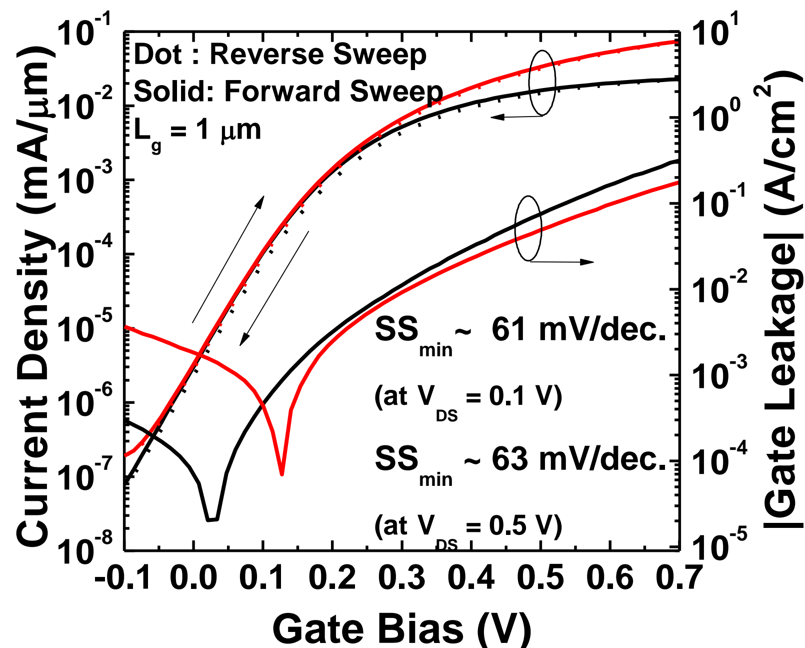
$V_{t,sat}$ (V) @ 1 μA/μm, V_{DS}=0.5V

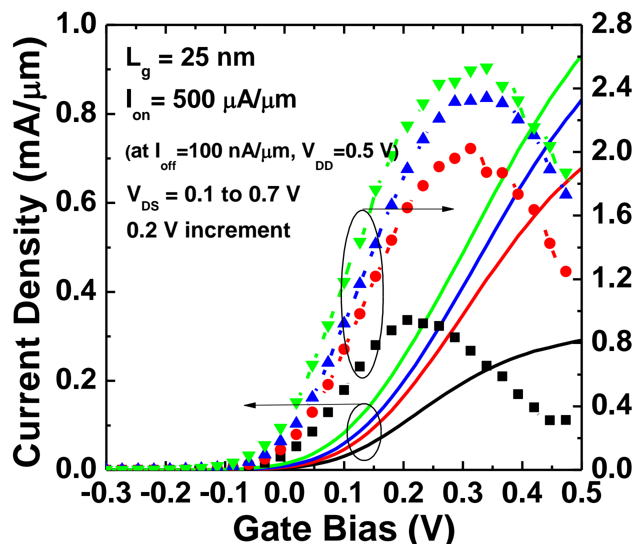
20 mm (columns) × 12 mm (rows)

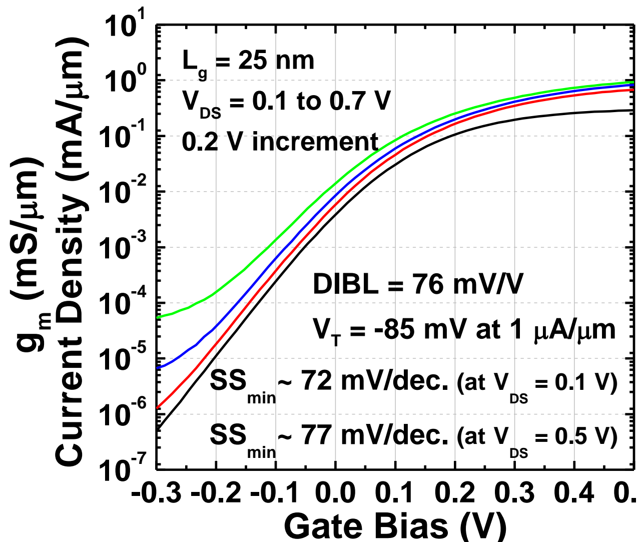
	1	2	3	4	5
A	-0.003	-0.041	0.022	-0.020	-0.049
B	0.036	-0.006	0.008	-0.042	-0.006
C	-0.032	0.042	-0.026	0.003	-0.020

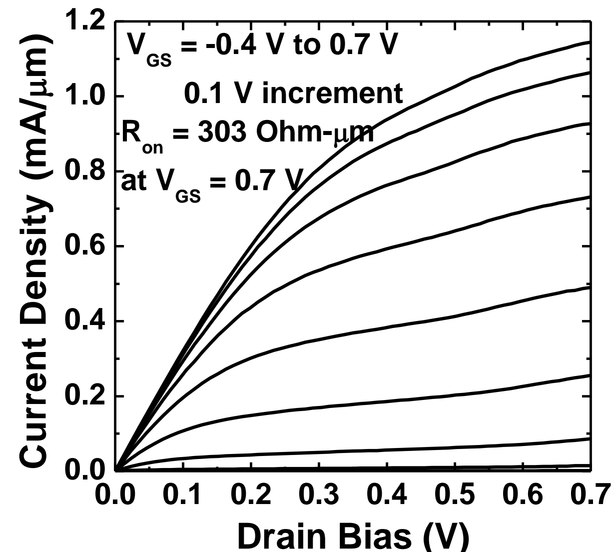
Hero device: VLSI 2014 late news (Sanghoon Lee)







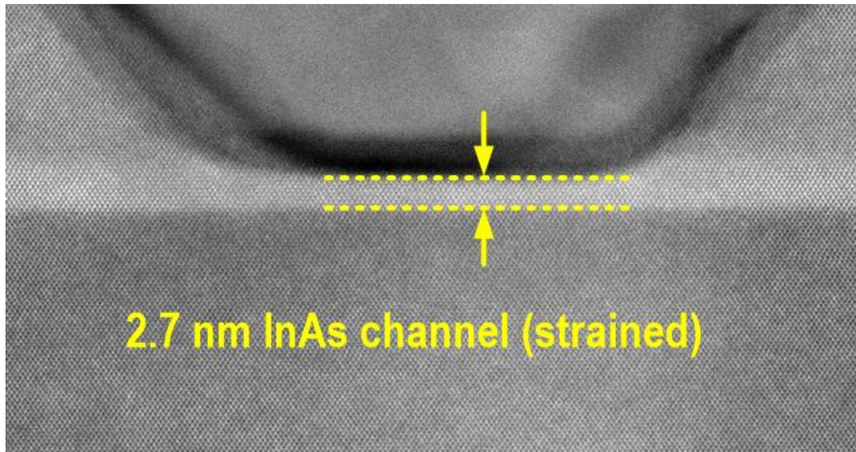


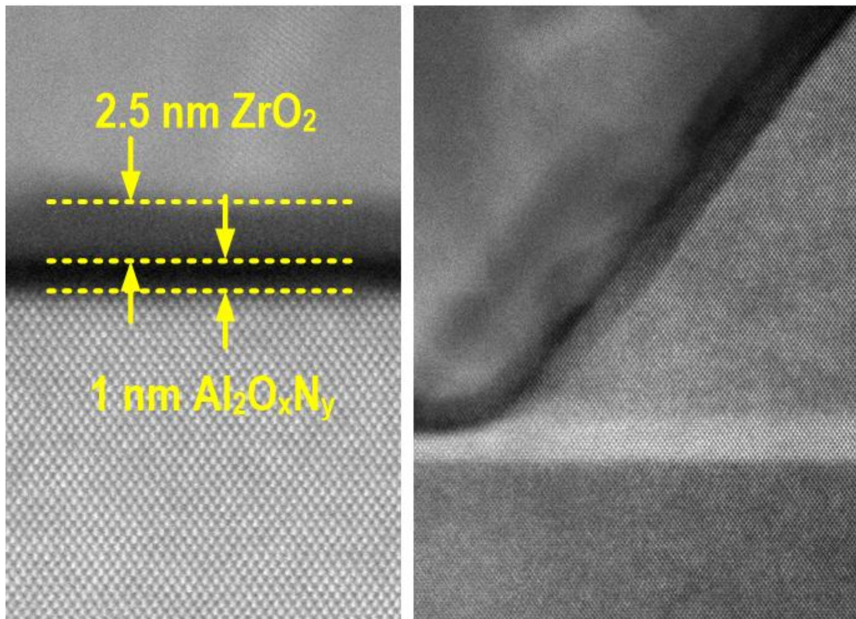


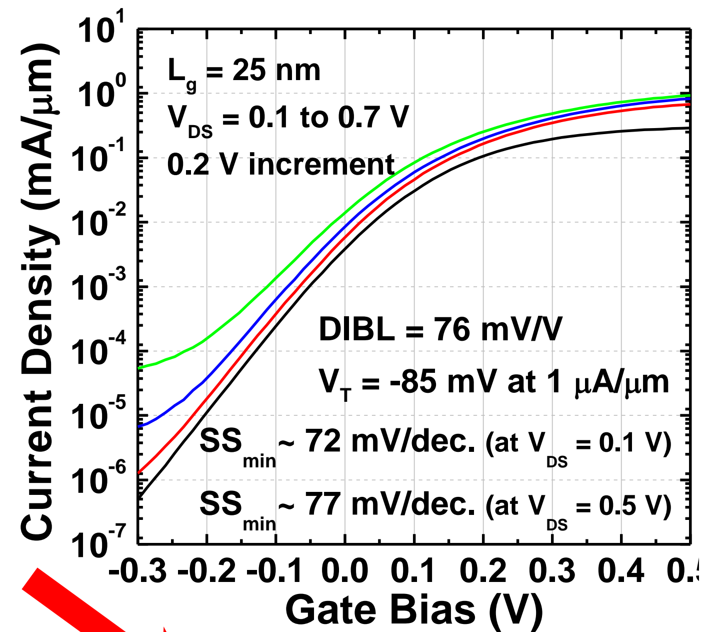
Courtesy of Sanghoon Lee (UCSB)

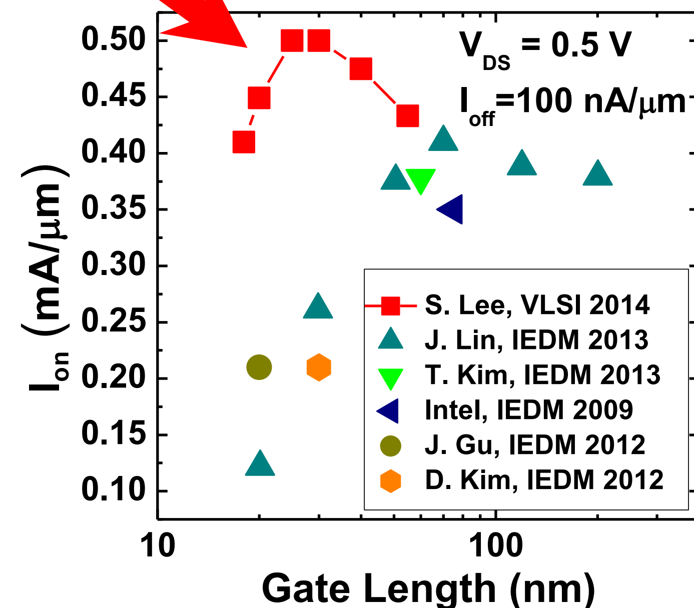
Reducing leakage (3): Ultra-thin channel

S. Lee et al., VLSI 2014



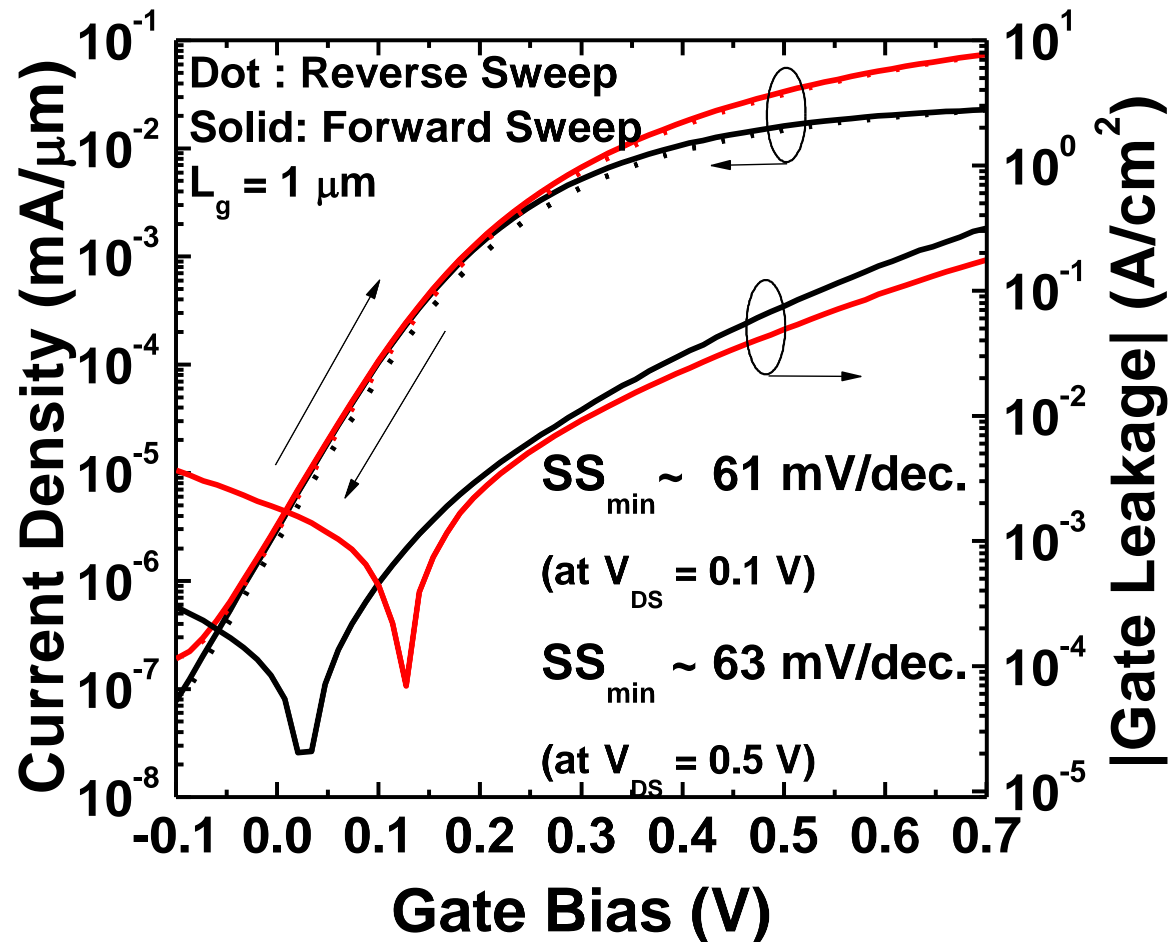






Record III-V MOS

MOSFET: 2.5nm ZrO_2/ 1nm Al_2O_3 / 2.5nm InAs



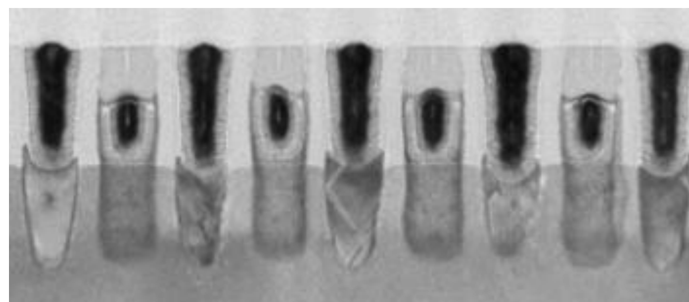
61 mV/dec Subthreshold swing at V_{DS}=0.1 V

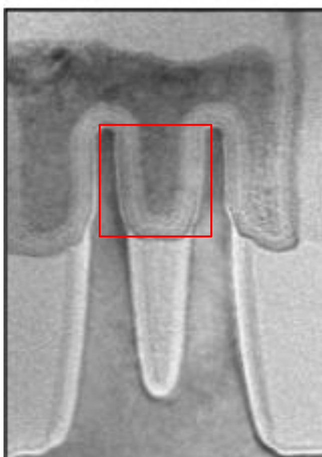
Negligible hysteresis

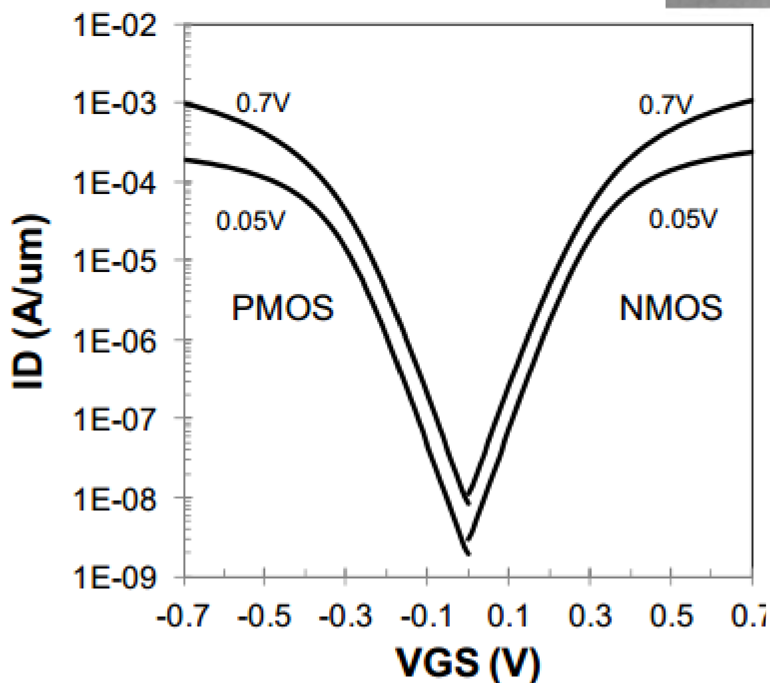
Compared to Intel 14nm finFET

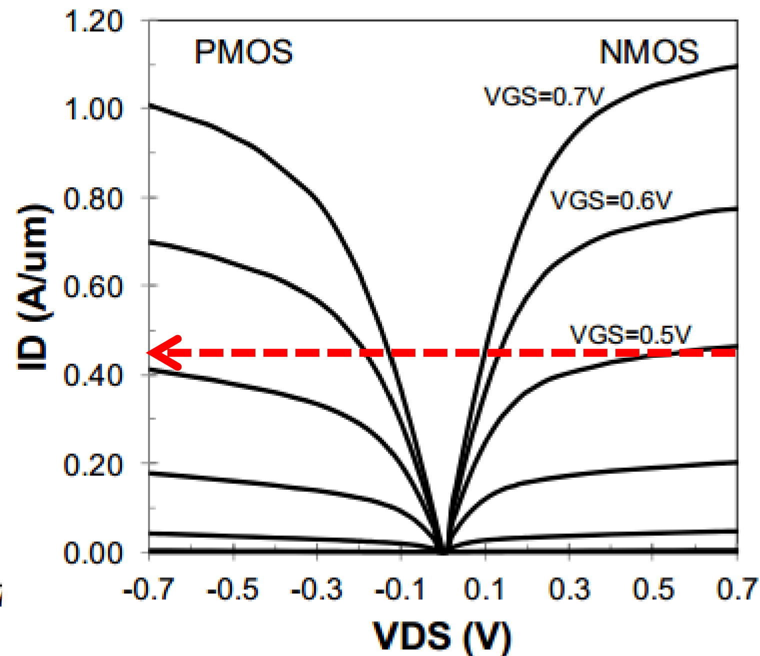
S. Natarajan et al, IEDM 2014, December, San Francisco

Layer	Pitch (nm)
Fin	42
Contacted Gate Pitch	70
Metal 0	56
Metal 1	70
Metal 2	52







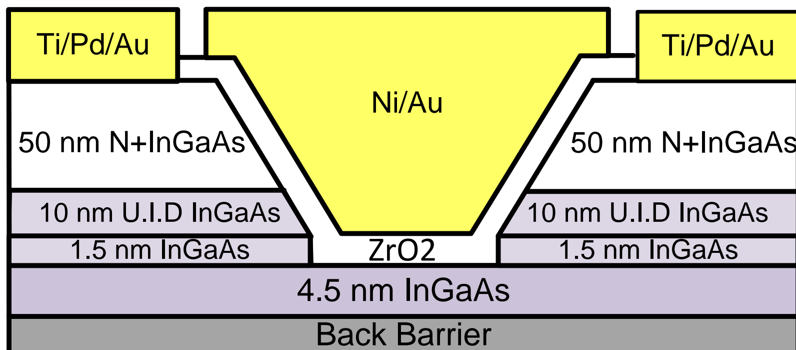


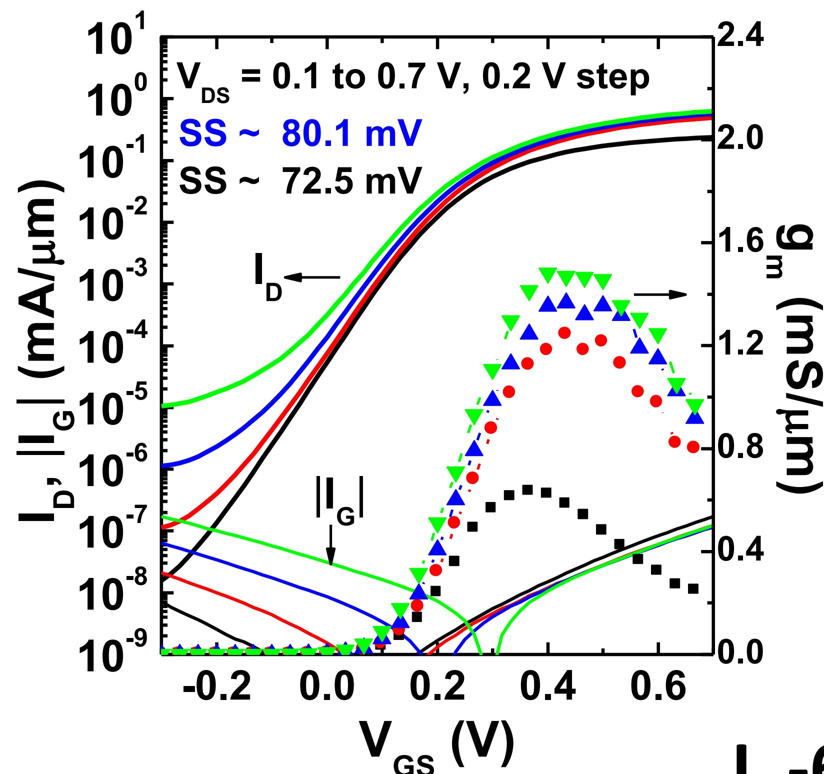
I_{off}=10nA/μm, I_{on}=0.45mA/μm @V_{DS}=0.5V ***per μm of fin footprint***

Re-normalizing to fin periphery: ~0.24 mA/μm

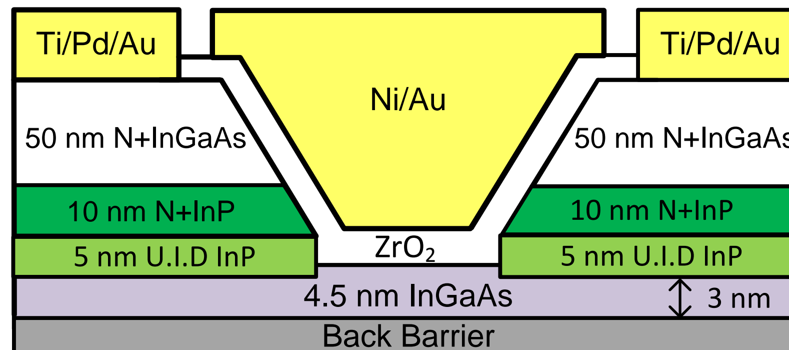
Reducing leakage (5): Recessed InP S/D spacer

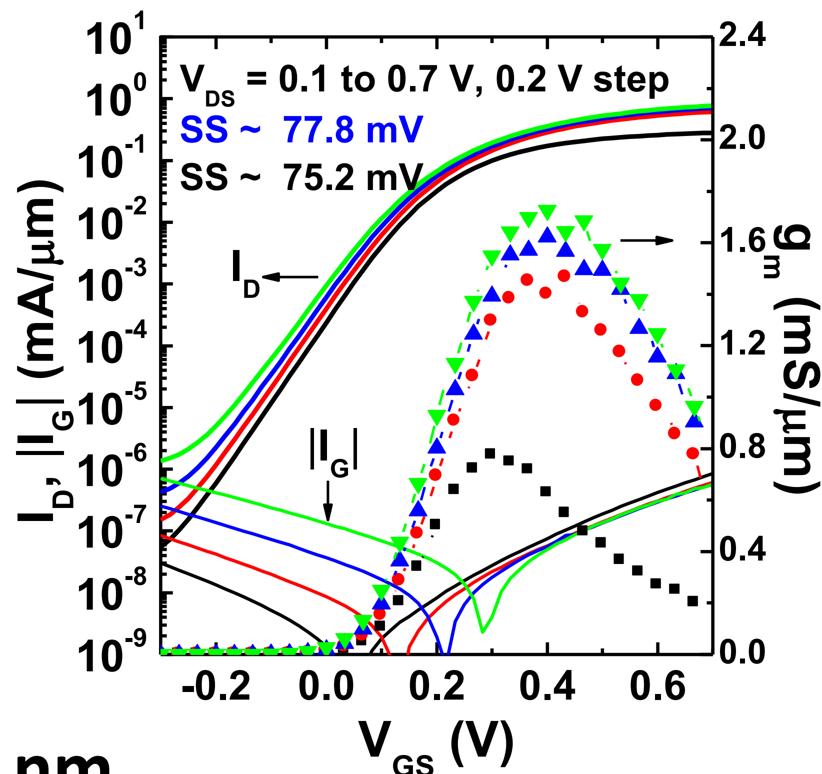
12 nm InGaAs spacer





5 nm Recessed InP spacer

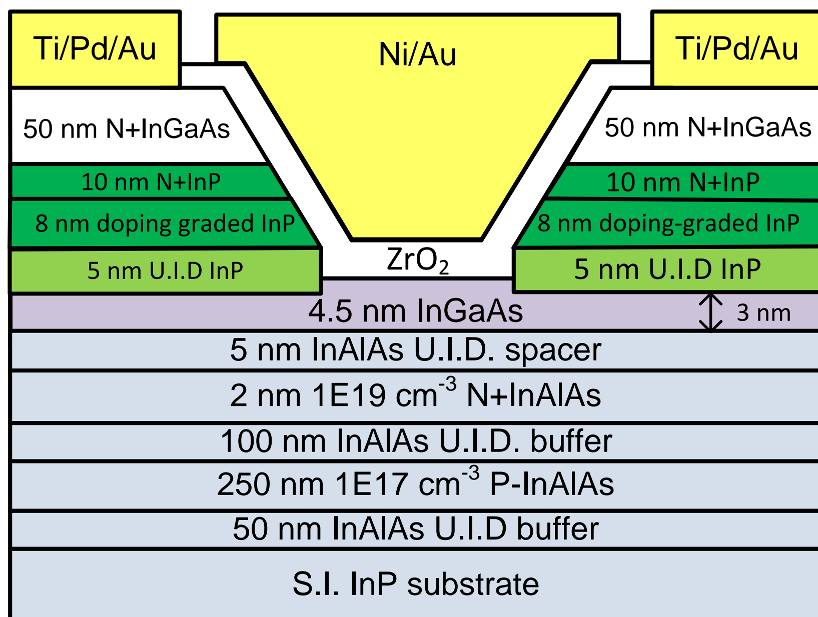




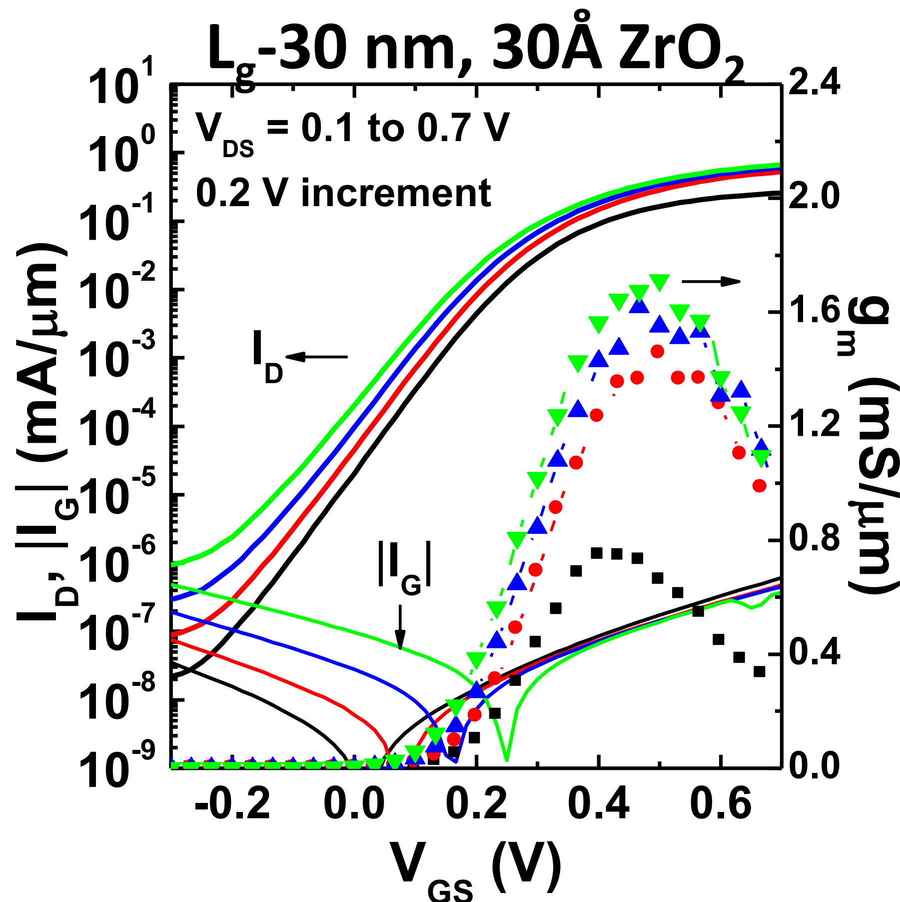
L_g-60 nm

Reducing leakage (6): Doping-graded InP spacer

C-Y Huang, 2014 IEDM



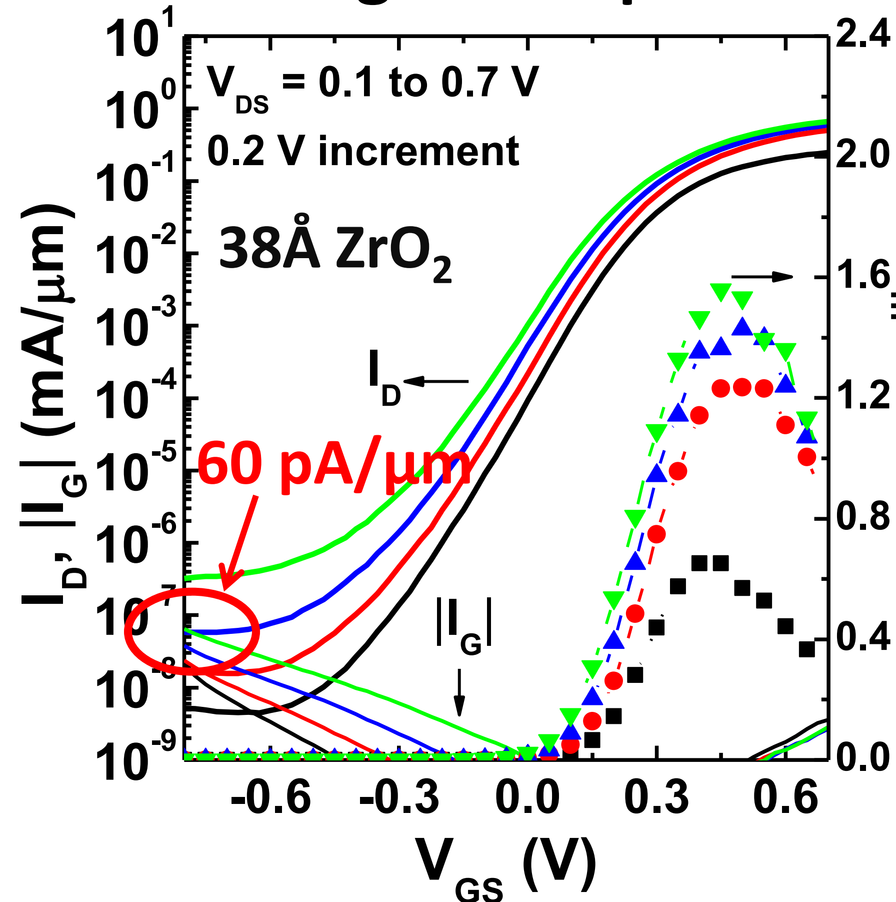
R_{on} at zero L_g (Ω·µm)	5 nm UID InP	13 nm UID InP	Doping graded InP
	~199	~364	~270

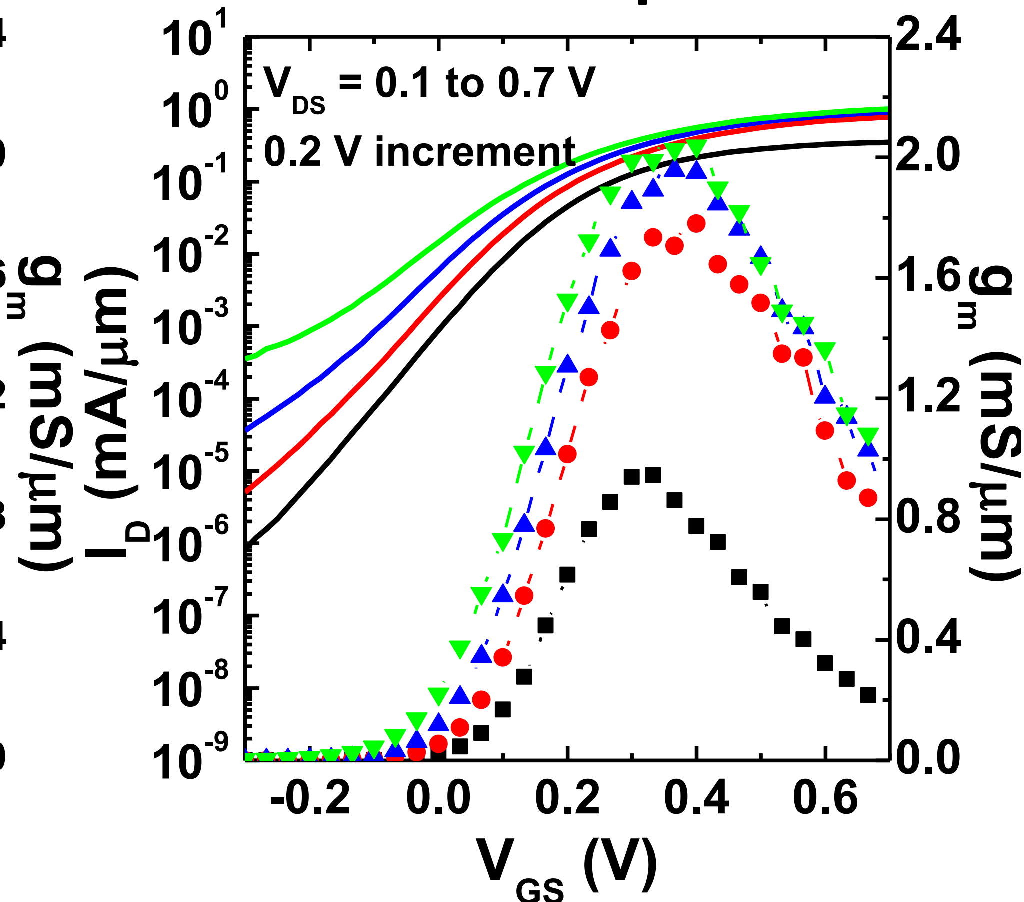


Doping-graded InP spacer reduces parasitic source/drain resistance and improves G_m.

Gate leakage limits I_{off}~300 pA/µm.

Reducing leakage (7): Thicker Dielectric





Minimum I_{off}~ 60 pA/µm at V_D=0.5V for L_g-30 nm

100:1 smaller I_{off} compared to InGaAs spacer

C-Y Huang, 2014 IEDM