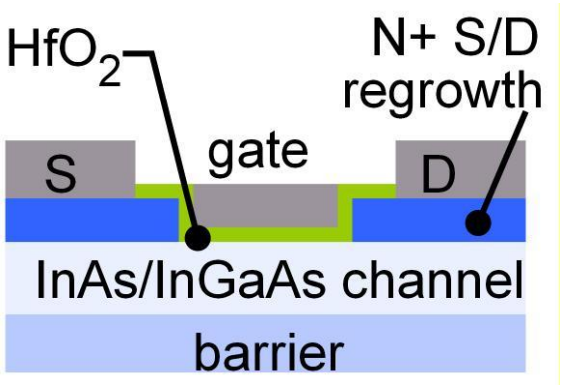
227th Electrochemical Society Meeting, Chicago, May 24-28, 2015

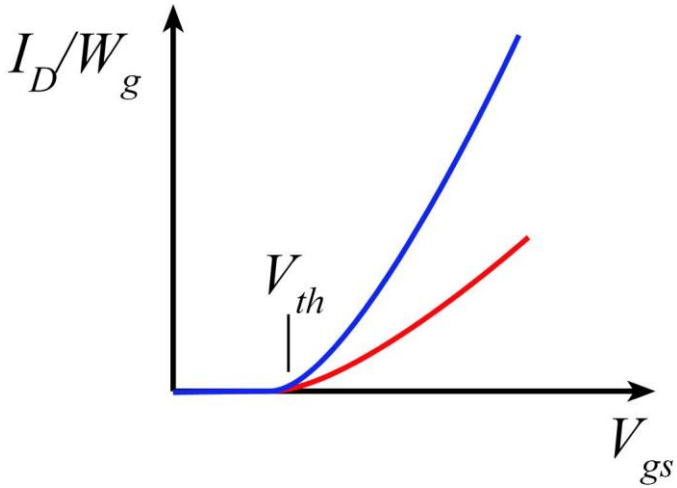
Record-Performance In(Ga)As MOSFETs Targeting ITRS High-Performance and Low-Power Logic

M. Rodwell, C. Y. Huang, S. Lee, V. Chobpattana, B. Thibeault, W. Mitchell, S. Stemmer, A. Gossard
University of California, Santa Barbara

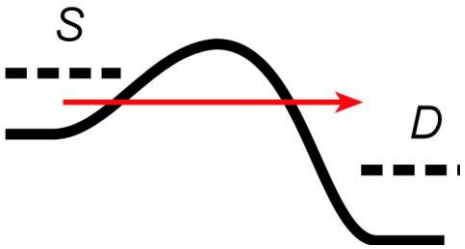
Why III-V MOS ?

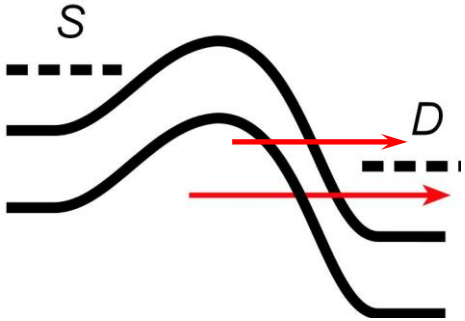
III-V vs. Si: Low m*→ higher velocity. Fewer states→ less scattering → higher current. Can then trade for lower voltage or smaller FETs.



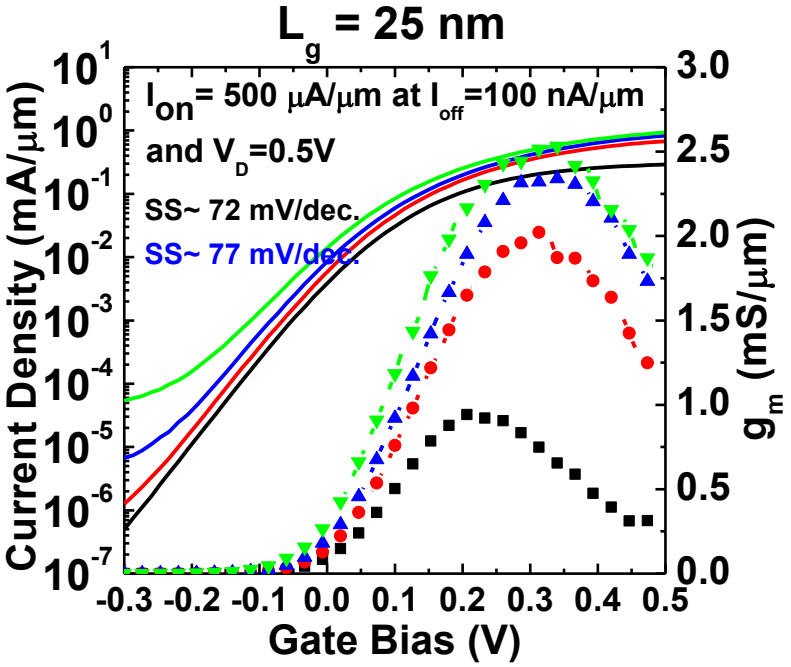


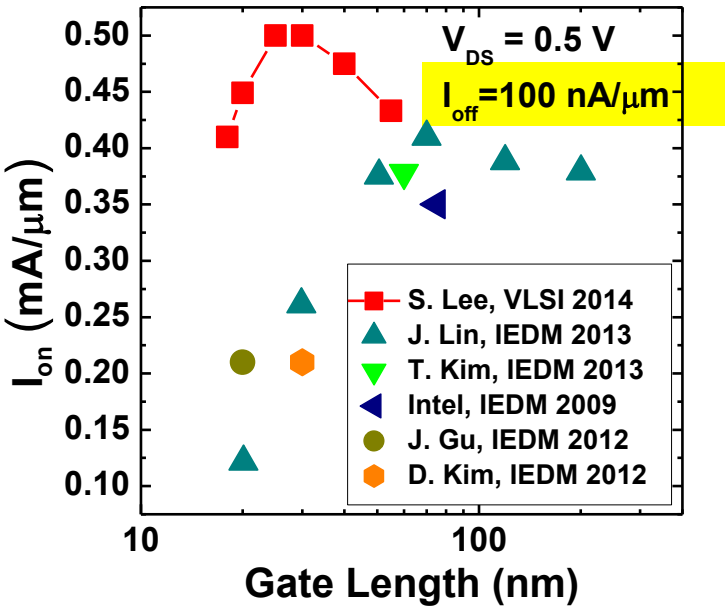
Problems: Low m*→ less charge. Low m* → more S/D tunneling. Narrow bandgap→ more band-band tunneling, impact ionization.





InGaAs/InAs FETs are leaky!





HP = High Performance: I_{off}=100 nA/μm

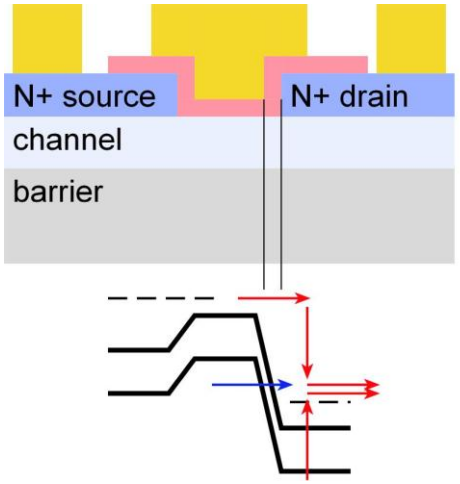
GP = General Purpose: I_{off}=1 nA/μm

LP = Low Power: I_{off}=30 pA/μm

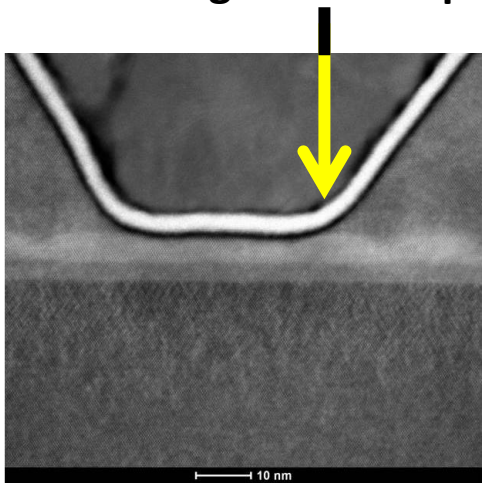
ULP = Ultra Low Power: I_{off}=10 pA/μm

Device Structures: Lateral Spacers & Tunneling

Small S/D contact pitch

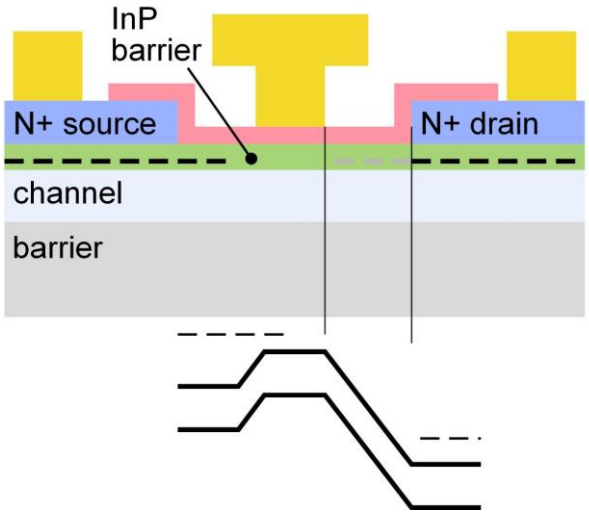


no lateral gate-drain space

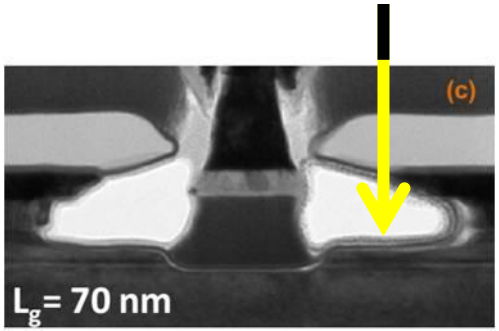


UCSB

MOS-HEMT with large contact pitch



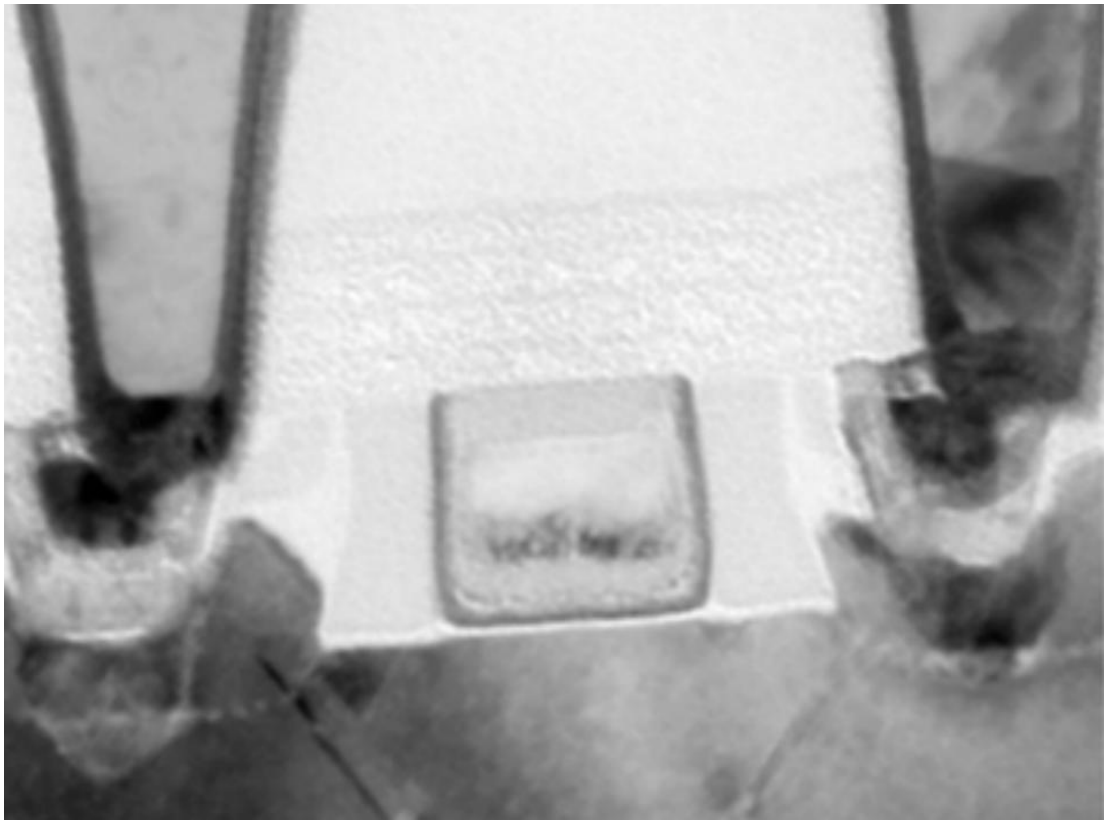
~70 nm gate-drain space



Lin, IEDM2013

We must build devices with small S/D pitch.

contact pitch ~ 3 times lithographic half-pitch
(technology node dimension)

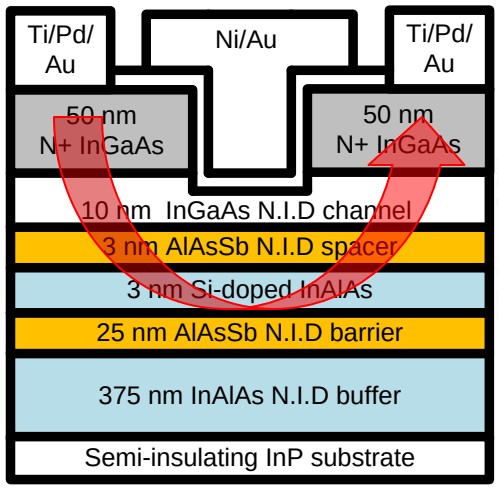


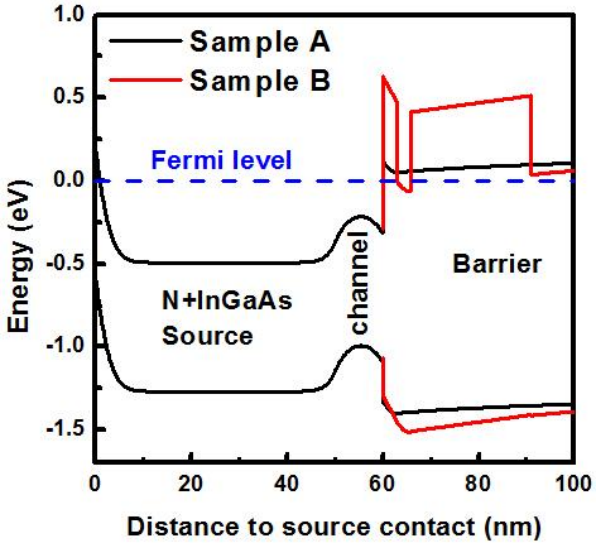
Intel 35nm NMOS

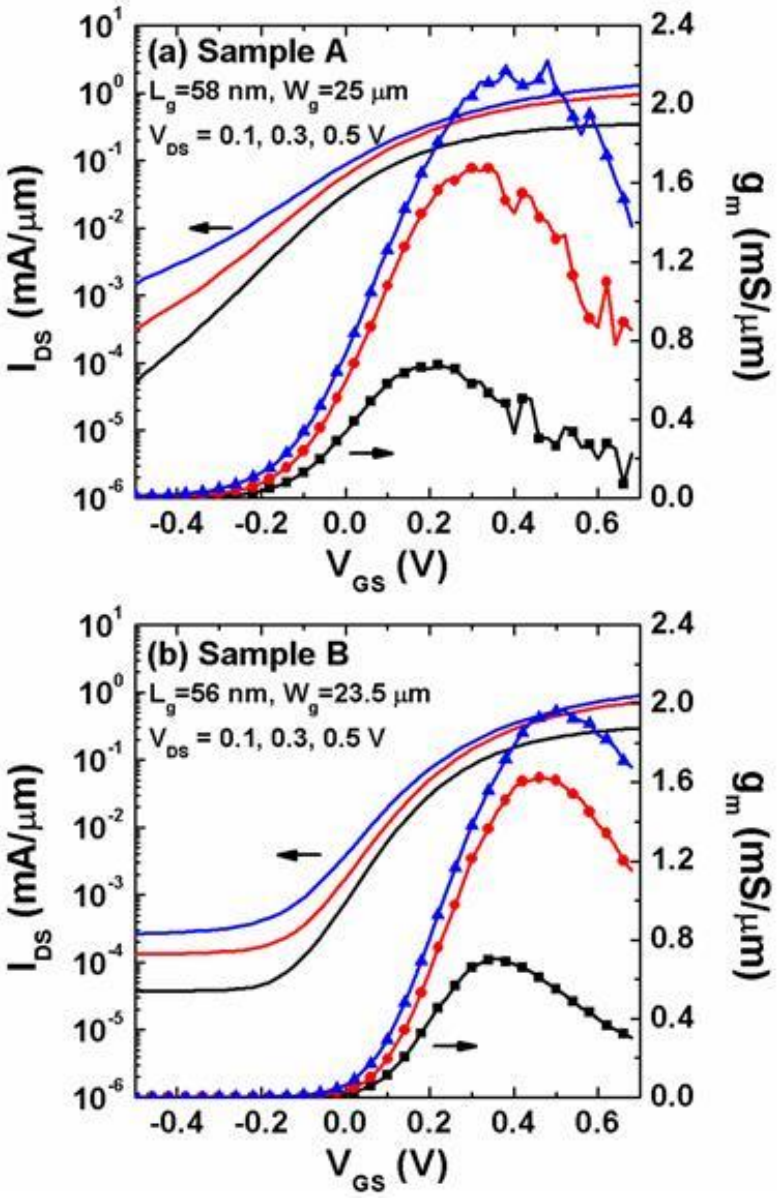
Small S/D pitch hard to realize if we require ~20-50nm lateral gate-drain spacers !

Reducing leakage (1)

- **Wide band-gap barriers or P-doped back barriers reduces bottom leakage path.**
- **<u>Solution 1</u>: AlAsSb barriers (Sample B) reduces subthreshold leakage.**
- **<u>Solution 2</u>: P-doped InAlAs barriers also work well.**







C. Y. Huang et al., APL., 103, 203502 (2013)

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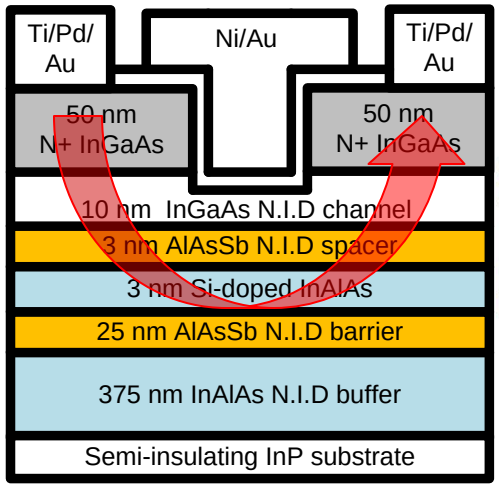
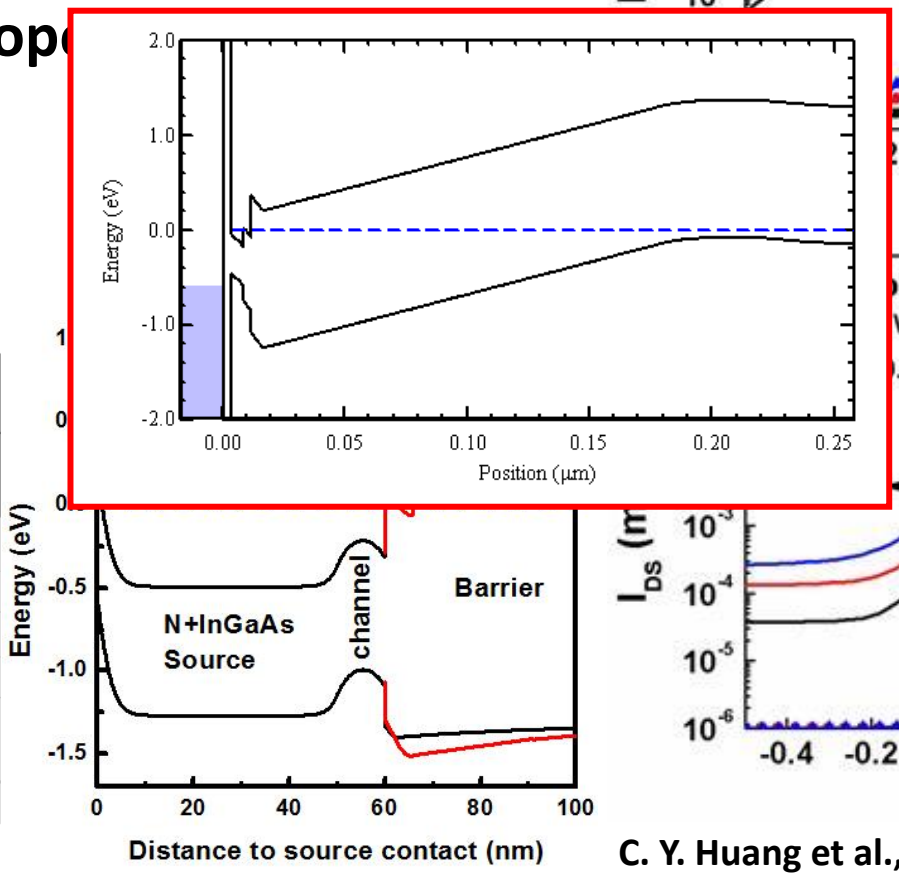
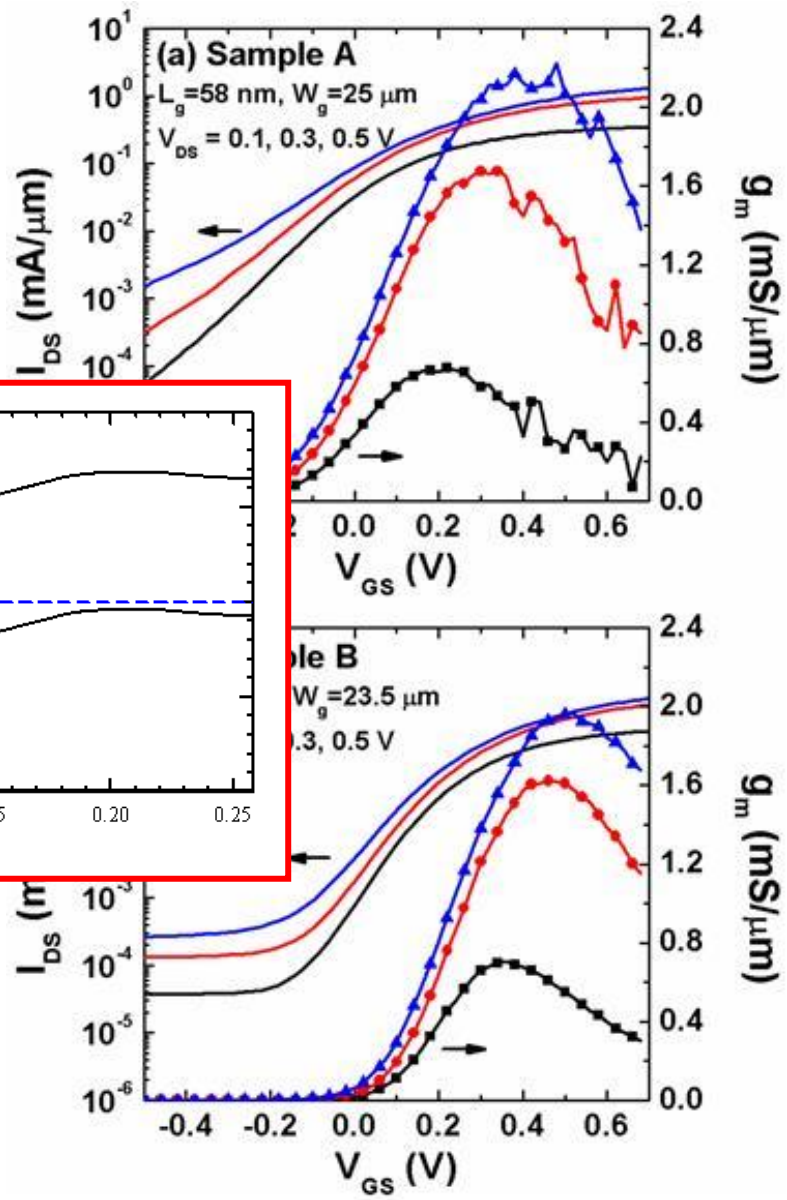
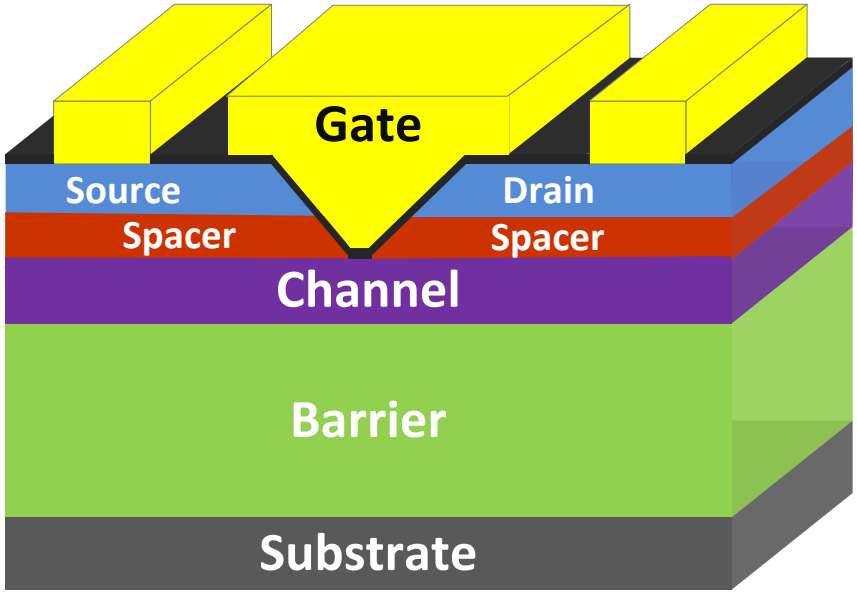


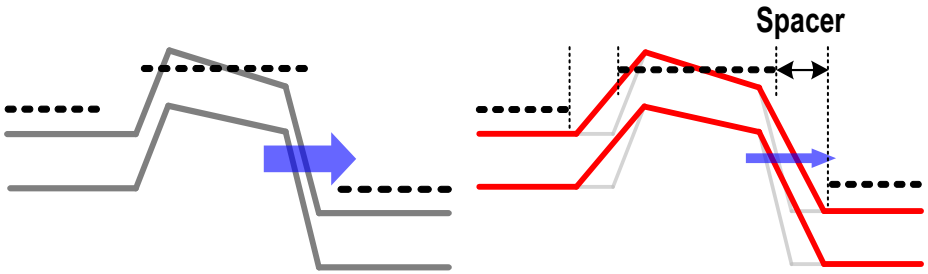


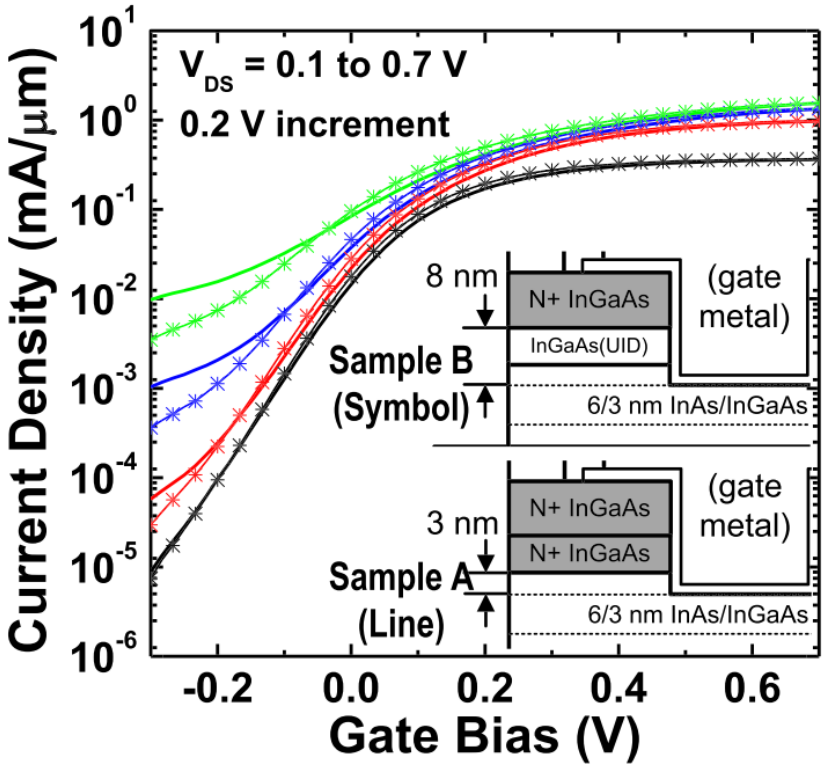


C. Y. Huang et al., APL., 103, 203502 (2013)

Reducing leakage (2): Source/Drain Vertical Spacer







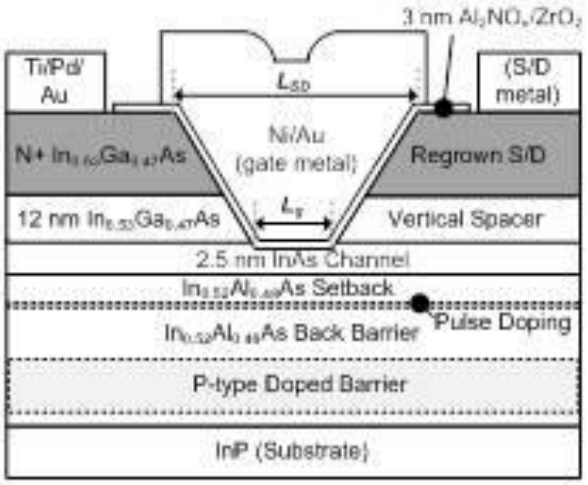
S. Lee et al., APL 103, 233503 (2013)

C. Y. Huang et al., DRC 2014.

Vertical spacers reduce the peak electric field, improve electrostatics, and reduce BTBT floor.

Vertical spacers: some details

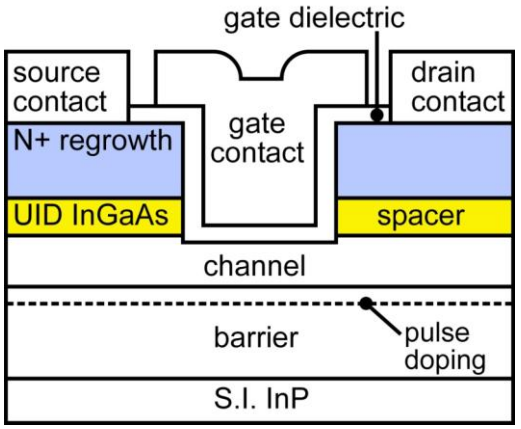
Minimum S/D contact pitch:
- **depends upon regrowth angle**
- **vertical growth reported in literature**
- **our recent results: vertical**



Spacer sidewalls are gated through the high-K.

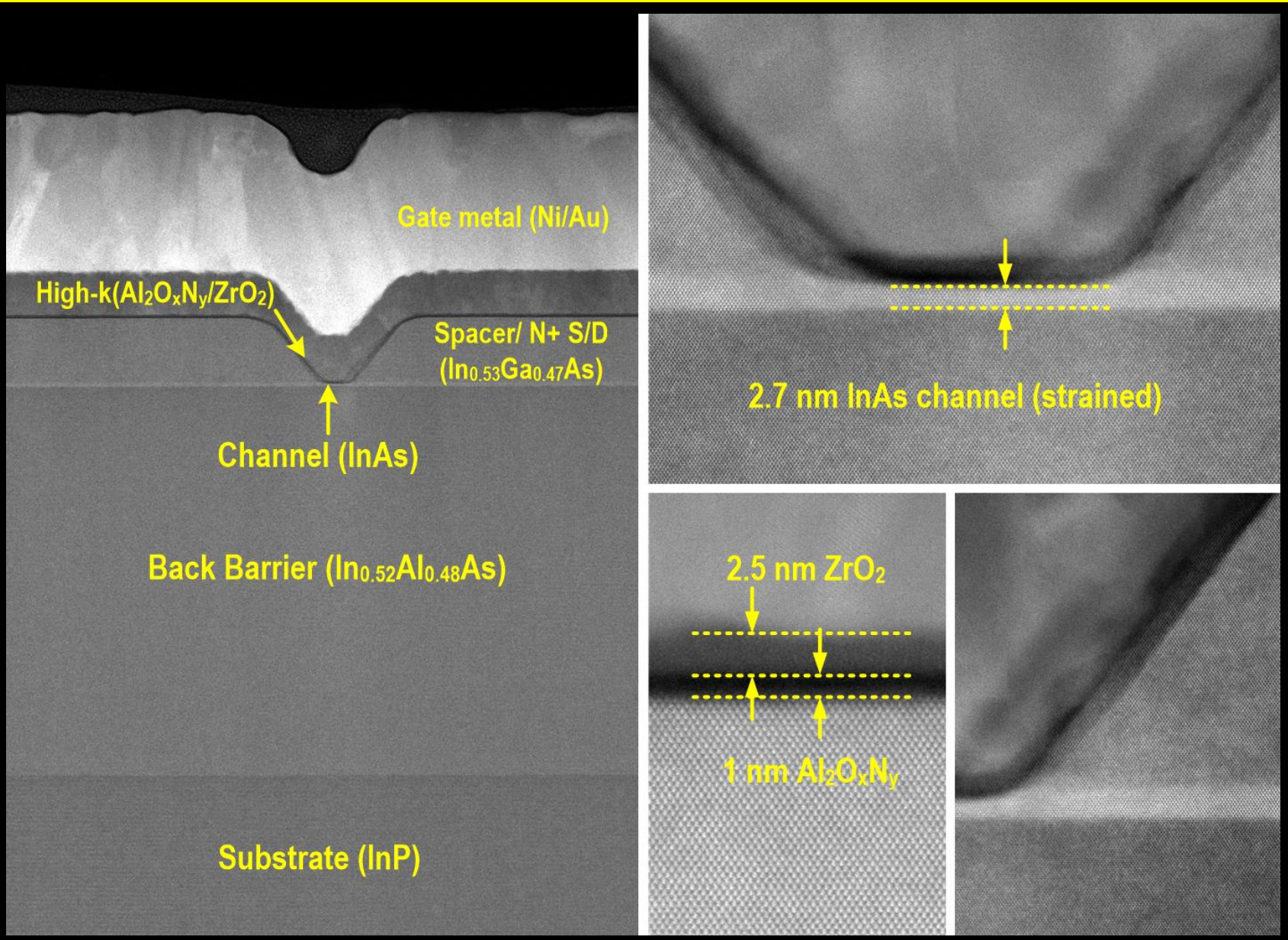
Capacitance to UID sidewalls is small.
- **added gate length→ adds ~0.3 fF/μm.**

Capacitance to N+ contacts layers is large.
- **easy to eliminate: low-ε_r sidewall spacer.**



Deliberate band offset between spacer & channel
- **compensates offset from strong quantization in channel.**

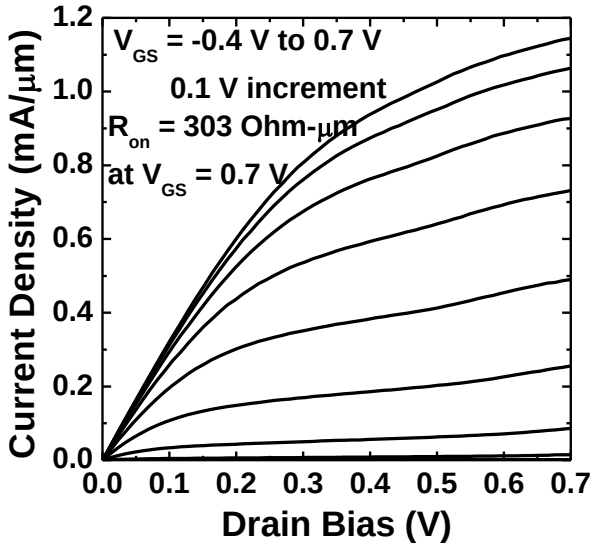
Reducing leakage (3): Ultra-thin channel

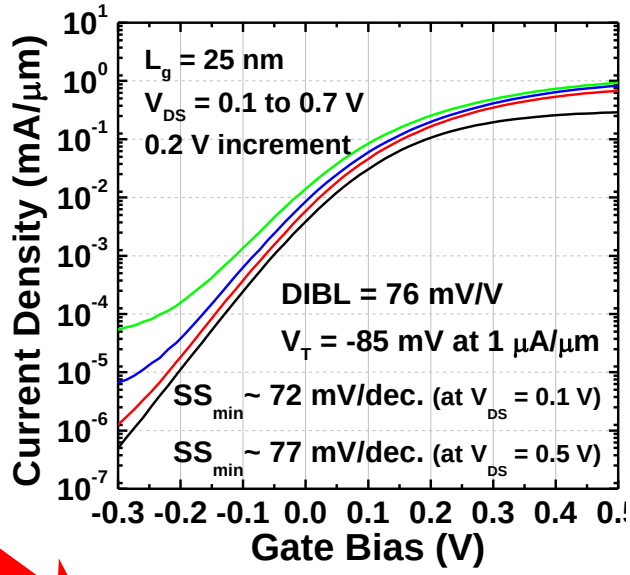


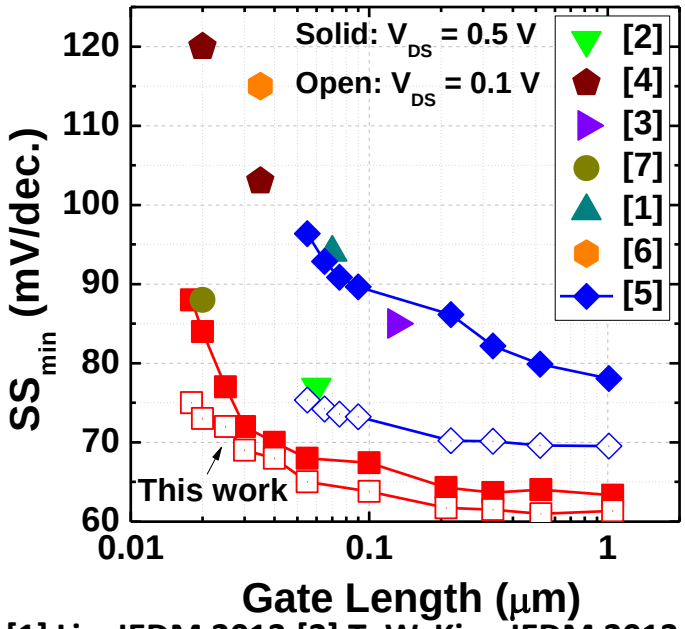
Courtesy of S. Kraemer (UCSB) *Heavy elements look brighter Lee *et al.*, 2014 VSLI Symposium

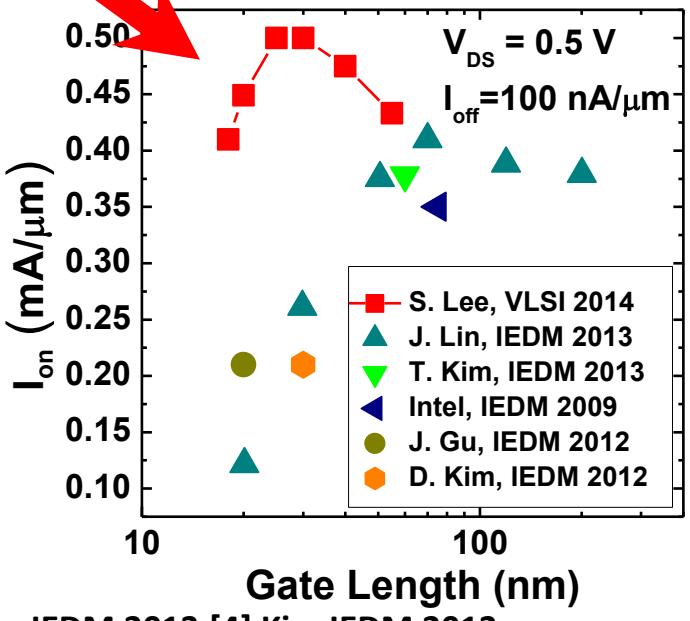
Reducing leakage (3): Ultra-thin channel

S. Lee et al., VLSI 2014



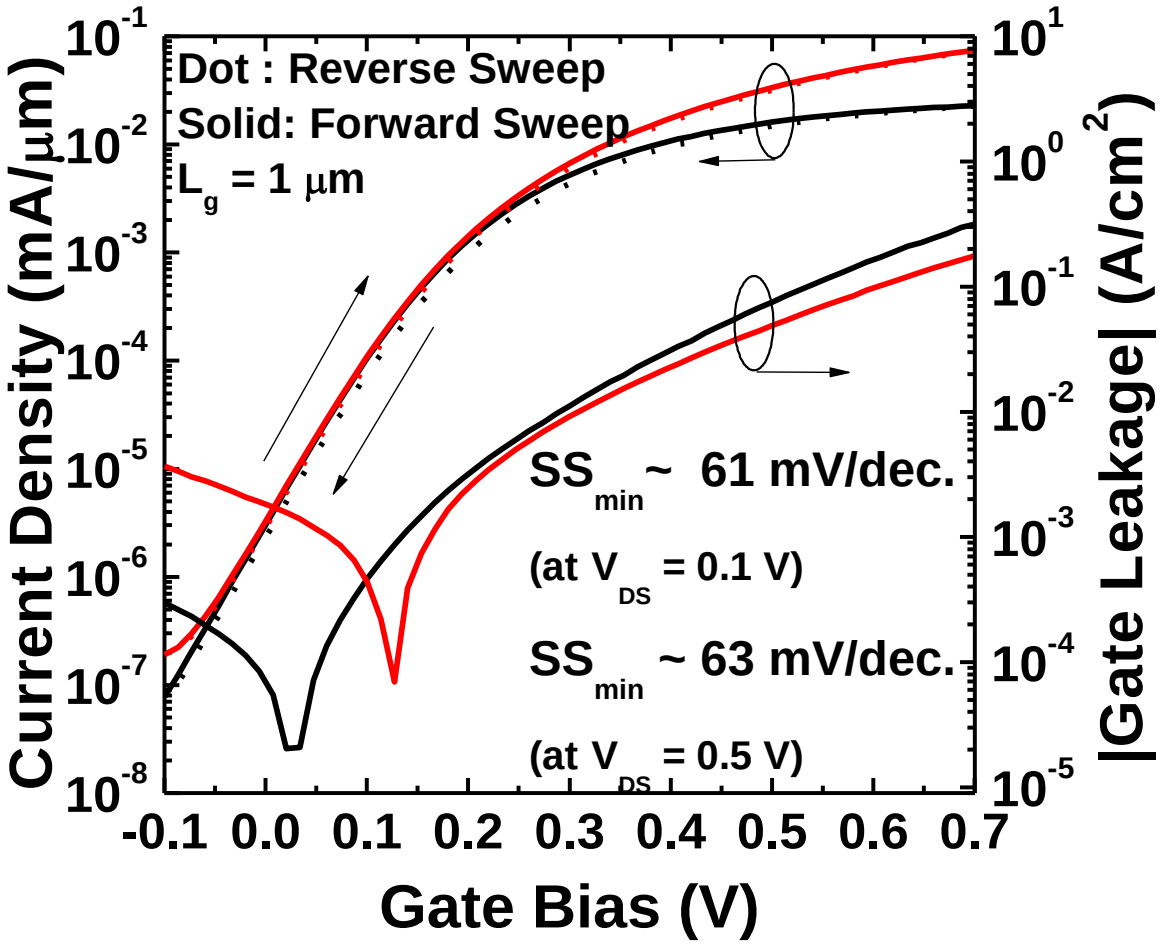






[1] Lin IEDM 2013,[2] T.-W. Kim IEDM 2013,[3] Chang IEDM 2013,[4] Kim IEDM 2013
[5] Lee APL 2013 (UCSB), [6] D. H. Kim IEDM 2012,[7] Gu IEDM 2012,[8] Radosavljevic IEDM 2009

MOSFET: 2.5nm ZrO_2/ 1nm Al_2O_3 / 2.5nm InAs



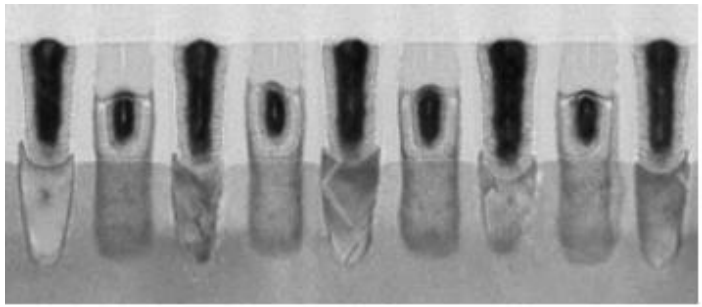
61 mV/dec Subthreshold swing at V_{DS}=0.1 V

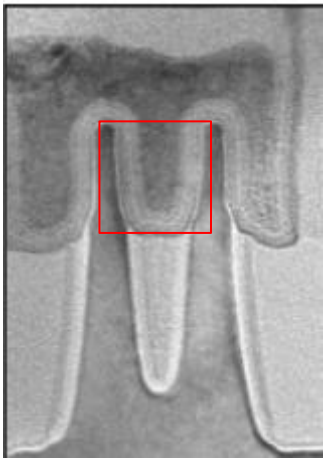
Negligible hysteresis

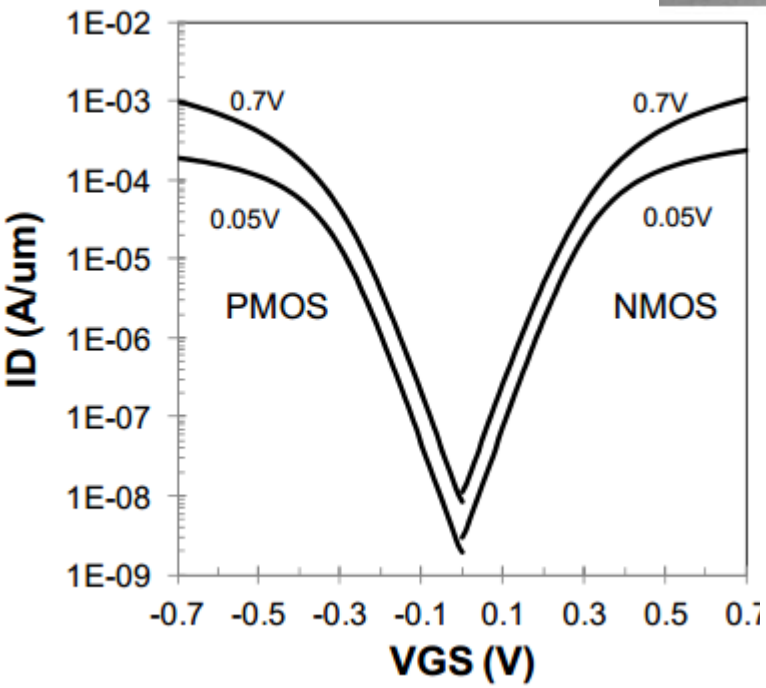
Compared to Intel 14nm finFET

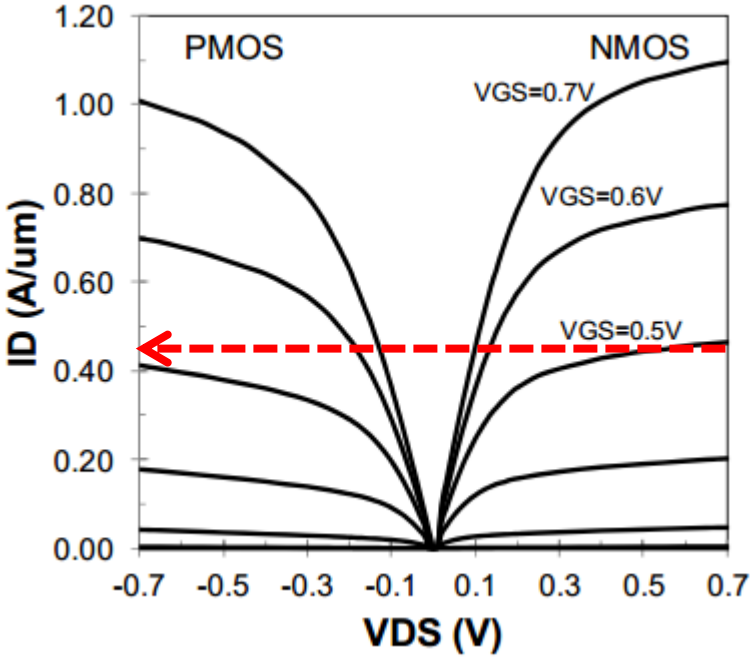
S. Natarajan et al, IEDM 2014, December, San Francisco

Layer	Pitch (nm)
Fin	42
Contacted Gate Pitch	70
Metal 0	56
Metal 1	70
Metal 2	52





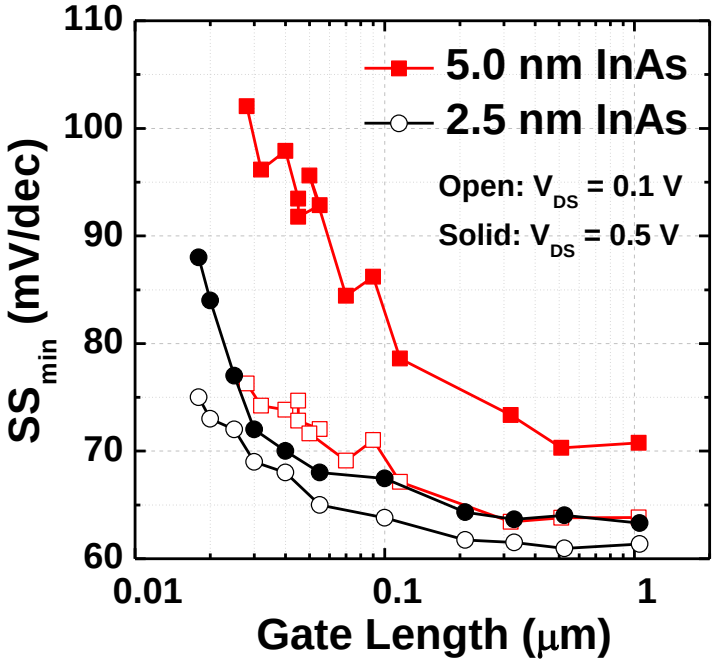


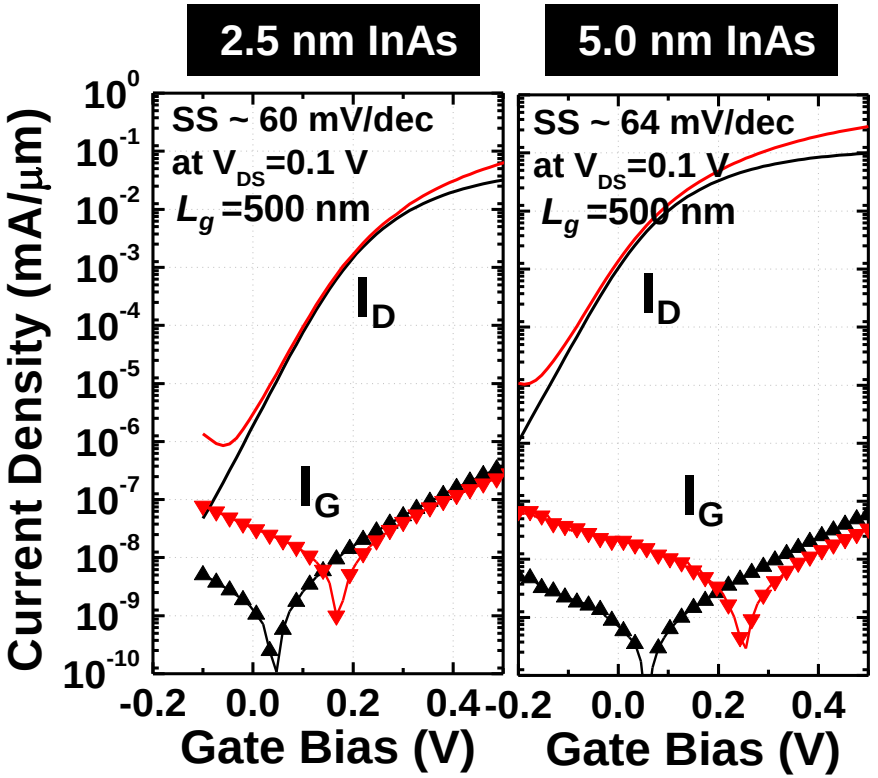


I_{off}=10nA/μm, I_{on}=0.45mA/μm @V_{DS}=0.5V ***per μm of fin footprint***

Re-normalizing to fin periphery: ~0.24 mA/μm

Off-state comparison: 2.5 nm vs. 5.0 nm-thick InAs channel





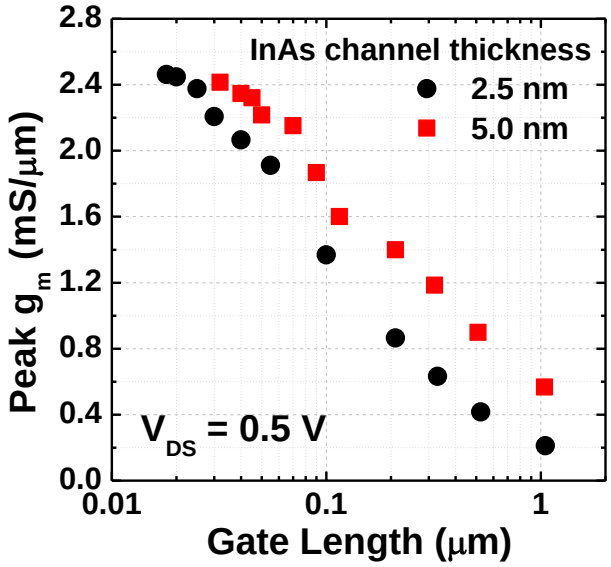
Better SS at all gate lengths

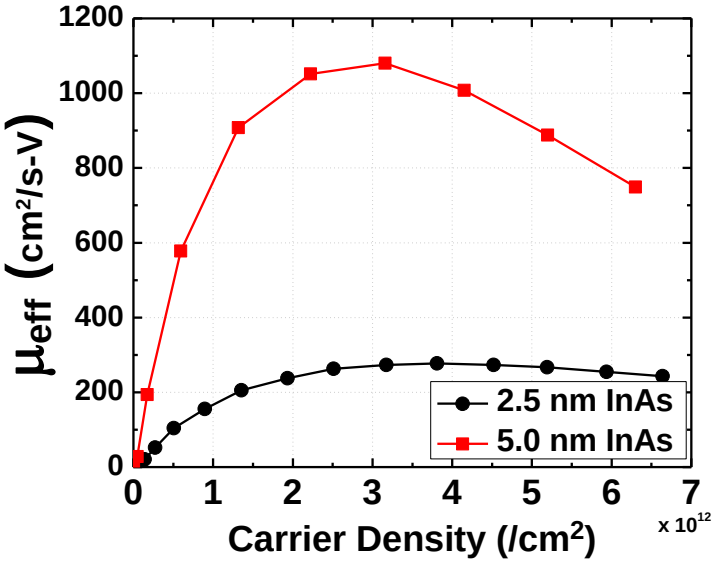
🡐 Better electrostatics (aspect ratio) and reduced BTBT (quantized E_g)

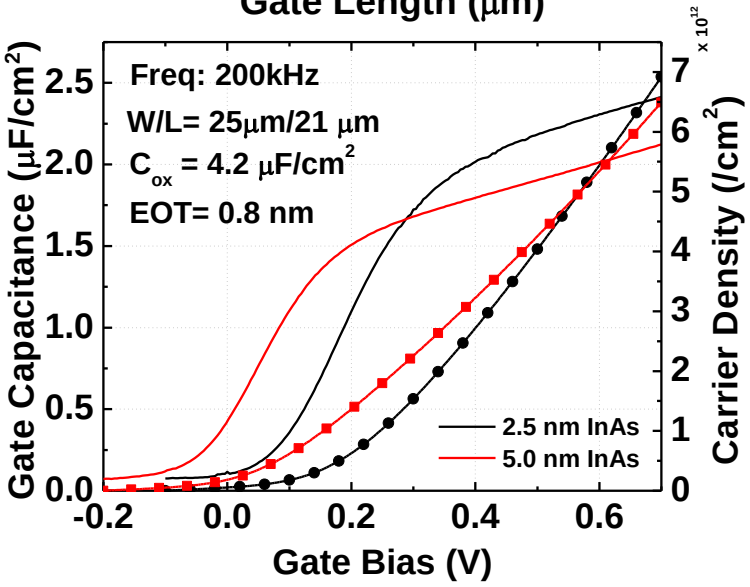
~10:1 reduction in minimum off-state leakage

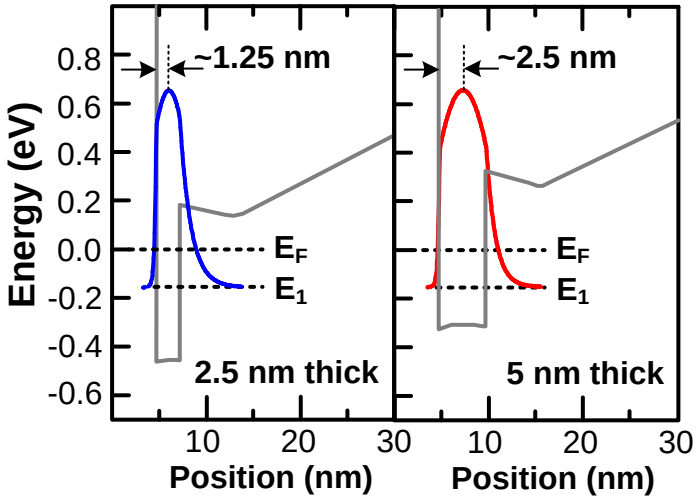
~5:1 increase in gate leakage 🡐 increased eigenstate

On-state comparison: 2.5 nm vs. 5.0 nm-thick InAs channel





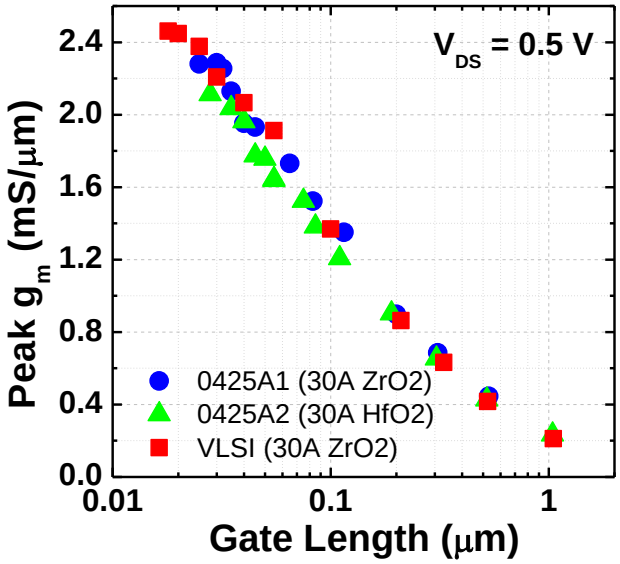


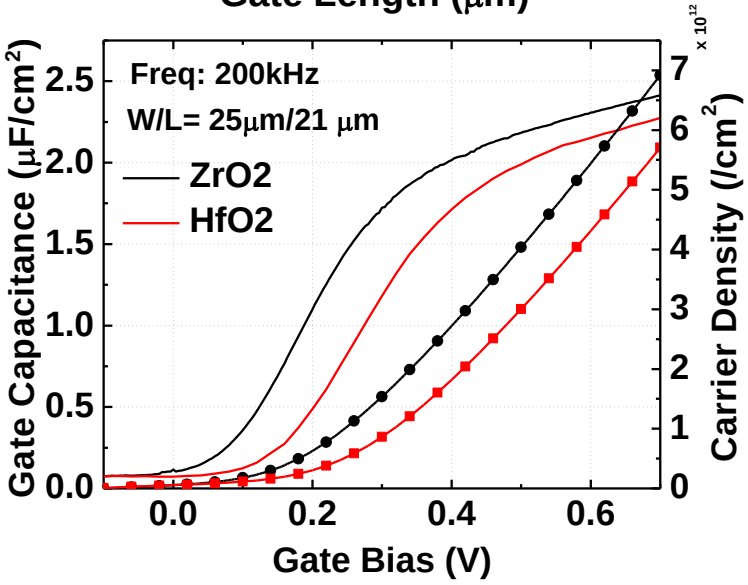


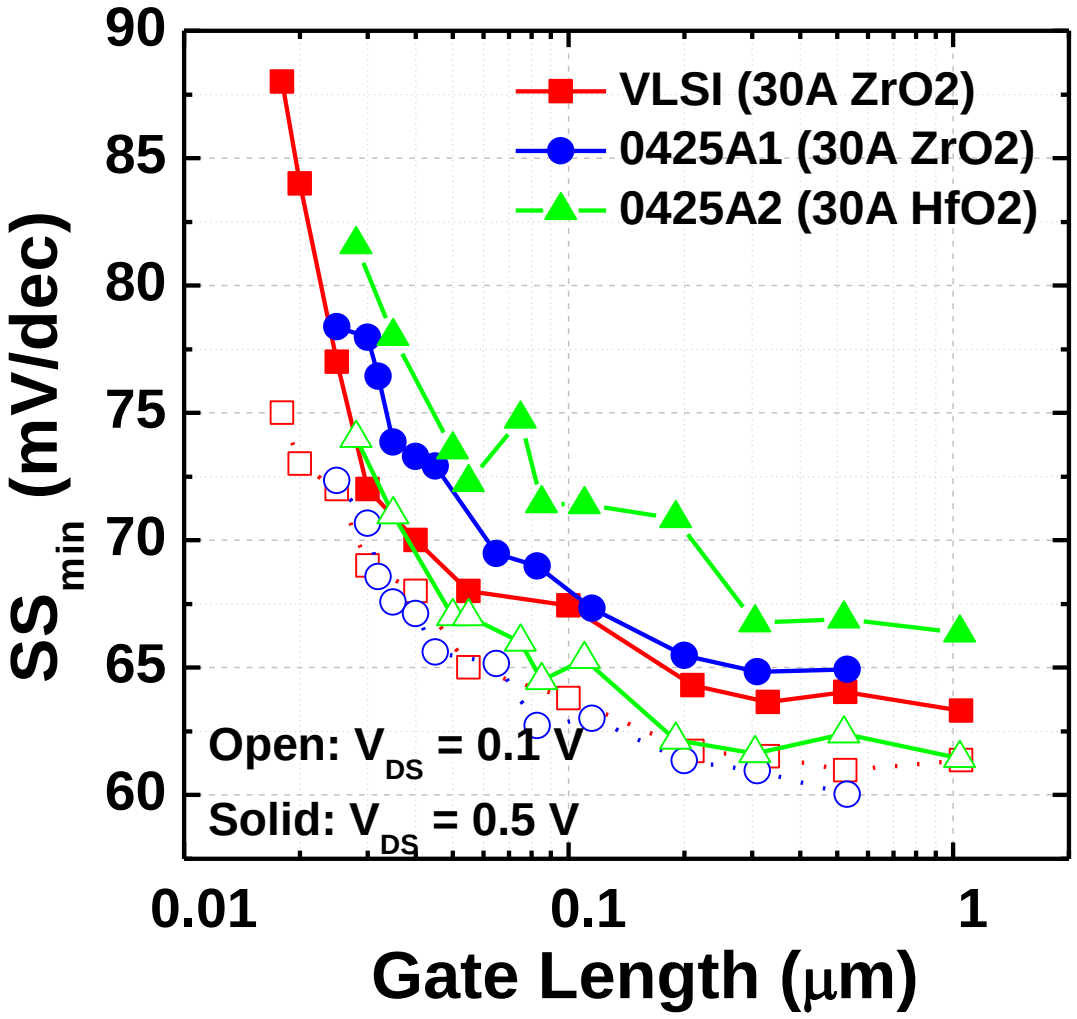
1D-Possion Schrodinger solver
(coded by W. Frensley, UT Dallas)

ZrO_2 vs. HfO_2: Peak g_m, SS, split-CV, and mobility

Comparison: two process runs ZrO_2, one run HfO_2, both 2nm (on 1nm Al_2O_3)



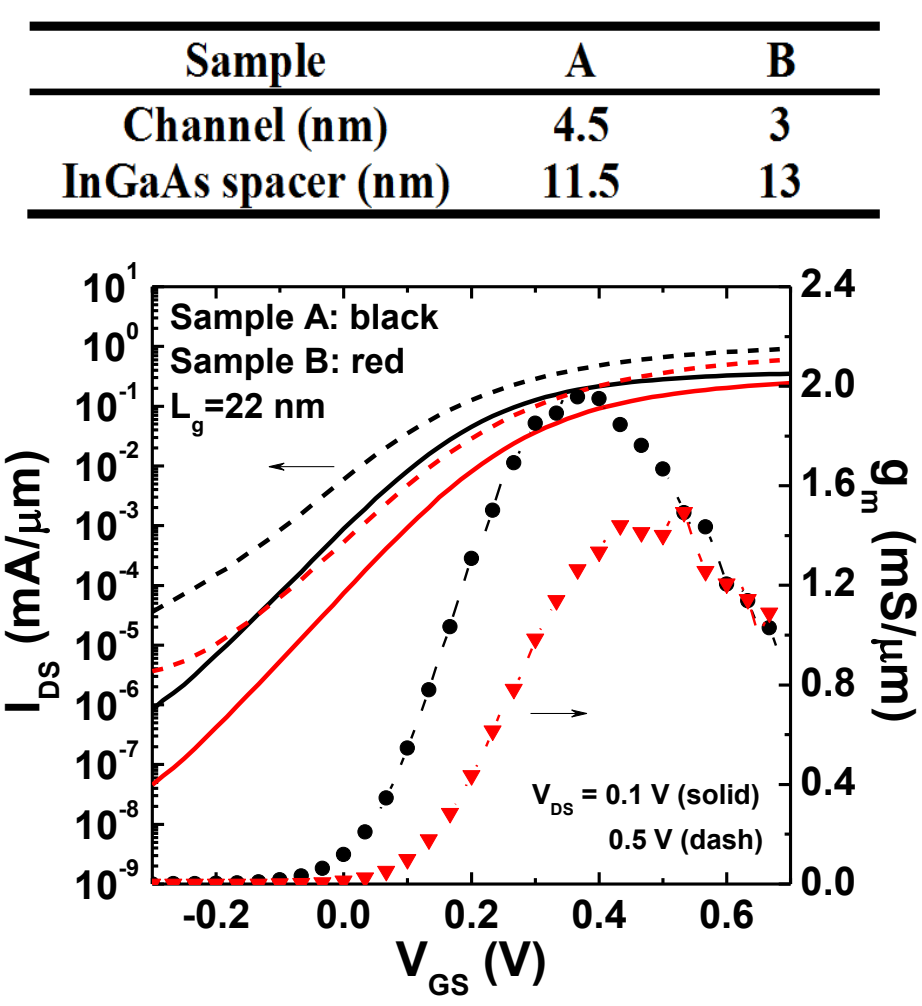


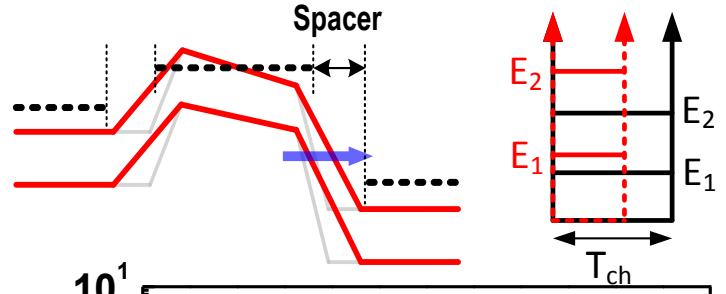


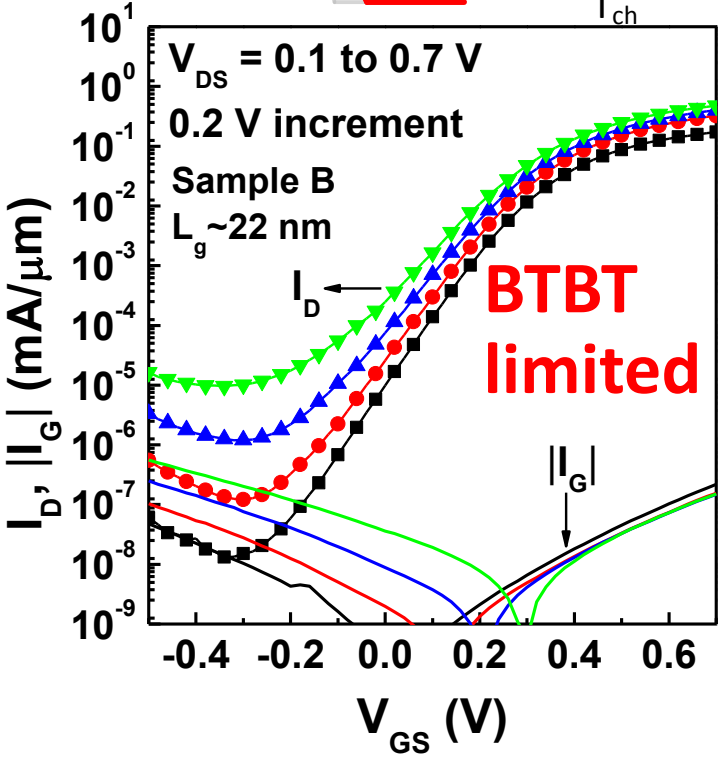
(1) ZrO_2 higher capacitance than HfO_2, (2) ZrO_2 results are reproducible

Reducing leakage (4): Thin InGaAs Channel

Sample	A	B
Channel (nm)	4.5	3
InGaAs spacer (nm)	11.5	13



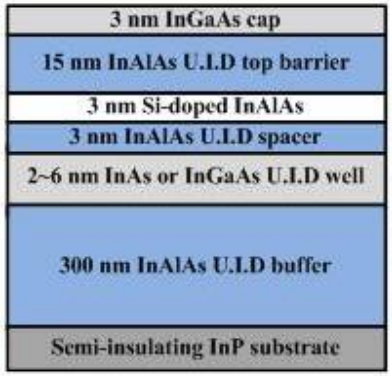


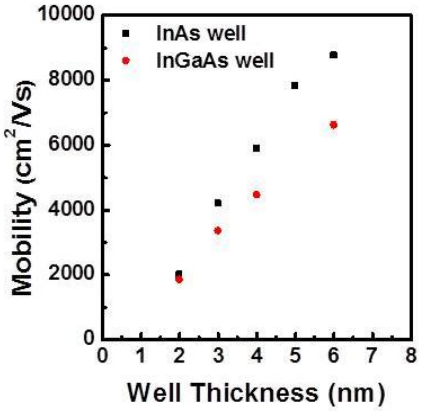


Reducing channel thickness improves electrostatics, increases confinement bandgap and reduces BTBT.

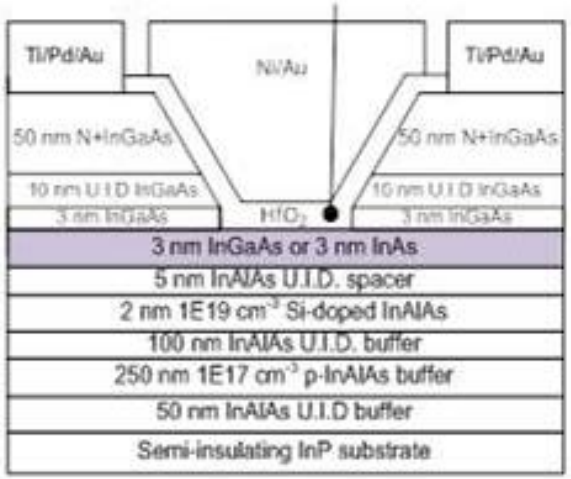
InGaAs vs. InAs Channel

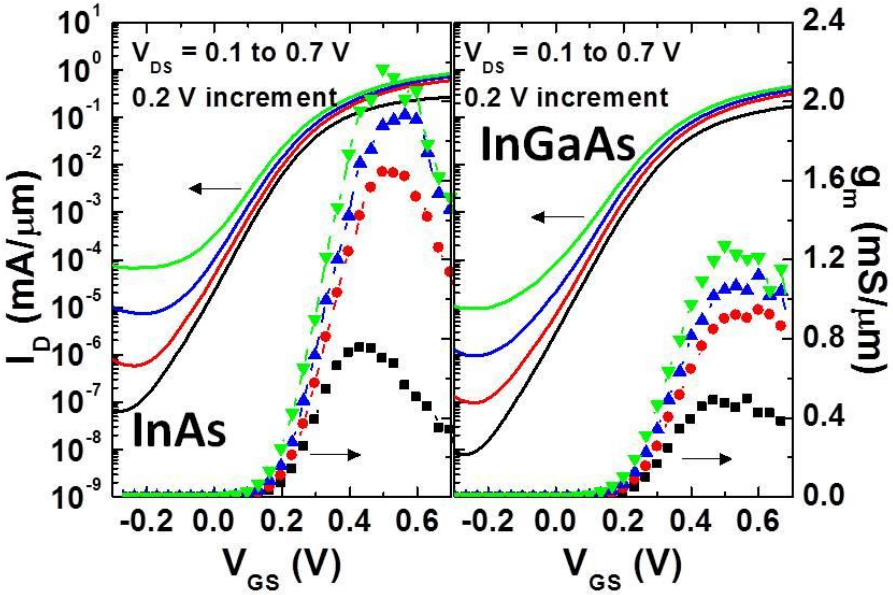
similar mobility in 2-3 nm thick quantum well



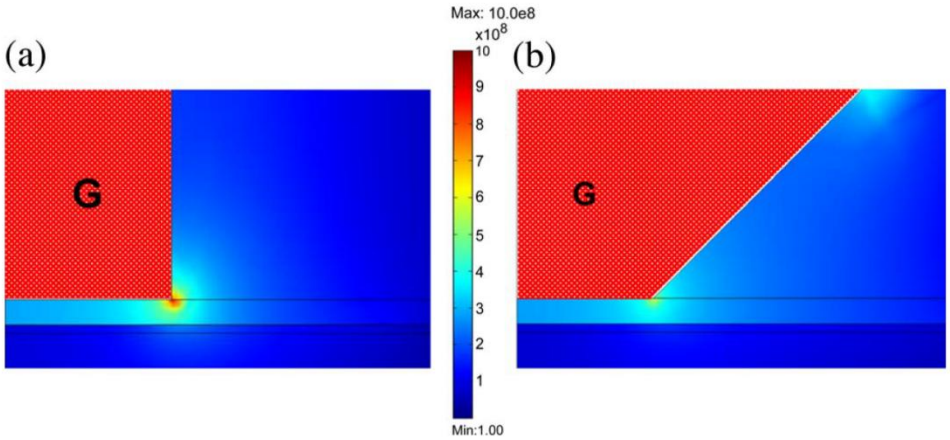


InGaAs has lower on-current in FET with 3nm thick channel ?!?

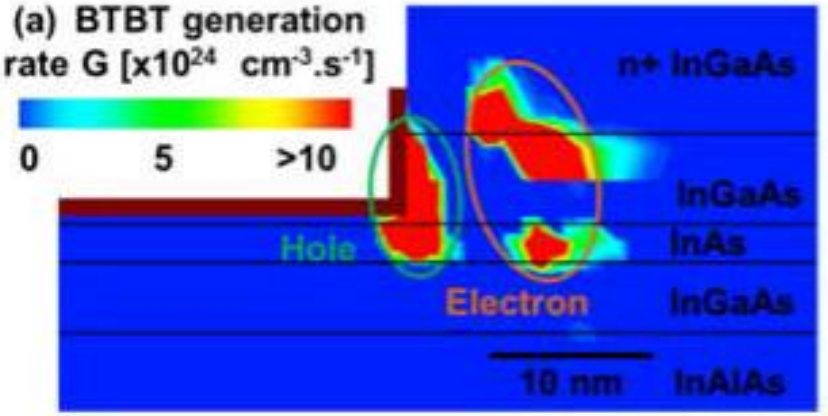




E-field and BTBT contour



R. Chu et al., EDL 29, 974 (2008)



J. Lin et al., EDL 35, 1203 (2014)

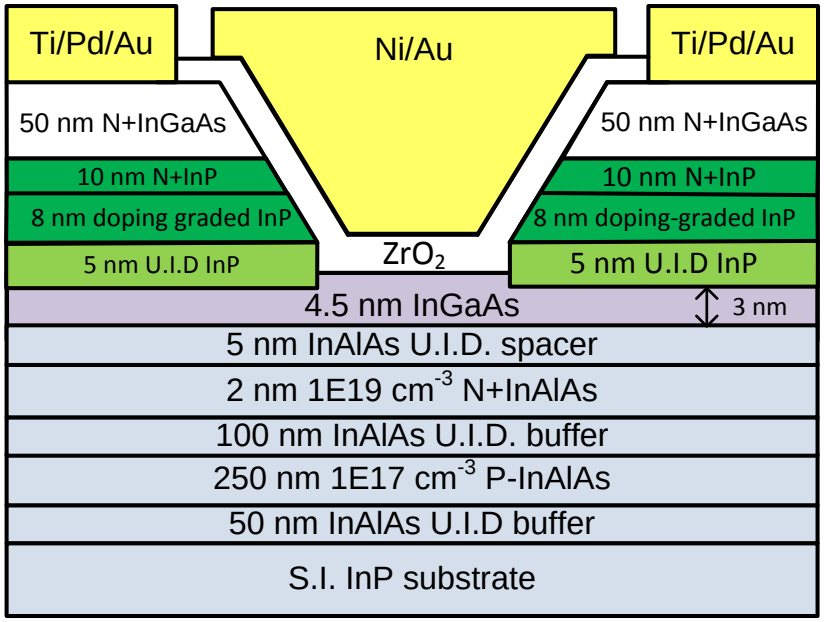
Concentrated electric field at the drain end of the channel

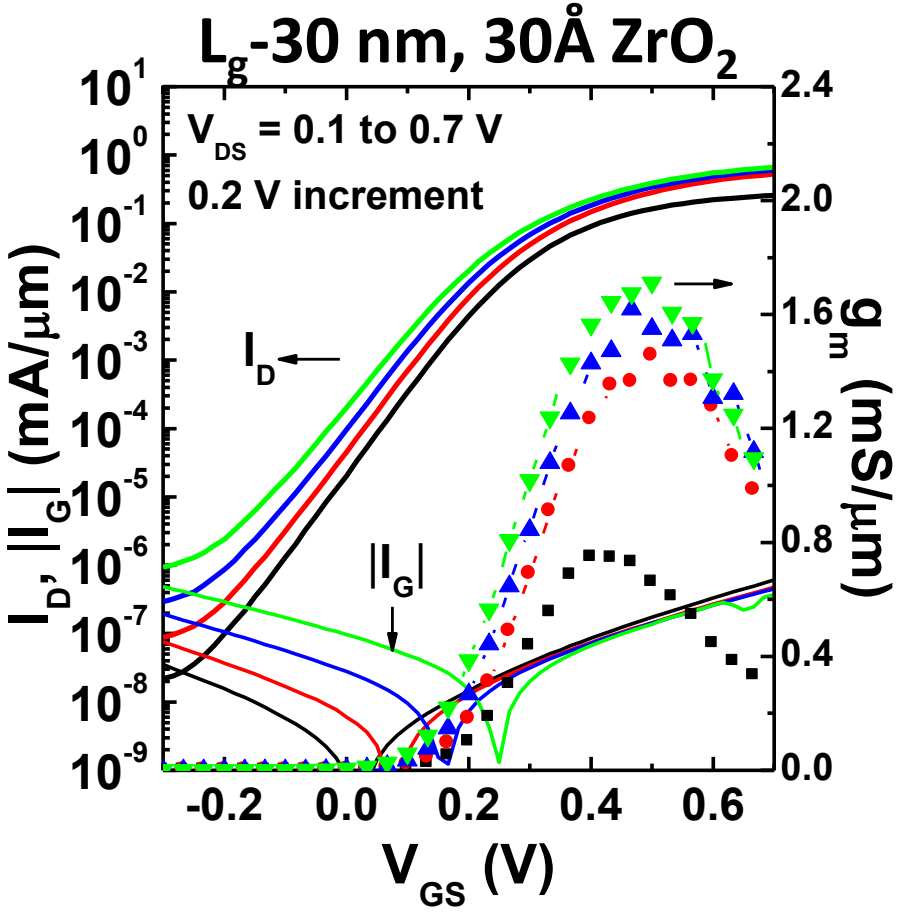
Solution:

Replace InGaAs with wide band-gap InP (Eg~1.35 eV)

Reducing leakage (5): Doping-graded InP spacer

C-Y Huang, 2014 IEDM



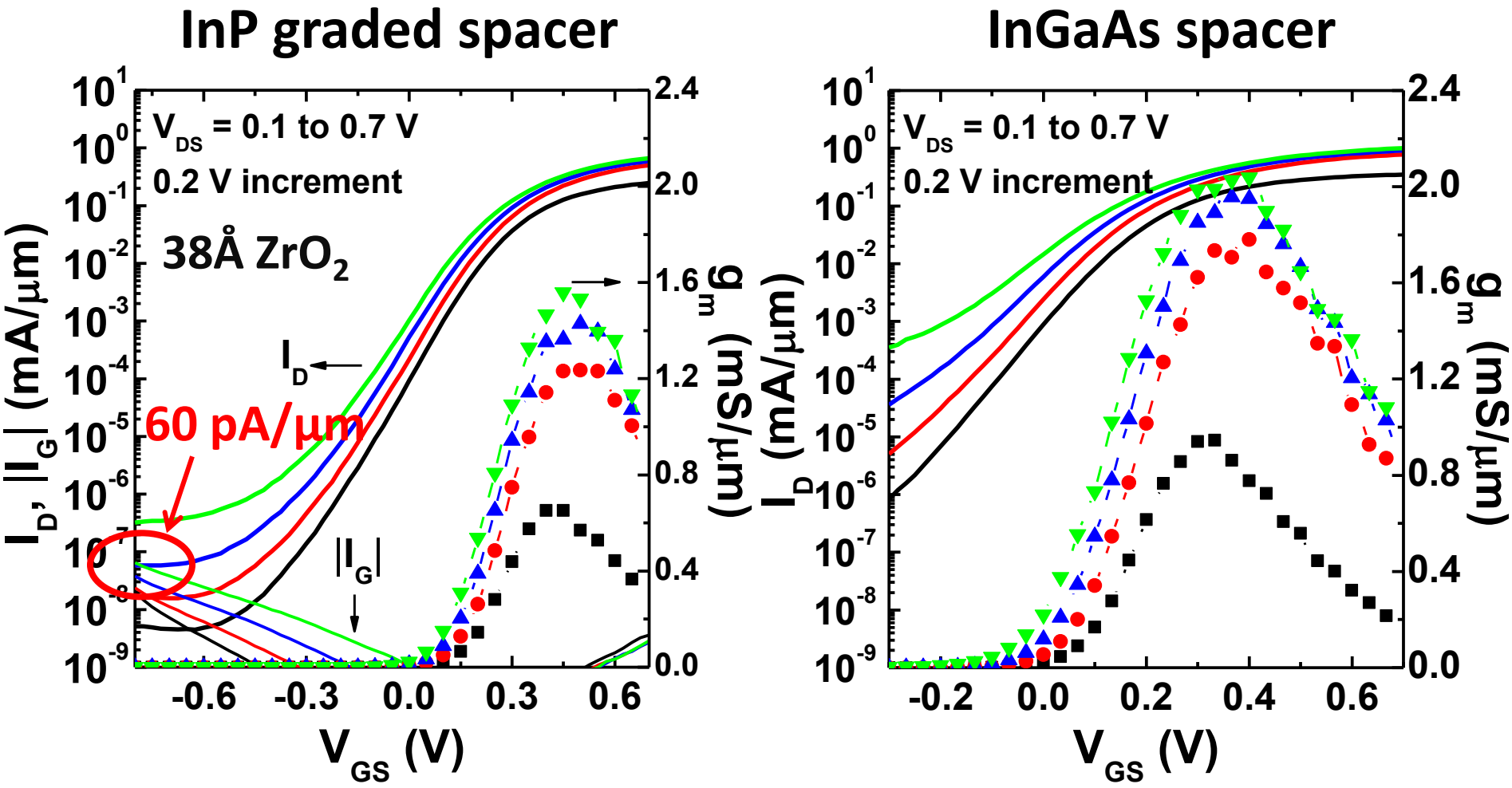


R_{on} at zero L_g (Ω·μm)	5 nm UID InP	13 nm UID InP	Doping graded InP
	~199	~364	~270

Doping-graded InP spacer reduces parasitic source/drain resistance and improves G_m.

Gate leakage limits I_{off}~300 pA/μm.

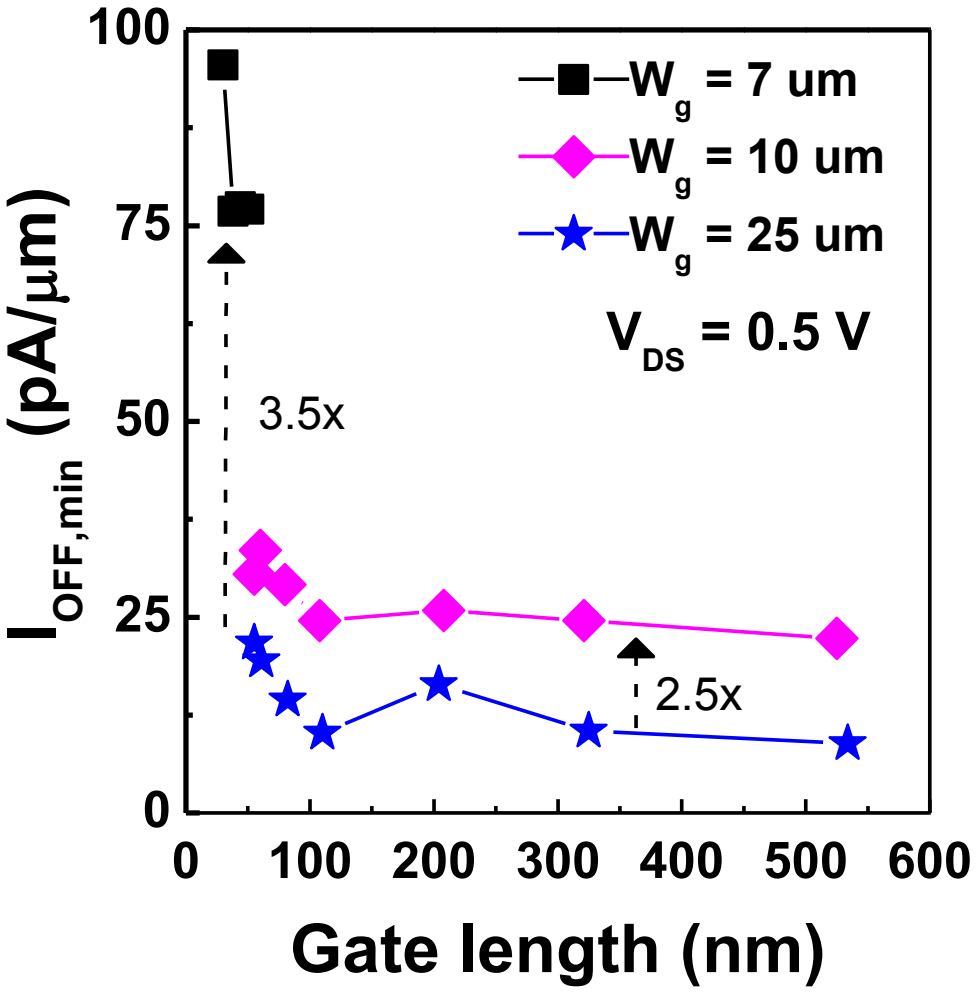
Reducing leakage (6): Thicker Dielectric

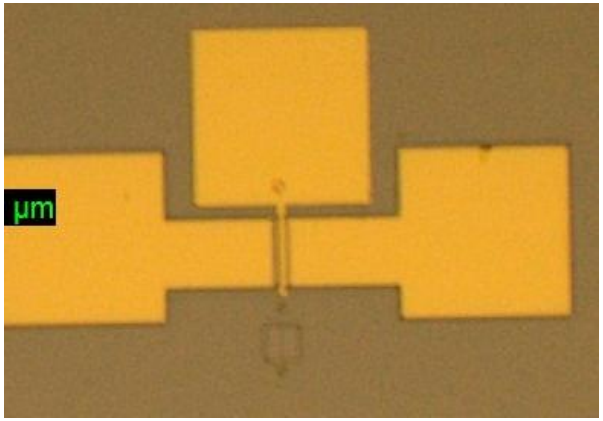


Minimum I_{off}~ 60 pA/μm at V_D=0.5V for L_g-30 nm

100:1 smaller I_{off} compared to InGaAs spacer

Leakage now dominated by imperfect isolation



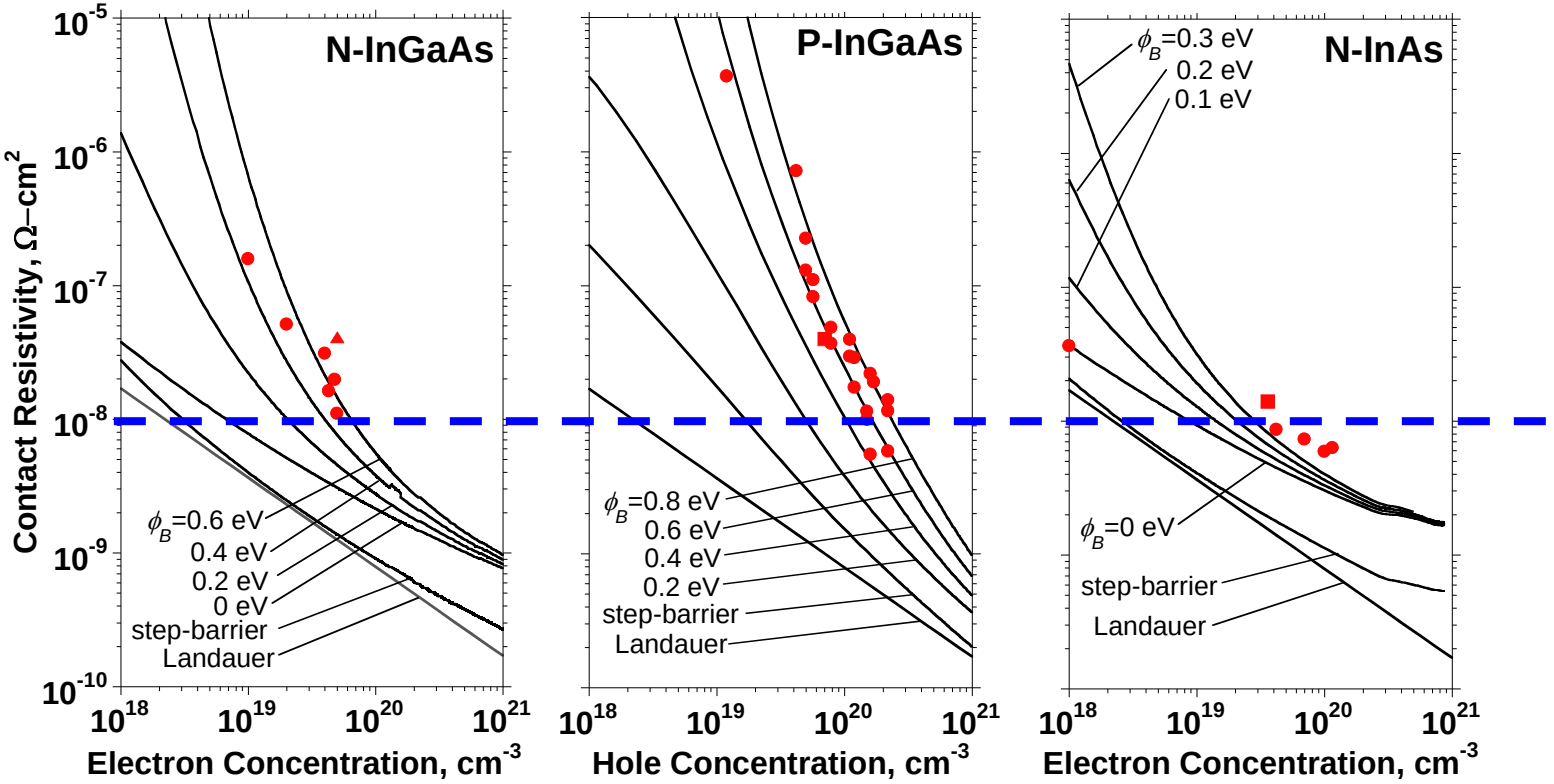


Leakage current is independent of gate width

→ leakage now dominated by imperfect device isolation, by edges of device mesa.

Refractory Contacts to In(Ga)As

Baraskar *et al*, Journal of Applied Physics, 2013



Refractory: robust under high-current operation / Low penetration depth: ~ 1 nm / Performance sufficient for 32 nm /2.8 THz node.

State-of-art in III-V contacts: ~5*10^{-9} Ω-cm²

Key: high doping, clean surfaces, high indium content for N-type

III-V on Si

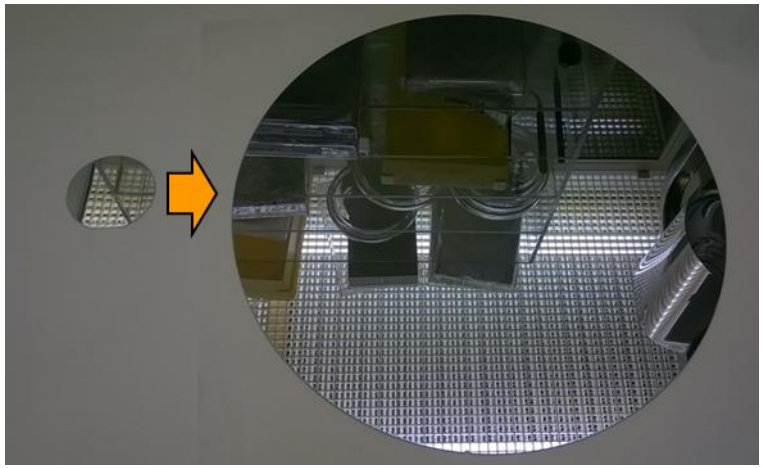
Ultrathin InAs-Channel MOSFETs on Si Substrates

Cheng-Ying Huang[1], Xinyu Bao[2], Zhiyuan Ye[2], Sanghoon Lee[1], Hanwei Chiang[1], Haoran Li[1], Varistha Chobpattana[3], Brian Thibeault[1], William Mitchell[1], Susanne Stemmer[3], Arthur Gossard[1,3], Errol Sanchez[2], and Mark Rodwell[1]

[1]ECE, University of California, Santa Barbara
[2]Applied Materials, Santa Clara
[3]Materials Department, University of California, Santa Barbara

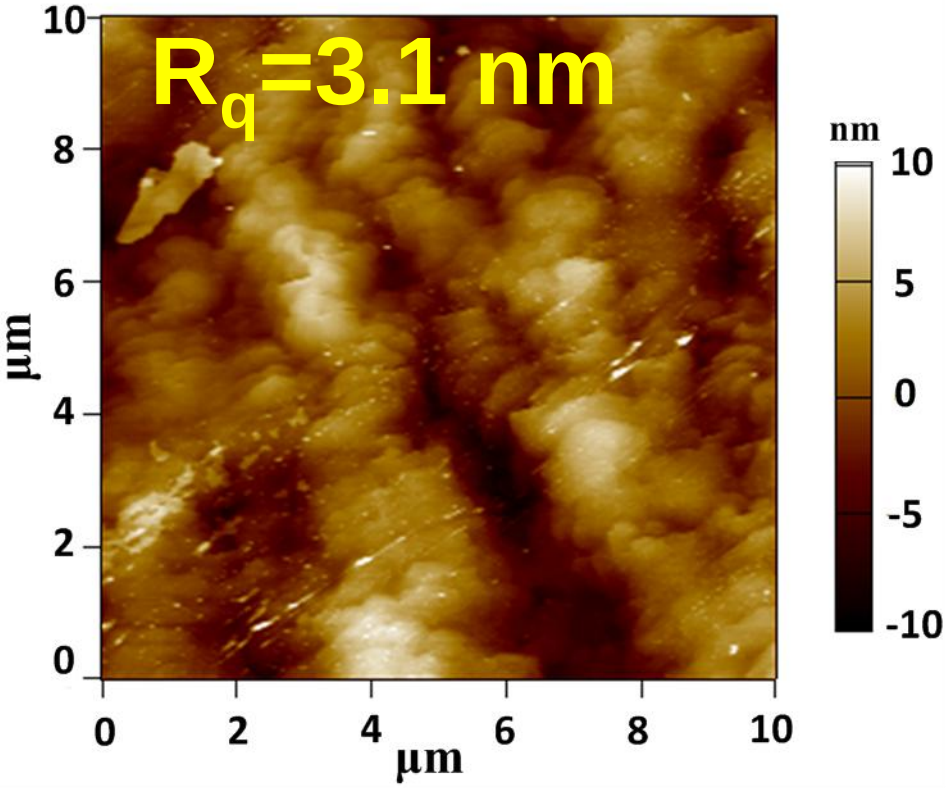
VLSI-TSA 2015
HsinChu, Taiwan

Applied Materials III-V buffer on Si

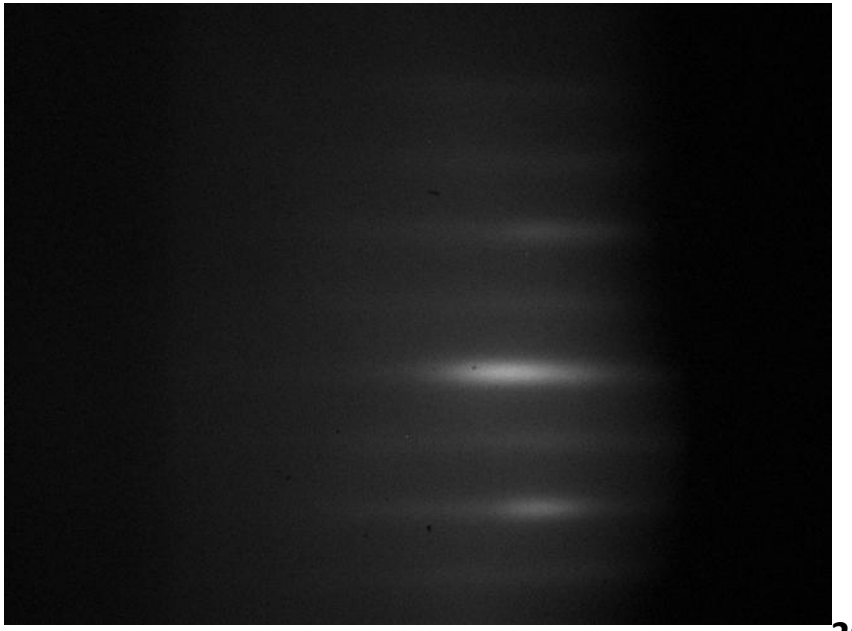


10 nm InP cap layer
50 nm InAlAs metamorphic buffer
20 nm <1E18 cm^{-3} P-InGaAs layer
300 nm InP metamorphic buffer
400 nm GaAs metamorphic buffer
Silicon substrate

Applied Materials MOCVD

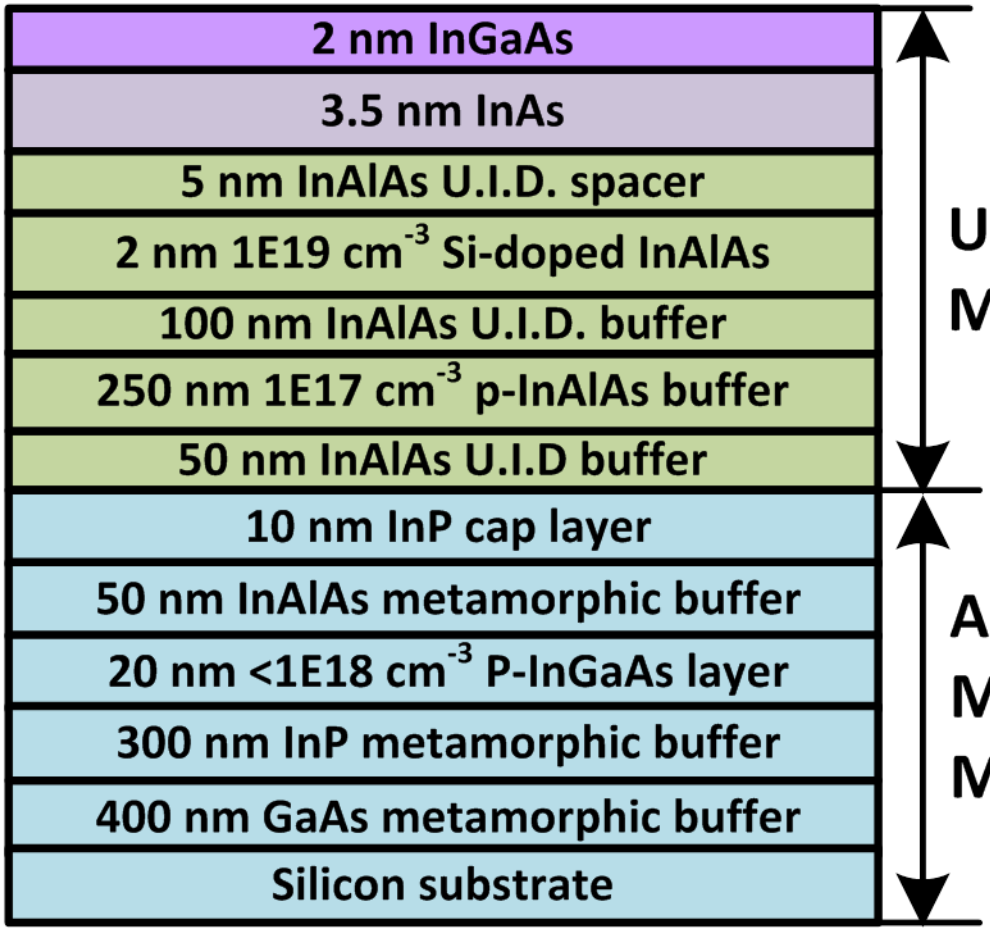


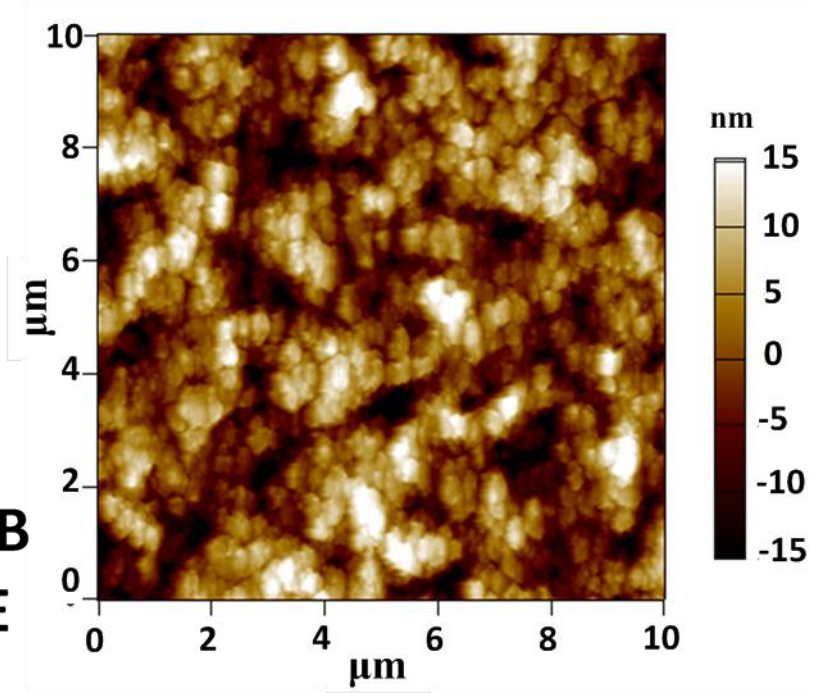
RHEED in MBE



UCSB III-V FET epitaxy

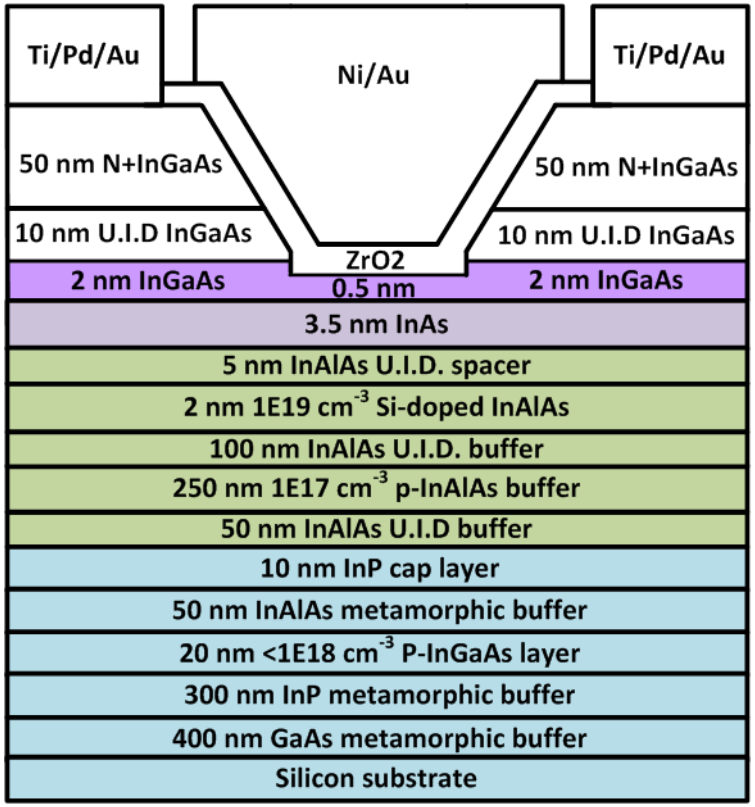
Surface roughness is degraded after FET epitaxy.

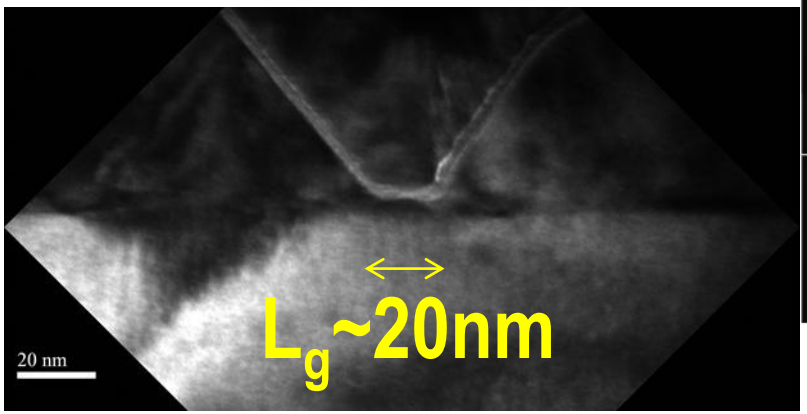


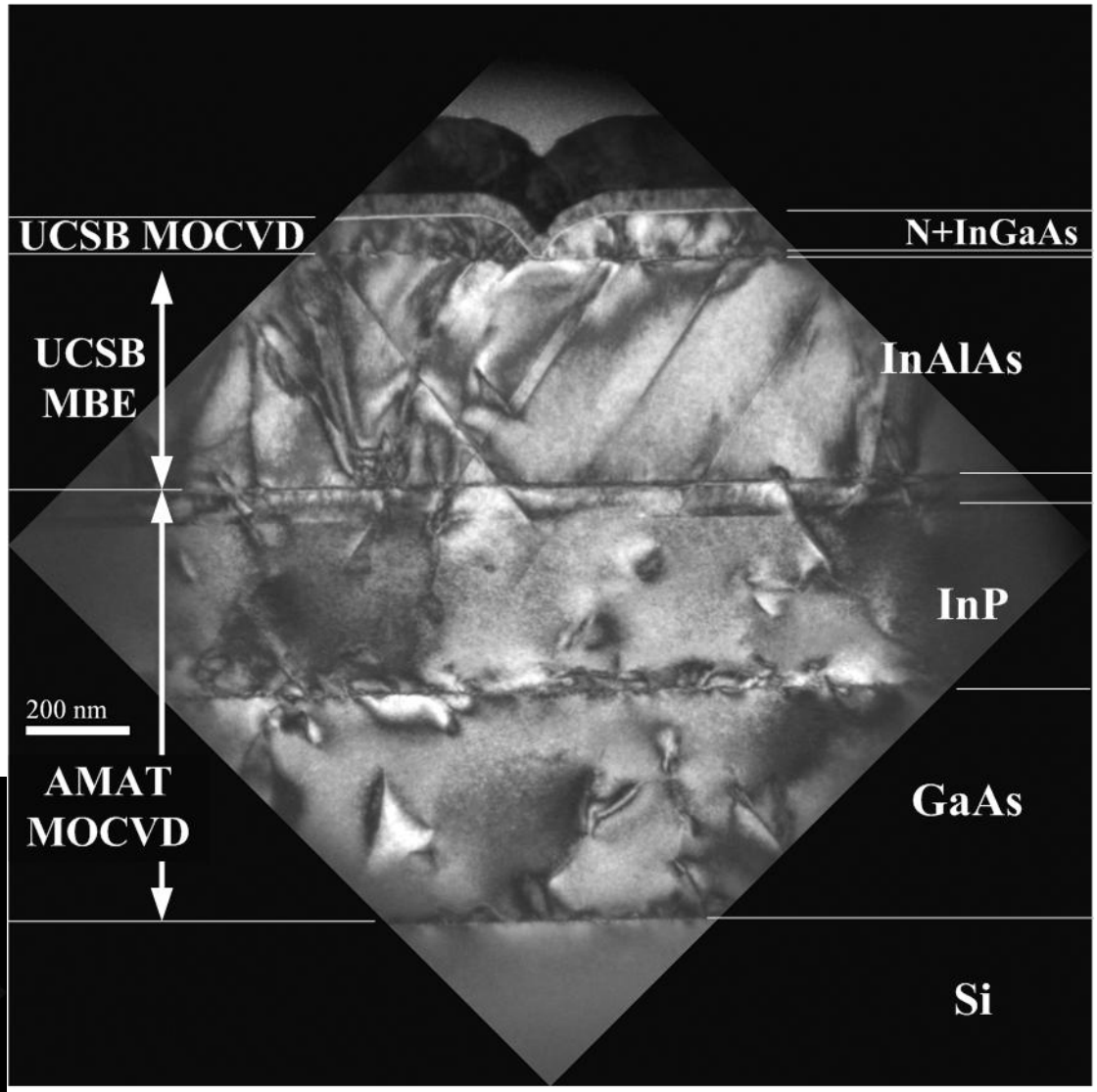


R_q= 6.9 nm

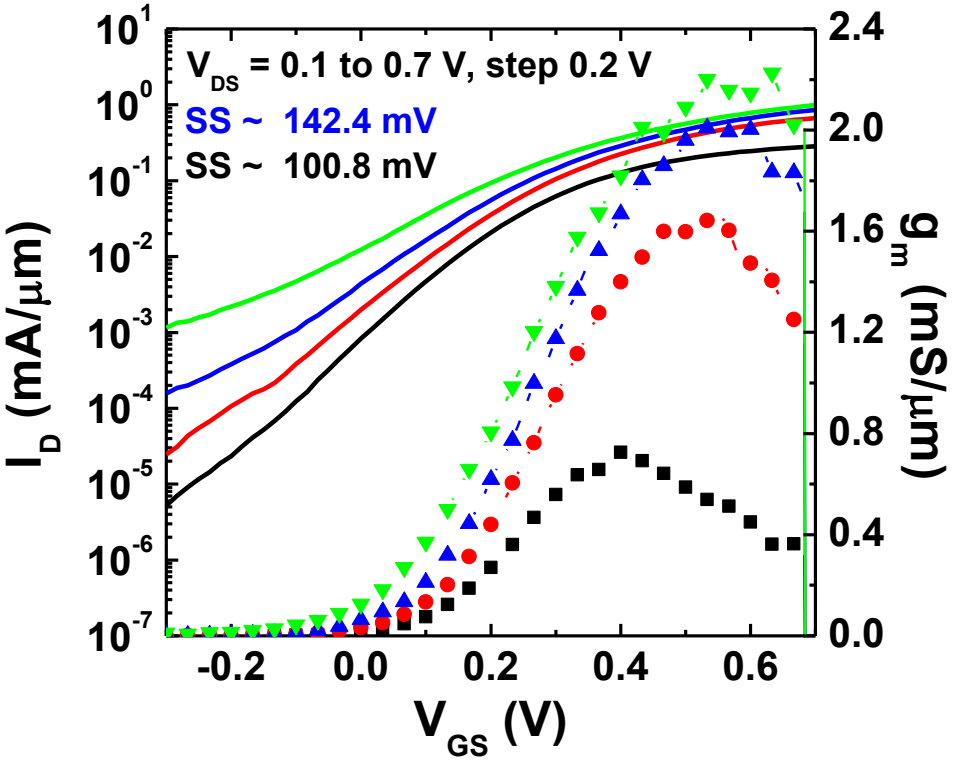
TEM images of III-V FET on Si

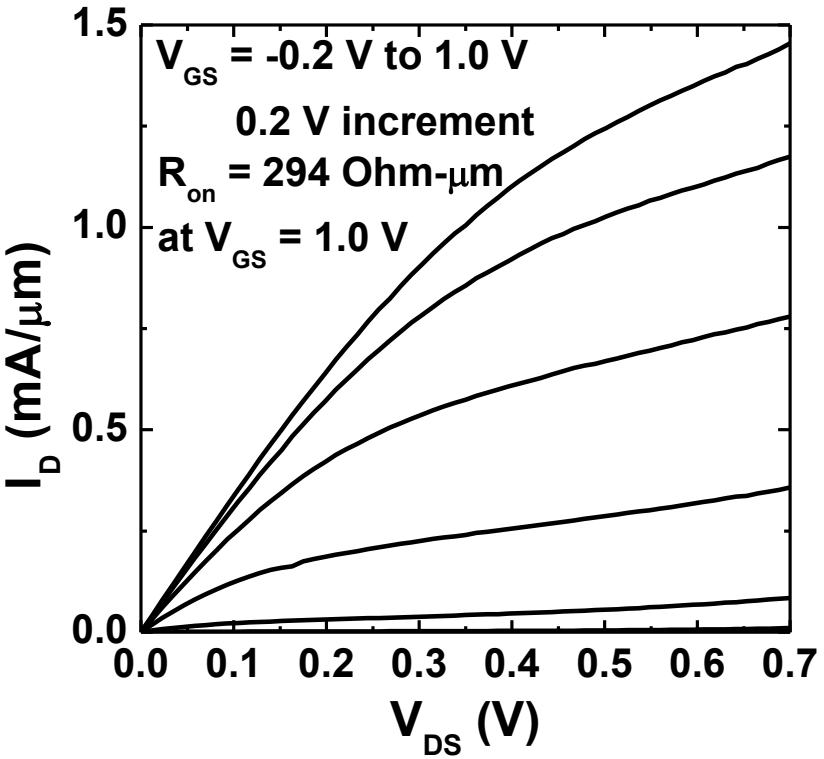






Short gate length: L_g-20 nm



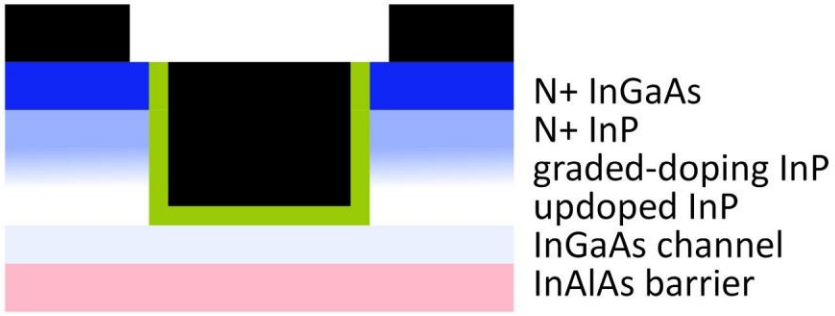


- High G_m~2.0 mS/μm at V_D=0.5 V.
- SS~140 mV/dec. at V_D=0.5 V and 101 mV/dec. at V_D=0.1 V
- High I_{on} >1.4 mA/um at V_{GS}=1V.

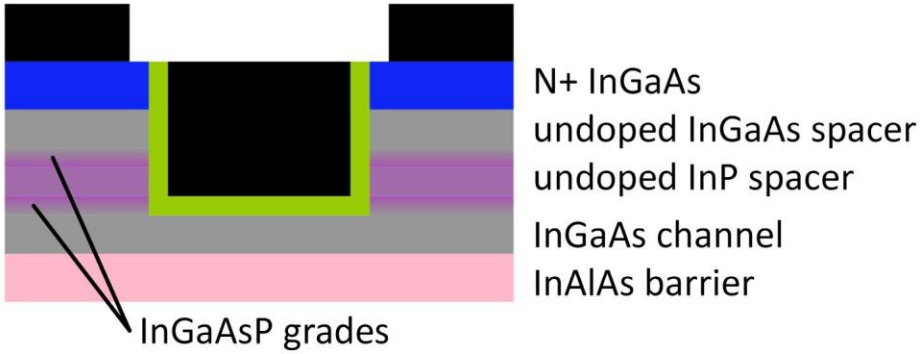
Future Work

Future Work: High Current & Low Leakage

Doping-graded InP spacers



InGaAs/InP spacers



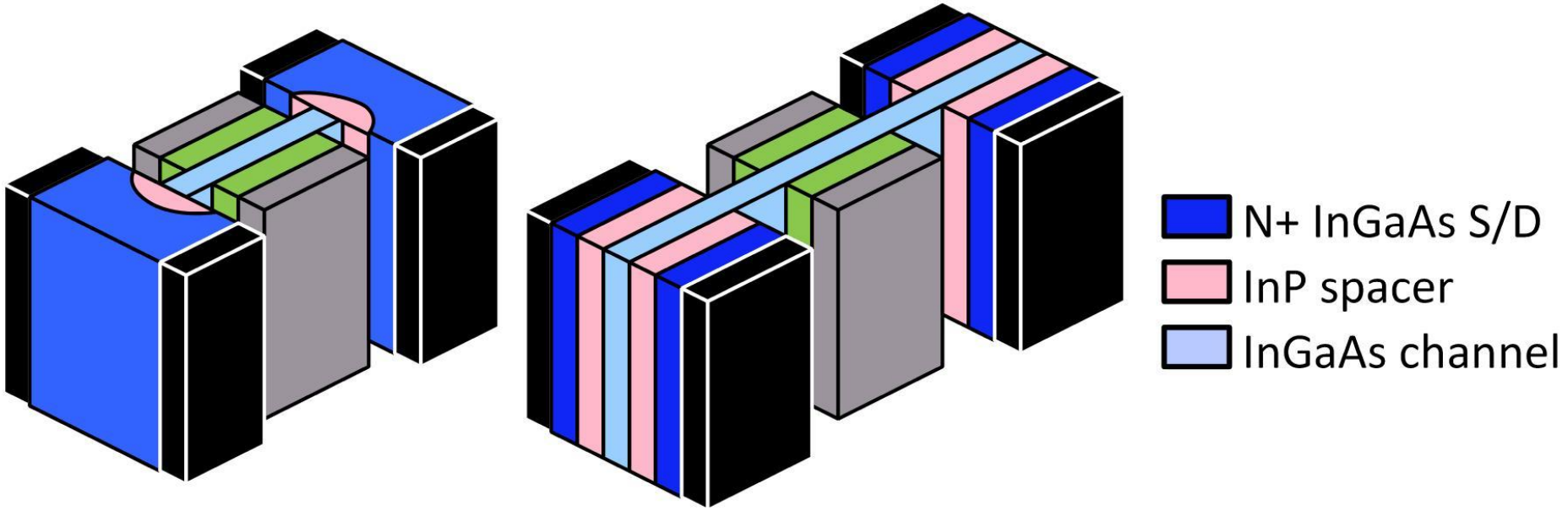
Wide-gap spacer near channel: reduces BTBT

Upper spacer: improves electrostatics

Thick InP spacers add source resistance, reduce I_{on}.

Solution: composite InP/InGaAs spacer with InGaAsP grades

Future Work: High Current & Low Leakage



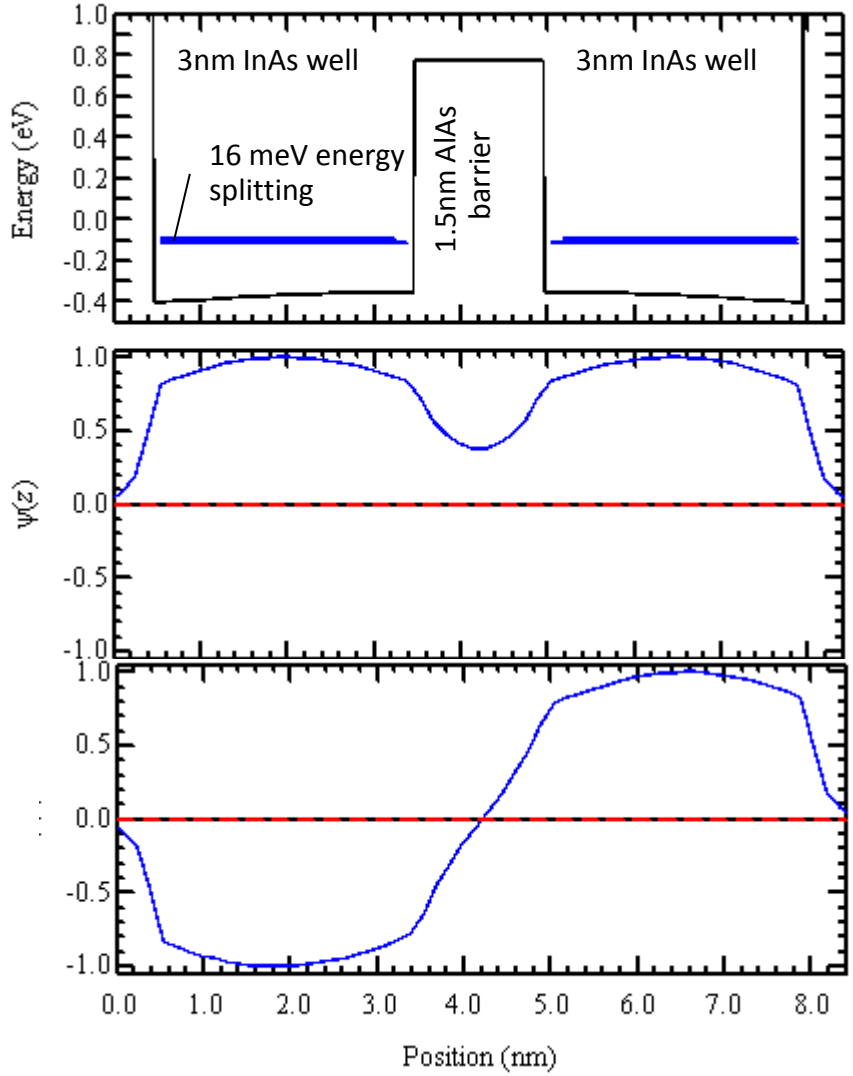
finFETs: better electostatics→ thick spacers not needed

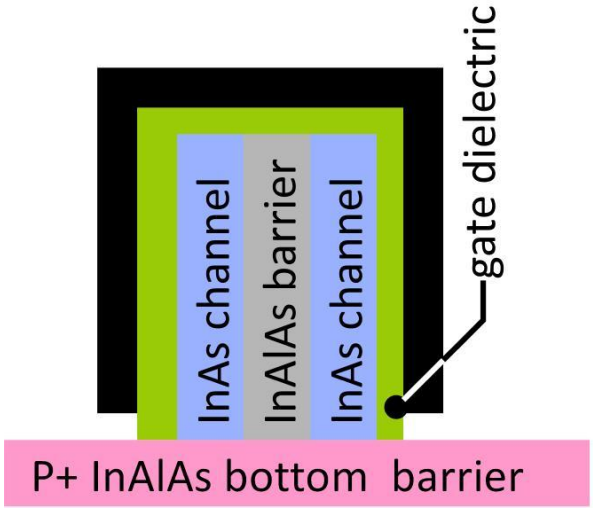
Need only thin InP spacer to supress BTBT

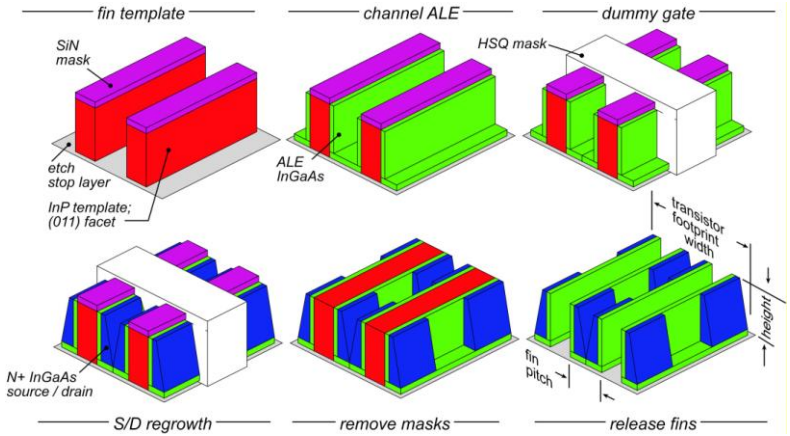
→ improved on-current

InP spacer formed during S/D regrowth.

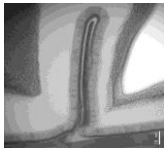
finFET with surface vs. bulk inversion.







Cohen-Elias *et al.*, DRC 2013



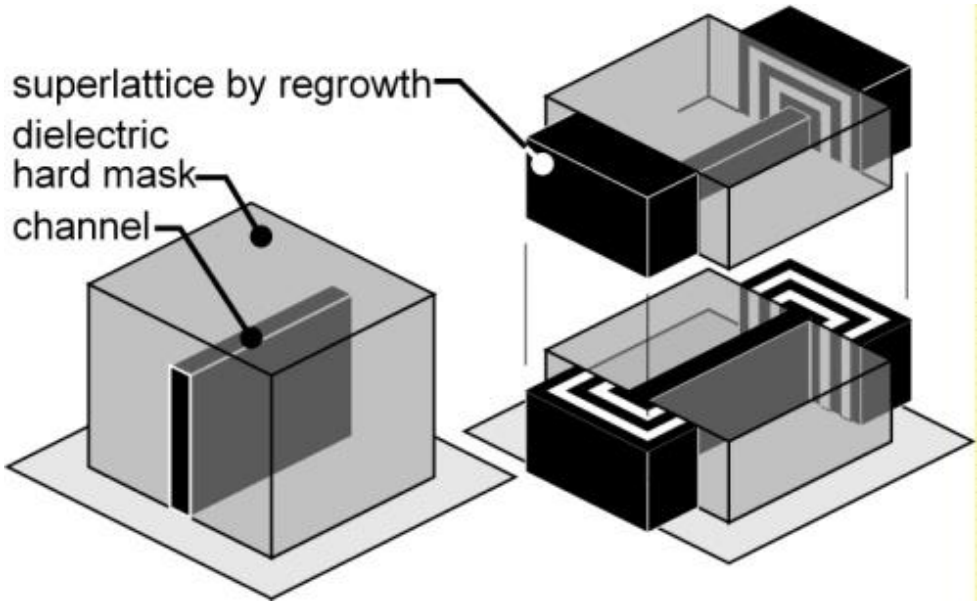
Next: Superlattice Steep FETs

Objective: low-power VLSI
0.1-0.2 V operation
>10:1 less switching energy

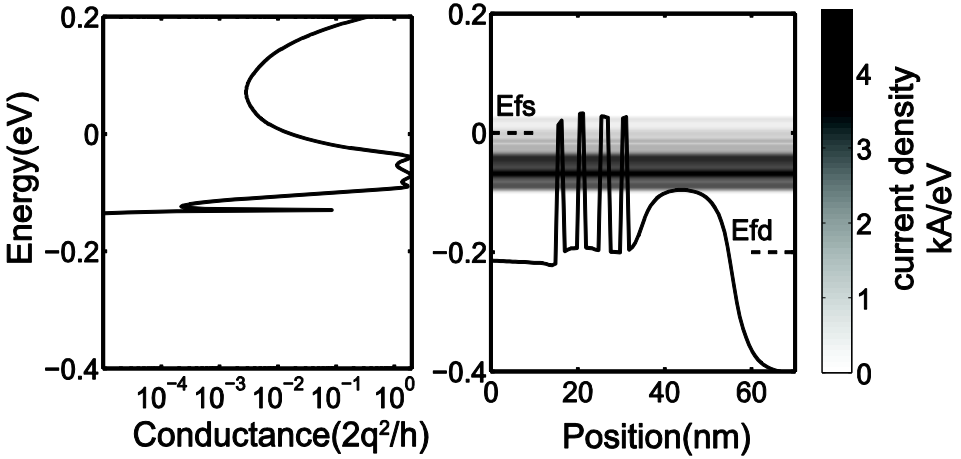
Approach: superlattice FET
energy filter in source
MOVCD regrowth

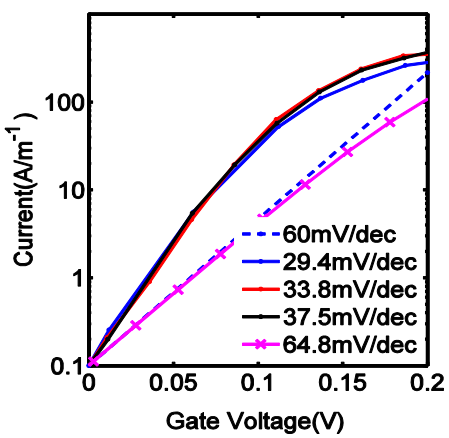
Impact: low-voltage,
high on-current (>> than T-FET)
→ fast, ultra-low-power VLSI logic

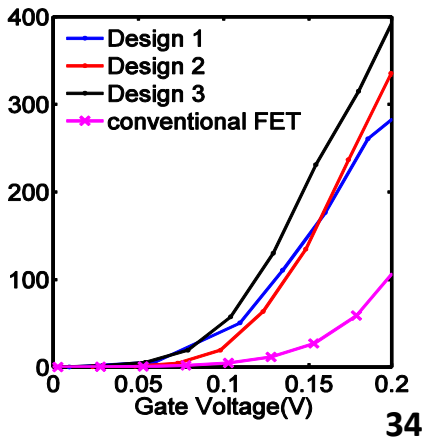
We can make it work.



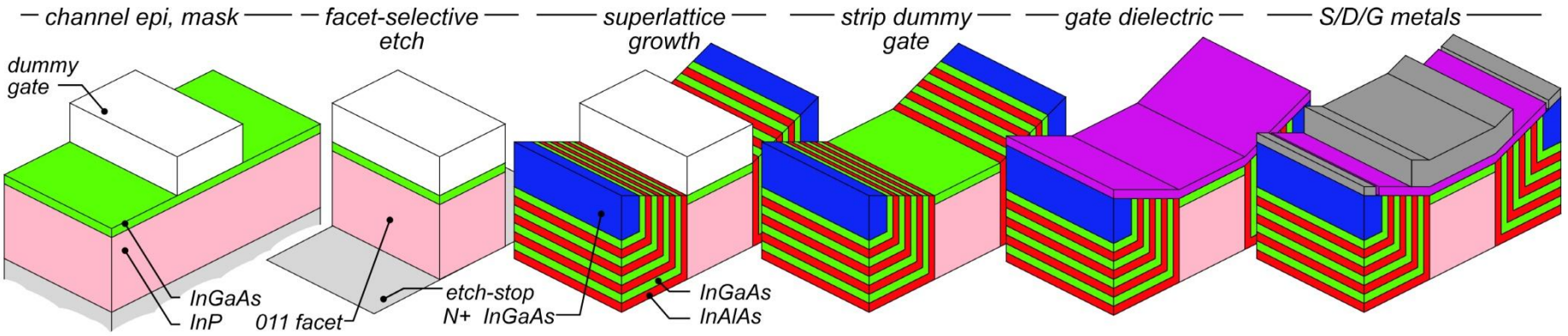
Long *et al.*, (Purdue/UCSB) IEEE EDL, December 2014







How we might build a superlattice FET



A simple extension of present planar III-V MOS process flow...

III-V MOS

For high-performance applications (I_{off}=100nA/μm)
- on-currents substantially better than Si at V_{DD}=0.5V

Lower-power applications (SP/LP/UPL)
- target off-currents as small as 10pA/μm
- InP spacers can provide such small leakage
- Problem: incrased access resistance, reduced I_{on}

Best solution:
- Thin (2-5nm) InP spacers in finFETs
- fin geometry fixes electrostatics
- InP spacers fix BTBT.

(end)