12 nm-Gate-Length Ultrathin-Body InGaAs/InAs MOSFETs with $8.3 \cdot 10^5$ I_{ON}/I_{OFF}

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Introduction: III-V InGaAs/InAs MOSFETs can provide high on-state current at lower V_{DD}, and are being considered as promising candidates to replace Si channels at future 7 or 5 nm technology nodes. At the 5 nm node, the International Technology Roadmap for Semiconductors (ITRS) targets 12 nm physical gate length [1]. At such small dimensions, few III-V MOSFETs have been reported, and the observed off-state leakage currents have been high [2-8]. High off-state leakage current arising from band-to-band tunneling (BTBT) near the drain end of channel makes it difficult to scale III-V MOSFETs to sub-10-nm generations. Previously we reported a FET using a 2.5 nm thick InAs channel to reduce I_{off} to 10 nA/μm for 25 nm L_g, simultaneously achieving record I_{on} (500 μA/μm at 100 nA/μm I_{off} and V_{DD}=0.5 V) [9]. To further reduce BTBT leakage current, we developed InGaAs-channel MOSFETs with 4.5 nm thick channels and graded-doping recessed InP source/drain spacer layers; these showed a minimum 60 pA/μm I_{off} at 30 nm L_g [10]. Here, we further reduce the physical gate length, and report 12 nm-L_g FETs with 1.5/1 nm InGaAs/InAs composite channels, and recessed doping-graded InP source/drain spacers. The FETs demonstrate high ~1.8 mS/μm transconductance (g_m), low ~107 mV/dec. subthreshold swing (SS), and low ~1.3 nA/μm minimum I_{off} at V_{DS}=0.5 V. For the first time, III-V InGaAs/InAs MOSFETs at 12 nm gate length were demonstrated with well-balanced on-off DC performance. The maximum I_{on}/I_{off} at V_{DS}=0.5 V is 8.3×10^5, confirming that III-V MOSFETs are scalable to sub-10-nm technology nodes.

Device Fabrication: Fig. 1 shows the device structure; [9,10] give the detailed process flow. The channel consists of a 1 nm InAs bottom channel and a 1.5 nm $In_{0.53}Ga_{0.47}As$ top channel. The devices have 12 to 1000 nm physical gate lengths (defined by the edges of regrown layers as shown in **Fig. 2a**). The InGaAs layer in the source/drain (S/D) region was partially removed by a digital etch, leaving ~0.5 nm InGaAs and 1 nm InAs to prevent the oxidation of the InAlAs barriers and ensure high crystalline quality MOCVD regrowth. The S/D layers grown by MOCVD have an un-doped InP spacer, a linearly doping-graded InP spacer, a Si-doped InP (~5×10^{19} cm^{-3}) layer and a Si-doped (4.0×10^{19} cm^{-3}) $In_{0.53}Ga_{0.47}As$ contact layer. The FETs have a ~3.4 nm ZrO_2 gate dielectric, including the AlON interfacial layer formed by the ALD cyclic TMA/nitrogen plasma pre-treatment. Ni/Au gate and Ti/Pd/Au S/D metal contacts were defined using liftoff. **Fig. 2b** shows the cross-sectional TEM images of a 12 nm-L_g device.

Results: Fig. 3 shows transfer characteristics of a 12 nm-L_g FET, achieving 1.8 mS/μm peak g_m at V_{DS}=0.5 V. The subthreshold swing, **Fig. 4**, is 98.6 mV/dec. at V_{DS}=0.1 V and 107.5 mV/dec. at V_{DS}=0.5 V. The minimum leakage current is as low as 1.3 nA/μm at V_{DS}=0.5 V, where I_{off} is limited by BTBT. This leakage current is sufficiently low to meet the requirement of high performance (HP, 100 nA/μm) logic applications, and close to the specification of standard performance (SP, 1 nA/μm) applications. **Fig. 5** shows the output characteristics of a 12 nm-L_g FET. The maximum I_D exceeds 1.25 mA/μm at V_{GS}=1.2 V and V_{DS}=0.7 V, and the on-resistance (R_{on}) at V_{GS}=1 V is 302 Ω·μm. The I_D at V_{GS}=1.2 V and V_{DS}=0.5 V is 1.1 mA/μm, showing maximum I_{on}/I_{off}~8.3×10^5. Examining (**Fig. 6**) g_m as a function of L_g, the present InGaAs/InAs channel devices show g_m slightly superior to our previously-reported devices using InP spacers and InGaAs channels [10] but lower g_m than devices using InGaAs spacers and InAs channels [9]. On-resistance, **Fig. 7**, ~262 Ω·μm when extrapolated to zero L_g, is also consistent with earlier results using similar InP spacers [10].

Fig. 8 shows SS vs. L_g and **Fig. 9** shows DIBL vs. L_g. As gate length decreases, SS and DIBL increase due to deteriorating electrostatics. Further thinning the channel would reduce such short-channel effects, but unfortunately we have found that InGaAs channels thinner than ~3.5 nm show poor g_m. InAs channels, in contrast, though showing high g_m even when 2.5 nm thick, show high BTBT leakage [9]. A tri-gate structure would improve electrostatics, allowing use of thicker channels and thinner source/drain spacers. Because only a thin InP high-field drain spacer layer would be required to suppress BTBT, on-state performance (g_m) would be improved [10].

Fig. 10 shows minimum I_{off} vs. L_g. The FETs reported here, having a 1.5/1 nm InGaAs/InAs composite channel and recessed InP spacers, show lower leakage current than FETs using 2.5 nm InAs channels and InGaAs S/D spacers [9], but larger leakage than FETs using 4.5 nm InGaAs channels and recessed InP spacers [10]. A clear tradeoff between I_{on} and I_{off} is observed in **Figs. 6, 10** and **11**. **Fig. 11** benchmarks I_{on} as a function of L_g at I_{off}=100 nA/μm and $V_{DS}=V_{GS}-V_{TH}$=0.5 V. The FETs reported here show I_{on}~311 μA/μm at L_g=42 nm, similar to [10].

Conclusion: We report III-V MOSFETs with 12 nm physical gate length, ultrathin 1.5/1 nm InGaAs/InAs composite channels, and recessed doping-graded InP S/D vertical spacers. The FETs demonstrate g_m~1.8 mS/μm transconductance, SS~107 mV/dec., minimum I_{off}~1.3 nA/μm at V_{DS}=0.5 V, and well-balanced on-off DC performance with maximum I_{on}/I_{off}~8.3×10^5. Band-to-band tunneling leakage current is well-controlled through the thin composite InGaAs/InAs channel, and by the recessed InP source/drain spacers. This work demonstrates that III-V MOSFETs can scale to the sub-10-nm technology nodes.

References:

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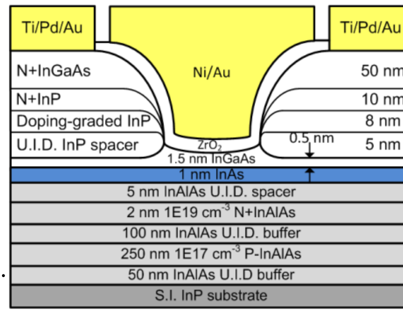

Fig. 1 (Top) Device structure of ultrathin body InGaAs/InAs MOSFETs.

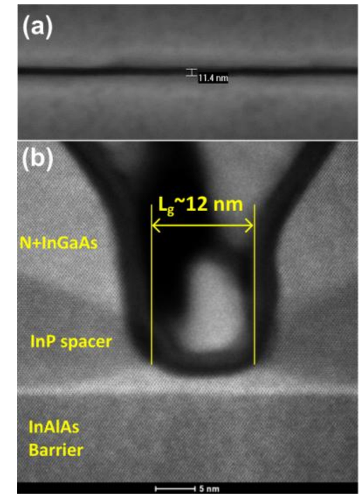

Fig. 2 (Right) (a) top-view SEM images before gate metal deposition, showing L_g~12 nm between the edges of regrown layers. (b) TEM image of the final device, showing a ~2.5 nm channel, recessed InP source/drain spacers, and ~12 nm L_g.

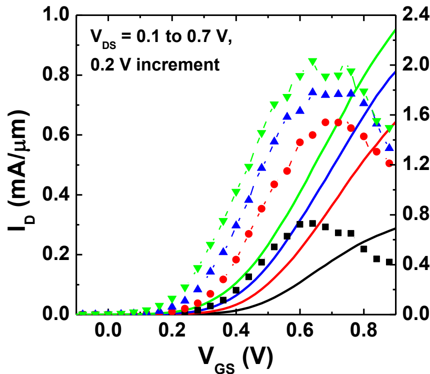

Fig. 3 I_D and transconductance g_m versus V_{GS} for a 12 nm-L_g FET.

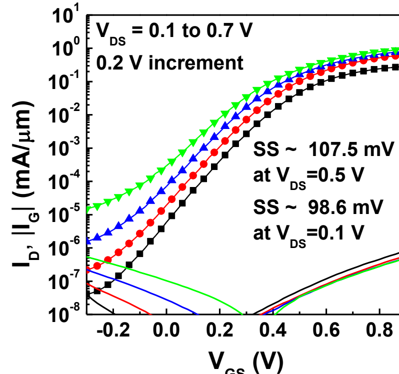

Fig. 4 Subthreshold characteristics for a 12 nm-L_g FET.

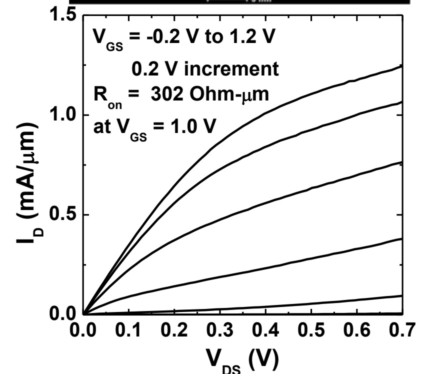

Fig. 5 Output characteristics for a 12 nm-L_g FET.

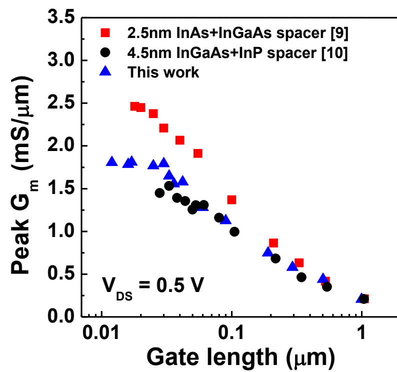

Fig. 6 g_m vs. L_g for this work, compared to [9,10].

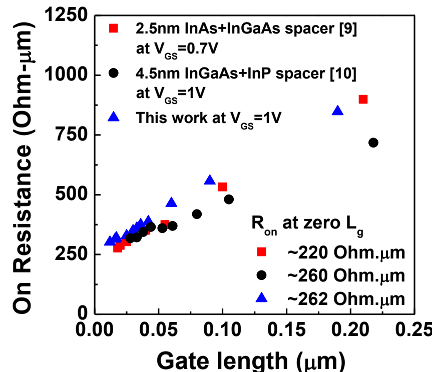

Fig. 7 R_{on} vs. L_g for this work, compared to [9,10].

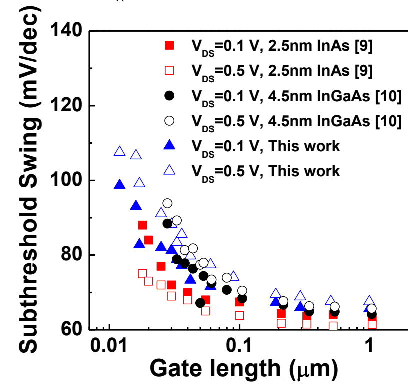

Fig. 8 *SS* vs. L_g for this work, compared to [9,10].

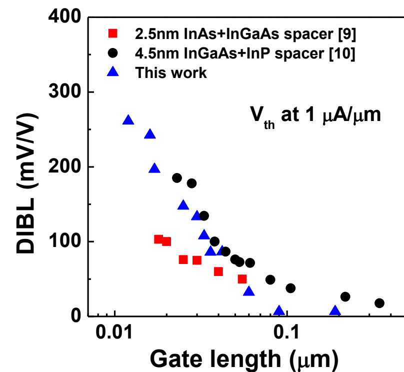

Fig. 9 DIBL vs. L_g for this work, compared to [9,10].

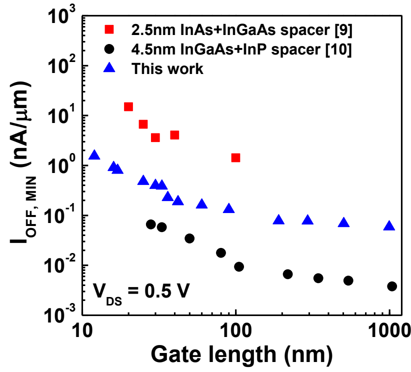

Fig. 10 Minimum I_{off} vs. L_g for this work, compared to [9,10].

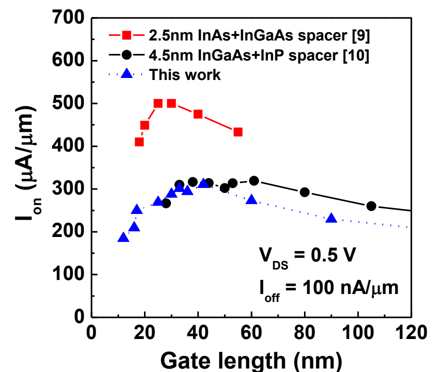

Fig. 11 I_{on} vs. L_g at I_{off}=100 nA/µm and V_{DS}=0.5V.