

# Comparison of Ultra-Thin InAs and InGaAs Quantum Wells and Ultra-Thin-Body Surface-Channel MOSFETs

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When transistor gate lengths ( $L_g$ ) are shrunk below 10 nm, channel thicknesses must be proportionally reduced to maintain electrostatic integrity [1]. At 7 nm  $L_g$ , InGaAs and InAs channels must be stringently evaluated at 2~4 nm channel thickness [2-4], yet transport in ultrathin III-V quantum wells and DC characteristics of ultra-thin-body MOSFETs have not been extensively reported. Here we compare electron Hall mobility of 2~6 nm  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  and strained InAs quantum wells, where both sides of the well are bounded by wide-gap semiconductor barriers. Thick InAs wells show higher mobility than thick InGaAs wells, but InAs wells lose their advantages in mobility as the thickness is reduced to 2 nm. We also compare DC characteristics of 3 nm InAs channel FETs to 3 nm  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  channel FETs. Unlike the quantum well results, the InAs FETs show much higher on-state current ( $I_{on}$ ) and transconductance ( $g_m$ ) than InGaAs FETs from 40 nm to 1  $\mu\text{m}$   $L_g$ . Yet, due to the larger bandgap, InGaAs FETs show ~10:1 lower leakage current than InAs FETs at short  $L_g$ .

Fig. 1 shows the quantum wells grown by solid source MBE, and the corresponding band diagram. Growth of strained InAs wells on InP substrates was optimized with a ~5.8:1 As/In beam flux ratio and a 375°C~400°C growth temperature. The top and bottom InAlAs barriers were grown at 490°C. Fig. 2 shows Hall mobility and electron concentration as a function of well thickness. It is clear that the mobility is higher in thick InAs wells than in thick InGaAs wells, but mobilities converge as the well is thinned to 2 nm. The electron concentration in the well also decreases with reduced well thickness due to increasing sub-band energy ( $E_0$ ) and hence reduced  $E_F - E_0$ .

As wells are thinned, the electron scattering time becomes dominated by interface roughness scattering, and the electron effective mass also increases because of the quantized sub-band energy and the non-parabolic conduction band. Given that InAs has larger conduction band non-parabolic coefficient, the electron effective mass of InAs increases more rapidly, and is reported to be similar to that of InGaAs at 2~3nm channel thickness [5]. This may explain the similar mobility observed for 2 nm InGaAs and InAs wells. The above data, taken alone, would suggest that increased indium content in 2-3nm thick MOSFET channels should have negligible effect on on-state current.

Fig. 3 shows the structure of surface channel MOSFETs with a 3 nm InAs or InGaAs channel. Refs. 2 and 3 give the process flow. Figs. 4 and 5 show the transfer and output characteristics of  $L_g$ -40 nm devices, respectively. Unlike the well results, InAs FETs show ~1.6:1 higher on-current and transconductance than InGaAs FETs. Fig. 6 shows  $I_{on}$  versus  $L_g$ , while Fig. 7 shows  $g_m$  versus  $L_g$ . At all gate lengths between 40 nm and 1  $\mu\text{m}$ ,  $I_{on}$  and  $g_m$  are higher for InAs FETs than for InGaAs FETs, indicating not only higher injection velocity but also higher electron mobility in the InAs channel than in the InGaAs channel. Fig. 8 compares the minimum  $I_{off}$  of the two devices. Due to its larger channel bandgap, at short  $L_g$  InGaAs FETs show one order of magnitude lower leakage current floor than InAs FETs, where  $I_{off}$  is dominated by band-to-band tunneling (BTBT) leakage. For long  $L_g$  devices, InAs FETs are still limited by BTBT, while InGaAs FETs limited by gate leakage. Fig. 9 and fig. 10 show subthreshold swing ( $SS$ ) and drain-induced barrier lowering ( $DIBL$ ) as a function of  $L_g$ , respectively. Thanks to thin channel and improved electrostatic integrity, both devices have excellent  $SS$ ~ 83 mV/dec at  $V_{DS}$ = 0.5 V and low  $DIBL$ ~110 mV/V for 40 nm- $L_g$  devices. FETs with yet thinner (2.7 nm) channels and  $\text{ZrO}_2$  gate dielectric layers [2] show further improvement in  $SS$  and  $I_{on}$ .

High indium content in thin surface-channel MOSFETs improves on-current despite having little effect on mobility in similarly thick wells bounded by semiconductor barriers. There are several possible explanations. In FET channels, there may be severe scattering from interface traps having energy levels within the conduction band, the traps arising from As-As antibonding or Ga dangling bonds [6]. The low  $g_m$  of InGaAs channels may be due to Fermi level pinning, at positive gate bias, from interface traps at energies within the conduction band, again from As-As antibonding states [7]; InAs has a larger energy separation between the conduction band and these states. Though population of the L valleys [8-11] can degrade mobility in [100] InGaAs MOSFETs, our tight-binding calculations show 0.65 eV  $\Gamma$ -L bound state energy separation in a 3 nm InGaAs well (vs. 0.90 eV in 3 nm InAs), hence at the  $V_{gs} - V_{th}$  corresponding to peak  $g_m$ , the L valley is unlikely to be populated with either material. Further investigation of electron transport in ultrathin channel III-V FETs would guide the device design for sub-10-nm III-V MOSFETs.

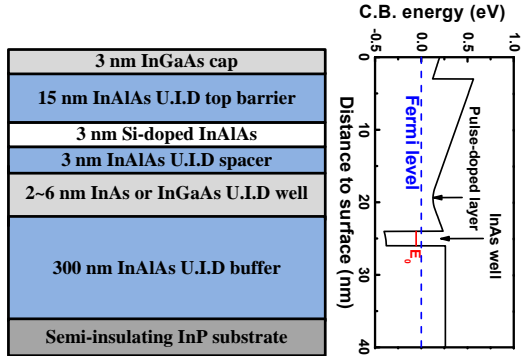


Fig. 1. Double heterostructure for the study of electron transport in quantum well and associated band diagram.

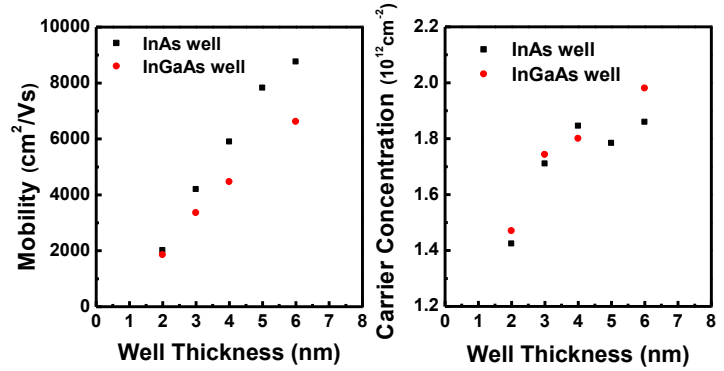


Fig. 2. Electron mobility and concentration as a function of quantum well thickness.

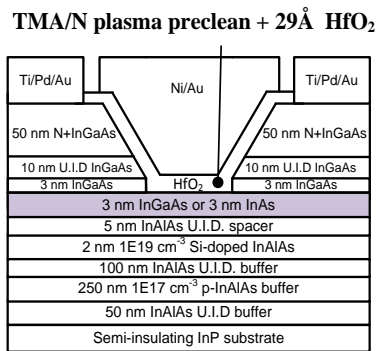


Fig. 3. Device structure of InAs or InGaAs surface channel MOSFETs.

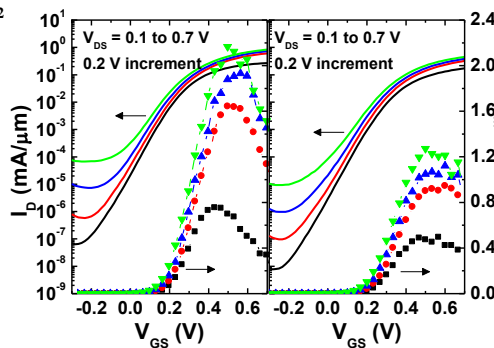


Fig. 4. Transfer characteristic of  $L_g=40$  nm InGaAs and InAs

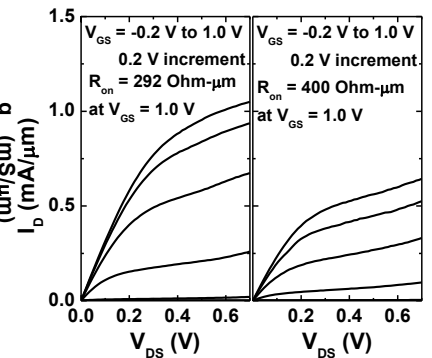


Fig. 5. Output characteristic of  $L_g=40$  nm InGaAs and InAs

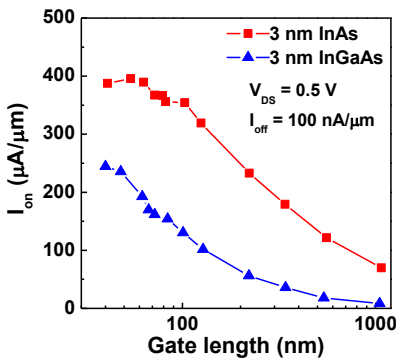


Fig. 6.  $I_{on}$  vs.  $L_g$  for two devices.

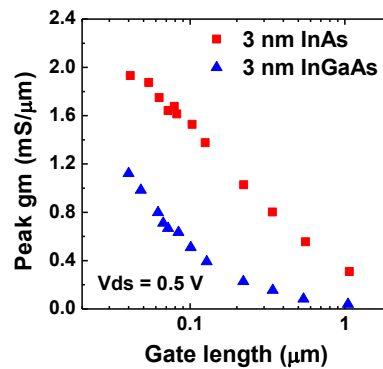


Fig. 7.  $g_m$  vs.  $L_g$  for two devices.

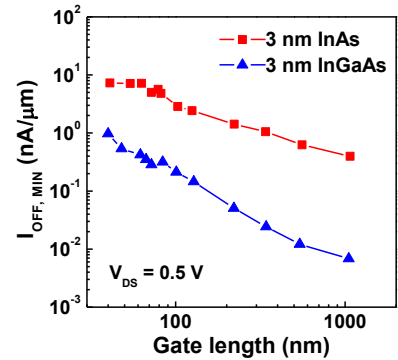


Fig. 8. Minimum  $I_{off}$  vs.  $L_g$  for two devices.

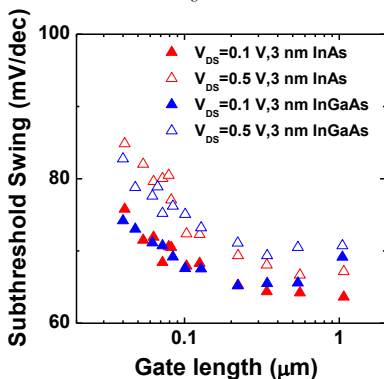


Fig. 9.  $SS$  vs.  $L_g$  for two devices.

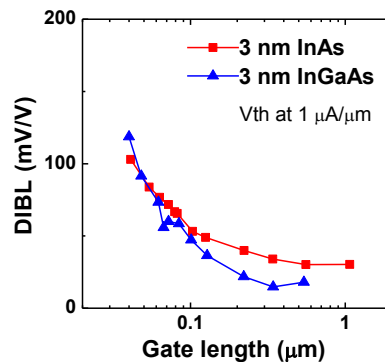


Fig. 10.  $DIBL$  vs.  $L_g$  for two devices.

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