A High-Dynamic-Range W-band Frequency-Conversion IC for Microwave Dual-Conversion Receivers

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***Abstract*—We present a high dynamic range W-band frequency conversion IC, incorporating a base-collector diode mixer and a 9:1 LO frequency multiplier, implemented in a 130 nm InP HBT technology. The IC was designed for a broadly tunable 1-22 GHz dual-conversion receiver using a 100 GHz first IF. In up-conversion, from 1-22 GHz to W-band, the IC has 7 dB conversion loss and 23 dB IIP3; in down-conversion, from W-band to 0.1-22 GHz, it has 8 dB conversion loss and 23 dBm IIP3. The IC tunes most of W-band (75–105 GHz) and consumes 2 W.**

***Index Terms*—Frequency conversion, Mixers, Dynamic range, InP HBT, Millimeter wave integrated circuits, MMICs**

I. INTRODUCTION

Millimeter-wave frequency conversion ICs – a mixer plus LO source– translate signal frequencies in mm-wave transmitters and receivers. A second potential application is in broadly-tunable *microwave dual-conversion receivers*, wherein spurious LO image and harmonic responses are avoided by first up-converting the frequency of the received signal, filtering, and then down-converting. Dual conversion is common in wide-tuning-range RF receivers; with THz InP IC technologies, the first IF can be placed at 100 GHz, and the spurious-free tuning range might approach 1-50 GHz.

In such frequency-conversion ICs, mixer dynamic range (noise, IP3) and bandwidth limit the receiver performance. Diode mixers exhibit better noise and IP3 than transistor mixers, but it is difficult to implement diode mixers in silicon because of the lack of high performance baluns and diodes [1]. Diode mixers require high LO power; if the LO tuning range must also be broad, design of the LO driver becomes challenging.

We present a high-dynamic-range W-band frequency up/down conversion IC (Fig. 1). We will describe the process technology, the IC's design, and the IC performance.

II. INP HBT TECHNOLOGY

The ICs were designed into a 130 nm InP HBT process. The process provides 50 Ω/square thin film resistors, 0.3 fF/μm^2 MIM capacitors, and three-levels of gold interconnections (M1-M3). A 0.13 × 2 μm^2 HBT exhibits a current gain cutoff frequency f_τ = 520 GHz and a maximum frequency oscillation f_{max} = 1.1 THz at I_C = 6.9 mA and V_{CE} = 1.6 V [2]. Low-loss normal and inverted microstrip lines are designed using M2 and M3 with a 5 μm thick BCB layer.

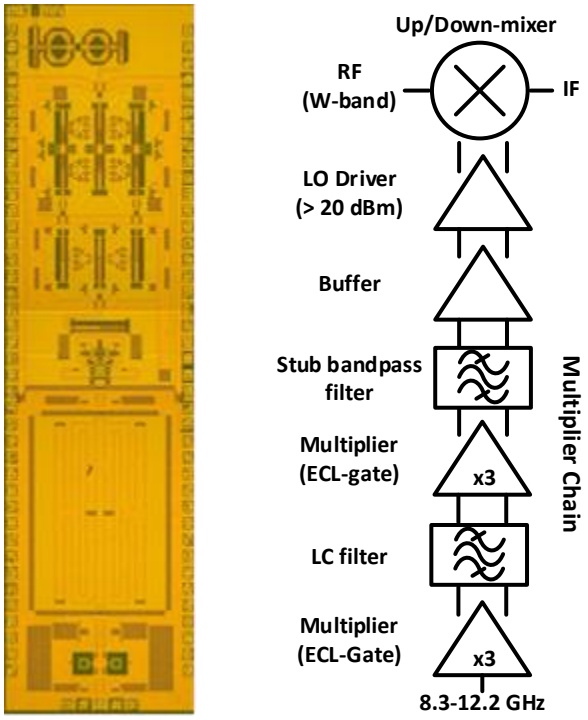


Fig. 1. Chip photograph (left) and block diagram of the mixer and LO chain (right) (chip size: 4300 × 1160 μm^2).

III. MIXER DESIGN

The core mixer (Fig. 2) consists of two baluns and four series-connected diode pairs. The diodes are HBT base-collector junctions; these have small minority carrier charge storage. Two additional baluns interface the mixer to single-ended LO and RF signals.

A. Base-collector diode

Diodes made from transistor junctions are very poor in

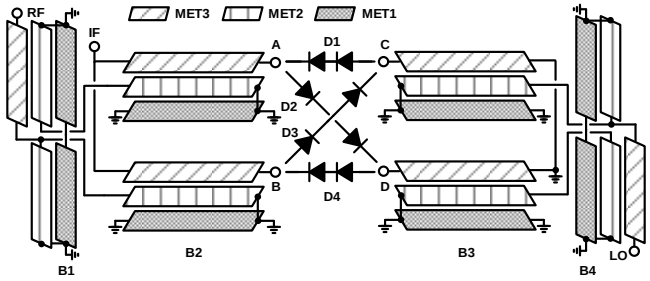


Fig. 2. Schematic of the mixer. B1-4 indicates baluns 1-4.

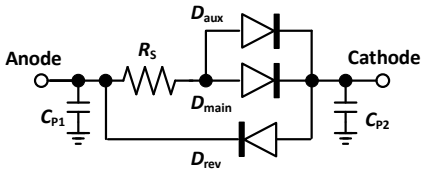


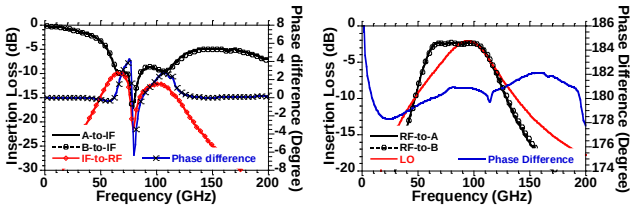
Fig. 3. Equivalent circuit model of the base-collector diode.

both GaAs and SiGe HBT technologies. The base-emitter diode has a thin depletion region and a resistive base contact, hence has a large RC time constant. The base-collector junction suffers from saturation (severe minority charge storage) and thus has a long reverse-recovery time.

In contrast, the base-collector junction in InP double-heterojunction bipolar transistors (DHBTs) is a heterojunction. This presents a large energy barrier to holes, preventing significant hole injection under forward junction bias from the base into the subcollector. Hole minority carrier storage is thereby eliminated. Although electron minority carrier storage in the base remains present in forward-biased DHBT base-collector junctions, the minority carrier storage time is small. The base-collector diode thus has characteristics similar to a Schottky diode. These diodes enable the design of high-performance mm-wave mixers. Diode models (Fig. 3) were developed from the Teledyne HBT foundry model and from measured *I-V* and *C-V* characteristics. The model consists of a series resistor (R_S), shunt capacitors ($C_{P1,2}$) and three diodes ($D_{main,\ aux,\ rev}$). To accurately predict mixer distortion, two parallel diodes in the model fit to the measured *C-V* characteristics in the turn-on region. D_{rev} models reverse leakage. A 1.44 μm^2 base-collector diode in the 130 nm InP DHBT technology has R_{on} = 22 Ω and $C_{depletion}$ = 5.5 fF.

B. Balun design

The baluns are key mixer components. There are four baluns in the mixer; each consists of two tri-plate [3] transmission-line sections (Fig. 2). Two baluns (B1,4) convert the single-ended LO and RF signals to differential format. Balun 2 couples the common-mode voltage at nodes A and B to the IF port and the differential voltage at nodes A and B to the RF port. Balun 4 similarly couples the



(i) (ii)

Fig. 4.: Simulated characteristics of the RF and LO baluns. Coupling of ports A and B (i) to the IF port are balanced and are low-loss within the targeted 1-25 GHz IF bandwidth. The IF-RF isolation (i) is better than 22 dB below 25 GHz. Coupling of ports A and B (ii) to the RF port are balanced and are low-loss within the targeted 75-100 GHz RF bandwidth.

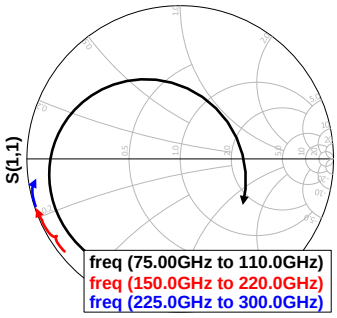


Fig. 5. Even-mode input impedance looking into the LO balun B3 from nodes C and D. Note the low impedance at the LO harmonics.

differential voltage at nodes C and D to the LO port and the common-mode voltage at these nodes to ground. Isolation between ports is shown in Fig. 4 Insertion loss is less than 3.5 dB across W-band with low phase and amplitude imbalance. These baluns provide low port impedances at the LO harmonics, which improves linearity by reducing harmonic signal mixing. Fig. 5 shows the balun even-mode input impedance, simulated over the tuning frequency range of the LO and of its second and third harmonics.

IV. LO Generation

The LO source (Fig. 6) consists of a 9:1 frequency multiplier chain and a LO driver amplifier. For high dynamic range (IP3), the mixer requires a high-power, > 20 dBm, LO drive signal. To cover W-band (75-110 GHz), the LO, hence the multiplier and driver, must tune over a 1.33:1 fractional bandwidth. Design of the high-power driver is discussed in [4]. The 9:1 frequency multiplier uses two cascaded triplers, each based upon cascade emitter-coupled logic (ECL) gate. These ECL gates convert a sinusoidal input into a square-wave output with a strong third harmonic. The desired third harmonic is the selected by band-pass filters. The first tripler output, at 20-34 GHz, is filtered by a small lumped-component Chebyshev filter. In simulations, spiral inductors functioned less well in the 60-100 GHz filter at the

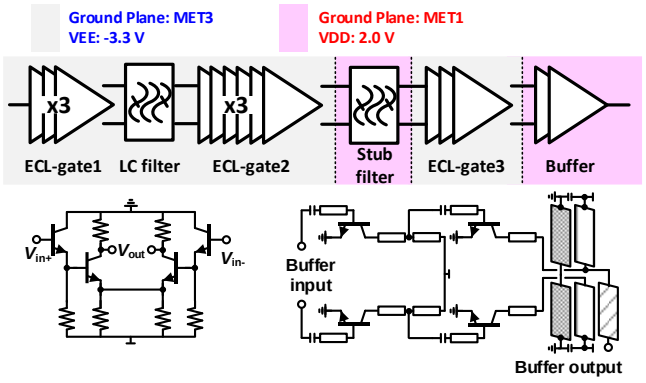


Fig. 6. LO multiplier chain: (a) block diagram (top), (b) schematic of the ECL gate (bottom left), and (c) schematic of the buffer (bottom right).

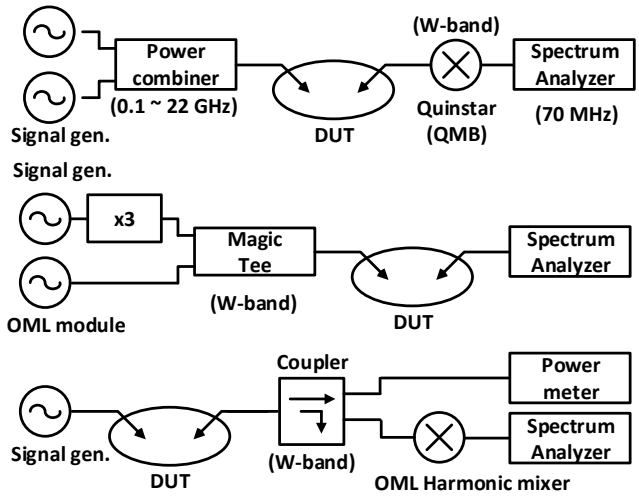


Fig. 7. Testing setup for measurement of up-conversion IIP3 (top), down-conversion IIP3 (middle), and of the spectrum and attenuation during up-conversion (bottom). The 3rd setup was also used to measure the spectrum of the LO multiplier chain

output of the second tripler; this filter instead uses series and shunt-stub transmission-lines. At the output of the second tripler, three cascaded ECL gates, followed by a two-stage reactively-tuned pseudo-differential common-emitter amplifier increase the LO drive amplitude to 9 dBm. This signal then drives the 20-22 dBm main LO driver [4].

V. Measurement Results

The ICs were characterized on-wafer. Tested ICs included the full designs of Fig. 1, plus test structures containing the mixer and main LO driver, but omitting the 9:1 multiplier. The latter IC was driven by an external 9 dBm LO. Separate multiplier chains were also fabricated and tested. Fig. 7 shows test configurations. The up-conversion gain was measured using an Agilent W-band power sensor (W8486A) directly, and Rohde & Schwarz's FSU spectrum analyzer

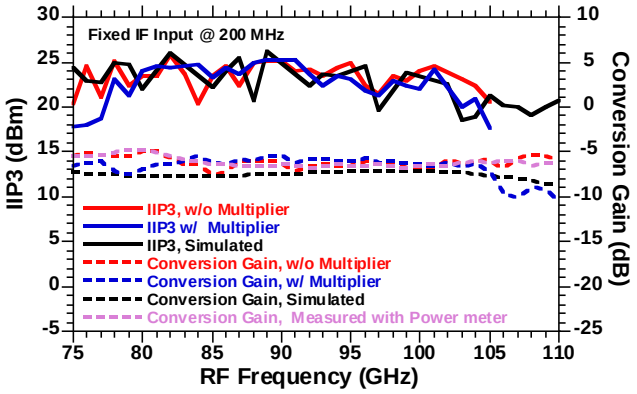


Fig. 8. Up-conversion gain and IIP3 at a fixed IF input frequency. Data is shown for ICs with and without 9:1 frequency multipliers.

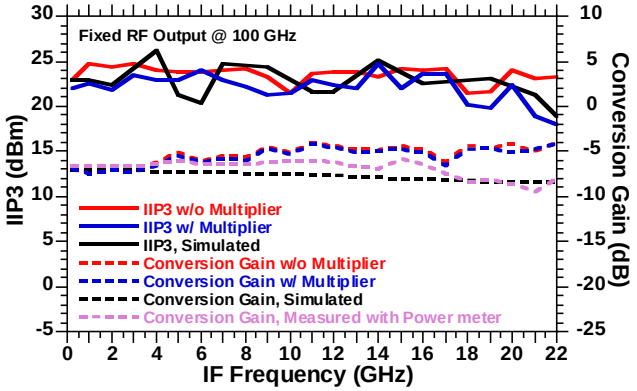


Fig. 9. Up-conversion gain and IIP3 at a fixed RF output frequency. Data is shown for ICs with and without 9:1 frequency multipliers.

after down-converting the W-band output signal with a balanced mixer from Quinstar. Fig. 8 and Fig. 9 show conversion gains and IIP3 for up-conversion. The up-conversion mixer has 7 dB conversion loss and an IIP3 of 23 dBm. The gains measured with the power sensor and with the spectrum analyzer were nearly equal. RF-to-LO isolation at W-band is about 30 dB. The down-conversion mixer has 8 dB conversion loss and an IIP3 of 23 dBm as (Fig. 10, Fig. 11). Fig. 12 shows measured output power of the LO multiplier chain without the LO drive amplifier. The multiplier chain provides 9 dBm output power over the tuning bandwidth. As this is sufficient to drive the LO drive amplifier into strong gain compression, the measured results of the conversion ICs with and without the multiplier chain show similar performance.

VI. Conclusion

We present a high-dynamic-range W-band frequency conversion IC. The IC contains a mixer and an integrated 9:1 frequency multiplier and LO power driver. The circuits were fabricated in a 130 nm InP HBT process. The passive diode

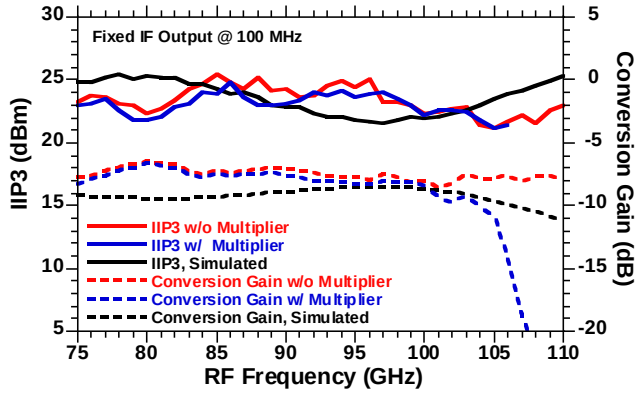


Fig. 10. Down-conversion gain and IIP3 at a fixed IF output frequency. Data is shown for ICs with and without 9:1 frequency multipliers.

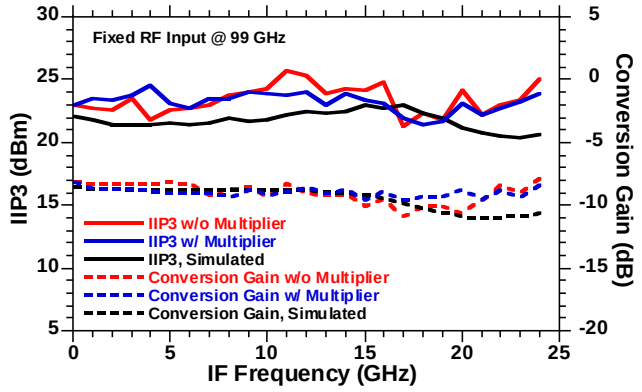


Fig. 11. Down-conversion gain and IIP3 at a fixed RF input frequency. Data is shown for ICs with and without 9:1 frequency multipliers.

mixer uses baluns and DHBT base-collector junction diodes. The conversion IC has 7 dB conversion loss and an IIP3 of 23 dBm in up-conversion. It has 8 dB conversion loss and an IIP3 of 23 dBm in down-conversion. The LO generation circuits including the LO drive amplifier provides enough power level over almost the entire W-band with 2 W power consumption.

We do not yet have noise figure measurements for the frequency converter. However, the noise figure of a passive diode mixer is usually very close to its insertion loss. We therefore expect 7-8 dB noise figure in either frequency up- or down- conversion.

Despite the high 100 GHz frequency of operation and the complexity of the IC (~150 transistors, ~330 passive elements), measured performance is close to simulation. Given that the 9:1 frequency multiplier contains two passive filters and 16 cascaded active stages, the correlation between design and measurement is particularly notable. This suggests that models of the 130 nm/1.1 THz Teledyne InP HBT technology are accurate. Further, the results

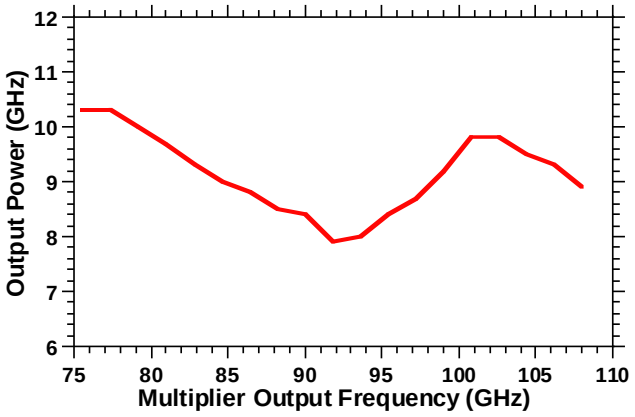


Fig. 12. Measured multiplier chain output power.

demonstrate that complex ICs can be fabricated in the technology.

The frequency conversion ICs were designed as part of a dual-conversion superheterodyne receiver with a 100 GHz first IF and a 1–25 GHz RF tuning range. Measured results for the full receiver will be reported in subsequent work.

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