A 130 nm InP HBT Integrated Circuit Technology for THz Electronics

M. Urteaga[1], J. Hacker[1], Z. Griffith[1], A. Young[1], R. Pierson[1], P. Rowell[1], M. Seo[2], and M.J.W. Rodwell[1]
[1]Teledyne Scientific Company, Thousand Oaks, CA, USA, email: Miguel.Urteaga@Teledyne.com
[2]SungKyunKwan University, Seoul, South Korea, [3]Dept. of ECE, University of California, Santa Barbara, USA

***Abstract*—**A 130 nm InP HBT IC technology has been developed capable of circuit demonstrations at > 600 GHz. Transistors demonstrate RF figures-of-merit f_t > 500 GHz and f_{max} > 1 THz. The HBTs support high current densities > 25 mA/μm^2 with a common-emitter breakdown voltage BV_{CEO} = 3.5V. The technology includes a multi-level thin-film wiring environment capable of low-loss THz signal routing and high integration density. A large-signal HBT model has been developed capable of accurately predicting circuit performance at THz frequencies. Circuit demonstrations include fundamental oscillators and amplifiers operating at > 600 GHz as well as integrated transmitter and receiver circuits.

I. Introduction

Progressive increases in transistor bandwidths are extending integrated circuit operation further and further into the THz frequency spectrum (0.3 to 3 THz). The highest fundamental frequency circuit operation from 3-terminal devices has been demonstrated in the Indium Phosphide (InP) material system, including the first demonstration of amplifier gain at >1 THz from a 25 nm InP high electron mobility transistor (HEMT) technology [1]. InP transistors benefit from high electron mobilities and saturation velocities, large heterojunction offsets for carrier confinement and high achievable doping levels for low Ohmic contact resistivities. Both highly-scaled HEMT and double heterojunction bipolar transistor (DHBT) technologies have been demonstrated with maximum frequencies of oscillation exceeding 1 THz [2], [3], [4]. Compared to InGaAs-channel HEMT technologies, InP DHBTs offer higher breakdown voltage at comparable bandwidths due to the wider bandgap InP collector.

In this work we described the development and performance of a 130 nm InP HBT integrated circuit technology targeting THz monolithic circuit demonstrations. Details of the transistor fabrication, performance and modeling are provided. A backend-of-line (BEOL) process suitable for thin-film transmission line wiring to THz frequencies has been developed. In this technology, complex integrated circuits have been demonstrated including: amplifiers and fundamental oscillators operating at > 600 GHz [5], [6] and full integrated transmitter [7] and receiver circuits.

II. 130 nm InP HBT IC Technology

HBT epitaxy is grown on 100 mm semi-insulating InP substrates using molecular beam epitaxy. The emitter cap is graded from $In_{0.53}Ga_{0.47}As$ to InAs and doped heavily (> 3x10^{19} cm^{-3}) to minimize Ohmic contact resistance. The N$^-$ InP emitter is also relatively highly doped (2x10^{18} cm^{-3}) to minimize potential drops in the depletion region while supporting high current densities. The base is carbon-doped InGaAs (25 nm) and includes compositional and doping grading to reduce base transit time. A doping level of > 1x10^{20} cm^{-3} is used closest to the base-emitter junction to reduce base Ohmic contact resistance. Typical base sheet resistance is ~800 Ω/□. Chirped-superlattice grading (InGaAs/InAlAs) is used at both the emitter-base (EB) and base-collector (BC) heterojunctions to smooth conduction band discontinuities. EB grading decreases the HBT turn-on voltage and improves the forward ideality factor compared to an abrupt junction [8]. The BC grade (33nm) consists of an InGaAs set-back followed by the superlattice grade and an InP pulse doping layer. The N$^-$ InP layer is 67 nm and doped at 5x10^{16} cm^{-3}, for a total collector thickness of 100 nm.

General scaling laws for InP HBTs have been outlined in [9]. A key challenge in the fabrication of THz InP HBTs is establishing low resistance Ohmic contacts that are thermally and electrically stable to thin semiconductor layers and implementing these contacts in a high-yield and scalable process flow. We utilize an electroplated emitter contact process with dielectric sidewall spacers to realize a self-aligned base-emitter junction. Details of this process for 250 nm HBTs are reported in [10]. A schematic of the HBT process flow is shown in Fig. 1. HBT device mesas are formed using wet-chemical etching. After the HBT contact formation and isolation, Benzocyclobutene (BCB) is used as a final HBT passivation and planarization layer. The BCB is etched back to expose the tall emitter contact eliminating the need for a precisely aligned via to this contact. Vias are formed to the base and collector contacts and an electroplated Au process is used to form the first interconnect level. A TEM cross-section of a fabricated 130 nm HBT is shown in Fig. 2.

DC characteristics of a 130 nm HBT are shown in Fig. 3 and Fig. 4. Typical peak current gain β ranges from 15-20. The common-emitter breakdown voltage BV_{CEO} = 3.5V (J_C=10μA/μm^2). The highly scaled emitter junction permits operation at high current (J_E >30mA/μm^2) and power (>50mW/μm^2) densities. On-wafer S-parameter measurements are performed using thin-film microstrip calibration structures with a multi-line Through-Reflect-Line (TRL) calibration, details of which can be found [11]. The HBT figures-of-merit f_t and f_{max} are extrapolated from least squares fits to single-pole

978-1-5090-3902-9/16/$31.00 ©2016 IEEE

transfer functions of the measured h_{21} and unilateral power gain (U), respectively. Fig. 5 shows the variation of f_t and f_{max} versus I_C at varying values of V_{CE} for a 0.13x2 μm^2 HBT [3]. At the peak f_{max} bias of I_C =6.9 mA V_{CE}=1.6 V, the HBT exhibits an extrapolated f_t/f_{max} of 521GHz/1.15THz.

HBT performance is strongly influenced by non-equilibrium electron transport in the collector where electrons entering the collector experience velocity overshoot prior to gaining sufficient energy to undergo Γ-L scattering [12]. The electron velocity profile, and hence collector transit time, is modulated by both the base-collector voltage and the collector current. Fig. 6 plots the variation of the forward delay time ($\tau_{ec}=1/2\pi f_t$) versus $1/I_C$ for a 0.13x4 μm^2 HBT. The delay time can be expressed as a function of the HBT's small-signal parameters as

$$\tau_{ec} = \frac{1}{2\pi f_t} = \tau_b + \tau_c + \frac{n_c kT}{qI_C}\left(C_{je} + C_{cb}\right) + (R_{ex} + R_c)C_{cb} \quad (1)$$

From (1) we would expect a linear dependence of τ_{ec} versus $1/I_C$ if the transit times (τ_c and τ_b) , junction capacitances (C_{je} and C_{cb}) and extrinsic resistances (R_{ex} and R_c) are not bias dependent. We observe this trend at low current densities in Fig. 6 but see a deviation from linear behavior at high currents due to collector velocity modulation. Using extracted values for the resistances and capacitances, the variation from the low current linear behavior can be used to determine τ_c + τ_b as function of bias (Fig. 7). We observe a minimum transit time delay of ~0.22 psec than can increase to > 0.5 psec at high collector- base voltages and low currents. The collector velocity modulation gives rise to collector-base capacitance cancellation [13] (Fig. 8) which enhances the HBT f_{max} at increasing values of I_C and $V_{CE.}$ At peak f_t bias, the forward delay is dominated by electron transit through the device. The relative contributions of the various delay terms are show in Fig. 9.

Large signal III-V HBT models have been developed that capture these velocity modulation effects and other phenomenon associated with the base-emittter and base-collector heterojunctions [14]. The accuracy of the model scales well with frequency and we see good agreement between measured and simulated IC performance to THz frequencies. In addition to model fidelity, accurate THz IC design requires a well-controlled transmission line wiring environment. Fig. 10 shows a schematic cross-section of our thin-film wiring environment utilizing a BCB (ε_r=2.7) interlayer dielectric with electroplated Au interconnects. Details of the HBT BEOL process can be found in [10]

III. THz Circuit Results

The 130 nm HBT technology has been used for numerous IC demonstrations at > 600 GHz. Fig. 11 shows a chip photograph and measured S-parameters for the highest frequency HBT amplifier that has been reported [5]. The 9-stage common-base amplifier demonstrates 22 dB gain at 670 GHz and ~ 20 dB gain from 600-680 GHz. On-wafer power measurements demonstrated a saturated output power of -4 dBm (0.4mW) at 585 GHz and -7.5 dBm (0.18 mW) at 670 GHz. Higher levels of power combining have been achieved using a dual-branch differential amplifier topology with 4-way output power combining [6]. Fig. 12 shows a chip photograph and measured S-parameters of this amplifier which demonstrates a peak gain of > 30dB and >20 dB gain at 620 GHz. The amplifier uses a differential topology with a unit cell consisting of 3 cascaded common-base stages that share a common-bias current. The amplifier demonstrated a saturated output power of 2.8 dBm (1.9 mW) at 585 GHz.

Custom THz waveguide circuit blocks are bulky and expensive making single-chip transceivers solutions desirable. Fig. 13 shows a chip photograph and measured output spectrum of an integrated 590 GHz transmitter. The circuit includes an integrated 195 GHz phase-locked loop for the LO source, an LO buffer amplifier, a 3rd-order sub-harmonic up-converting mixer and a differential common-base output amplifier like Fig. 12. The architecture is similar to that reported in [7] but with the addition of the output amplifier. The circuit has 167- 130 nm HBTs with a P_{DC} = 1.08 W. The measured transmitter phase noise is -75 dBc at a 100 kHz offset and the measured on-wafer output power correcting for probe loss is -2.0 dBm.

IV. Conclusion

A 130 nm HBT integrated circuit technology has been developed capable of demonstrating fully integrated transceivers at 600 GHz. The availability of single-chip sources and receivers will open new opportunities for applications in the THz spectrum. Additionally, the technology can be exploited for applications at lower frequencies including: high efficiency mm-wave power amplifiers, ultra-low power mm-wave beamformer circuits and mm-wave data converters.

Acknowledgment

This work was supported by DARPA CMO Contract No. HR0011-09-C-0060. The views, opinions and/or findings contained in this article are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Defense Advanced Research Projects Agency, or the Department of Defense. Program support from Dr. Dev Palmer (DARPA) and Dr. Alfred Hung (ARL) is gratefully acknowledged.

References

[1] X. Mei, et. al., *IEEE Electron Device Lett.* vol. 36, no. 4, pp. 327-229, April 2015. [2] R.Lai et. al. *2007 IEEE Electron Device Meeting*, Dec., Washington, DC. [3] M. Urteaga et. al. *2011 Device Research Conference*, June, Santa Barbara, CA. [4] V. Jain et. al. *2011 Device Research Conference*, June, Santa Barbara, CA. [5] J. Hacker, et. al, *2013 IEEE International Microwave Symposium,* June, Seattle, WA. [6] M. Seo, et. al, *2103 IEEE International Microwave Symposium,* June Seattle, WA. [7] M. Seo, et. al, *2012. International Microwave Symposium Digest*, June, Montreal, Canada..[8] W. Liu, *Handbook of III-V Heterojunction Bipolar Transistors.* New York, NY: John Wiley and Sons, 1998. [9] M. Rodwell, et. al, *Proc. of IEEE*, vol. 96, no.12, Feb 2008. [10] M. Urteaga, et. al. 2011 *Indium Phosphide and Related Materials (IPRM) Conference,*June, Berlin, Germany. [11] D.F. Williams, et. al. *IEEE Trans. on Terahertz Science and Technology*, vol. 4, no. 3, pp. 433-439. [12] T. Ishibashi, *IEEE Trans. Electron Devices*, vo. 37, no. 12, Dec. 1990. [13] Y. Bester, et. al, *IEEE*

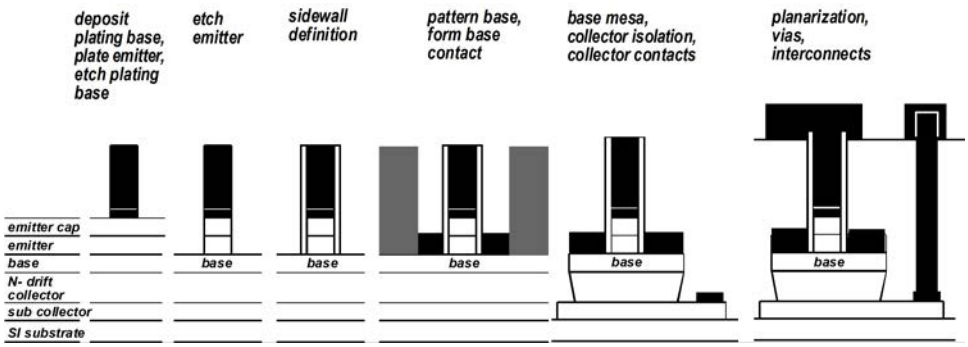

Fig. 1 Schematic illustration of 130 nm HBT front-end-of-line process flow

Fig. 2 TEM Cross-section of 130 nm InP HBT. Collector Ohmic contacts are not shown in image.

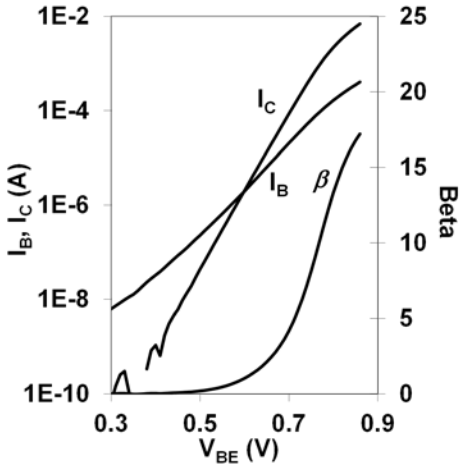

Fig. 3 Gummel characteristics of 0.13x2 μm^2 HBT.

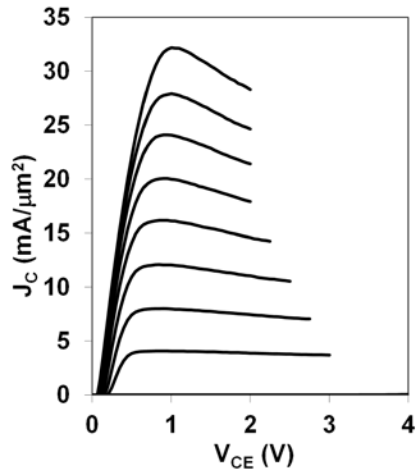

Fig. 4 Common-emitter IV characteristics of 0.13 μm HBT normalized to emitter area.

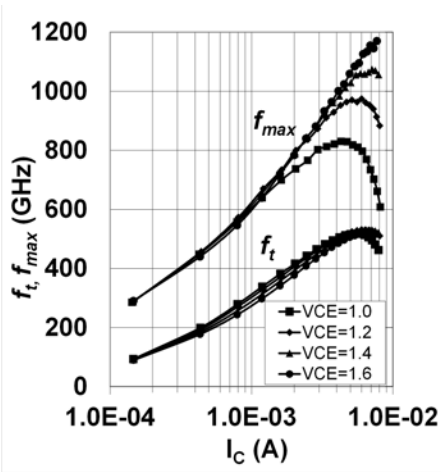

Fig. 5 Extrapolated f_t and f_{max} versus collector current for 0.13x2 μm^2 HBT at varying V_{CE}

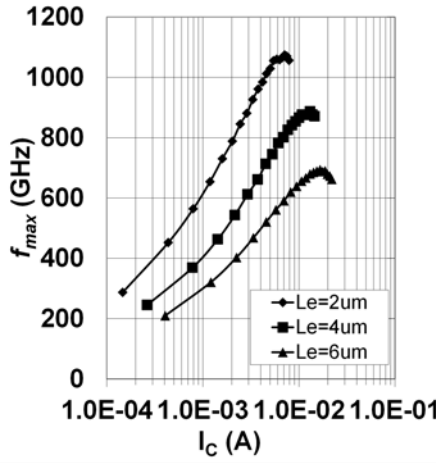

Fig. 6 Extrapolated f_{max} versus collector current for varying emitter length L_E (V_{CE} = 1.4 V)

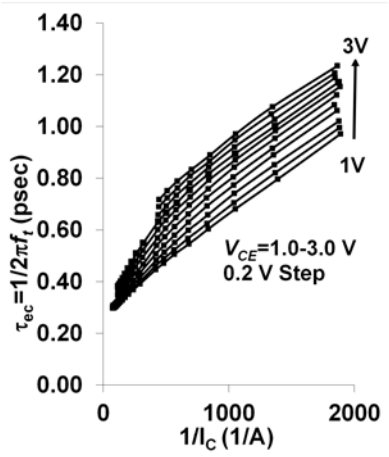

Fig. 7 Variation of forward delay time ($\tau_{ec}=1/2\pi f_t$) versus 1/I_C for varying V_{CE} for 0.13x4 μm^2 HBT

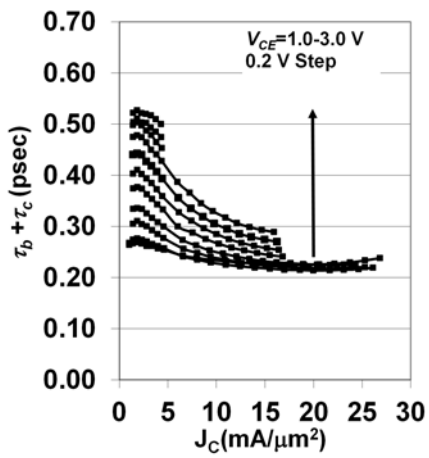

Fig. 8 Extracted bias dependence of HBT transit delay ($\tau_c+\tau_t$) versus J_C for varying V_{CE} for 0.13x4 μm^2 HBT

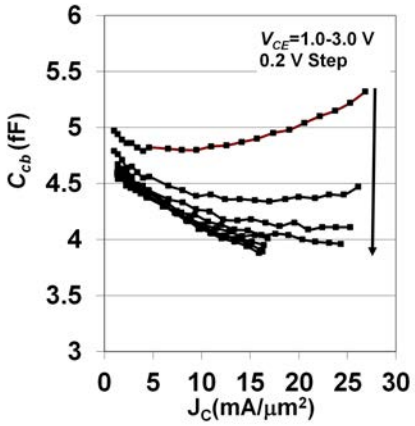

Fig. 9 Extracted bias dependence of HBT collector-base capacitance (C_{cb}) versus J_C for varying V_{CE} for 0.13x4 μm² HBT

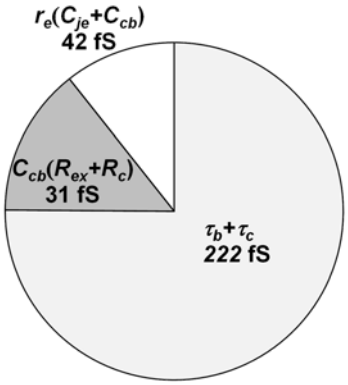

Fig. 10 Relative delay contributions to transistor (0.13x2 μm²) forward delay when biased at close to peak f_t

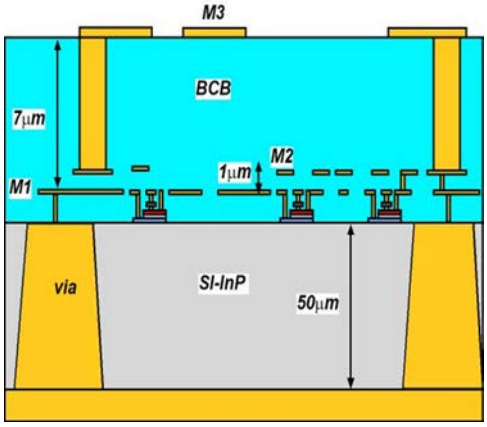

Fig. 11 Schematic cross-section (not to scale) of InP HBT IC thin-film wiring environment

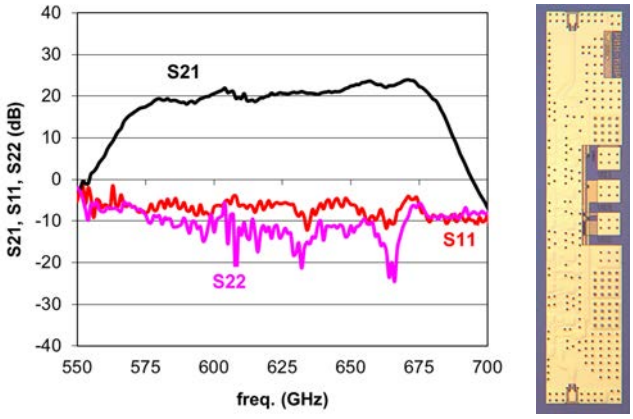

Fig. 12. Measured S-parameters and chip phototraph of 9-stage common-base amplifier using CPW-G wiring from [5]. Chip dimensions: 1.2 x0.25 mm².

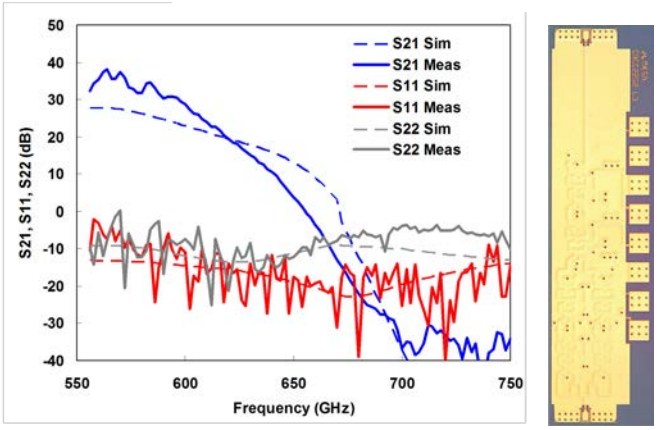

Fig. 13. Measured S-parameters and chip phototraph of differenential common-base amplifier from [6]. Chip dimensions: 1.36 x0.34 mm².

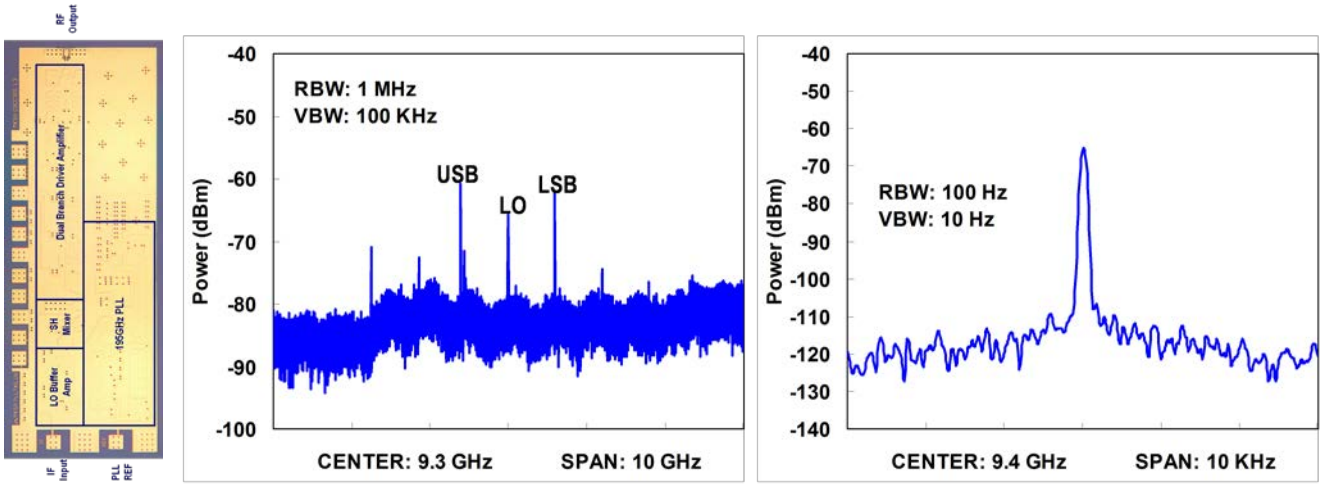

Fig. 14 Chip photograph and measured down-converted output spectrum of an integrated 590 GHz transmitter. For this measurement f_{IF} = 1 GHz and f_{LO} = 196.9 GHz (from PLL driving 3rd order sub-harmonic mixer). The output spectrum was measured using on-wafer probes coupled to a down-converting mixer with f_{LO}= 600 GHz. The output power measurement is uncalibrated.