A 30 GSample/s InP/CMOS Sample-Hold Amplifier with Active Droop Correction

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Abstract — We report a 30 GS/s sample-hold amplifier implemented in a combined InP HBT and Si CMOS heterogeneous integration technology. The high-speed signal path is entirely in InP, but droop in the sampled voltage arising from HBT bias currents is suppressed by an integrated CMOS feedback circuit. Under this closed-loop control, in hold mode, the droop rate of the single-ended outputs is reduced to 20 mV/ns. InP-CMOS interconnect parasitics are isolated from the high-speed signal path by isolation resistors and active bootstrapping. Given an 8 GHz input sampled at 32 GHz, the circuit shows input-referred P1dB and IIP3 of 0.5 dBm and 5.8 dBm, respectively. The total power consumption is 2.7 W and the chip area is 815 × 855 μm².

Index Terms — InP HBT, CMOS, Diverse Accessible Heterogeneous Integration (DAHI), sample and hold amplifier.

I. Introduction

High-speed analog to digital converters (ADCs) serve applications in satellite and wireless communications and in military radar. Wideband, linear, low-noise sample-and-hold amplifier (SHA) are critical components in wideband ADCs, particularly in the front-end of time-interleaved designs.

High-speed and wide-bandwidth THAs and SHAs have been reported in InP HBT, SiGe BiCMOS, and Si CMOS technologies [1]-[3]. InP HBT processes, with high f_{max}/f_{τ} and high breakdown, offer the potential for simultaneous high bandwidth and high linearity. An extremely wideband yet linear SHA was implemented in an InP HBT technology [1].

Yet, InP HBT technologies have key weakness; scales of digital integration are vastly more limited than in Si CMOS, and the low D.C. current gains (β) of InP HBTs can result in large D.C. errors in mixed-signal circuits. In all-InP sample-hold and track-hold amplifiers, the buffer amplifier following the sampling stage has significant AC input conductance and significant DC input bias currents. During the hold mode, the input conductance causes differential low-frequency droop in the sampled signal, while the DC input bias currents discharge the hold capacitors, introducing $dV/dt = I/C_{hold}$ voltage ramps on common-mode and differential held signals. Increasing the hold capacitor to decrease these effects comes at the expense of decreased IC bandwidth.

In [4], a heterogeneous InP/CMOS technology was used to implement both a wideband, low-distortion all-InP HBT track-hold amplifier and, separately, a time-interleaved array of CMOS sample-hold amplifiers with a broadband InP input buffer. Here we report sample-hold amplifiers in a combined InP HBT / Si CMOS technology, in which the InP HBTs provide the entire high-speed signal path, and the CMOS FETs provide DC correction to reduce bias-current-induced ramp errors in the sampled signals.

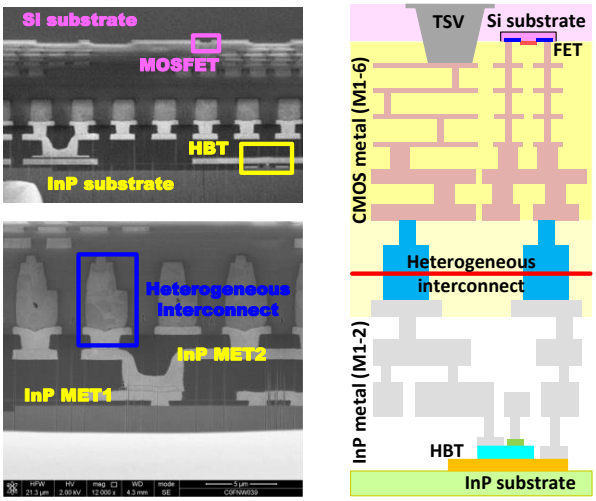
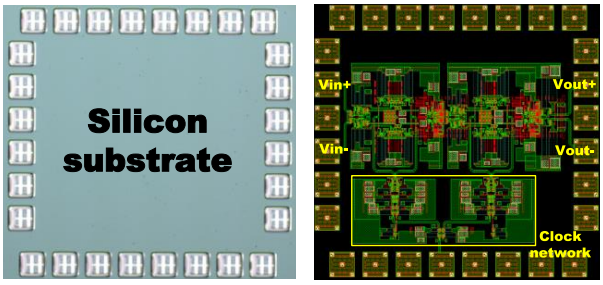


Fig. 1. TEM (left) and representative (right) cross section of InP HBT and Si CMOS heterogeneous integration technology.



(a) (b)

Fig. 2. (a) Die photograph of a SHA. The bottom of the silicon substrate and probe pads are shown. (b) layout for an InP chip.

Fig. 1 shows a cross-section of the InP/Si heterogeneous integration technology. Teledyne Scientific Company 0.25 μm InP HBT ICs and GlobalFoundries 0.13 μm LP/RF CMOS ICs are electrically connected with Direct Bond Interfaces (DBIs), 2.5 μm octagonal Cu islands that mate with identical

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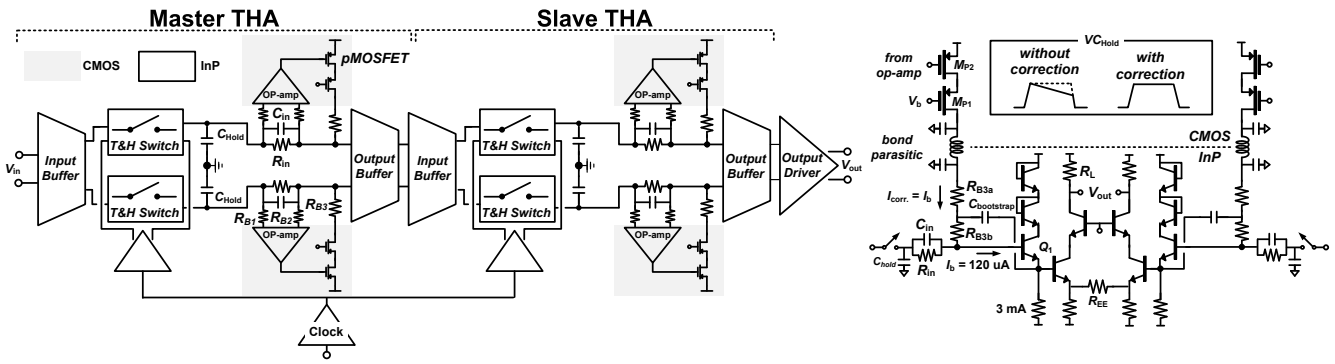

(a) (b)

Fig. 3. (a) Simplified block diagram of the SHA, and (b) the droop-corrected output buffer.

structures on the adjoining CMOS. HBTs with a 6 μm × 0.25 μm emitter finger exhibit BV_{CEO} = 4.5 V, f_{max} = 860 GHz, and f_τ = 390 GHz [5]. The InP process provides two levels of gold interconnects, 0.3 fF/μm² MIM capacitors and 50 Ω/square thin-film-resistors. The DBI pitch is 5 μm and the height of the DBI wiring stack from the InP top-metal to CMOS top-metal is 7 μm. The Si CMOS wafer is bonded to the InP HBT wafer, with the InP wafer bonded to the heat-sink. IC bond pads are fabricated on the back surface of the thinned silicon substrate and are connected to the routing metal with through-silicon vias (TSVs).

II. Circuit Design

The SHA is a pair of track-hold amplifiers (Fig. 3a), each with input buffer, track-hold switch, and output buffer. Design is similar to [1], with a linearized input buffer, feedthrough cancellation, and fast base-collector diodes as switches. The output driver provides a fast 50 Ω interface. Key differences from [1] lie in the use of a CMOS closed loop correction circuit (Fig. 3a) to suppress the output buffer's DC input bias current, and in the design of the output buffer itself (Fig. 3b).

For fast operation, the output buffer collector current is 3mA, and the HBT current gain (β) is 25, hence the HBT base current I_b is 120 μA. Given a 200 fF hold capacitor, the base current, if not corrected, would produce a 600 mV/ns ramp rate. I_b mismatches then produce errors in the differential V_{out}; even with matched I_b, the large ramp introduces error voltages which can exceed the circuit linear common-mode range.

In the compensation circuit, a PMOS current source provides the HBT buffer's input DC bias current. The PMOS current source is a cascode, as the PMOS FET R_{DS} would otherwise load C_{hold} and cause the sampled voltage to droop. The difference between the HBT bias current and the PMOS correction current passes through a series monitoring resistance, with errors in the bias current producing a voltage drop across this resistance. The error voltage is sensed by a two-stage CMOS op-amp [6] integrator which then controls the PMOS current source. To maintain wide circuit bandwidth and minimize added noise, the monitoring resistance is AC bypassed by a shunt capacitor. Precision in the bias current

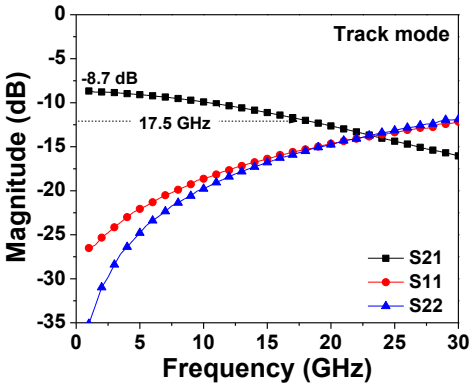

Fig. 4. Measured singled-ended S-parameters of the THA.

correction is determined by the OP-amp offset voltage V_{os}; this can be minimized by appropriate OP-amp design.

The high-speed signal path is isolated from DBI bond parasitics by R_{B3a} and R_{B3b}, with bootstrapping for additional isolation. The high-speed path is isolated from op-amp loading by R_{B1} and R_{B2}.

III. Experimental Results

Fig. 2 shows a SHA die photograph. The total IC area is 815 × 855 μm². The SHA consumes 2.7 W. The clock distribution network operates from a – 2.5 V supply and draws 260 mA, while the remaining circuits use a – 5 V supply.

A THA was first tested. Fig. 4 shows its measured S-parameters. The single-ended input and output return losses are better than -15 dB over the 3-dB bandwidth. The THA has over 17 GHz bandwidth in track mode. Time domain measurements were performed using an Agilent 86100D oscilloscope and the differential output calculated using the scope's built in functions.

Fig. 5 shows the hold-phase output waveform of the SHA for a 2.2 GHz input sampled at 1 GHz. The single-ended droop rate was approximately 20 mV/ns, substantially less than the 600 mV/ns expected without compensation.

Fig. 6(a) and (b) show THA output waveforms given a 0.25 GHz input sampled at 1 GHz, and given an 8 GHz input

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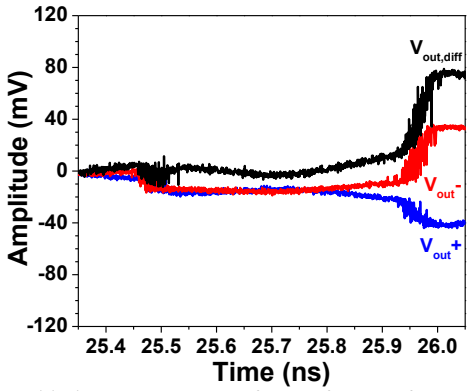
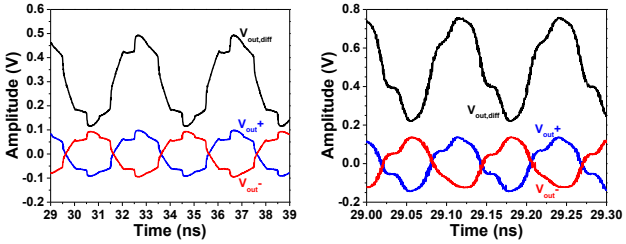
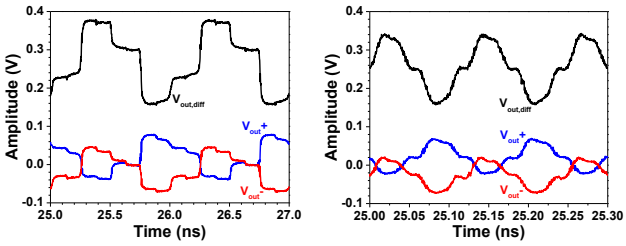


Fig. 5. Hold-phase output waveform of SHA for a 2.2 GHz sinusoidal input signal with 1 GHz clock frequency.



(a) (b)

Fig. 6. Measured differential- and single-ended output waveforms of the THA (a) a 0.25 GHz sinusoidal input signal with 1 GHz clock frequency, and (b) an 8 GHz sinusoidal input signal with 32 GHz clock frequency.



(a) (b)

Fig. 7. Measured differential- and single-ended output waveforms of the SHA (a) a 1 GHz sinusoidal input signal with 4 GHz clock frequency, and (b) an 8 GHz sinusoidal input signal with 32 GHz clock frequency.

sampled at 32 GHz, respectively. Fig. 7(a) and (b) show SHA output waveforms for an 1 GHz input sampled at 4 GHz, and for an 8 GHz input sampled at 32 GHz, respectively.

Fig. 8 shows the measured input-referred 1-dB compression points and the input-referred third order intercept points (IIP3), the latter measured with 100 MHz tone spacing. The spectral characteristics of the SHA beat frequency test with $f_{in} = f_s + \Delta f$, $f_s = 20$ GHz, and $\Delta f = 2$ MHz are shown in Fig. 9. Second- and third-harmonic distortion are better than -45 dBc and -72 dBc at -12 dBm input power.

IV. Conclusion

A high-speed SHA was designed and fabricated in InP HBT and Si CMOS heterogeneous integration technology. The

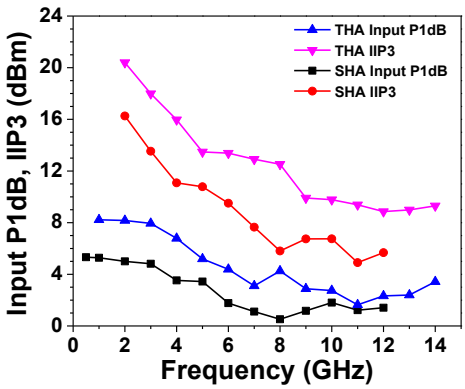


Fig. 8. Measured input-referred P1dB and IIP3 as a function of input frequency given a 32 GHz sampling frequency.

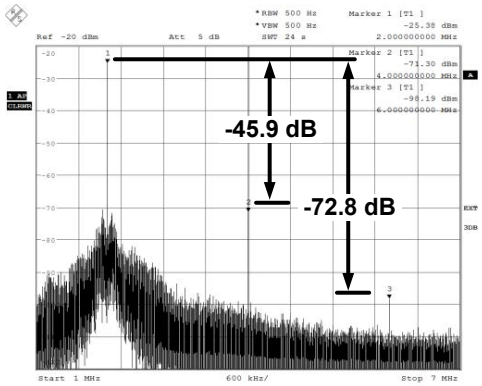


Fig. 9. Beat frequency test of the SHA with 20.002 GHz input signal sampled at 20 GHz (single-ended measurement).

SHA uses InP HBTs for the high-speed signal path and CMOS for DC correction of droop. DBI bond parasitics, though small, are isolated by resistors and bootstrapping. circuits. The resulting droop, at 20 mV/ns, is sufficiently small for ns hold periods even in a wideband circuit.

V. Acknowledgment

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