Transistor and IC design for 50GHz and above

Mark Rodwell, UCSB

mm-wave systems:
Prof. U. Madhow & group: UCSB

mm-wave ICs
S-K Kim, R. Maurer, A. Ahmed, H. Yu, H-C. Park, T. Reed, UCSB
Prof. J. Buckwalter & group, UCSB
J. Hacker, Z. Griffith: Teledyne Scientific and Imaging
M. Seo: Sungkyunkwan University

mm-Wave Transistors:
J. Rode, P. Choudhary, B. Markman, Y. Fang, J. Wu,
A.C. Gossard, B. Thibeault, W. Mitchell: UCSB
M. Urteaga, B. Brar: Teledyne Scientific and Imaging
Why mm-wave wireless?
Overview
mm-Waves: high-capacity mobile communications

spatially-multiplexed mm-wave base stations

spatially-multiplexed mm-wave base stations

mm-wave backhaul

or optical backhaul

140 GHz, 10 Gb/s Adaptive Picocell Backhaul

array: 2x32

4 units

90° (h) by 10° (v) scan

individual antennas 1.4x12 mm

25mm

44mm

60 GHz, 1 Tb/s Spatially-Multiplexed Base Station

128 users/face, 512 total users, each beam 2Gb/s

205 mm

29mm

Needs→ research:

RF front end: phased array ICs, high-power transmitters, low-noise receivers

IF/baseband: ICs for multi-beam beamforming, for ISI/multipath suppression, ...
**mm-Waves: benefits & challenges**

**Large available spectrum**

![Graph showing Rain Attenuation vs Frequency](image1)

- **Rain Attenuation** in dB/Km:
  - Rain: 25, 50, 100 mm/hr
  - Humidity: 95%
  - Temperature: 35°C
  - Fog: 1G/m³

- **Frequency (GHz)**: 0, 50, 100, 200, 300, 350

- **Rain Attenuation (dB/Km)**: 0.01, 1, 10, 100

- **Note**: High attenuation in foul weather

**Massive # parallel channels**

- **Angular resolution** = \( \frac{\text{wavelength}}{\text{array width}} \)

- **Equation**:
  \[
  N = \frac{B^2}{\lambda R + 1}
  \]

- **Line-of-sight MIMO**

- **Spatial Multiplexing**

**Need phased arrays** (overcome high attenuation)

- **Equation**:
  \[
  \frac{P_{\text{received}}}{P_{\text{transmit}}} \propto N_{\text{receive}} N_{\text{transmit}} \frac{\lambda^2}{R^2} e^{-\alpha R}
  \]

**Need mesh networks**

- **High-frequency signals are easily blocked.**

- **Blockage is avoided using beamsteering and mesh networks.**

- **This is easier at high frequencies.**
mm-Wave Wireless Needs Phased Arrays

**isotropic antenna** → weak signal → short range

\[
\left( \frac{P_{\text{received}}}{P_{\text{transmitted}}} \right) \propto \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R}
\]

**highly directional antenna** → strong signal, but must be aimed

\[
\left( \frac{P_{\text{received}}}{P_{\text{transmitted}}} \right) \propto D_t D_r \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R}
\]

no good for mobile

must be precisely aimed → too expensive for telecom operators

**beam steering arrays** → strong signal, steerable

\[
\frac{P_{\text{received}}}{P_{\text{transmitted}}} \propto N_{\text{receive}} N_{\text{transmit}} \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R}
\]

32-element array → 30 (45?) dB increased SNR
Millimeter-wave imaging

10,000-pixel, 94GHz imaging array → 10,000 elements

Demonstrated:
SiGe (UCSD/Rebeiz)
~1.3kW: 10,000 elements

Lower-power designs:
InP, CMOS, SiGe
(UCSB, UCSD, Virginia Poly.)

235 GHz video-rate synthetic aperture radar

1 transmitter, 1 receiver
100,000 pixels
20 Hz refresh rate
5 cm resolution @ 1km
50 Watt transmitter
(tube, solid-state driver)
mm-wave imaging radar: TV-like resolution

mm-waves $\rightarrow$ high resolution from small apertures

What you see in fog

What 10GHz radar shows

What you want to see

goal: $\sim 0.2^\circ$ resolution, $10^3$-$10^6$ pixels

Large $N \times N$ phased array

Frequency-scanned $1 \times N$ array

ultimate: $\sim 400$ GHz; intermediate: $\sim 140$ GHz
mm-wave systems
Target Systems
arrays
Antenna & array basics

Overall array sets beamwidth and gain

horizontal beamwidth \( \approx \frac{\lambda}{\text{array width}} \) (radians)

vertical beamwidth \( \approx \frac{\lambda}{\text{array height}} \)

Gain (directivity) \( \approx \frac{4\pi \cdot \text{array area}}{\lambda^2} \)

Individual element sets maximum beam steering range.

horizontal steering \( \approx \frac{\lambda}{\text{element width}} \) (radians)

vertical steering \( \approx \frac{\lambda}{\text{element height}} \)
Electronic Beamsteering, a.k.a. phased array

Phase-shifters bring signals back into phase at physical angle $\theta$.

Path length difference $\Delta l = D_v \sin \theta$

Required electrical phase shift between adjacent elements $\Delta \phi = 2\pi \cdot \Delta l / \lambda$. 
Reminder: Multipath Propagation

Given large angular beamwidth (low - directivity antennas)
Many objects in antenna beam pattern.
Many signal paths : multi - path propagation

Each path has different length, different delay.
Reflecting surface boundary condition : possible phase shift.
Each path has different signal strenght
    Directivity of antennas
    Strenght of reflection
Fading vs Intersymbol interference

(Delay spread \(\ll\) Symbol period) \(\rightarrow\) Fading

LOS and NLOS signals arrive with symbol periods \(~\) aligned
Carriers are out of phase \(\rightarrow\) interference \(\rightarrow\) possibly very weak signal
fix : two receiving antennas at appropriate separation

(Delay spread \(>\) Symbol period) \(\rightarrow\) Intersymbol interference

One bit period interferes with another
need adaptive equalizer in receiver
or use ODFM \(\ll\) longer symbol periods
Beamforming can suppress ISI

\[ \text{Delay spread} \approx \frac{H^2}{2Dc} \]

1 Gbaud with 10° array beamwidth:
- multipath mostly causes fading
- not much ISI

10 Gbaud with 10° array beamwidth:
- significant fading and significant ISI

Solution 1: larger arrays
- narrower beamwidth

Solution 2: multiple arrays
- multiple receivers to handle fading?
  - can sum these to form narrow nulls!
  - also handles fading and ISI

\( H \) receive array \quad \( H \) transmit array
\( V \) receive array \quad \( V \) transmit array

\[ 1 \text{ inch} \]

1Gbaud \quad 10 \text{ Gbaud}
Optimum array size for low system power

\[ \frac{P_{\text{receive}}}{P_{\text{transmit}}} \propto N^2 \frac{\lambda^2}{R^2} \rightarrow P_{\text{transmit}} \propto \frac{1}{N^2} \]

Total system power = \( \frac{P_{\text{transmit}}}{\text{efficiency}} + N(\text{power of LNA, phase shifters...}) \)

Do large arrays save power?

At optimum-size array, target PA output power is typically 10-200 mW
How big should be the array?

Large arrays:
- more directive $\rightarrow$ less PA power needed
- more channels $\rightarrow$ cost, DC power

Large arrays: more directive $\rightarrow$ less SNR loss with NLOS nulling

*eases multipath equalization*
Data delay equalization in large arrays

Simple arrays retime the carrier but not the modulation timing skew $= \frac{D \sin \theta}{c}$; must be below $\sim T_{\text{symbol}} / 2$

$\rightarrow$ bandwidth $\approx \frac{c}{D \sin \theta}$

Very large arrays:
compensate by *array tiling*
with modulation retimed between tiles
systems
mm-Wave LOS MIMO: multi-channel for high capacity

\[ N = \frac{B^2}{\lambda R} + 1 \]

\[ B = ND \]

\[ \text{#channels} \propto \frac{(\text{aperture area})^2}{(\text{wavelength} \cdot \text{distance})^2} \]

---

Torklinson: 2006 Allerton Conference
Sheldon: 2010 IEEE APS-URSI
Spatial Multiplexing: massive capacity RF networks

multiple independent beams
each carrying different data
each independently aimed
# beams = # array elements

Hardware: multi-beam phased array ICs
100-1000 GHz Wireless Needs Mesh Networks

Object having area $\sim \lambda R$ will block beam.

...high-frequency signals are easily blocked.

Blockage is avoided using beamsteering and mesh networks.

...this is easier at high frequencies.
mm-wave propagation
Fair-Weather Propagation

H = 0, 4, 9.2 km; ν = 7.5, 1, 0.08 g/m³

- **Fair weather**
- 2-5 dB/km
- 200-300 GHz
- 125-165 GHz
- 75-110 GHz
- 4 km elevation
- 9 km elevation
- 75-110 GHz
- 125-165 GHz
- 200-300 GHz
- 2-5 dB/km

Wiltse, 1997 IEEE Int. APS Symposium, July
Foul Weather Propagation

**Rain:**
- $10^{-3}$: 25mm/hr, 11dB/km
- $10^{-4}$: 50-85mm/hr, 19dB/km
- $10^{-5}$: 100+mm/hr: 30dB/km

**Rain Attenuation, dB/km**
- 30 dB/km
- 100 mm/hr
- 50 mm/hr

**Frequency, Hz**
- $10^9$ to $10^{12}$

**35°C, 95% Humidity**
- loss (dB/km)~(frequency/60GHz)$^2$
- 11 dB/km@200 GHz, 5.5dB/km@140GHz

**Extreme Fog** ($1g/m^3$)
- ~$(25 \text{ dB/km}) \times (\text{frequency/500 GHz})$

---

Karasawa, Maekawa, IEEE Proc, Vol 85, #6, June 1997
Rosker; Wallace, 2007 IEEE IMS
Worst-case attenuation roughly constant over 50-250 GHz.

$10^{-5}$ outage rate: equal losses over 50-300 GHz

$10^{-3}$ outage rate: equal losses over 50-200 GHz

*target should be 50-250 GHz links.*

*Exclusive use of VLSI Si processes forces use of 50-180GHz*
detailed link analysis
Example Link budgets (60 GHz)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>B: Bit rate</td>
<td>1.00E+10/sec</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>6.00E+10 Hz</td>
</tr>
<tr>
<td>i: Wavelength</td>
<td>5.00E-03 m</td>
</tr>
<tr>
<td>Required SNR (measured as Eb/No)</td>
<td>6.3 dB</td>
</tr>
<tr>
<td>Receiver bandwidth</td>
<td>2.16E+09 Hz</td>
</tr>
<tr>
<td>SNR (measured as KTB, B from above cell)</td>
<td>13.0 dB</td>
</tr>
<tr>
<td>F: Receiver noise figure</td>
<td>4.5 dB</td>
</tr>
<tr>
<td>R: Transmission range</td>
<td>50.0 m</td>
</tr>
<tr>
<td>Vertical beam angle, FWHM</td>
<td>2.5 deg</td>
</tr>
<tr>
<td>Horizontal beam angle, FWHM</td>
<td>11.3 deg</td>
</tr>
<tr>
<td>Transmitter</td>
<td>2.653E-02 dB/m</td>
</tr>
<tr>
<td>Vertical angle scanned, total</td>
<td>5.0 deg</td>
</tr>
<tr>
<td>Homogonous angle scanned, total</td>
<td>90.4 deg</td>
</tr>
<tr>
<td>Total # array elements</td>
<td>16</td>
</tr>
<tr>
<td>Vertical angle scanned, total</td>
<td>5.0 deg</td>
</tr>
<tr>
<td>Horizontal angle scanned, total</td>
<td>90.4 deg</td>
</tr>
<tr>
<td>Total # rows and columns</td>
<td>2 # rows 8 # columns</td>
</tr>
<tr>
<td>Array height</td>
<td>2.29 wavelengths</td>
</tr>
<tr>
<td>Array width</td>
<td>5.1 wavelengths</td>
</tr>
<tr>
<td>Array height</td>
<td>1.15E-01 meters</td>
</tr>
<tr>
<td>Array width</td>
<td>2.54E-02 meters</td>
</tr>
<tr>
<td>antenna directivity, dB</td>
<td>31.62 dB</td>
</tr>
<tr>
<td>Packaging loss (receiver)</td>
<td>2 dB</td>
</tr>
<tr>
<td>Packaging loss (transmitter)</td>
<td>2 dB</td>
</tr>
<tr>
<td>Horizontal beam angle, FWHM</td>
<td>11.3 deg</td>
</tr>
<tr>
<td>Beam aiming loss (edge of beam)</td>
<td>3 dB</td>
</tr>
<tr>
<td>Prec. received power at 1E-9 BER</td>
<td>-46.00 dBm</td>
</tr>
<tr>
<td>geometric path loss</td>
<td>1.33E-04 dB</td>
</tr>
<tr>
<td>geometric path loss, dB</td>
<td>-38.75 dB</td>
</tr>
<tr>
<td>path obstruction loss (foliage, glass)</td>
<td>4.00 dB</td>
</tr>
<tr>
<td>atmospheric loss</td>
<td>1.3266681 dB</td>
</tr>
<tr>
<td>atmospheric loss</td>
<td>26.53 dB/km</td>
</tr>
</tbody>
</table>

\[ P_{\text{received}}(4QPSK) = Q^2 \cdot kT \times B \]

\[ P_{\text{received}} / P_{\text{trans}} = (D_t \cdot D_r / 16\pi^2) (\lambda / R)^2 \]

\[ D = 4\pi A_{\text{eff}} / \lambda^2 \approx \frac{4\pi}{\theta_{\text{FWHM}}^\circ \phi_{\text{FWHM}}^\circ} \approx \frac{41,000}{\theta_{\text{FWHM}}^\circ \phi_{\text{FWHM}}^\circ} \]

Note various margins allocated.
Rain losses calculated from rain rate.
Example Link budgets (140 GHz)

Note various margins allocated. Rain losses calculated from rain rate.
hardware:
rough numbers
140 GHz, 10 Gb/s Adaptive Picocell Backhaul

array: 2x32

4 units

90° (h) by 10° (v) scan

individual antennas 1.4x12 mm

25mm

44mm
140 GHz, 10 Gb/s Adaptive Picocell Backhaul

350 meters range in 50mm/hr rain

Realistic packaging loss, operating & design margins

PAs: 24 dBm $P_{\text{sat}}$ (per element)

LNAs: 4 dB noise figure
340 GHz, 160 Gb/s MIMO Backhaul Link

Eight 20 Gb/s MIMO units: each an 8x8 array

individual antennas: 6x6 mm

→ 1° beamwidth; 8° beamsteering
340 GHz, 160 Gb/s MIMO Backhaul Link

Eight 20 Gb/s MIMO units: each an 8x8 array

1° beamwidth; 8° beamsteering

600 meters range in five-9's rain

Realistic packaging loss, operating & design margins

PAs: 21 dBm $P_{\text{sat}}$ (per element)

LNAs: 7 dB noise figure
60 GHz, 1 Tb/s Spatially-Multiplexed Base Station

2x64 array on each of four faces.
Each face supports 128 users, 128 beams: 512 total users.
Each beam: 2Gb/s.

200 meters range in 50 mm/hr rain
Realistic packaging loss, operating & design margins

PAs: 20 dBm $P_{out}$, 26 dBm $P_{sat}$ (per element)
LNAs: 3 dB noise figure
mm-Wave Wireless Transceiver Architecture

- Custom PAs, LNAs → power, efficiency, noise
- Si CMOS beamformer → integration scale

...similar to today's cell phones.
400 GHz frequency-scanned imaging radar

What your eyes see-- in fog

What you see with X-band radar

What you would like to see
400 GHz frequency-scanned imaging car radar

Eight 1x8 modules

1x64 endfire array

30 cm x 30 cm diffraction grating

cylindrical lens: 30 cm aperture

frequency-scanned beam

individual antennas: 0.4 mm x 5.0 mm

38 mm
400 GHz frequency-scanned imaging car radar

Range: see a basketball at 300 meters (10 seconds warning) in heavy fog
(10 dB SNR, 28 dB/km, 1 foot diameter target, 65 MPH)

Image refresh rate: 60 Hz

Resolution 64×512=32,800 pixels

Angular resolution: 0.10 degrees

Angular field of view: 9 by 97 degrees

Aperture: 12" by 12"

Component requirements:
10 mW peak power/element,
3% pulse duty factor
6.5 dB noise figure,
5 dB package losses
5 dB manufacturing/aging margin
Transistors and IC technologies
"Useful (frequency) range" means those frequencies at which acceptable-performance IC blocks can be realized, not the highest frequency of a published research result.

<table>
<thead>
<tr>
<th>foundry</th>
<th>process</th>
<th>nominal $f_{\text{max}}$</th>
<th>useful range</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBM (GF !)</td>
<td>9HP</td>
<td>320 GHz</td>
<td>~170 GHz</td>
</tr>
<tr>
<td>TowerJazz</td>
<td>SBC13H3</td>
<td>270 GHz</td>
<td>~140 GHz</td>
</tr>
<tr>
<td>TowerJazz</td>
<td>SBC18H4 (near release)</td>
<td>350 GHz</td>
<td>~180 GHz</td>
</tr>
<tr>
<td>ST Microelectronics</td>
<td>S9MW</td>
<td>270 GHz</td>
<td>~140 GHz</td>
</tr>
<tr>
<td>ST Microelectronics</td>
<td>SB55 (development)</td>
<td>340 GHz</td>
<td>~180 GHz</td>
</tr>
</tbody>
</table>
### Production Semiconductor Processes for mm-Wave

<table>
<thead>
<tr>
<th>VLSI CMOS Processes</th>
<th>process</th>
<th>nominal $f_{\text{max}}$</th>
<th>useful range</th>
</tr>
</thead>
<tbody>
<tr>
<td>various (IBM, GF, TSMC)</td>
<td>65nm bulk CMOS</td>
<td>~250GHz</td>
<td>~130GHz</td>
</tr>
<tr>
<td>IBM (GF !)</td>
<td>45nm PD-SOI (high leakage power)</td>
<td>~300 GHz</td>
<td>~150 GHz</td>
</tr>
<tr>
<td>IBM (GF !)</td>
<td>32 nm UTB-SOI</td>
<td>~300 GHz</td>
<td>~150 GHz</td>
</tr>
<tr>
<td>ST Microelectronics</td>
<td>28 nm UTB-SOI</td>
<td>similar to above</td>
<td></td>
</tr>
<tr>
<td>various</td>
<td>22nm, ~14nm UTB-SOI</td>
<td>poorer than above</td>
<td></td>
</tr>
<tr>
<td>Intel, IBM/GF</td>
<td>22nm, ~14nm finFET</td>
<td>likely poorer than above,</td>
<td></td>
</tr>
</tbody>
</table>

Generations beyond 28/32nm:
- progressively poorer performance in 100+ GHz ICs
- progressively lower transmitter power at all frequencies
# Semiconductor Processes for mm-Wave Production

## Production III-V foundries

<table>
<thead>
<tr>
<th>foundry</th>
<th>process</th>
<th>nominal $f_{\text{max}}$</th>
<th>useful range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Northrop-Grumman (low-volume)</td>
<td>600nm InP HBT: 4V: higher-power transmitters</td>
<td>&gt;300GHz</td>
<td>~150 GHz</td>
</tr>
<tr>
<td>Northrop-Grumman (low-volume)</td>
<td>100nm InP HEMT (FET) for very low noise receivers</td>
<td>&gt;350GHz</td>
<td>~200 GHz</td>
</tr>
<tr>
<td>Qorvo (Tri-Quint)</td>
<td>TQP13 HEMT power amps, low-noise -amps</td>
<td>~~150GHz</td>
<td>100 GHz</td>
</tr>
</tbody>
</table>

These processes are best for single-stage add-on power amps, low-noise amps; both to increase system range.
Research Semiconductor Processes

### Research institutions with some "foundry-like" access

<table>
<thead>
<tr>
<th>foundry</th>
<th>process</th>
<th>nominal f&lt;sub&gt;max&lt;/sub&gt;</th>
<th>useful range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Teledyne</td>
<td>250nm InP HBT</td>
<td>700GHz</td>
<td>~250 GHz</td>
</tr>
<tr>
<td>Teledyne</td>
<td>130nm InP HBT</td>
<td>1100 GHz</td>
<td>~450 GHz</td>
</tr>
<tr>
<td>IHP</td>
<td>130nm SiGe BiCMOS</td>
<td>500GHz</td>
<td>~250 GHz</td>
</tr>
</tbody>
</table>

microwave GaN HEMT is a production technology

*mm-wave* GaN HEMT *may become* a production technology

mm-wave InP HBT may become a production technology
mm-wave CMOS (examples)

260 GHz amplifier:
65nm bulk CMOS, Over-neutralized to reach $G_{\text{max}}$, 9.2 dB, 4 stages
Momeni ISSCC, March 2013

150 GHz amplifier: 65 nm bulk CMOS, 8.2 dB, 3 stages (250GHz $f_{\text{max}}$)
Seo et al. (UCSB), JSSC, December 2009
mm-Wave CMOS won't scale much further

Gate dielectric can't be thinned → on-current, $g_m$ can't increase

![Graph](image)

Shorter gates give no less capacitance dominated by ends; ~1fF/μm total

Maximum $g_m$, minimum $C$ → upper limit on $f_T$ about 350-400 GHz.

Tungsten via resistances reduce the gain
Inac et al, CSICS 2011

Present finFETs have yet larger end capacitances
III-V high-power transmitters, low-noise receivers

**Cell phones & WiFi:**
GaAs PAs, LNAs

**mm-wave links need**
high transmit power,
low receiver noise

- **0.47 W @86GHz**
  H Park, UCSB, IMS 2014

- **0.18 W @220GHz**
  T Reed, UCSB, CSICS 2013

- **1.9mW @585GHz**
  M Seo, TSC, IMS 2013
InP Bipolar Transistors
Why InP Bipolar Transistors?

InP better electron transport than Si collectors
higher electron velocity 3.5 vs $1.0 \times 10^7$ cm/s
plus wider bandgap $\rightarrow$ higher breakdown field

InGaAs base, base-emitter heterojunction:
very low base sheet resistances

Implications:
$\sim 3:1$ higher $(f_\tau, f_{\text{max}})$ at a given scaling node
higher breakdown* at a given $(f_\tau, f_{\text{max}})$
but...InP HBT not a production technology

*BREAKDOWN is too complicated to summarize with BVCEO.
BVCBO vs. BVCEO vs. safe operating area?
Bottom line: look at $V_{ce}$ used in published IC data for a given IC technology.
Transistor scaling laws: \((V,I,R,C,\tau)\) vs. geometry

**Depletion Layers**
\[
C = \varepsilon \cdot \frac{A}{T}
\]
\[
\tau = \frac{T}{2v}
\]
\[
I_{\text{max}} = \frac{4\varepsilon v_{\text{sat}}(V_{\text{appl}} + \phi)}{A} \frac{T^2}{T}
\]

**Bulk and Contact Resistances**
\[
R \approx \rho_{\text{contact}} / A
\]
contact te rms dominate

**Fringing Capacitances**
\[
C_{\text{facing}} / L \sim \varepsilon
\]

**Thermal Resistance**
\[
\Delta T_{\text{IC}} \propto \frac{P_{\text{IC}}}{K_{\text{th}} L}
\]
\[
\Delta T_{\text{transistor}} \sim \frac{P}{\pi K_{\text{th}} L} \ln\left(\frac{L}{W}\right)
\]

**Available quantum states to carry current**
\[
\Delta k = \pi / L
\]
\[
E \propto k^2
\]
capacitance, transconductance contact resistance
Bipolar Transistor: Structure & Models

\[ \frac{1}{2 \pi f_T} = \tau_{base} + \tau_{collector} + C_{je} \frac{nkT}{qI_E} + C_{bc} \left( \frac{nkT}{qI_E} + R_{ex} + R_{coll} \right) \]

\[ R_{be} = \beta / g_m \]

\[ g_m = \frac{qI_E}{nkT} \]

\[ C_{be} = C_{je} + g_m (\tau_b + \tau_c) \]

\[ \tau_b \approx T_b^2 / 2D_n + T_b / v_{thermal} \]

\[ \tau_c \approx T_c / 2v_{"sat"} \]
Base-Collector Distributed RC Parasitics

\[
R_{\text{ex}} = \rho_{\text{contact,emitter}} / A_{\text{emitter}}
\]

\[
R_{\text{spread}} = \rho_s W_e / 12 L_E
\]

\[
R_{\text{gap}} = \rho_s W_{\text{gap}} / 4 L_E
\]

\[
R_{\text{spread,contact}} = \rho_s W_{\text{bc}} / 6 L_E
\]

\[
R_{\text{contact}} = \rho_{\text{contact,base}} / A_{\text{base_contacts}}
\]

\[
C_{cb,e} = \varepsilon A_{\text{emitter}} / T_c
\]

\[
C_{cb,gap} = \varepsilon A_{\text{gap}} / T_c
\]

\[
C_{cb,\text{contact}} = \varepsilon A_{\text{base_contacts}} / T_c
\]
The time constant, $f_{\text{max}}$, for a Simple Hybrid-π model is given by:

$$f_{\text{max}} \approx \sqrt{f_{\tau}/8\pi R_{bb} C_{cbi}}$$

where

$$\tau_{cb} = R_{bb} C_{cbi} = C_{cb,\text{contact}} R_{\text{contact}} + C_{cb,\text{gap}} (R_{\text{contact}} + R_{\text{spread,contact}} + R_{\text{gap}}/2) + C_{cb,e} (R_{\text{contact}} + R_{\text{spread,contact}} + R_{\text{gap}} + R_{\text{spread}})$$

$R_{bb}$ = true total base resistance

$C_{cbi} + C_{cbx}$ = true total $C_{cb}$

$C_{cbi} : C_{cbx}$ ratio set to fit $f_{\text{max}}$ from above
BJT Space-Charge-Limited Current (Kirk effect)

\[ \frac{\partial^2 \phi}{\partial x^2} = \frac{\rho}{\varepsilon} = \left( qN_D - \frac{J}{\nu} \right) / \varepsilon \]

\[ \Rightarrow I_{\text{max}} = 2\varepsilon v_{\text{eff}} A_E (V_{cb} + V_{cb,\text{min}} + 2\phi) / T_c^2 \]

\[ A_{jbe} = 0.6 \times 4.3 \ \mu m^2 \quad V_{cb} = 0 \ V \]

\[ I_{\text{b step}} = 180 \ \mu A \]

\[ J_e (mA/\mu m^2) \]

\[ V_{ce} (V) \]

\[ J_e (mA/\mu m^2) \]

\[ V_{cb} = 0.6 \ V \]

\[ J_e (mA/\mu m^2) \]

\[ C_{cb} / A_e \ (pf/(fF/\mu m^2)) \]

\[ f_{\tau}, f_{\text{max}} \]

Decreased \( (f_{\tau}, f_{\text{max}}) \), increased \( C_{cb} \) at high \( J \).

Kirk threshold increases with increased \( V_{ce} \).
InP: Electron velocity modulation

More collector voltage → less distance before scattering → more transit time

less collector voltage

more collector voltage

heavy X valley
heavy L valley
light Γ valley

(f_\text{t}, f_{\text{max}}) decrease with increased V_{ce}. C_{cb} is modulated by I_c.
Reduced $g_m$ at extreme current densities

**Boltzmann**

Energy diagram showing occupancy and Fermi level $E_F$.

**Fermi-Dirac**

Energy diagram showing occupancy and Fermi level $E_F$.

**Highly Degenerate**

Energy diagram showing occupancy and Fermi level $E_F$.

High currents $\rightarrow$ transconductance less than $qI/kT \rightarrow$ bandwidth decreases

Problem in InP, not silicon: silicon has larger electron effective mass, more valleys
Bipolar Transistor Design

\[ \tau_b \approx \frac{T_b^2}{2D_n} \]

\[ \tau_c = \frac{T_c}{2v_{sat}} \]

\[ C_{cb} = \frac{\varepsilon A_c}{T_c} \]

\[ I_{c,\text{max}} \propto v_{sat} A_e \left( V_{\text{ce,operating}} + V_{\text{ce,punch-through}} \right) / T_c^2 \]

\[ \Delta T \propto \frac{P}{L_E} \left[ 1 + \ln \left( \frac{L_e}{W_e} \right) \right] \]

\[ R_{ex} = \rho_{\text{contact}} / A_e \]

\[ R_{bb} = \rho_{\text{sheet}} \left( \frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e} \right) + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}} \]
Bipolar Transistor Design: Scaling

\[ \tau_b \approx \frac{T_b^2}{2D_n} \]

\[ \tau_c = \frac{T_c}{2\nu_{sat}} \]

\[ C_{cb} = \varepsilon A_c / T_c \]

\[ I_{c,\text{max}} \propto \nu_{sat} A_e (V_{ce,\text{operating}} + V_{ce,\text{punch-through}}) / T_c^2 \]

\[ \Delta T \propto \frac{P}{L_E} \left[ 1 + \ln \left( \frac{L_e}{W_e} \right) \right] \]

\[ R_{ex} = \rho_{\text{contact}} / A_e \]

\[ R_{bb} = \rho_{\text{sheet}} \left( \frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e} \right) + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}} \]
Energy-limited vs. field-limited breakdown

$E_{\text{gap,base}}$

$E_{\text{gap,collector}}$

emitter

base

collector

band-band tunneling: base bandgap
impact ionization: collector bandgap
Making faster bipolar transistors

- To double the bandwidth:
  - Change:
    - Emitter & collector junction widths: decrease 4:1
    - Current density (mA/\(\mu\text{m}^2\)): increase 4:1
    - Current density (mA/\(\mu\text{m}\)): constant
    - Collector depletion thickness: decrease 2:1
    - Base thickness: decrease 1.4:1
    - Emitter & base contact resistivities: decrease 4:1

Narrow junctions.

Thin layers

High current density

Ultra low resistivity contacts
Refractory Contacts to In(Ga)As

Refractory: robust under high-current operation / Low penetration depth: ~ 1 nm / Performance sufficient for 32 nm / 2.8 THz node.

Why no ~2THz HBTs today?

Problem: reproducing these base contacts in full HBT process flow
THz HBTs: The key challenges

Obtaining good base contacts
*in HBT vs. in contact test structure*
(emitter contacts are fine)

RC parasitics along finger length
metal resistance, excess junction areas

THz HBTs: double base metal process

Blanket surface clean (UV O$_3$ / HCl) 
strips organics, process residues, surface oxides

Blanket base metal 
no photoresist; no organic residues 
Ru refractory diffusion barrier 
2 nm Pt : penetrates residual oxides

Thick Ti/Au base pad metal  liftoff 
thick metal→ low resistivity
Reducing Emitter Length Effects

Before:
- Large base post
- Small base post undercut
  - 1100 nm
  - 220 nm

After:
- Small base post
- Large base post undercut
  - 830 nm
  - 50 nm

Rode et al., IEEE TED, Aug. 2015
Reducing Emitter Length Effects

before

HBT64A

Pt/Ti/Pd/Au

100 nm

after

HBT64J

Ti/Au

Pt/Ru/Pt

InGaAs

InP

TiW

Mo

W

thicker Au base metal

narrower collector junction

Rode et al., IEEE TED, Aug. 2015
InP HBTs: 1.07 THz @200nm, ?? @ 130nm

Rode et al., IEEE TED, Aug. 2015
130nm / 1.1 THz InP HBT: ICs to 670 GHz

614 GHz fundamental VCO
M. Seo, TSC / UCSB

340 GHz dynamic frequency divider
M. Seo, UCSB/TSC
IMS 2010

620 GHz, 20 dB gain amplifier
M. Seo, TSC
IMS 2013
also: 670GHz amplifier
J. Hacker, TSC
IMS 2013 (not shown)

300 GHz fundamental PLL
M. Seo, TSC
IMS 2011

204 GHz static frequency divider (ECL master-slave latch)
Z. Griffith, TSC
CSIC 2010

220 GHz 180 mW power amplifier
T. Reed, UCSB
CSICS 2013

81 GHz 470 mW power amplifier
H-C Park UCSB
IMS 2014

Integrated 300/350GHz Receivers:
LNA/Mixer/VCO
M. Seo TSC

600 GHz Integrated Transmitter
PLL + Mixer
M. Seo TSC
Towards a 3 THz InP Bipolar Transistor

Extreme base doping $\rightarrow$ low-resistivity contacts $\rightarrow$ high $f_{\text{max}}$

Extreme base doping $\rightarrow$ fast Auger ($NP^2$) recombination $\rightarrow$ low $\beta$.

Solution: very strong base compositional grading $\rightarrow$ high $\beta$
1/2-THz SiGe HBTs

500 GHz $f_{\text{max}}$ SiGe HBTs  Heinemann et al. (IHP), 2010 IEDM

16-element multiplier array @ 500GHz (1 mW total output)
U. Pfeiffer et. al. (Wuppertal / IHP), 2014 ISSCC
Towards a 2 THz SiGe Bipolar Transistor

### Similar scaling
- **InP:** 3:1 higher collector velocity
- **SiGe:** good contacts, buried oxides

### Key distinction: Breakdown
InP has:
- thicker collector at same $f_\tau$
- wider collector bandgap

### Key requirements:
- low resistivity Ohmic contacts
- note the high current densities

<table>
<thead>
<tr>
<th></th>
<th>InP</th>
<th>SiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>emitter</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>junction width</td>
<td>64</td>
<td>18</td>
</tr>
<tr>
<td>access resistivity</td>
<td>2</td>
<td>0.6</td>
</tr>
<tr>
<td><strong>base</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>contact width</td>
<td>64</td>
<td>18</td>
</tr>
<tr>
<td>contact resistivity</td>
<td>2.5</td>
<td>0.7</td>
</tr>
<tr>
<td><strong>collector</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>thickness</td>
<td>53</td>
<td>15</td>
</tr>
<tr>
<td>current density</td>
<td>36</td>
<td>125</td>
</tr>
<tr>
<td>breakdown</td>
<td>2.75</td>
<td>1.3?</td>
</tr>
<tr>
<td>$f_\tau$</td>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td>$f_{\text{max}}$</td>
<td>2000</td>
<td>2000</td>
</tr>
</tbody>
</table>

Assumes collector junction 3:1 wider than emitter.
Assumes SiGe contacts no wider than junctions.
InP Field-Effect Transistors
State of the art in InP HEMTs

First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process

Xiaobing Mei, et al, IEEE EDL, April 2015 (Northrop-Grumman)
**HEMTs: Key Device for Low Noise Figure**

2:1 to 4:1 increase in $f_t \rightarrow$ greatly improved noise @ 200-670 GHz.

Better range in sub-mm-wave systems; or use smaller power amps.

or enable yet higher-frequency systems

Hand-derived modified Fukui Expression, fits CAD simulation extremely well.
**FET Design**

\[ C_{gd} \approx C_{gs,f} \approx \varepsilon W_g \]

\[ g_m = C_{g-ch} \cdot (v / L_g) \]

\[ C_{g-ch} = \frac{L_g W_g}{T_{ox} / \varepsilon_{ox} + T_{well} / 2\varepsilon_{well} + (q^2 / \text{well state density})} \]

\[ v \propto \left( \frac{\text{voltage division ratio between the above three capacitors}}{\text{the above three capacitors}} \right)^{-1/2} \cdot \frac{1}{\sqrt{\text{transport mass}}} \]

\[ R_{DS} \approx \frac{L_g}{W_g v \varepsilon} \quad R_S = R_D = \frac{\rho_{\text{contact}}}{L_{S/D} W_g} \]
FET Design: Scaling

\[ C_{gd} \approx C_{gs,f} \approx \varepsilon W_g \]

\[ g_m = C_{g-ch} \cdot \left( \frac{v}{L_g} \right) \]

\[ C_{g-ch} = \frac{L_g W_g}{T_{ox}/\varepsilon_{ox} + T_{well}/2\varepsilon_{well} + (q^2/\text{well state density})} \]

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\[ \frac{C_{gd}}{C_{gs,f}} \approx \varepsilon W_g \]

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\[ C_{g-ch} = \frac{T_{ox}/\varepsilon_{ox} + T_{well}/2\varepsilon_{well} + (q^2/\text{well state density})}{L_g W_g} \]

\[ v \propto \left( \text{voltage division ratio between the above three capacitors} \right)^{-1/2} \]

\[ R_{DS} \approx \frac{L_g}{(W_g v \varepsilon)} \]

\[ R_S = R_D = \frac{\rho_{\text{contact}}}{L_{S/D} W_g} \]
# FET Scaling Laws (these now broken)

![Diagram of FET with InAlAs barrier, source, drain, gate, channel barrier, and N+ regions.]

## FET Parameter Changes

<table>
<thead>
<tr>
<th>FET Parameter</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>gate length</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>current density (mA/mm)</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>transport mass</td>
<td>constant</td>
</tr>
<tr>
<td>2DEG electron density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>gate-channel capacitance density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>dielectric equivalent thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>channel thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>channel state density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>contact resistivities</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

*fringing capacitance does not scale → linewidths scale as (1 / bandwidth)*
FET Scaling Laws (these now broken)

Gate dielectric can't be much further scaled. Not in CMOS VLSI, not in mm-wave HEMTs

\[
g_m/W_g \text{ (mS/\mu m) hard to increase} \quad \rightarrow \quad C_{\text{end}}/g_m \text{ prevents } f_\tau \text{ scaling.}
\]

Shorter gate lengths degrade electrostatics
\[
\rightarrow \text{ reduced } g_m/G_{ds} \rightarrow \text{ reduced } f_{\text{max}}/f_\tau
\]
Why THz HEMTs no longer scale

HEMTs: gate barrier also lies under S/D contacts → high S/D access resistance

As gate length is scaled, gate barrier must be thinned for high $g_m$, low $G_{ds}$.
HEMTs: High gate leakage when gate barrier is thinned → cannot thin barrier
Towards at 2.5 THz HEMT

First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process

Xiaobing Mei, et al, IEEE EDL, April 2015 (Northrop-Grumman)

FET scaling laws; 2:1 higher bandwidth

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>gate length</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>current density (mA/mm), g_m (mS/mm)</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>transport mass</td>
<td>constant</td>
</tr>
<tr>
<td>gate-channel capacitance density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>contact resistivities</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

Need thinner dielectrics, better contacts
Record III-V MOS

S. Lee et al., VLSI 2014

- $L_g \approx 25$ nm
- 2.7 nm InAs channel (strained)
- 2.5 nm ZrO$_2$
- 1 nm Al$_2$O$_3$N$_x$

Vertical Spacer

N+ S/D

$g_m = 25$ nm

SS $\approx 72$ mV/dec.

SS $\approx 77$ mV/dec.

$I_{on} = 500 \mu{A/\mu{m}}$ at $I_{off} = 100$ nA/\mu{m}

and $V_D = 0.5$ V

$V_{DS} = 0.5$ V

$I_{off} = 100$ nA/\mu{m}

$V_D$ = best UTB SOI silicon
Excellent III-V gate dielectrics

$\text{SS}_{\text{min}} \sim 61 \text{ mV/dec.}$

$\text{at } V_{DS} = 0.1 \text{ V}$

$\text{SS}_{\text{min}} \sim 63 \text{ mV/dec.}$

$\text{at } V_{DS} = 0.5 \text{ V}$

$2.5 \text{ nm ZrO}_2$

$1 \text{ nm Al}_2\text{O}_3$

$2.5 \text{ nm InAs}$

61 mV/dec Subthreshold swing at $V_{DS} = 0.1$ V

Negligible hysteresis
III-V MOS
@ $L_g = ???$

Huang et al.,
2015 DRC
Image courtesy of S. Kraemer (UCSB)
Towards at 2.5 THz HEMT

VLSI III-V MOS

<table>
<thead>
<tr>
<th>Material</th>
<th>Thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N+InGaAs</td>
<td>50</td>
</tr>
<tr>
<td>N+InP</td>
<td>10</td>
</tr>
<tr>
<td>Doping-graded InP</td>
<td>8</td>
</tr>
<tr>
<td>U.I.D. InP spacer</td>
<td>0.5</td>
</tr>
<tr>
<td>InP spacer</td>
<td>8</td>
</tr>
<tr>
<td>N+InP</td>
<td>0.5</td>
</tr>
<tr>
<td>1.5 nm InGaAs</td>
<td></td>
</tr>
<tr>
<td>1 nm InAs</td>
<td></td>
</tr>
<tr>
<td>5 nm InAlAs U.I.D. spacer</td>
<td></td>
</tr>
<tr>
<td>2 nm 1E19 cm⁻³ N+InAlAs</td>
<td></td>
</tr>
<tr>
<td>100 nm InAlAs U.I.D. buffer</td>
<td></td>
</tr>
<tr>
<td>250 nm 1E17 cm⁻³ P-InAlAs</td>
<td></td>
</tr>
<tr>
<td>50 nm InAlAs U.I.D. buffer</td>
<td></td>
</tr>
<tr>
<td>S.l. InP substrate</td>
<td></td>
</tr>
</tbody>
</table>

THz III-V MOS

<table>
<thead>
<tr>
<th>Material</th>
<th>VGS (V)</th>
<th>ID,</th>
<th>IG</th>
<th>(mA/mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1 V</td>
<td>0.2 0.4 0.6 0.8 1.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.5 V</td>
<td>0.2 0.4 0.6 0.8 1.0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

C. Y. Huang et al., DRC 2015

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>gate length</td>
<td>36</td>
</tr>
<tr>
<td>EOT</td>
<td>0.8</td>
</tr>
<tr>
<td>well thickness</td>
<td>5.6</td>
</tr>
<tr>
<td>effective mass</td>
<td>0.05</td>
</tr>
<tr>
<td>effective mass</td>
<td>0.08</td>
</tr>
<tr>
<td>effective mass</td>
<td>0.08</td>
</tr>
<tr>
<td># bands</td>
<td>1</td>
</tr>
<tr>
<td>S/D resistivity</td>
<td>150</td>
</tr>
<tr>
<td>extrinsic $g_m$</td>
<td>2.5</td>
</tr>
<tr>
<td>on-current</td>
<td>0.55</td>
</tr>
<tr>
<td>$f_T$</td>
<td>0.70</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>0.81</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>1.4</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>2.0</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>2.7</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>1.4</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>2.0</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>2.7</td>
</tr>
</tbody>
</table>

$V_{ds} = 0.1$ to $0.7$ V
$0.2$ V increment

SS ~ 107.5 mV at $V_{ds}=0.5$ V
SS ~ 98.6 mV at $V_{ds}=0.1$ V
mm-wave measurements
On-Wafer Network Analysis: 750+ GHz

• Agilent, Rhode/Schwarz network analyzer,

• *Oleson Microwave Lab or Virginia Diodes* frequency extenders

• micro-coax wafer probes with waveguide connections
  GGB Industries,
  Cascade Microtech
  University of Virginia.

• Internal bias Tee’s in probes

• Mostly on-wafer calibration standards.
On-Wafer Through-Reflect-Line (TRL) Calibration

Through line should be long for large probe separation. Minimizes probe-probe coupling. Measurements normalized to the line characteristic impedance.

Either open or short needed. Standards need not be accurate. "Open" must have $\Gamma$ closer to that of open than that of short. Ports 1 & 2 must be symmetric.

$\Delta L = 90$ deg @ center frequency. $\lambda/8 < \Delta L < 3\lambda/8$

Please see also: http://www.ece.ucsb.edu/Faculty/rodwell/publications_and_presentations/publications/204vg.ppt
On-Wafer Line Reflect Linie Calibration

Extended Reference planes
transistors placed at center of long on-wafer line
LRL standards placed on wafer
large probe separation → probe coupling reduced
still should use the best-shielded probes available

Problem: substrate mode coupling
method will FAIL if lines couple to substrate modes
→ method works very poorly with CPW lines
need on wafer thin-film microstrip lines

Note that calibration is to line Zo; line Zo is complex at lower frequencies, and must be determined.
Difficulties with >100 GHz On-Wafer Calibration

Data on two layouts of 65 nm MOSFET

Measured Y-parameters correlate reasonably with expected device model.

Small errors in measured 2-port parameters result in large changes in Unilateral gain and Rollet's stability factor; neither measurement is credible.

$Y_{12}$ appears to be the key problem.

IC $S_{ij}$ measurements are fine. Transistor $f_{\text{max}}$ measurements are hard.
Packaging and antennas
The Antenna Feed Loss Problem

array elements are many $\lambda$ long
overall array can be very big
$\rightarrow$ **high feed line losses**

One solution: waveguide-fed arrays of slots

Use to feed array tile: overall array needs steering
Using lenses to reduce feed loss

Lenses on individual array elements.

...or on the overall array.

Here the challenge is maintaining constant beamwidth over wide steering angles.
mm-wave interfaces: packaging

Wire-bonds:
With care, >60GHz can be coupled over wire-bonds. Coupling of multiple lines remains problematic.

Flip-chip bonds
Standard C4 bonds very capacitive; tuning OK @ 60GHz. Possibly higher. Option: more highly scaled bonds. Must contact vendors. Heat removal problematic in flip-chip ICs

Flexible polyimide interconnect substrate
Used in Cascade micotech multi-signal probes, in some 60GHz products. Ground integrity, low inductance mm-wave connections. Must identify vendor.

mm-wave interfaces: packaging

Through-silicon vias for RF grounding (TowerJazz, also IBM/GF)
very low ground inductance
low losses, low crosstalk in mm-wave IC-package connections

RF Ground Solutions

• Deep Silicon Vias
  • Extremely “localized” grounding. DSVs can be placed within several μms of active devices.
  • <5pH/via. < 50 W/via
  • In production now

• Through-Silicon Vias
  • Through-Silicon Vias for low inductance / low resistance emitter ground leads
  • 1000 μm² Pad can produce 22pH inductance to ground with less than 1W/via
  • In prototype now
mm-wave IC Design
Reactively-Tuned IC Design: Concepts
What's the most gain we can get? Do we care?


\[ G_{ma} = \frac{S_{21}}{S_{12}} \cdot \left( K - \sqrt{K^2 - 1} \right) \]

where \( K = \frac{1 - \|S_{11}\|^2 - \|S_{22}\|^2 + \|S_{11}S_{22} - S_{12}S_{21}\|^2}{2 \cdot \|S_{12}S_{21}\|} \) (Rollet stability factor).


\[ G_{ms} = \frac{S_{21}}{S_{12}} \]

Unilateral gain: lossless feedback until \( S_{12} = 0 \), then match

\[ U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{21}G_{12})} \]

Singhakowinta's gain:

appropriate lossless reactive feedback, match

\[ G_{max,s} = (2U - 1) + 2U^{1/2}(U - 1)^{1/2} \]

Highest feasible gain given unconditional stability

---


What's the most gain we can get? Do we care?

Low-noise amplifiers
designed for low noise figure, fairly high IP3

Power amplifiers
designed for high Psat, PAE, sufficiently low IM3

IF amplifiers
designed for low noise figure, high IP3.

Practical amplifiers are rarely designed for highest gain.

Real-world relevance of $G_{ma}$, $G_{ms}$, $G_{max}$, is not clear.

Practical designs would benefit from new theory
Quantities similar to $G_{ma}$, $G_{ms}$, $G_{max}$, above
But under constraints of high-power or low-noise tuning.
I know of no such published work.
RF-IC Design: Simple & Well-Known Procedures

1: (over)stabilize at the design frequency guided by stability circles

2: Tune input for $F_{\text{min}}$ (LNAs) or output for $P_{\text{sat}}$ (PAs)

3: Tune remaining port for maximum gain

4: Add out-of-band stabilization.

There are many ways to tune port impedances: microstrip lines, MIM capacitors, transformers. Choice guided by tuning losses. No particular preferences.

For BJT’s, MAG/MSG usually highest for common-base.

Common-base gain is however reduced by:
- base (layout) inductance
- emitter-collector layout capacitance.
Low-Noise Amplifier Design

Inductive emitter/source degeneration
simultaneous S11 and noise match
reduces gain, improves IP3

Additional in-band stabilization (output port) as needed
Input tuning for $F_{\text{min}}$
Output match
Out-of-band stabilization
For maximum saturated output power, & maximum efficiency, device intrinsic output must see optimum loadline set by:

\[ P_{\text{max}} = \frac{1}{8}(V_{\text{max}} - V_{\text{min}})I_{\text{max}} \]

breakdown, maximum current, maximum power density.

Parasitic C's and R's represented by external elements...
PAs with corporate combining

34 GHz InP HBT power amplifier - J. Hacker Teledyne

W-band InP HBT power amplifier - UCSB

34 GHz InP HBT power amplifier - J. Hacker Teledyne
The equivalent circuit: a multi-section transmission-line transformer. Shunt elements (inductors, capacitors) can also be added. Line parameters are adjusted to reach $Z_{l,\text{opt}}$ and to match input.

CAD approach:
all similar lines defined by shared variables, simultaneously adjusted
mm-wave IC Interconnects
Transmission Lines

A pair of wires with *regular spacing, dielectric loading* along the length.

These have inductance per unit length and capacitance per unit length.

Forward and reverse waves propagate.

Reflections will occur if lines are not terminated in $Z_0$. 
Transmission Lines for On-Wafer Wiring

- **microstrip line**
  - Geometry: W
  - Voltages: 0V, +V
  - Currents: I

- **coplanar waveguide**
  - Geometry: W+2S, W
  - Voltages: 0V, 0V
  - Currents: I/2, I, I/2
Skin loss

Skin depth $\delta = \sqrt{\frac{2}{\omega \mu \sigma}}$

Gold: $\delta \approx 200 \text{ nm @ 100GHz}$, $640 \text{ nm @ 10 GHz}$

Series resistance per unit length:

$$R_{\text{series}} / L \approx \frac{1}{\delta \sigma} \frac{1}{W} + \frac{1}{\delta \sigma} \frac{1}{W + 2H}$$

Attenuation per unit distance

$$\alpha \approx \frac{R_{\text{series}} / L}{2Z_0} \propto \sqrt{f}$$

Exponential signal decay

$$V(z) = V_o \exp(-\alpha z) \exp(-j2\pi z / \lambda_g)$$
In dielectric: waves of form $\vec{E}_0 e^{j\omega t} e^{\pm jk_x x} e^{\pm jk_y y} e^{\pm jk_z z}$

$$k_x^2 + k_y^2 + k_z^2 = k^2 = \varepsilon_r \omega^2 / c^2 = (2\pi / \lambda_d)^2$$

Waves can propagate *laterally* on transmission-line:

$k_y = 0$ and $k_x = n\pi / W$ for $n = 0, 1, 2, ...$

$\rightarrow k_z^2 = \varepsilon_r \omega^2 / c^2 - \left( n\pi / W \right)^2$
Lateral Modes (2)

\[ k_z^2 = \varepsilon_r \omega^2 / c^2 - (n\pi / W)^2 \]

1) Multi-mode propagation if \( W > \lambda_d / 2 \).

\[ \beta_z = \sqrt{\varepsilon_r \omega^2 / c^2 - (n\pi / W)^2} \]

2) Evanescent propagation \( e^{-\alpha_z z} \) if \( W < \lambda_d / 2 \):

\[ \alpha_z = \sqrt{(n\pi / W)^2 - \varepsilon_r \omega^2 / c^2} \]
Lateral Modes (3) → Junction Parasitics

Evanescent propagation \( e^{-\alpha_z z} \) if \( W \approx \lambda_d/2 \):

Reactive power in evanescent modes → junction parasitics

ADS library junction models, or electromagnetic simulation.

Lessons:

- Lines must be much narrower than a half-wavelength.
- Must model junction parasitics.
Substrate Modes

Substrate with top, bottom metal surfaces
→ modes with \( h = \frac{\lambda_d}{2}, \lambda_d, 3\frac{\lambda_d}{2} \ldots \)

Substrate with no top metal → tranverse \( E \)-mode;
strongly confined as \( \frac{\lambda_d}{4} \rightarrow T \); weakly confined at low frequencies.
These dielectric slab modes can propagate in $x$ and in $z$.

Nonzero mode coupling ("radiation") loss at all frequencies.

Very strong mode coupling when $h \geq \frac{\lambda_d}{4}$
Modes couple strongly when $k_{y,CPW} = k_{y,\text{substrate mode}}$

Given thick substrate, $H \gg \lambda_d$:

- mode coupling loss, dB/mm $\propto (\text{line transvers e dimensions})^2 \cdot$ frequency $^2$
- "radiation loss"
Transmission lines: the problem

If we use narrow lines and thin substrates then skin-effect losses will be large.

If we use wide lines and thick substrates then lateral modes and substrate radiation will be major problems.
III-V MIMIC Interconnects -- Classic Substrate Microstrip

Thick Substrate → low skin loss

Zero ground inductance in package

No ground plane breaks in IC

High via inductance

TM substrate mode coupling

12 pH for 100 μm substrate -- 7.5 Ω @ 100 GHz

Strong coupling when substrate approaches ~λd/4 thickness

lines must be widely spaced

ground vias must be widely spaced

all factors require very thin substrates for >100 GHz ICs → lapping to ~50 μm substrate thickness typical for 100+ GHz
Parasitic slot mode

- V 0V +V

Parasitic microstrip mode

+V +V +V 0V

Hard to ground IC to package

Repairing ground plane with ground straps is effective only in simple ICs. In more complex CPW ICs, ground plane rapidly vanishes → common-lead inductance → strong circuit-circuit coupling.

ground plane breaks → loss of ground integrity

substrate mode coupling or substrate losses

poor ground integrity

loss of impedance control

ground bounce

coupling, EMI, oscillation

40 Gb/s differential TWA modulator driver note CPW lines, fragmented ground plane

35 GHz master-slave latch in CPW note fragmented ground plane

175 GHz tuned amplifier in CPW note fragmented ground plane

III-V: semi-insulating substrate → substrate mode coupling

Silicon conducting substrate → substrate conductivity losses

No ground vias
No need (?) to thin substrate

Coplanar Waveguide

No need to thin substrate

Hard to ground IC to package
If It Has Breaks, It Is Not A Ground Plane!

coupling / EMI due to poor ground system integrity is common in high-frequency systems whether on PC boards ...or on ICs.
No clean ground return? → interconnects hard to model

35 GHz static divider
interconnects have no clear local ground return
interconnect inductance is non-local
interconnect inductance has no compact model

8 GHz clock-rate delta-sigma ADC
thin-film microstrip wiring
every interconnect can be modeled as microstrip
some interconnects are terminated in their Zo
some interconnects are not terminated
...but ALL are precisely modeled
III-V MIMIC Interconnects -- Thin-Film Microstrip

- Narrow line spacing → IC density
  - Happy face

- No substrate radiation, no substrate losses
  - Happy face

- Fewer breaks in ground plane than CPW
  - Happy face

- ...But ground breaks at device placements
  - Sad face

- Still have problem with package grounding
  - Sad face

- ...Need to flip-chip bond

- Thin dielectrics → narrow lines
  - Sad face
  - High line losses
  - Low current capability
  - No high-$Z_0$ lines

\[
Z_0 \sim \frac{\eta_0}{\varepsilon_r^{1/2}} \left( \frac{H}{W + H} \right)
\]

InP 34 GHz PA
(Jon Hacker, Teledyne)
III-V MIMIC Interconnects -- Inverted Thin-Film Microstrip

- narrow line spacing → IC density

- Some substrate radiation / substrate losses

- No breaks in ground plane

- ... no ground breaks at device placements

- still have problem with package grounding

- ... need to flip-chip bond

- thin dielectrics → narrow lines
  → high line losses
  → low current capability
  → no high-\(Z_o\) lines

- InP 150 GHz master-slave latch

- InP 8 GHz clock rate delta-sigma ADC
VLSI mm-wave interconnects with ground integrity

- narrow line spacing → IC density
- no substrate radiation, no substrate losses
- negligible breaks in ground plane
- negligible ground breaks @ device placements
- still have problem with package grounding
  ...need to flip-chip bond
- thin dielectrics → narrow lines
  → high line losses
  → low current capability
  → no high-$Z_0$ lines

Also:
Ground plane at *intermediate level* permits critical signal paths to cross supply lines, or other interconnects without coupling. (critical signal line is placed above ground, other lines and supplies are placed below ground)
Modeling Interconnects, Passives in Tuned IC's

Interconnects are tuning elements

Narrow bandwidths → precision is critical

Initial IC simulation uses CAD-systems' library of passive element models.

Second design cycle: 2.5-Dimensional electromagnetic simulation of:
lines, junctions, stubs, capacitors, resistors, pads.

Third design cycle: 2.5-D simulation of entire IC wiring (if possible);
otherwise, of large blocks (gain stages)

150-200 GHz HBT amplifier, Urteaga et al, IEEE JSSCC, Sept. 2003

185GHz HBT amplifier, Urteaga et al, IEEE IMS, May. 2001

ICs in Thin-Film (Not Inverted) Microstrip

*Note breaks in ground plane at transistors, resistors, capacitors*
ICs in Thin-Film (Not Inverted) Microstrip

Note breaks in ground plane at transistors, resistors, capacitors
ICs in Thin-Film Inverted Microstrip

100 GHz differential TASTIS Amp.  512nm InP HBT
Power supply problems

- Local resonances between bypass cap and supply interconnects
- Global LC standing-wave resonances on supply bus
- Detuning of individual stages
- Coupling, feedback via supply → oscillation, loss of path isolation
Power supply problems

The supply impedance will detune individual stages.
Power supply problems

Model the supply in all simulations. "If it is on the {IC, PCB, probe station}, put it in the simulation."

Here, the supply is terminated by 50 Ohms through a bias T. This avoids resonances.

More generally, we must simulate system for wide range of external supply impedance.
Transmission-lines in 500+ GHz ICs

Inverted microstrip: the problem is ground via inductance

(metal 3 ground plane above)
Transmission-lines in 500+ GHz ICs

Grounded CPW: lower ground inductance, metal 3 ground plane suppresses ground bounce

J. Hacker, Teledyne IMS 2013

(metal 3 ground plane above)
Differential mm-wave stages

Common-emitter
M. Seo, Teledyne

Virtual ground → avoids ground via inductance ✓
Avoids power-supply coupling ✓
Potential problems with common mode ✗

Common-base
M. Seo, 2013 IMS
In all amplifiers, stability must be ensured from DC-$f_{\text{max}}$. Differential & common-mode stability must be ensured from DC-$f_{\text{max}}$. Simple LNA inductive tuning is, for example, problematic.
No common-mode instability problem.
Power-supply is virtual ground.
No supply detuning of output network
Improved power-supply isolation (oscillation, unwanted signal coupling)
20+ GHz
digital &
mixed-signal
design
longer interconnects:  
lines terminated in $Z_0$ → no reflections.

Shorter interconnects:  
lines NOT terminated in $Z_0$ .  
But they are *still* transmission-lines.  
Ignore their effect at your peril !

If length << wavelength,  
or line delay<<risetime,  
short interconnects behave  
as lumped $L$ and $C$.  

Modeling: 2.5D, library Tline, or $L$-$C$
Design Flow: Digital & Mixed-Signal IC's

All interconnects: thin-film microstrip environment. Continuous ground on one plane.

2.5-D simulations run on representative lines. various widths, various planes same reference (ground) plane.

Simulation data manually fit to CAD line model effective substrate $\varepsilon_r$, effective line-ground spacing.

Width, length, substrate of each line entered on CAD schematic. rapid data entry, rapid simulation.

Resistors and capacitors: 2.5-D simulation $\rightarrow$ RLC fit RLC model used in simulation.
High Speed ECL Design

Followers associated with inputs, not outputs
Emitters never drive long wires.
(Instability with capacitive load)

Double termination for least ringing, send or receive termination for moderate-length lines, high-Z loading saves power but kills speed.

Current mirror biasing is more compact.
Mirror capacitance → ringing, instability.
Resistors provide follower damping.
High Speed ECL Design

Layout: short signal paths at gate centers, bias sources surround core. Inverted thin film microstrip wiring.

Key: transistors in on-state operate at Kirk limited-current. → minimizes $C_{cb}/I_c$ delay.

Key: transistors designed for minimum ECL gate delay*, not peak ($f_r$, $f_{max}$).
*hand expression, charge-control analysis

Example: 8:1 205 GHz static divider in 256 nm InP HBT.

205 GHz divider, Griffith et al, IEEE CSIC, Oct. 2010
Differential stages: schematic vs. floorplan
Example: 40 GS/s S/H clock buffer

$I_{tail} = 6\ mA$

$I_{tail} = 12\ mA$
Example: 40 GS/s S/H clock buffer
Example: 40 GS/s S/H clock buffer
20GHz Op-Amps for Linear 2 GHz Amplification

Even for 2 GHz operation, loop bandwidths must be 20-40 GHz. Need very fast transistors.

Reduce distortion with strong negative feedback.

Physically small feedback loop; bias components surround active core.
86 GHz
Power Amplifier
mm-Wave Power Amplifier: **Challenges**

- **needed:** High power / High efficiency / Small die area (low cost)

**Extensive power combining**

\[
PAE = \eta_{\text{drain/collector}} \left(1 - \frac{1}{\text{Gain}}\right) \cdot \eta_{\text{power-combiner}}
\]

**Compact power-combining**

- Class E/D/F are poor @ mm-wave
  - insufficient \( f_{\text{max}} \)
  - high losses in harmonic terminations

**Efficient power-combining**

**Goal:** efficient, compact mm-wave power-combiners
Parallel Power-Combining

Output power: $P_{\text{OUT}} = N \times V \times I$
Parallel connection increases $P_{\text{OUT}}$ ✓

Load Impedance: $Z_{\text{OPT}} = V / (N \times I)$
Parallel connection decreases $Z_{\text{opt}}$ ✗

High $P_{\text{OUT}}$ → Low $Z_{\text{opt}}$

Needs impedance transformation: lumped lines, Wilkinson, ...

High insertion loss ✗
Small bandwidth
Large die area
Series Power-Combining & Stacks

Parallel connections: $I_{out} = N \times I$
Series connections: $V_{out} = N \times V$

Output power: $P_{out} = N^2 \times V \times I$
Load impedance: $Z_{opt} = V/I$
Small or zero power-combining losses ✔
Small die area ✔
How do we drive the gates?

Local voltage feedback:
drives gates, sets voltage distribution

Design challenge:
need uniform RF voltage distribution
need ~unity RF current gain per element
...needed for simultaneous compression of all FETs.

Shifrin et al., 1992 IEEE-IMS; Rodwell et al., U.S. Patent 5,945,879, 1999; Pornpromlikit et al., 2011 CSICS
Two separate transmission lines ($m_3$-$m_2$, $m_2$-$m_1$)

$\rightarrow$ E, H fields between $m_3$ and $m_1$ perfectly shielded
Sub-$\lambda/4$ Baluns for Series Combining

Balun combiner:
- 2:1 series connection
- each source sees 25 $\Omega$
- $\rightarrow$ 4:1 increased $P_{out}$

Standard $\lambda/4$ balun:
- long lines
- $\rightarrow$ high losses $\times$
- $\rightarrow$ large die $\times$

Sub-$\lambda/4$ balun:
- stub $\rightarrow$ inductive tunes transistor $C_{out}$ $\checkmark$
- short lines $\rightarrow$ low losses $\checkmark$
- short lines $\rightarrow$ small die $\checkmark$

Park et al., 2013 CSICS, 2014 IEEE-IMS
Baluns in **Real ICs**

1) \( M_1 \) as a GND
2) Slot-type transmission lines (\( M_1-M_2 \)), AC short (2 pF MIM)
3) Microstrip line (\( M_2-M_3 \)), E-field shielding **NOT** negligible
4) **Sidewalls** between \( M_3-M_1 \) (Faraday cages), \( \lambda/16 \) length
Two-Stage PA IC Test Results (86GHz)

Gain: **17.5 dB**

$P_{SAT}$: $>200$ mW @ 3.0 V

PAE: $>30\%$

**Power density (power/die area)**

- $= 307$ mW/mm$^2$ (including RF pads)
- $= 927$ mW/mm$^2$ (core area)

[H. Park et al, CSICS 2013]

30% PAE W-Band InP Power Amplifiers Using Sub-Quarter-Wavelength Baluns for Series-Connected Power-Combining
4:1 series-connected 81GHz power amplifier

17 dB Gain
470 mW $P_{\text{sat}}$
23% PAE
Teledyne 250 nm InP HBT
2 stages, 1.0 mm$^2$ (incl pads)

Park et al., 2014 IEEE-IMS
IC example:
220 GHz
power amplifier
Millimeter-wave imaging

10,000-pixel, 94GHz imaging array → 10,000 elements

Demonstrated:
SiGe (UCSD/Rebeiz)
~1.3kW: 10,000 elements

Lower-power designs:
InP, CMOS, SiGe
(UCSB, UCSD, Virginia Poly.)

235 GHz video-rate synthetic aperture radar

1 transmitter, 1 receiver
100,000 pixels
20 Hz refresh rate
5 cm resolution @ 1km
50 Watt transmitter
(tube, solid-state driver)
90 mW, 220 GHz Power Amplifier

Reed (UCSB) and Griffith (Teledyne): CSIC 2012
Teledyne 250 nm InP HBT

- Amplifier gains (dB)
- Frequency (GHz)
- 3dB bandwidth = 240GHz
- S_{21,mid-band} = 15.4dB
- S_{11}
- S_{22}

8-cell, 2-stage PA

P_{DC} = 4.46W

- P_{out}, mW
- P_{in}, mW
- 220GHz operation

8-cell, 2-stage PA

active area, 1.02 x 0.85 mm
die: 2.42 x 1.22 mm
214 GHz InP HBT Power Amplifier

Gain: 25dB S21 Gain at 220GHz
Saturated output power: 164mW at 214GHz
Output Power Density: 0.43 W/mm
PAE: 2.4%

Technology: 250 nm InP HBT

(no die photo) 2.5mm x 2.1 mm

Reed et al, 2014 CSICS http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6659187&tag=1
214 GHz 180mW Power Amplifier (330 mW design)

Reed, Griffith CSICS2013
Teledyne 250 nm InP HBT
220 GHz power amplifiers; 256nm InP HBT
ICs in Thin-Film (Not Inverted) Microstrip

*Note breaks in ground plane at transistors, resistors, capacitors*
220 GHz measurement

- Small Signal Measurement
  - VNA with 140-220 and 206-340 GHz frequency extender heads
  - LRRM Probe-tip Calibration

- Power Sweep Measurement
  - 220 GHz frequency multiplier chains and sub-mm wave power meter
  - Insertion Loss Calibration
  - Forced Air cooling
Power combined modules

Summary of state-of-the-art WR04-band SSPAs

- Nuvotronics
- Raytheon-RRI

Blue = Teledyne 250nm InP HBT

- 16-Cell SSPA
- 8-Cell SSPA
- 4-Cell SSPA
- NGAS 1-chip module
- NGAS 4-chip module
- 16-Cell, Gen-2
mm-Wave power
Teledyne: 1.9 mW, 585 GHz Power Amplifier

M. Seo et al., Teledyne Scientific: IMS2013

- 12-Stage Common-base
- 2.8 dBm $P_{\text{sat}}$
- >20 dB gain up to 620 GHz

**What limits output power in sub-mm-wave amplifiers?**
Sub-mm-wave PAs: need more current!

3 μm max emitter length (> 1 THz $f_{\text{max}}$)
2 mA/μm max current density
$I_{\text{max}} = 6$ mA

Maximum 3 Volt p-p output

Load: 3V/6mA = 500 Ω

**Combiner cannot provide 500 Ω loading**
Multi-finger HBTs: more current, lower $f_{\text{max}}$

More current → lower cell load resistance

**Reduced $f_{\text{max}}$, reduced RF gain:**
- common-lead inductance $\rightarrow Z_{12}$
- feedback capacitance $\rightarrow Y_{12}$
- phase imbalance between fingers.

**Worse at higher frequencies:**
- less tolerant of cell parasitics
- less current per cell
- higher required load resistance
Can optimum load be reached?

- emitter-collector capacitance
- unequal emitter inductances
Sub-mm-wave transistors: need more current

**InP HBTs:**
- thinner collector → more current
- hotter → improve heat-sinking
- or: longer emitters → thicker base metal

**GaN HEMTs:**
- much higher voltage
- 100+ GHz: large multi-finger FETs not feasible

*Need high current to exploit high voltage.*

**Example:**
- 2mA/μm, 100 μm max gate width, 50 Volts
- 200mA maximum current
- 50 Volts/200mA = 250 Ω load → unrealizable.

*Need more mA/μm or longer fingers*
50-500GHz Wireless
IC example:
150 GHz CMOS amplifier
3-stage 150-GHz Amplifier; IBM 65 nm CMOS


Acknowledgement:
IBM

- 153 GHz
- 158.4 GHz

Power Added Efficiency (%)

Output power (dBm), Gain (dB)

Gain

P_{out}

153.0GHz
158.4GHz

140 150 160 170 180 190 200
Frequency (GHz)

S21 (measured using power sensor)

S21(meas)
S21(sim)
S11 (meas)
S11 (sim)
S22 (meas)
S22 (sim)

Frequency (GHz)

S21
S11 (meas)
S11 (sim)
S22

Stability factor (K)

K-factor

0 1 2 3

140 160 180
Frequency (GHz)

S-parameter (dB)

-20 -15 -10 -5 0 5

Input power (dBm)

Output power (dBm)

PAE

153 GHz
153 GHz
158.4 GHz
158.4 GHz
153 GHz
158.4 GHz

153.0GHz
158.4GHz

Dummy-prefilled microstrip lines
IC example: 140 GHz spatial multiplexing
Massive Spatial Multiplexing

Two applications:

Spatially multiplexed networks
multiple independent beams
carrying independent data
\rightarrow spectral re-use for massive capacity

mm-wave line-of-sight MIMO
spatial multiplexing
for increased capacity

These use similar signal processing hardware
Arrays for **single**-beam links

Single-beam arrays:  
steerable, high gain, for mm-wave links.

Simple hardware:  
one RF port for IC, one phase-shifter for each element
Multi-beam links: hardware design

multiple independent beams
each carrying different data
each independently aimed
# beams = # array elements

Hardware: multi-beam phased array ICs
Multi-Beam Links: Analog Beamformer Matrix

I/Q matrix at baseband

varying coefficients
→ track/aim beams

Designs: March tapeout
GF (ex IBM) 45nm SOI
16 beams: 32 x 32 matrix
1024 matrix elements
area: 2.25 mm²
power: 2.25W
bandwidth: ~5 GHz?
aggregate ~160 Gb/s.

Also for tapeout
140 GHz front-ends for these
Multi-Beam Links: Analog Beamformer Matrix

\[ \pm g_m \]
\[ \pm 2g_m \]
\[ \pm 4g_m \]
\[ \pm 8g_m \]
Multi-Beam Links: Analog Beamformer Matrix

I/Q matrix at baseband

**varying coefficients**
→ track/aim beams

**Designs: March tapeout**
GF (ex IBM) 45nm SOI
16 beams: 32 x 32 matrix
1024 matrix elements
area: 2.25 mm²
power: 2.25 W
bandwidth: ~5 GHz ?
aggregate ~160 Gb/s.

**Also for tapeout**
140 GHz front-ends for these later: RF for 38GHz, 60 GHz
140 GHz MIMO receiver front-end

Size: 1075 x 1760 um²

Single-channel layout

RF Ch.1

IF

RF Ch.2

IF

RF Ch.3

IF

RF Ch.4

IF

0°

0°

0°

0°

LO

90° hybrid

Power div.
## Single-ended vs differential

<table>
<thead>
<tr>
<th></th>
<th>Single-ended</th>
<th>Differential</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gain</strong></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>Power consumption</strong></td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td><strong>Design complexity</strong></td>
<td>Low</td>
<td>High (Balun is required)</td>
</tr>
<tr>
<td><strong>Isolation (S12) &amp; Stability</strong></td>
<td>Low</td>
<td>High (C\text{gd} cancellation)</td>
</tr>
<tr>
<td><strong>Power supply (VDD &amp; VSS) immunity</strong></td>
<td>Poor</td>
<td>Good</td>
</tr>
</tbody>
</table>

Power supply immunity is critical $\rightarrow$ differential structure
Low noise amplifier

LNA design:
3-stage differential CS amplifier
$C_{gd}$ cancellation
Transformers for matching networks and sing.-to-diff.
SGF vs PGF

Simulation results includes BSIM model and PEX results (PEX → capacitance and resistance due to PC, CA and M1)

*PC: poly, CA: connection between poly and metal 1, M1: metal
FET footprint

Series gate feeding

Parallel gate feeding
FET footprint - PGF

- PGF and SGF have similar performances (MSG, NF)
- SGF is hard to extract the inductance of the gate feeding line
- Source can directly connect to ground (M1 is the ground plane)
FET modeling

Parallel Gate Feeding

Transistor modeling:
BSIM + PEX + EM simulation (BSIM & PEX from the foundry)
FET differential pair layout

C_{gd} cancellation – better isolation & gain
Matching networks

For matching:
Optimize transistor size & transformer diameter

Center-tapped transformer for DC biasing (VDD, VGS)
LNA layout

Size: 315 x 170 um²
Gain & NF

Gain 19.2 dB (peak gain 20 dB @ 145 GHz)
NF: 5.2 dB
IIP3: -5.84 dBm, Input P1dB: -13.87 dBm
### Summary - LNA

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gain</strong></td>
<td><strong>19.2 dB (Peak 20 dB @ 145 GHz)</strong></td>
</tr>
<tr>
<td><strong>NF</strong></td>
<td><strong>5.2 dB</strong></td>
</tr>
<tr>
<td><strong>IIP3</strong></td>
<td><strong>-5.8 dBm</strong></td>
</tr>
<tr>
<td><strong>Input P1dB</strong></td>
<td><strong>-13.87 dBm</strong></td>
</tr>
<tr>
<td><strong>Power consumption</strong></td>
<td><strong>41 mA @ 1 V</strong></td>
</tr>
<tr>
<td><strong>Size</strong></td>
<td><strong>315 x 170 (\text{um}^2)</strong></td>
</tr>
</tbody>
</table>
Down-conversion mixer

Mixer design:
Single-balanced active I/Q mixer
CS buffer for testing (buffer gain ≈ 1)

Size: 140 x 230 \text{um}^2
Mixer core layout

IF output (C1)

LO + (LB)

LO – (LB)

M1 ground plane

RF input (LB)

FET

BEOL: M1-M2-M3-C1-C2-B1-B2-B3-UA-UB-LB
Four-channel receiver

LO distribution network:
Wilkinson power divider
Quadrature hybrid (I/Q generation)
Layout

Single-channel layout

Wilkinson power divider

Size: 1075 x 1760 \( \text{um}^2 \)
Conversion gain & NF (single-channel)

Gain 17 dB (single-channel IF_I output)
NF : 5.8 dB (dsb)
Linearity (single-channel)

RF @ 140 GHz with 10 MHz spacing
LO @ 139 GHz

IIP3: -10.7 dBm, Input P1dB: -18.74 dBm
### Summary - receiver

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gain</strong></td>
<td>17 dB (Single-channel IF_I output)</td>
</tr>
<tr>
<td><strong>NF</strong></td>
<td>5.8 dB</td>
</tr>
<tr>
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<td>-10.7 dBm</td>
</tr>
<tr>
<td><strong>Input P1dB</strong></td>
<td>-18.7 dBm</td>
</tr>
<tr>
<td><strong>Power consumption</strong></td>
<td>41 mA (LNA) + 2 mA (I/Q mixer)  + 14 mA (IF-I/Q buffers)  @ 1 V (Single-channel)</td>
</tr>
<tr>
<td><strong>Size</strong></td>
<td>1075 x 1760 um²</td>
</tr>
</tbody>
</table>
IC example:
94 GHz
low-power-array
Millimeter-wave imaging

10,000-pixel, 94GHz imaging array → 10,000 elements

Demonstrated: SiGe (UCSD/Rebeiz) 
~1.3kW: 10,000 elements

Lower-power designs: InP, CMOS, SiGe 
(UCSB, UCSD, Virginia Poly.)

System concept: Bruce Wallace DARPA. 1st ICs (SiGe) Rebeiz, UCSD.
Millimeter-wave imaging

10,000-pixel, 94GHz imaging array → 10,000 elements

Demonstrated:
SiGe (UCSD/Rebeiz)
~1.3kW: 10,000 elements

Lower-power designs:
InP, CMOS, SiGe
(UCSB, UCSD, Virginia Poly.)

100 pixel × 100 pixel image → 10,000 array elements.
~130 mW DC power per element → 1.3 kW system power requirement.
Problem: required size and weight of heat sink.
94 GHz low-power IC design: transistors

Teledyne: 130nm InP HBT: high-$f_{\text{max}}$ bias

Teledyne: 130nm InP HBT: low-power bias

At 1mW dissipation, $\sim$17 dB gain is feasible $\rightarrow$ low power ICs.

Teledyne: M. Urteaga et al: 2011 DRC

130nm $\times$ 3 $\mu$m emitter
94 GHz low-power IC design: transistors

RF: transistor must be sized to make impedance-matching possible

FETs & BJT:s: \( Z_{in} \approx R_{g/BB} + (j\omega C_{gs/be})^{-1} \approx (K/g_m) + (f_t/jf)(1/g_m) \propto 1/g_m \)

BJTs: \( g_m \approx I_E/26 \text{ mV} \).

FETs: \( g_m \approx I_S/300 \text{ mV} \).

→ low-power mm-wave ICs should use BJT:s
(ignores \( P_{sat}, \text{IP3 considerations} \))
Phased array

IC can transmit on vertical (V) or horizontal (H) polarizations (one at a time).
IC can receive on vertical (V) and horizontal (H) polarizations (simultaneously).
Each mode has phase-shifter, VGA.
Signal distribution on backplane.
InP IC: requires low-speed CMOS digital control IC.
Low-power, low-voltage mm-wave design

Extensive use of current mirrors, translinear techniques

Gain & switching

Low-power T/R switching

VGA / switch

Multiplier → mixer, modulator, phase-shifter
Low-power, low-voltage mm-wave design

Antenna switch

backplane T/R switch

PA & V/H switch

LNA

Rx on/off
Rx on/off
Rx on/off

~ λ/4

VCC

VCC

Input

Output

50 Ω @ Rx off
50 Ω @ Rx off
50 Ω @ Rx off

~ 1 mA

1 mA

1 mA

1 mA

Rx VGA 1st bias
Rx bias circuit

VGA 2nd stage

VGA 1st stage

50 Ω @ Tx off

Output

H_{Output}

H_{On}

6/0.13

V_{On}

12/0.13

V_{Output}

VCC

VCC

VCC

Input

Input

Input

Rx output
/Tx input

Tx on/off

Tx on/off

Tx on/off

TX

Rx

VCC

VCC

VCC

~ 1 mA

1 mA

1 mA

1 mA

Rx VGA

VGA 1st bias

Input

Input

Input

Rx on/off

Rx on/off

Rx on/off

Rx on/off

Phase-shifter and control circuits

Sub-quarter wavelength balun

\[ \lambda / 4 \text{ delay} \]

Input

Output

\[ I_{\text{out}} \]

\[ I_{b_{\text{out}}} \]

\[ I_{Q_{\text{out}}} \]

\[ Q_{\text{bias}} + Q_{\text{bias}} = 3.2 \text{ mA} \]

External Current DAC

\[ \text{W} \quad 2\text{W} \quad 4\text{W} \]

\[ Q_{\text{Ctrl}} \]

\[ I_{\text{Ctrl}} \]

\[ 2/0.13 \]

Matching

\[ I_{\text{bias}} + Q_{\text{bias}} = 3.2 \text{ mA} \]

760 um x 640 um
Phase-shifter measurement results (1 V)

Power consumption: 4.2 mA @ 1 V
Low-noise amplifier

- Noise matching for input
- Conjugate matching for inter-stage
- Gain matching for output
- Power consumption: 2 mA @ 1.5 V

660 um x 510 um
LNA Measurement results (1 V)

Power consumption: 2.0 mA @ 1 V
Gain: 16.3 dB @ 94 GHz (peak gain)
Noise measurement setup

**Calibration**

Noise Source (NSI-9095W) → -1 dB → W-band Amplifier → Mixer (LO @ 94 GHz) → NFA (N8972A)

**Measurement**

Noise Source (NSI-9095W) → -1 dB → DUT → W-band Amplifier → Mixer (LO @ 94 GHz) → NFA (N8972A)

Loss before the DUT: compensated using the NFA’s internal function therefore, measured gain should be subtracted by -1 dB
Transceiver measurement results

---

**Rx, 1 V**

- **S(2,1), V**
- **S(2,1), H**
- **S(1,1), V**
- **S(1,1), H**
- **S(2,2), V**
- **S(2,2), H**

**Frequency (GHz)**

- **Gain (dB)**
- **Output Power (dBm)**
- **Input Power (dBm)**

---

**Tx, 1.5 V**

- **S(2,1), V**
- **S(2,1), H**
- **S(1,1), V**
- **S(1,1), H**
- **S(2,2), V**
- **S(2,2), H**

**Frequency (GHz)**

- **Gain (dB)**
- **Output Power (dBm)**
- **Input Power (dBm)**
Receiver noise

![Graph showing the noise figure (NF) and S(2,1) measurements vs frequency. The graph includes data points for both measured and simulated NF values, as well as S(2,1) measurements using PNA and NFA.]
94 GHz transceiver: performance summary

<table>
<thead>
<tr>
<th></th>
<th>@Vcc=1.5V</th>
<th>@Vcc=1.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Amplifier + V/H SW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Power P3dB (dBm)</td>
<td>6.9</td>
<td>3.5</td>
</tr>
<tr>
<td>Power Gain @P3dB (dB)</td>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td>PAE (%)</td>
<td>17</td>
<td>12.7</td>
</tr>
<tr>
<td>Pdiss @ P3dB (mW)</td>
<td>27.2</td>
<td>16.9</td>
</tr>
<tr>
<td>Pdiss (small-signal) (mW)</td>
<td>22.5</td>
<td>16.4</td>
</tr>
<tr>
<td>Pdiss (core exclude bias ckt) (mW)</td>
<td>17.55</td>
<td>11.45</td>
</tr>
<tr>
<td>Size (exclude Pads) (µm)</td>
<td>475x475</td>
<td>475x475</td>
</tr>
<tr>
<td>Power Gain (Rx/Tx) (dB)</td>
<td>12.5/10.9</td>
<td>13.4/11.5</td>
</tr>
<tr>
<td>NF (max gain) (dB)</td>
<td>4.8/7.8</td>
<td>4.6/7.7</td>
</tr>
<tr>
<td>NF (max gain - 6dB) (dB)</td>
<td>7.1/9.4</td>
<td>6.6/9.3</td>
</tr>
<tr>
<td>Input P1dB (dBm)</td>
<td>-12.4/-9.6</td>
<td>-15.9/-15</td>
</tr>
<tr>
<td>OIP3 (dBm)</td>
<td>6.7/7.6</td>
<td>-1.8/-3</td>
</tr>
<tr>
<td>Pdiss (mW)</td>
<td>9</td>
<td>6.4</td>
</tr>
<tr>
<td>Pdiss (core exclude bias ckt) (mW)</td>
<td>6.9</td>
<td>4.6</td>
</tr>
<tr>
<td>Size (exclude Pads) (µm)</td>
<td>530*900</td>
<td>530*900</td>
</tr>
<tr>
<td>LNA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Gain (dB)</td>
<td>15.1</td>
<td>16.3</td>
</tr>
<tr>
<td>NF (dBm)</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Input P1dB (dBm)</td>
<td>-21.9</td>
<td>-24.5</td>
</tr>
<tr>
<td>OIP3 (dBm)</td>
<td>-1.7</td>
<td>-3</td>
</tr>
<tr>
<td>Pdiss (mW)</td>
<td>4.95</td>
<td>3.95</td>
</tr>
<tr>
<td>Pdiss (core exclude bias ckt) (mW)</td>
<td>3.5</td>
<td>2</td>
</tr>
<tr>
<td>Size (exclude Pads) (µm)</td>
<td>480*280</td>
<td>480*280</td>
</tr>
<tr>
<td>Phase Shifter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Gain (Rx/Tx) (dB)</td>
<td>-5±1.5</td>
<td>-5±1.5</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>14.9</td>
<td>14.6</td>
</tr>
<tr>
<td>Input P1dB (dBm)</td>
<td>9</td>
<td>6</td>
</tr>
<tr>
<td>OIP3 (dB)</td>
<td>10.9</td>
<td>2</td>
</tr>
<tr>
<td>Pdiss (mW)</td>
<td>6.5</td>
<td>4.2</td>
</tr>
<tr>
<td>Pdiss (core exclude bias ckt) (mW)</td>
<td>6.5</td>
<td>4.2</td>
</tr>
<tr>
<td>Size (exclude Pads) (µm)</td>
<td>660*340</td>
<td>660*340</td>
</tr>
<tr>
<td>SPDT Antenna T/Rx SW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Loss (dB)</td>
<td>2</td>
<td>1.8</td>
</tr>
<tr>
<td>Isolation (dB)</td>
<td>19.5</td>
<td>18.5</td>
</tr>
<tr>
<td>P1dB (dBm)</td>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td>Pdiss (mW)</td>
<td>6.8</td>
<td>4.8</td>
</tr>
<tr>
<td>Pdiss (core exclude bias ckt) (mW)</td>
<td>4.8</td>
<td>2.8</td>
</tr>
<tr>
<td>Size (exclude Pads) (µm)</td>
<td>200*680</td>
<td>200*680</td>
</tr>
<tr>
<td>Rx Channel</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Gain (dB)</td>
<td>21</td>
<td>22.7</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>8.5</td>
<td>8</td>
</tr>
<tr>
<td>Fractional BW (%)</td>
<td>7.6</td>
<td>7.5</td>
</tr>
<tr>
<td>Input P1dB (dBm)</td>
<td>-22.9</td>
<td>-27.9</td>
</tr>
<tr>
<td>OIP3 (dBm)</td>
<td>-16.3</td>
<td>-24.3</td>
</tr>
<tr>
<td>Pdiss (mW)</td>
<td>19.2</td>
<td>12.9</td>
</tr>
<tr>
<td>Pdiss (core exclude bias ckt) (mW)</td>
<td>17.25</td>
<td>11</td>
</tr>
<tr>
<td>Tx Channel</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Gain (dB)</td>
<td>22.2</td>
<td>22.4</td>
</tr>
<tr>
<td>Pout (P3dB) (dBm)</td>
<td>3.8</td>
<td>0.1</td>
</tr>
<tr>
<td>Fractional BW (%)</td>
<td>6.7</td>
<td>6.7</td>
</tr>
<tr>
<td>Output P1dB (dBm)</td>
<td>0.8</td>
<td>-3.4</td>
</tr>
<tr>
<td>OIP3 (dBm)</td>
<td>10</td>
<td>3.8</td>
</tr>
<tr>
<td>Pdiss (mW)</td>
<td>39.7</td>
<td>28.7</td>
</tr>
<tr>
<td>Pdiss (core exclude bias ckt) (mW)</td>
<td>31.5</td>
<td>20.5</td>
</tr>
</tbody>
</table>

Simulation
IC example: 1-25 GHz dual-conversion receiver
Dual Conversion: Wide Tuning

Low (2GHz) IF $\rightarrow$ image & LO responses close to RF carrier

High (100GHz) IF $\rightarrow$ image & LO responses far from RF carrier

Dual conversion: a standard approach in RF receivers.

Modern THz IC processes $\rightarrow$ 100 GHz IF easily feasible
$\rightarrow$ Image-response-free 1-50 GHz receiver
W-band Waveguide Filters

1 GHz filter bandwidth is easy; 100 MHz should be just feasible.

our effort: design the ICs, purchase the filter.
Choice of Frequency Plan

LO below IF:
- triplers have residual output @ 2f_in
  → maximum 1.5:1 tuning ratio
  → maximum 67-100 GHz LO tuning
  ~1-33 GHz RF tuning
- Need 67-100GHz LO driver PA
- present designs (lower-risk)

LO above IF:
- maximum 100-150 GHz LO tuning
  ~1-50 GHz RF tuning
- Need 100-150GHz LO driver PA
- At ~200-300mW output power
  higher-risk.
Full receiver configuration: 2 chips to ease testing
Receiver: down-conversion block

Ground Plane: MET1

VDD: 2.0 V

Down-mixer

Matching & Balun

LO Driver (> 20 dBm)

Ground Plane: MET3  MET1

100 GHz

Buffer

Microstrip line filter

Multiplier (ECL_Gate) x3

IF A

Mixer

LO Driver (> 21 dBm)

Buffer

Microstrip line filter

Multiplier x3

LC filter

Multiplier Chain

Ground Plane: MET3

VEE: -3.3 V

11.1 GHz

Ground Plane: MET1

VDD: 2.0 V

Down-mixer

Matching & Balun

LO Driver (> 20 dBm)

Ground Plane: MET3  MET1

100 GHz

Buffer

Microstrip line filter

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11.1 GHz

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LC filter

Multiplier Chain

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VEE: -3.3 V

11.1 GHz

Ground Plane: MET1

VDD: 2.0 V

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LO Driver (> 20 dBm)

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100 GHz

Buffer

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IF A

Mixer

LO Driver (> 21 dBm)

Buffer

Microstrip line filter

Multiplier x3

LC filter

Multiplier Chain

Ground Plane: MET3

VEE: -3.3 V

11.1 GHz

Ground Plane: MET1

VDD: 2.0 V

Down-mixer

Matching & Balun

LO Driver (> 20 dBm)

Ground Plane: MET3  MET1

100 GHz

Buffer

Microstrip line filter

Multiplier (ECL_Gate) x3

IF A

Mixer

LO Driver (> 21 dBm)

Buffer

Microstrip line filter

Multiplier x3

LC filter

Multiplier Chain

Ground Plane: MET3

VEE: -3.3 V

11.1 GHz
Receiver: up-conversion block

Ground Plane: MET1

VDD: 2.0 V

LNA

LO Driver (> 20 dBm)

Ground Plane

MET3  MET1

VEE: -3.3 V

Ground Plane: MET1

4300 um x 1160 um

Multiplier Chain

70-100 GHz

Buffer

LC filter

x3

Multiplier (ECL_Gate)

VEE: -3.3 V

7.88-11.1 GHz

Multiplier (ECL_Gate)

Matching & Balun

Up-mixer

Mixer

LO Driver (> 21 dBm)

Buffer

Microstrip line filter

Multiplier x3

LC filter

Multiplier x3
Mixer

Diode mixer:
High dynamic range.
base-collector diodes: no saturation
series-connected $\rightarrow$ high IP3
requires high LO drive power

Baluns:
tri-plane design
some are sub-quarter-wavelength
9:1 LO Multiplier

Ground Plane: MET3
VEE: -3.3 V

Ground Plane: MET1
VDD: 2.0 V

ECL_gate1 Filter1 ECL_gate2 Filter2 ECL_gate3 Amp.

2500 um x 1160 um

Output Power (GHz) vs Multiplier Output Frequency (GHz)

Output Spectra
Differential LO Driver Amplifier: 67-100GHz

Ultra-broadband LO driver
limited by 67GHz substrate mode?
data shows otherwise.

High Power
required by high-IP3 mixer
>100mW over full bandwidth
> 250mW at most frequencies.

Topology
4:1 series connected by baluns
*compact, efficient, ultra-broadband*
2 cascaded stages
Differential LO Driver Amplifier: 67-100GHz

- **$S_{21}$, $S_{11}$, and $S_{22}$**
  - Frequency, GHz: 20 to 120
  - Magnitude, dB: -30 to 0

- **$P_{3dB}$ and Peak PAE**
  - Frequency, GHz: 40 to 110
  - $P_{3dB}$ in dBm: 10 to 24
  - Peak PAE in %: 5 to 30

- **Simulated vs. Measured**
  - Graphs compare simulated and measured performance.
High dynamic range IF amplifier

low noise figure
high third-order intercept
low/moderate gain

Common-emitter
Pseudo-differential
Strong inductive degeneration
   high IP3.
   partly converges noise & $S_{11}$ tuning

*2nd harmonic short
First IF Amplifier

- 5.5-6 dB gain
- 95-105GHz
- 6.5 dB noise figure
- WITHOUT PADS: 551 um X 575 um,
  100 mW DC power

Simulations

- 5.5-6 dB gain
- 95-105GHz
- 6.5 dB noise figure
- 20.7dBm IIP3
  (26.7dBm OIP3)

baluns for probe testing only
IF Amplifier measurement results

Low-gain (high-IIP3) design

Power consumption: 94 mA @ 2 V
Peak gain: 4.3 dB @ 95 GHz, 4.0 dB @ 100 GHz

Low-gain (high-IIP3) design

Power consumption: 97 mA @ 2 V
Peak gain: 5.9 dB @ 95 GHz, 5.7 dB @ 100 GHz
IF Amplifier measurement results

- **OIP3 (dBm)**
  - Breakout OIP3, Vcc = 2V
  - Breakout OIP3, Vcc = 1.5V
  - Simulated OIP3, Vcc = 2V
  - Simulated OIP3, Vcc = 1.5V
  - De-embedded OIP3, Vcc = 2V
  - De-embedded OIP3, Vcc = 1.5V

- **Noise Figure (dB)**
  - Simulated Noise Figure
  - Measured Noise Figure
  - De-embedded Noise Figure

- **Frequency (GHz)**
  - Breakout OIP3, Vcc = 2V
  - Breakout OIP3, Vcc = 1.5V
  - Simulated OIP3, Vcc = 2V
  - Simulated OIP3, Vcc = 1.5V
  - De-embedded OIP3, Vcc = 2V
  - De-embedded OIP3, Vcc = 1.5V

- **Frequency (GHz)**
  - Simulated Noise Figure
  - Measured Noise Figure
  - De-embedded Noise Figure
Performance: upconversion block

- **IIP3, w/o Mul (dBm)**
- **IIP3, Sim (dBm)**
- **IIP3 w/ Mul. (dBm)**
- **Conversion Gain, w/o Mul. (dB)**
- **Conversion Gain, Sim (dB)**
- **Conversion Gain, w/ Mul. (dB)**
- **Conversion Gain, Power meter (dB)**

**IF Frequency (GHz):**

- Fixed RF input @ 200 MHz
- Fixed IF frequency @100GHz

**RF Frequency (GHz):**

- Fixed RF input @ 200 MHz
Upconversion measurement: Gain, IM3

Harmonic mixer
LO = (RF+IF)/n

In our test:
n=10 and IF = 1 GHz

Frequency measurement: Harmonic mixer
Power measurement: power meter

*Harmonic mixer LO frequency was adjusted to measure LO feedthrough (Harmonic mixer IF = 1 GHz)
Downconversion measurement: IP3
mm-Wave Wireless
mm-Wave Wireless Electronics

Mobile communication @ 2Gb/s per user, 1 Tb/s per base station

Requires: large arrays, complex signal processing, high $P_{out}$, low $F_{min}$

VLSI beamformers
VLSI equalizers
III-V LNAs & PAs (?)