Scalable GaSb/InAs Tunnel FETs With Nonuniform Body Thickness

Jun Z. Huang, Pengyu Long, Michael Povolotskyi, Gerhard Klimeck, *Fellow, IEEE*, and Mark J. W. Rodwell, *Fellow, IEEE*

***Abstract*— GaSb/InAs heterojunction tunnel FETs are strong candidates in building future low-power ICs, as they could provide both steep subthreshold swing and large on-state current (I_{ON}). However, at short-channel lengths, they suffer from large tunneling leakage originating from the small bandgap and small effective masses of the InAs channel. As proposed in this paper, this problem can be significantly mitigated by reducing the channel thickness, meanwhile retaining a thick source-channel tunnel junction, thus forming a design with a nonuniform body thickness. Because of the quantum confinement, the thin InAs channel offers a large bandgap and large effective masses, reducing the ambipolar and source-to-drain tunneling leakage at off-state. The thick GaSb/InAs tunnel junction, instead, offers a low tunnel barrier and small effective masses, allowing a large tunnel probability at on-state. In addition, the confinement-induced band discontinuity enhances the tunnel electric field and creates a resonant state, further improving I_{ON}. Atomistic quantum transport simulations show that ballistic I_{ON} = 284 A/m is obtained at 15-nm channel length, I_{OFF} = 1 x 10^{-3} A/m, and V_{DD} = 0.3 V, while with uniform body thickness, the largest achievable I_{ON} is only 25 A/m. Simulations also indicate that this design is scalable to sub-10-nm channel length.**

***Index Terms*—Heterojunction tunnel FETs (TFETs), nonuniform body thickness, scalable TFETs.**

I. Introduction

TUNNEL FET (TFET), a promising replacement of classical MOSFET for future low-power ICs, has been intensively studied over a decade. The advantages of TFET come from its steep subthreshold swing (SS) that overcomes the 60 mV/decade limit of a conventional MOSFET, allowing substantial supply voltage (V_{DD}) scaling [1]. However, because of low tunnel probability, the steep SS usually occurs at very low current level [2], [3]. This leads to insufficient ON-state current (I_{ON}) and thus large switching delay (CV_{DD}/I_{ON}). Various approaches have been proposed to improve the low I_{ON}. In particular, GaSb/InAs heterojunction-based TFETs [4]–[10] can considerably boost I_{ON} due to their broken/staggered-gap band alignment.

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J. Z. Huang, P. Long, M. Povolotskyi, and G. Klimeck are with the Network for Computational Nanotechnology, Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: junhuang1021@gmail.com).

M. J. W. Rodwell is with the Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA 93106-9560 USA.

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However, as the channel length scales to sub-20 nm as projected by International Technology Roadmap for Semiconductors (ITRS) for the next technology nodes [11], the GaSb/InAs n-type TFETs suffer from large ambipolar and source-to-drain tunneling leakage due to the small bandgap and the small effective masses of the InAs channel. These leakages can be reduced by reducing the body thickness [12], because the bandgap and the effective masses of the InAs channel increase as the body thickness decreases. Meanwhile, the large bandgap and large effective masses also reduce the tunneling probability across the tunnel junction. The resonant TFET with a reversed InAs/GaSb heterojunction can have a steep SS at short gate length [12], but the I_{ON} is limited by the narrow resonant transmission peak [13]. The channel heterojunction design with a large bandgap AlInAsSb alloy as the channel material has also been proposed [14], [15] to mitigate the short-channel effects. However, a good-quality dielectric on top of AlInAsSb has not been experimentally demonstrated yet. Therefore, InP, a material with a high-quality dielectric already demonstated, has been investigated as the alternative channel material [16]. It is found that the lattice-mismatched InP channel imposes biaxial compressive strain on the GaSb/InAs tunnel junction, compromising the improvement.

In this paper, we show that, by reducing the InAs channel body thickness meanwhile retaining a relatively large body thickness at the source tunnel junction, the leakage can be significantly reduced without compromising the large source tunnel probability, thereby the scalability of GaSb/InAs TFETs is greatly improved. We highlight some important simulation details in Section II and then present the simulation results in Section III for the uniform body thickness and in Section IV for the nonuniform case. Device variabilities and nonidealities are discussed in Section V. Finally, the conclusion is drawn in Section VI.

II. Device Structures and Simulation Method

The structures of the GaSb/InAs ultrathin-body (UTB) n-type TFETs are shown in Fig. 1. We consider double-gate structures, since they provide better electrostatic con-

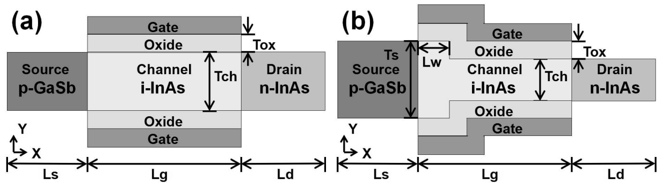

Fig. 1. GaSb/InAs n-type TFETs with (a) conventional uniform and (b) proposed nonuniform body thickness. The oxide and the gate in (b) are conformal to the channel, so that the oxide thickness is equal to that of (a). Here, T_{ch}/T_{ox} is the channel/oxide thickness, ϵ_{ox} is the oxide dielectric constant, $L_s/L_g/L_d$ is the source/channel/drain length, and N_s/N_d is the source/drain doping density. The extra parameters in (b) are the source thickness T_s and the wide channel length L_w.

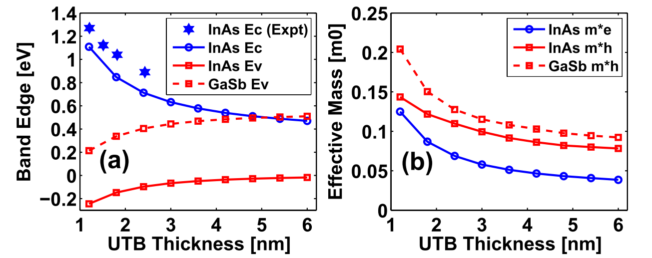

Fig. 2. (a) Conduction and valence band edges (E_c and E_v) and (b) electron and hole effective masses ($m*e$ and $m*h$) of the GaSb and InAs UTBs, as functions of the UTB thickness. The confinement is in the [001] orientation and the effective masses are in the [100] orientation.

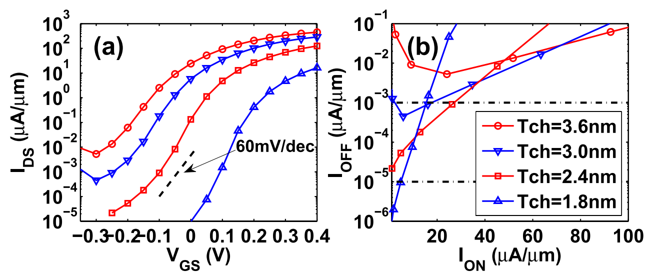

Fig. 3. (a) I_{DS}–V_{GS} characteristics (V_{DS} = 0.3 V) of the uniform device [Fig. 1(a)] as a function of the body thickness T_{ch}. Confinement/transport is in the [001]/[100] orientation. L_g = 15 nm, T_{ox} = 1.8 nm, ϵ_{ox} = 9.0, N_s = –5 x 10^{19}/cm^3, and N_d = +2 x 10^{19}/cm^3. (b) I_{ON}–I_{OFF} curves with V_{DD} = 0.3 V.

trol over the channel than the single-gate counterparts [17]. In practice, such structures can be realized by the 3-D FinFET geometries [18]. The devices are simulated and optimized by solving Poisson equation and open-boundary Schrödinger equation [19] self-consistently within NEMO5 tool [20]. The Hamiltonian employed is in the atomistic sp^{3}d^{5}s* tight-binding (TB) basis, including spin-orbit coupling, with the room temperature TB parameters fitted to the band structures as well as the wave functions of density functional theory calculations for better transferability [21], [22]. Due to the high semiconductor-to-oxide barrier height [23], the oxide is treated as an impenetrable potential barrier and only modeled in the Poisson equation. However, at very thin body thicknesses, even a small penetration of the wave function into the dielectric might significantly increase the effective body thickness. The physical body thickness would need to be accordingly adjusted to obtain the desired bound state energies. Electron–phonon scattering is neglected in the data presented. We have found in simulations that at 15-nm channel length, I_{OFF} due to source–drain tunneling dominates over that arising from electron–phonon scattering. This agrees with studies in [24]–[26], where the impact of phonon scattering on the I–V characteristics of InAs homojunction and GaSb/InAs heterojunction nanowire TFETs was found to be very small due to the direct bandgaps and the short-channel lengths ($\leq$20 nm). The discrete nature of dopants and bulk/interface defects is not considered in the simulations; their effects will be discussed in Section V.

III. Uniform Body Thickness

First, we analyze the conventional case with uniform body thickness, as shown in Fig. 1(a). The band edges and the effective masses of the UTB structures for different body thicknesses are plotted in Fig. 2. Energy value of 0 eV corresponds to the valence band edge of bulk InAs. The calculated conduction band edge (E_c) of the InAs UTB has a mismatch circa 0.2 eV with the experiment data [27], but its variations with respect to the UTB thickness agree well with the experiment.[1] The mismatch could be due to the experimental error (note that the experiment data have a distribution) and that the measurement was performed at low temperature (our TB parameters are at room temperature). It is observed that the InAs UTB bandgap (InAs E_c–InAs E_v) and the tunnel barrier height (InAs E_c–GaSb E_v) both increase as the UTB thickness becomes smaller; the effective masses (electron and hole) of the InAs UTB also increase significantly as the UTB thickness decreases.

Therefore, the I–V characteristic of the device is a strong function of the UTB thickness. Indeed, as shown in Fig. 3(a), a large body thickness ($T_{ch} = 3.6$ or 3 nm) leads to a large turn-ON current, but also a large SS and a high I_{OFF}. A small body thickness ($T_{ch} = 1.8$ nm) gives rise to a small SS and a low I_{OFF}, but a small turn-ON current. With $I_{OFF} = 1 \times 10^{-3}$ A/m and $V_{DD} = 0.3$ V, the optimal body thickness for $L_g = 15$ nm is around 2.4 nm, providing $I_{ON} = 25$ A/m [Fig. 3(b)]. This is too low for any practical logic application.

IV. Nonuniform Body Thickness

The proposed design that can overcome this dilemma is shown in Fig. 1(b). Compared with Fig. 1(a), this design has reduced body thickness *only* in part of the channel region (and in the drain). Three parameters need to be optimized, i.e., T_s, T_{ch}, and L_w. In this paper, we fix T_s to be 3.6 nm and then optimize T_{ch} and L_w to maximize I_{ON}. As shown in Fig. 4(a), there is an optimal L_w for each T_{ch} and the optimal L_w is smaller for smaller T_{ch}, which will be explained in a moment. A tradeoff of T_{ch} is also clearly observed, since a large T_{ch} does not have sufficiently large bandgap and effective masses needed for the leakage suppression, while a small T_{ch} would

[1]The experimental data [27] reported energy difference between the lowest conduction band state of InAs quantum well and the highest valence band state of AlSb quantum well. To obtain from this data, the quantized state energy of the InAs well with respect to the InAs bulk valence band edge, the reported values were shifted up by the valence band offset between bulk AlSb and InAs, equal to 0.18 eV [28], and, finally, adjusted by subtracting the quantization energy of the heavy hole state in the AlSb quantum well, equal to 0.03 eV in our TB calculation for a 5-nm well width.

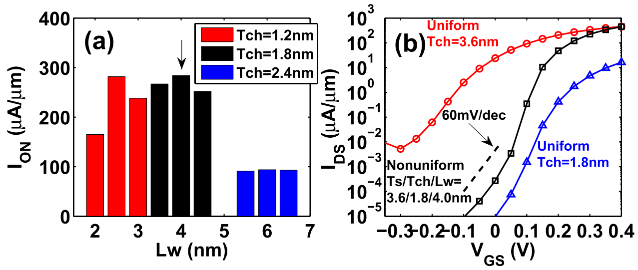

Fig. 4. (a) I_{ON} (at V_{DD} = 0.3 V and I_{OFF} = 1 x 10^{-3} A/m) of the nonuniform design [Fig. 1(b)] for different values of L_W and T_{ch}, with fixed T_s = 3.6 nm. (b) Full I_{DS}–V_{GS} characteristics of the $T_s/T_{ch}/L_W$ = 3.6/1.8/4 nm case in (a), in comparison with the uniform 3.6 nm and uniform 1.8 nm cases. All other device parameters are the same as those in Fig. 3.

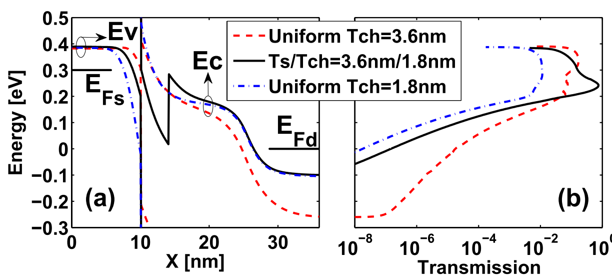

Fig. 5. Comparison of (a) band diagrams and (b) transmission functions of the three cases in Fig. 4(b): uniform 3.6-nm body thickness, uniform 1.8-nm thickness, and nonuniform 3.6-/1.8-nm body thickness.

affect the ON-state transmission due to the large reflection at the waveguide discontinuity. With $T_{\text{ch}} = 1.8$ nm and $L_w = 4$ nm, we obtain the largest I_{ON} (284 A/m), which is more than an order of magnitude larger than that of the uniform case (25 A/m). The full I_{DS}–V_{GS} curve is further displayed in Fig. 4(b) along with two uniform thickness cases, showing that both steep SS and large turn-ON current are simultaneously obtained in the nonuniform case.

The improvements can be better understood from the band diagrams and the transmissions plotted in Fig. 5, where the three cases in Fig. 4(b) are compared. Above the channel E_c, the nonuniform 3.6/1.8 nm case has larger transmission than the uniform 1.8 nm case, giving rise to its larger turn-ON current. This is due to its smaller tunneling barrier height and smaller effective masses at the tunnel junction. Its transmission over channel E_c is even larger than the uniform 3.6 nm case, benefiting from its larger tunneling electric field and resonance-enhanced tunneling, both resulting from the confined band offset. Below the channel E_c, the nonuniform 3.6/1.8 nm case has steeper transmission slope than the uniform 3.6 nm case, implying steeper SS. This is partly due to the larger channel bandgap and larger channel effective masses, partly due to the better electrostatics at the channel-drain junction, and partly due to the smaller drain Fermi degeneracy (the energy distance between the drain Fermi level and the drain E_c).

The local density of states (LDOS) is further shown in Fig. 6. Similar to the channel heterojunction design [14], [29], the confined conduction band edges in the channel form a quantum well, which creates a quasi-bound state. The energy

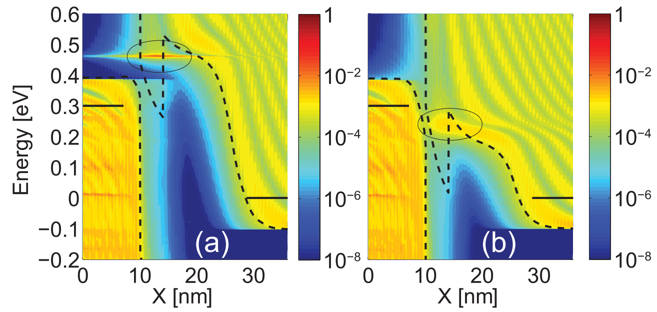

Fig. 6. LDOS (in logarithmic scale) of the optimized design in Fig. 4, at (a) OFF-state and (b) ON-state. Band diagrams (dashed lines) and contact Fermi levels (solid lines) are superimposed. The quasi-bound states are highlighted (circles).

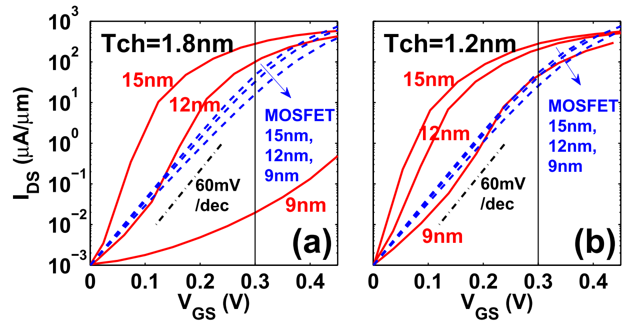

Fig. 7. I_{DS}–V_{GS} characteristics (V_{DS} = 0.3 V) of the proposed TFETs, in comparison with Si MOSFETs (also from quantum ballistic simulations), for three channel lengths (L_g = 15, 12, and 9 nm). (a) $T_s/T_{ch}/L_W$ = 3.6/1.8/4 nm for TFETs and T_{ch} = 1.8 nm for MOSFETs. (b) $T_s/T_{ch}/L_W$ = 3.6/1.2/2.5 nm for TFETs and T_{ch} = 1.2 nm for MOSFETs.

level of this state needs to be aligned with the channel conduction band edge at the ON-state, so that it enhances I_{ON}. At the OFF-state, in order to reduce the phonon-assisted tunneling (PAT) leakage, the energy of this state has to be higher than the valence band edge at the source by at least the optical phonon energy [30]. In the proposed designs, the energy separation of ~ 75 meV is maintained, that is significantly larger than the bulk optical phonon energy of InAs: $\hbar\omega_{op} \approx$30meV. Note that the energy of the quantized optical phonon both in an InAs wire of $\sim 3\times3$ nm^2 cross section [31] and in an InAs UTB of 1.8 nm thickness [32] is almost the same as in bulk, because the bulk optical phonon dispersion is almost flat in k space. Therefore, for the short-channel devices ($L_g \le 15$ nm) considered in this paper, the source-to-drain direct tunneling leakage is much larger than the PAT leakage and the ballistic simulation captures the dominant leakage mechanism. In order to meet these requirements, L_w needs to be adjusted for a given T_{ch}, as shown in Fig. 4(a). In fact, a smaller T_{ch} leads to a larger confined band offset, and thus, L_w needs to be reduced properly to shift the quasi-bound state upward.

ITRS 2020 and 2023 technology nodes require channel length L_g to be scaled to about 12 and 9 nm [11]. At such short-channel lengths, the source-to-drain tunneling leakage becomes more prominent. As compared in Fig. 7(a), when L_g is reduced from 15 to 12 nm, I_{ON} of TFET drops from

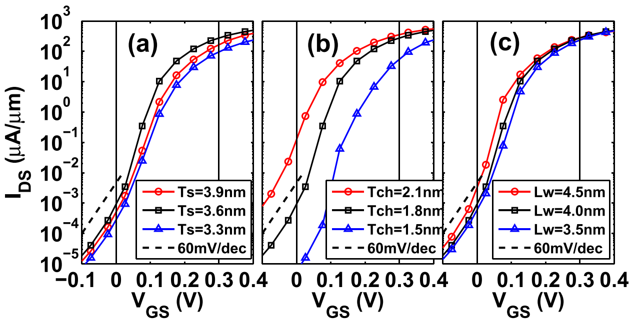

Fig. 8. Sensitivities of the I_{DS}–V_{GS} curve (V_{DS} = 0.3 V) to the variations of (a) T_s, (b) T_{ch}, and (c) L_w, for optimized design in Fig. 4. The amount of T_s and T_{ch} variations is one monolayer (about ±0.3 nm) and the L_w variation is ±0.5 nm.

284 to 106 A/m, while I_{ON} of Si MOSFET only drops from 49 to 41 A/m. When L_g is further scaled to 9 nm, the TFET cannot provide a decent ON/OFF ratio and does not possess an advantage over Si MOSFET. To improve the scalability, the channel thickness (T_{ch}) can be reduced from 1.8 to 1.2 nm to enlarge the channel bandgap and channel effective masses. As shown in Fig. 7(b), the SS of TFET degrades less, with $I_{ON} = 209$ A/m (50 A/m) obtained at $L_g = 12$ nm (9 nm), which is still considerably larger than $I_{ON} = 47$ A/m (31 A/m) of Si MOSFET.

V. Variabilities and Nonidealities

Fig. 8 shows the sensitivities of the I–V curve to the geometry variations. We find that the I–V curve can tolerate certain amount of T_s and L_w variations (under these variations, the resonant state energies at OFF-state are checked and found to be still higher than the source valence band edge by at least 30 meV), it is, however, very sensitive to the channel thickness (T_{ch}) variations resulting in unacceptable I_{OFF} or I_{ON} level. We note that, given a few nanometer body thickness, the dc characteristics and threshold voltage of both uniform [Fig. 3(a)] and nonuniform [Fig. 8(b)] TFETs vary strongly with the channel thickness. Given such geometries, a viable VLSI TFET technology must control the channel thickness to within a precision of a single atomic plane. Techniques to obtain this precision in fabrication include semiconductor growth by atomic layer epitaxy [33], or confined lateral epitaxial overgrowth [34] within dielectric regions formed by atomic layer deposition. Note that MOSFETs with 2.5-nm thickness InAs channel [35] and 1.5-/1-nm thickness InGaAs/InAs channel [36] have been reported recently. In addition, the proposed design concept can be generalized to nanowire structures with nonuniform cross section. As shown in [12], nanowire TFETs can relax the critical body thickness of UTB TFETs.

Other possible variations in device dimensions, including line edge roughness and surface roughness [37], [38], the random dopant fluctuations (RDFs) [37], [39], and the steepness of the thickness transition between T_s and T_{ch}, may also impact the device performance. Note that studies in [37] and [39] report that the relative variation in the ON-current, as a result of random source dopant variation, decreases as the TFET body thickness or cross section becomes larger. In our devices, the source thickness is 3.6 nm, which is larger than the best uniform thickness case (2.4 nm), so our design will be less sensitive to the RDF.

Fabrication nonidealities, such as the bulk and interface defects, would also degrade the device performances through trap-assisted tunneling (TAT) and Shockley–Read–Hall (SRH) generation. The TAT affects SS [40], [41] and is a serious issue for all III–V semiconductor-based MOSFETs and TFETs. However, recently, there has been a significant progress in fabricating high-quality dielectric/III–V semiconductor interfaces. For example, in [35], a 2.5-nm-thick InAs channel MOSFET with a 0.7-/3-nm $Al_2O_xN_y/ZrO_2$ gate dielectric has SS = 61mV/decade (at $L_g = 1$ μm and $V_{DS} = 0.1$ V), indicating low defect density, whether bulk or at the dielectric–semiconductor interface. The SRH generation increases the leakage current floor [40], [41]. The SRH leakage depends on the intrinsic carrier concentration, which is proportional to $\exp(-E_g/2kT)$, where E_g is the bandgap, k is the Boltzmann's constant, and T is the temperature [40]. Therefore, even if the thin portion of the channel was to have a larger bulk defect density, the SRH generation rate in this region would be decreased because of the increased bandgap arising from quantization.

VI. Conclusion

We have shown that by designing a nonuniform body thickness, the ON/OFF current ratio and scalability of the GaSb/InAs n-type TFETs can be greatly improved. The predictions, however, are based on ideal ballistic quantum transport simulations, various leakage mechanisms and fabrication nonidealities may degrade the device performances and need to be checked in the future. It should also be emphasized that such designs require precise control in fabrication of the device dimensions, in particular the channel thickness. To further improve the design, an additional nonuniformity or heterojunction could be placed in the source side to form devices akin to the triple-heterojunction designs [15], [16].

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References

[1] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, 2011.

[2] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[3] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014.

[4] D. K. Mohata *et al.*, "Demonstration of MOSFET-like on-current performance in arsenide/antimonide tunnel FETs with staggered hetero-junctions for 300mV logic applications," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2011, pp. 33.5.1–33.5.4.

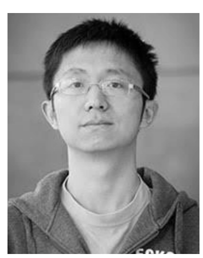
[5] Y. Lu *et al.*, "Performance of AlGaSb/InAs TFETs with gate electric field and tunneling direction aligned," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 655–657, May 2012.

[6] G. Zhou *et al.*, "Novel gate-recessed vertical InAs/GaSb TFETs with record high ION of 180μA/μm at VDS=0.5V," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2012, pp. 32.6.1–32.6.4.

[7] Z. Jiang, Y. He, G. Zhou, T. Kubis, H. G. Xing, and G. Klimeck, "Atomistic simulation on gate-recessed InAs/GaSb TFETs and performance benchmark," in *Proc. 71st Annu. Device Res. Conf. (DRC)*, Jun. 2013, pp. 145–146.
[8] S. Brocard, M. G. Pala, and D. Esseni, "Large on-current enhancement in hetero-junction tunnel-FETs via molar fraction grading," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 184–186, Feb. 2014.
[9] M. G. Pala and S. Brocard, "Exploiting hetero-junctions to improve the performance of III–V Nanowire tunnel-FETs," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 115–121, May 2015.
[10] E. Lind, E. Memišević, A. W. Dey, and L. E. Wernersson, "III-V heterostructure nanowire tunnel FETs," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 96–102, May 2015.
[11] (2015). *ITRS*. [Online]. Available: http://www.itrs2.net/
[12] U. E. Avci and I. A. Young, "Heterojunction TFET scaling and resonant-TFET for steep subthreshold slope at sub-9nm gate-length," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2013, pp. 4.3.1–4.3.4.
[13] P. Long, E. Wilson, J. Z. Huang, G. Klimeck, M. J. W. Rodwell, and M. Povolotskyi, "Design and simulation of GaSb/InAs 2D transmission-enhanced tunneling FETs," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 107–110, Jan. 2016.
[14] P. Long, J. Z. Huang, M. Povolotskyi, G. Klimeck, and M. J. W. Rodwell, "High-current tunneling FETs with $(1\bar{1}0)$ orientation and a channel heterojunction," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 345–348, Mar. 2016.
[15] P. Long *et al.*, "Extremely high simulated ballistic currents in triple-heterojunction tunnel transistors," in *Proc. 74th Annu. Device Res. Conf. (DRC)*, Jun. 2016, pp. 1–2.
[16] P. Long, J. Z. Huang, M. Povolotskyi, D. Verreck, G. Klimeck, and M. J. W. Rodwell, "High-current InP-based triple heterojunction tunnel transistors," in *Proc. 28th Int. Conf. Indium Phosph. Rel. Mater. (IPRM)*, Jun. 2016, pp. 1–2.
[17] M. Luisier and G. Klimeck, "Atomistic full-band design study of InAs band-to-band tunneling field-effect transistors," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 602–604, Jun. 2009, doi: 10.1109/LED.2009.2020442
[18] J.-P. Colinge, "The SOI MOSFET: From Single Gate to Multigate," in *FinFETs Other Multi Gate Transistors*, J.-P. Colinge, Ed. New York, NY, USA: Springer, 2008, pp. 1–48.
[19] M. Luisier, A. Schenk, W. Fichtner, and G. Klimeck, "Atomistic simulation of nanowires in the $sp^3d^5s^*$ tight-binding formalism: From boundary conditions to strain calculations," *Phys. Rev. B*, vol. 74, no. 20, p. 205323. Nov. 2006.
[20] S. Steiger, M. Povolotskyi, H.-H. Park, T. Kubis, and G. Klimeck, "NEMO5: A parallel multiscale nanoelectronics modeling tool," *IEEE Trans. Nanotechnol.*, vol. 10, no. 6, pp. 1464–1474, Nov. 2011.
[21] Y. P. Tan, M. Povolotskyi, T. Kubis, T. B. Boykin, and G. Klimeck, "Tight-binding analysis of Si and GaAs ultrathin bodies with subatomic wave-function resolution," *Phys. Rev. B*, vol. 92, no. 9, p. 085301, 2015.
[22] Y. Tan *et al.* (Jun. 2016). *Tight Binding Parameters by DFT Mapping*. [Online]. Available: https://nanohub.org/resources/15173
[23] J. Robertson and B. Falabretti, "Band offsets of high K gate oxides on III-V semiconductors," *J. Appl. Phys.*, vol. 100, no. 1, pp. 014111-1–014111-8, Jul. 2006.
[24] M. Luisier and G. Klimeck, "Simulation of nanowire tunneling transistors: From the Wentzel–Kramers–Brillouin approximation to full-band phonon-assisted tunneling," *J. Appl. Phys*, vol. 107, no. 8, pp. 084507-1–084507-6, Apr. 2010.
[25] F. Conzatti, M. G. Pala, D. Esseni, E. Bano, and L. Selmi, "Strain-induced performance improvements in InAs nanowire tunnel FETs," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2085–2092, Aug. 2012, doi: 10.1109/TED.2012.2200253
[26] U. E. Avci *et al.*, "Energy efficiency comparison of nanowire hetero-junction TFET and Si MOSFET at Lg=13nm, including P-TFET and variation considerations," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2013, pp. 33.4.1–33.4.4.
[27] B. Brar, H. Kroemer, J. Ibbetson, and J. H. English, "Photoluminescence from narrow InAs-AlSb quantum wells," *Appl. Phys. Lett.*, vol. 62, no. 25, pp. 3303–3305, Jun. 1993.
[28] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, "Band parameters for III–V compound semiconductors and their alloys," *J. Appl. Phys.*, vol. 89, no. 11, pp. 5815–5875, Jun. 2001.
[29] K. Ganapathi and S. Salahuddin, "Heterojunction vertical band-to-band tunneling transistors for steep subthreshold swing and high on current," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 689–691, May 2011.
[30] S. O. Koswatta, S. J. Koester, and W. Haensch, "On the possibility of obtaining MOSFET-like performance and sub-60-mV/dec swing in 1-D broken-gap tunnel transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 12, pp. 3222–3230, Dec. 2010.
[31] M. Salmani-Jelodar, A. Paul, T. Boykin, and G. Klimeck, "Calculation of phonon spectrum and thermal properties in suspended <100> $In_XGa_{1-X}As$ nanowires," *J. Comput. Electron.*, vol. 11, no. 1, pp. 22–28, Mar. 2012.
[32] S. Mukherjee *et al.*, (Sep. 2016). *Band structure lab*. [Online]. Available: https://nanohub.org/tools/bandstrlab/
[33] S. M. Bedair, "Selective-area and sidewall growth by atomic layer epitaxy," *Semicond. Sci. Technol.*, vol. 8, no. 6, pp. 1052–1062, 1993.
[34] L. Czornomaz *et al.*, "First demonstration of InGaAs/SiGe CMOS inverters and dense SRAM arrays on Si using selective epitaxy and standard FEOL processes," in *IEEE Symp. VLSI Technol. Dig. Tech. Papers*, Jun. 2016, pp. 1–2.
[35] S. Lee *et al.*, "Record Ion (0.50mA/μm at V_{DD}=0.5V and I_{off}=100nA/μm) 25nm-gate-length ZrO2/InAs/InAlAs MOSFETs," in *IEEE Symp. VLSI Technol., Dig. Tech. Papers*, Jun. 2014, pp. 1–2.
[36] C.-Y. Huang *et al.*, "12 nm-gate-length ultrathin-body InGaAs/InAs MOSFETs with 8.3•10^5 ION/OFF," in *Proc. 73rd Annu. Device Res. Conf. (DRC)*, Jun. 2015, p. 260.
[37] G. Leung and C. O. Chui, "Stochastic variability in silicon double-gate lateral tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 84–91, Jan. 2013.
[38] F. Conzatti, M. G. Pala, and D. Esseni, "Surface-roughness-induced variability in nanowire InAs tunnel FETs," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 806–808, Jun. 2012.
[39] S. S. Sylvia, K. M. M. Habib, M. A. Khayer, K. Alam, M. Neupane, and R. K. Lake, "Effect of random, discrete source dopant distributions on nanowire tunnel FETs," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2208–2214, Jun. 2014.
[40] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, "Temperature-dependent $I-V$ characteristics of a vertical $In_{0.53}Ga_{0.47}As$ tunnel FET," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 564–566, Jun. 2010.
[41] U. E. Avci *et al.*, "Study of TFET non-ideality effects for determination of geometry and defect density requirements for sub-60mV/dec Ge TFET," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2015, pp. 34.5.1–34.5.4.

Jun Z. Huang received the B.E. degree from Nankai University, Tianjin, China, in 2004, the M.E. degree from Shanghai Jiao Tong University, Shanghai, China, in 2010, and the Ph.D. degree from The University of Hong Kong, Hong Kong, in 2013, all in electrical engineering.

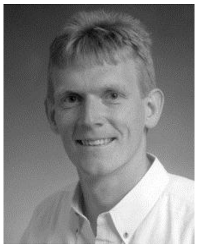
Since 2013, he has been a Post-Doctoral Researcher in network for computational nanotechnology with Purdue University, West Lafayette, IN, USA.



Pengyu Long received the B.S. degree in electronic science and technology from the Huazhong University of Science and Technology, Wuhan, China, in 2012, and the M.S. degree in electrical engineering from Purdue University, West Lafayette, IN, USA, in 2015, where he is currently pursuing the Ph.D. degree in electric engineering with Network for Computational Nanotechnology.

Michael Povolotskyi received the Ph.D. degree in electrical engineering from the University of Rome Tor Vergata, Rome, Italy, in 2004.

In 2008, he joined network for computational electronics with Purdue University, West Lafayette, IN, USA, where he involved in the design and development of an atomistic nanoelectronics simulation package NEMO5, theoretical study of semiconductor devices, and development of simulation methodologies.



Gerhard Klimeck (S'91–M'95–SM'04–F'13) received the Ph.D. degree from Purdue University, West Lafayette, IN, USA, in 1994.

He is currently the Reilly Director with the Center for Predictive Materials and Devices, and Network for Computational Nanotechnology, and also a Professor of Electrical and Computer Engineering.

Mark J. W. Rodwell (M'89–SM'99–F'03) received the Ph.D. degree from Stanford University, Stanford, CA, USA, in 1988.

His research group develops nanometer MOSFFETs, terahertz transistors, and millimeter-wave/terahertz ICs. He holds the Doluca Family Endowed Chair in electrical and computer engineering with the University of California at Santa Barbara (UCSB), Santa Barbara, CA, USA. He directs the UCSB node of the NSF Nanofabrication Infrastructure Network.

Prof. Rodwell received the 2010 IEEE Sarnoff Award, the 2012 IEEE Marconi Prize Paper Award, and the 1997 IEEE Microwave Prize.