

Making better transistors: beyond yet another new materials system.

In ~55 years of IC development, industry has concentrated on making switches smaller; universities have mostly concentrated on the complementary role of making them from new materials. Thus has university electron device research progressed from silicon to germanium and SiGe, the arsenide, phosphide and then antimonide III-V's, then carbon nanotubes, and today 2D semiconductors. Beyond SiGe, there seems but little hope that these more recent materials might benefit transistors in computer ICs.

Perhaps we should focus instead on improving their shape ? Corrugating a FET channel, in the style of a folded piece of paper, produces a device with transport distance much larger than its footprint; we can use this to improve electrostatics and suppress source-drain tunneling currents in few-nm-footprint transistors. Corrugating the channel in the perpendicular direction increases the drive current per unit IC area, which we then might trade for lower-voltage, lower-power operation. With FETs, making low-resistance yet small contacts is as much a problem as is making short gates: should we corrugate the metal-semiconductor interface to reduce the interface resistance ?

Or, should we change their band structure ? In tunnel FETs, we can add several heterojunctions, and so increase the desired on-state tunneling currents while decreasing the unwanted off-state leakage currents. Yet, I can offer nothing beyond this single example, albeit one that I presently find of great interest.

Finally, perhaps we might change their function ? One focus of this workshop is to explore the merging of logic and memory. We might do this at either within the transistor or within low-level logic design. It is not yet clear to this circuit designer that a logic-plus-memory transistor would be markedly more useful than, for example, simple merged logic using pass transistors and gate capacitances. I will do my best to examine their potential utility.