INVITED PAPER

InP HBT Technologies for THz Integrated Circuits

This paper describes the operation and scaling of InP heterojunction bipolar transistors (HBTs) to terahertz frequencies.

By Miguel Urteaga, *Senior Member IEEE*, Zach Griffith, *Senior Member IEEE*, Munkyo Seo, *Senior Member IEEE*, Jonathan Hacker, *Fellow IEEE*, and Mark J. W. Rodwell, *Fellow IEEE*

ABSTRACT | Highly scaled indium phosphide (InP) heterojunction bipolar transistor (HBT) technologies have been demonstrated with maximum frequencies of oscillation (f_{max}) of >1 THz and circuit operation has been extended into the lower end of the terahertz (THz) frequency band. InP HBTs offer high radio-frequency (RF) output power density, millivolt (mV) threshold uniformity, and high levels of integration. Integration with multilevel thin-film wiring permits the realization of compact and complex THz monolithic integrated circuits (TMICs). Circuit results reported from InP HBT technologies include: 200-mW power amplifiers at 210 GHz, 670-GHz amplifiers and fundamental oscillators, and fully integrated 600-GHz transmitter circuits. We review the state of the art in THz-capable InP HBT devices and integrated circuit (IC) technologies. Challenges in extending transistor bandwidth and in circuit design at THz frequencies will also be addressed.

KEYWORDS | Heterojunction bipolar transistor (HBT), indium phosphide (InP), terahertz (THz)

I. INTRODUCTION

Transistors in the indium phosphide (InP)-based material system have demonstrated the highest reported radio-frequency (RF) figures of merit. Both field-effect high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) have been demonstrated with maximum frequencies of oscillation (f_{max}) exceeding 1 THz [1]–[5]. These record bandwidths are achieved by coupling the advantageous material properties of the InGaAs/InP material system (high electron mobilities in both quantum-well channels and p-doped bases, large heterojunction offsets for carrier confinement, and high achievable doping levels for low Ohmic contact resistivities) with aggressive lateral and vertical scaling of transistor geometries.

As transistor bandwidths have increased, new classes of monolithic integrated circuits (ICs) have emerged extending IC operating frequencies and functionality into the terahertz (THz) frequency regime (defined as 0.3–3 THz). The highest frequency solid-state amplifiers have been reported in InP HEMT technologies including the first demonstration of a solid-state amplifier at >1 THz [6]. InP HBT amplifiers have been demonstrated operating to >0.6 THz [7], [8]. Compared to InP HEMTs, double-heterojunction bipolar transistors (DHBTs) with a wide bandgap InP collector will have a higher breakdown voltage at a given current gain cutoff frequency f_t. Combined with their high available drive current, InP HBTs are ideal for submillimeter and THz power generation—demonstrations of this capability include the first >200-mW power amplifier (PA) operating at >200 GHz [9].

HBTs offer excellent threshold control and high intrinsic transconductance and are easily integrated with dense multilevel thin-film wiring. This permits the realization of compact analog circuit blocks operating to THz frequencies. Oscillators [10], frequency dividers [11], [12], and mixers [13] have all been realized operating to THz frequencies using design techniques common to silicon radio-frequency integrated circuit (RFIC) design. Using these blocks, complex integrated transmitter and

Manuscript received June 20, 2016; revised December 12, 2016; accepted January 4, 2017. Date of publication May 2, 2017; date of current version May 18, 2017. This work was supported by the Defense Advanced Research Projects Agency (DARPA) Contracts Management Office (CMO) under Contract HR0011-09-C-0060. The views opinions and/or findings in this article are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Defense Advanced Research Projects Agency, or the U.S. Department of Defense. (*Corresponding author: Miguel Urteaga.*)

M. Urteaga, **Z. Griffith**, and **J. Hacker** are with Teledyne Scientific Company, Thousand Oaks, CA 93021 USA (e-mail: miguel.urteaga@teledyne.com).

M. Seo was with Teledyne Scientific Company, Thousand Oaks, CA 93021 USA. He is now with the Department of Electrical Engineering, Sungkyunkwan University, South Korea (e-mail: mkseo@skku.edu).

M. J. W Rodwell is with the Electrical and Computer Engineering Department, University of California, Santa Barbara, CA 93021 USA (e-mail: rodwell@ece.ucsb.edu).

Digital Object Identifier: 10.1109/JPROC.2017.2692178

receiver ICs have been demonstrated at frequencies from 300 GHz [15], [16], [17] to 600 GHz [18].

The availability of compact single-chip sources and receivers at THz frequencies can have a transformative impact in a range of applications including: instrumentation, imaging, remote sensing, and communications. The size, weight, and power (SWaP) of systems currently realized by cascading bulky and expensive waveguide split-block assemblies for each RF component can be greatly reduced and the realization of arrays at $\lambda/2$ element spacings can be envisioned.

In this paper, we review the current state of the art for InP HBT performance and opportunities and challenges for further extending transistor bandwidth. Submillimeter-wave PAs in HBT technologies are also reviewed with a focus on recent advances that have significantly increased available output power from ICs and power combined modules around 200 GHz. Finally, we address transmitter and receiver component design at THz frequencies and progress toward the realization of compact integrated exciter and receiver circuits.

II. THz BIPOLAR TRANSISTOR TECHNOLOGIES

Scaling laws and roadmaps for doubling InP HBT bandwidth have been developed following similar analyses performed for Si devices [19], [20]. These roadmaps establish paths for obtaining useful circuit performance in the THz frequency range at 250- and 130-nm scaling generations, where the transistor scaling generation refers to the emitter junction width, which is generally the finest feature in the device. In addition to vertical and lateral scaling of transistor dimensions, increasing HBT bandwidth requires a simultaneous reduction in emitter and base contact resistivities and an increase in operating current density (normalized to emitter junction area). A key challenge in the fabrication of THz InP HBTs is, therefore, establishing low resistance Ohmic contacts that are thermally and electrically stable to thin semiconductor layers and implementing these contacts in a high-yield and scalable process flow.

A. HBT Design and Process Flows

InP HBT epitaxial layers can be grown by molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD). DHBT structures using InP emitter and collector regions are preferred due to the higher breakdown voltage provided by the wider bandgap InP collector. High-performance DHBTs have been realized with both InGaAs and GaAsSb base semiconductor layers. The GaAsSb system has a type II band offset with InP which eliminates the conduction band barrier at an abrupt GaAsSb/InP base-to-collector interface [21]. However, hole mobilities in GaAsSb are lower than those of InGaAs [22], resulting in higher base sheet resistances at comparable thicknesses and doping levels. The highest reported f_{max} from a GaAsSb-based HBT is 882 GHz, as reported in [23].

Our DHBTs are grown by MBE and utilize an InGaAs base layer with grading layers between both the InP emitter and collector regions to remove conduction band discontinuities. The base-emitter grade reduces HBT turn-on voltage and has been found to improve the forward current ideality factor (N_C) compared to an abrupt base-emitter junction [24]. A proper base-collector grade design is critical to avoid current blocking and to enable high current density operation. Our grade consists of a chirped superlattice of InAlAs/InGaAs layers with a linear varying composition followed by a pulse doping layer to compensate for the induced quasi-electric field [25]. The grading layers must also be vertically scaled through successive HBT scaling generations. For our 130-nm DHBT process, 30 nm of setback and grading layers are followed by a 70-nm N^-InP layer.

An example of a self-aligned mesa HBT process flow is outlined in Fig. 1. In InP HBTs, the critical alignment is between the emitter and base contacts, and the self-alignment referred to is between the outer edge of the emitter contact and the inner edge of the base contact. Typical base sheet resistance for scaled-InP HBT epitaxy is in the range of 500–1000 Ω/sq. and minimizing the base-emitter spacing is critical for RF performance. The spacing must be sufficient to avoid short circuits between the emitter and base electrodes, and maintain adequate transistor current gain. The surface recombination velocity of InGaAs is significantly less than GaAs (10^3–10^4 cm/s versus 10^6cm/s [24]) and the current gain in highly scaled InP HBTs can be limited by base current recombination at the base contact through a surface inversion layer created by interface trap states [26]. The THz HBTs that we report on have base-to-emitter separations of <40 nm and current gains β in the range of 15–20.

Methods for forming self-aligned base-emitter contacts include undercut of the emitter semiconductor [27] or emitter metal electrode [28] to permit evaporation and liftoff of a thin-base metal contact or the use of dielectric sidewall spacers to separate the emitter and base metals [29], [30], [31], [32]. In spacer processes, the sidewalls, typically Si_xN_y or SiO_2, are formed using a conformal dielectric deposition followed by an anisotropic reactive ion etch. This is facilitated by having an emitter contact with a vertical sidewall profile and large height-to-width aspect ratio. We form our emitter contacts using an Au-electroplating process on a refractory metal plating base. After forming the Au contact, a combination dry/wet etch process is used to form the emitter mesa. Similar

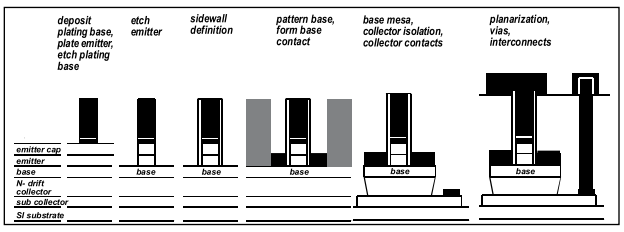

Fig. 1. ***Self-aligned mesa-HBT process flow.***

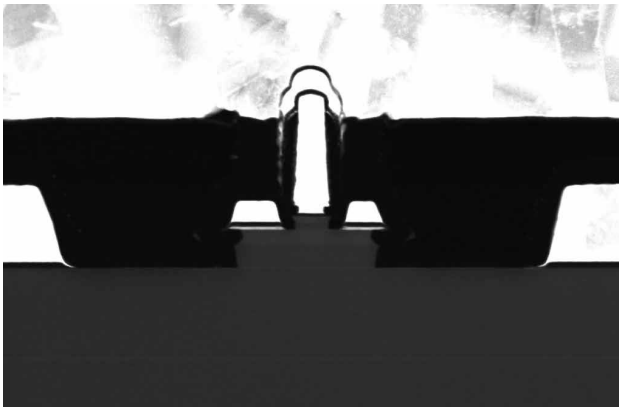

Fig. 2. ***TEM cross section of 130-nm InP HBT.***

emitter contact profiles can also be obtained using dry-etched refractory metal emitter contacts [29], [33].

Ohmic contact resistivities are critical to scaled HBT performance. With proper surface preparation and contact selection, Ohmic contact resistivities approaching 3.5–4x the Landauer limit have been reported to highly doped n-type and p-type InAs and InGaAs layers [34]. Contact resistivities of $(0.6\pm0.4)\times10^{-8}\,\Omega\text{-cm}^2$ were obtained for molybdenum-based contacts to n-type InAs layers with $8.2\times10^{19}\text{cm}^{-3}$ active carrier concentration in [35]. The contacts were deposited *in situ* in the MBE growth chamber immediately after epitaxy growth to avoid surface oxidation and contamination from exposing the sample to air. In [36], contact resistivities of $(1.0\pm0.7)\times10^{-8}\,\Omega\text{-cm}^2$ and $(1.5\pm0.9)\times10^{-8}\,\Omega\text{-cm}^2$ were obtained to p-type InGaAs layers doped at $1.5\times10^{20}\text{cm}^{-3}$ using *in situ* and *ex situ* iridium-based contacts, respectively. These record low contact resistivities were achieved on relatively thick (100 nm) epitaxial layers using simplified process flows for fabrication of transmission line model (TLM) structures used for contact resistance extraction. If implemented in device process flows, these resistivities of $1\times10^{-8}\,\Omega\text{-cm}^2$ are suitable for 32-nm scaling generation HBTs with projected transistor cutoff gain frequencies >1.4 THz [20].

To date, contact resistances obtained in full HBT process flows with thinned epitaxial structures are higher, particularly for the base Ohmic contact. For THz bandwidth devices, the base semiconductor thickness is typically <30 nm and base doping levels are made as high as possible to minimize Ohmic contact resistivities. P-doping levels of $> 8\times10^{19}\text{cm}^{-3}$ using a carbon doping source are routinely realized in both InGaAs and GaAsSb systems. High-doping reduces HBT current gain due to Auger recombination. To mitigate this, both doping grading and compositional grading of the base semiconductor can be utilized to introduce a drift field that reduces base transit time.

Our 130-nm HBT process utilizes a 25-nm InGaAs base layer that includes both compositional and doping grading. The Ohmic contact metallurgy is selected to minimize penetration depth into the semiconductor, and the process flow is optimized to minimize surface contamination and process induced damage to the semiconductor surface. Base contact resistivities of $\sim5\times10^{-8}\,\Omega\text{-cm}^2$ with an associated base sheet resistance of ~800 Ω/sq. are extracted from TLM measurements on HBT samples.

HBT device mesas are formed using wet-chemical etch processes that can selectively remove either InP or InGaAs/InAlAs containing layers. After the HBT contact formation and isolation, a spin-on-dielectric, benzocyclobutene (BCB), is used as a final HBT passivation and planarization layer. The BCB is etched back to expose the tall emitter contact eliminating the need for a precisely aligned via to this contact. Vias are formed to the base and collector contacts and an electroplated Au process is used to form the first interconnect level. A TEM cross section of a fabricated 130-nm HBT is shown in Fig. 2.

B. THz HBT Performance

Highly scaled InP DHBTs operate at high current and power densities. Owing to the wide bandgap InP collector, significantly higher breakdown voltages are obtained compared to SiGe bipolar and InGaAs HEMT technologies with comparable bandwidths. At the 250-nm scaling generation, our DHBTs have a 150-nm collector thickness and demonstrate a common-emitter (CE) breakdown voltage $BV_{CEO}\sim$ 4.5 V ($J_E = 10\ \mu\text{A}/\mu\text{m}^2$). At the 130-nm scaling generation, the collector region is scaled to 100 nm with a corresponding breakdown voltage $BV_{CEO}\sim$ 3.5 V. CE IV characteristics for a 130-nm HBT are shown in Fig. 3. Extremely high current (>30 $\text{mA}/\mu\text{m}^2$) and power (>50 $\text{mW}/\mu\text{m}^2$) densities are obtainable due to the highly scaled emitter junction. HBT current gain is limited by the high base doping and narrow base-emitter spacing used to minimize base contact and access resistances. Typical values of β are ~25 and ~18 for our 250- and 130-nm HBTs, respectively.

Accurate high-frequency characterization of THz bandwidth transistors is challenging. Vector network analyzer extenders and on-wafer probes are available that cover

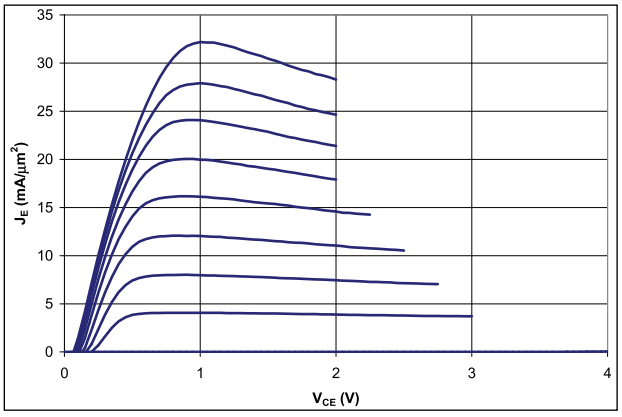

Fig. 3. ***Measured CE I-V characteristics 130-nm HBT [3].***

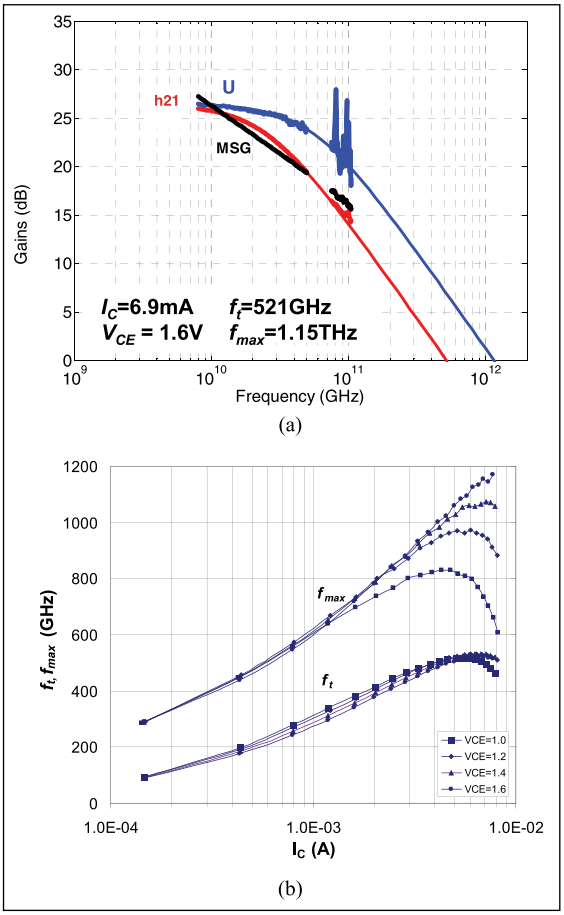

Fig. 4. ***(a) Measured short circuit current gain (H_{21}) and unilateral power gain (U) of 0.13×2 μm² InP HBT [3]. (b) Variation of HBT f_t and f_{max} versus bias.***

frequencies to >1 THz. However, the small parasitics of high-scaled devices make accurate measurement and modeling difficult even at frequencies ~ 1/10th of transistor cutoff frequencies. Reverse transmission ($S12$) measurements are particularly susceptible to corruption through coupling between on-wafer probes or by unwanted mode propagation in semiconductor substrates. To address this, we use extended reference plane thin-film microstrip calibration structures with the ground plane formed in first level metal (M1) and the signal line in the topmost metal [37]. A multiline through-reflect-line (TRL) calibration is performed using on-wafer standards. By placing the calibration reference plane in the middle of a 400-μm-long microstrip line, the on-wafer probes can be adequately spaced apart. The capacitive and inductive loading effects of vias through the BCB interconnect layers are deembedded from the measurements using open and short circuit deembedding structures [38].

Fig. 4(a) shows the measured transistor power gains of a $0.13 \times 2\ \mu m^2$ InP HBT taken from [3]. Measurements were performed from 8–50 GHz and 75–105 GHz. The HBT figures of merit f_t and f_{max} are extrapolated from least squares fits to single-pole transfer functions of the measured f_{max} and unilateral power gain (U), respectively. Fits are performed on the data to 50 GHz, as measurements of U show considerable variation at high frequencies (>75 GHz). The HBT exhibits an extrapolated f_t/f_{max} of 521 GHz/1.15 THz, when biased for peak f_{max} Fig. 4(b) shows the variation of the transistor f_t and f_{max} versus bias. At a total power dissipation of 1.2 mW ($I_C = 1.2$ mA and $V_{CE} = 1.0$ V), the HBT exhibits an f_t/f_{max} of 338 GHz/639 GHz. The high performance achieved at low bias levels makes the devices well suited for analog blocks (variable gain amplifiers, phase shifters, LNAs) in power-constrained RF systems such as millimeter-wave phased arrays with large numbers of elements.

Fig. 5 summarizes the current state of the art for bipolar transistors in terms of RF figures of merit f_t and f_{max}. In this summary, only InP HBTs with $f_t > 300$ GHz and $f_{max} > 600$ GHz have been considered, a reasonable estimate for the bandwidth required to produce useful fundamental circuit operation at the lower end of the THz frequency spectrum (0.3 THz). For organizations with multiple reported results, the graph includes the highest reported f_{max} for a given emitter scaling generation. For comparison, the highest reported bandwidth SiGe HBTs are included on the same graph. InP HBTs achieve much higher bandwidths at comparable scaling generations while realizing ~2x higher breakdown voltage (BV_{CEO}) than SiGe devices. For clarity, InP HEMT and GaN HEMT technologies have not been included in Fig. 5. The highest reported f_{max} for any transistor technology was reported for a 25-nm InP HEMT technology with extrapolated f_t/f_{max} of 0.61 THz/1.5THz [53] enabling amplifier gain at 1 THz. For GaN HEMTs, the highest reported f_{max} of 582 GHz was obtained in a 20-nm gate length technology with a simultaneous f_t of 310 GHz [54].

Efforts to further increase InP HBT bandwidth are being actively pursued. As previously discussed, Ohmic contact resistances required for 32-nm scaling generation devices

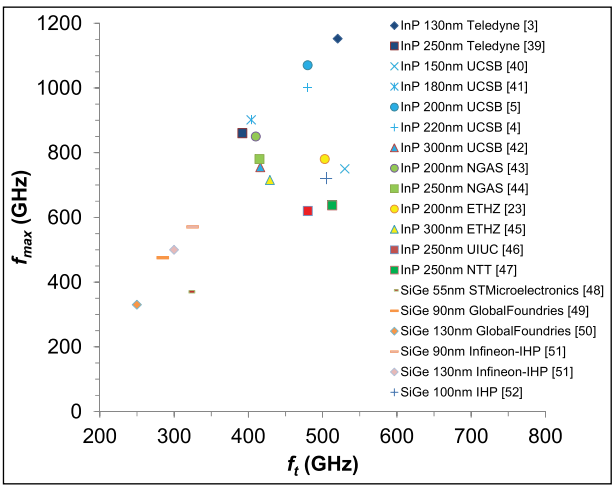

Fig. 5. ***Summary of state-of-the-art RF figures of merit reported for bipolar transistor technologies.***

have been demonstrated showing the feasibility for implementation in full-HBT process flows. As HBT dimensions continue to scale, the impact of extrinsic parasitics elements is also becoming larger. Two impediments to InP HBT performance are the extrinsic parasitic capacitance associated with the base contact pad and base metal sheet resistance down the length of the emitter stripe for narrow-mesa devices [5]. HBT layout and process flows must be tailored to minimize the impact of these parameters as devices continue to scale.

Further shrinking transistor dimensions also presents challenges for maintaining acceptable transistor current gain (β). Current values of β in highly scaled InP processes are low (~15–20) but acceptable for tuned circuit applications. Current gain is presently limited by surface recombination currents that scale with emitter periphery. To maintain β as transistors scale, improvements in surface passivation or epitaxy design will need to be implemented [26]

HBT scaling roadmaps outlined in [20] are driven by thermal considerations. A constant linear current density (mA/μm) is maintained through successive scaling generations to limit the temperature rise in the transistors as the areal current density is increased. Higher performance at a given technology node can therefore be obtained by improving the thermal resistance of the transistor permitting operation at higher linear current densities for the same junction temperature rise. Some recent efforts have looked at transferring InP HBTs to higher thermal conductivity substrates to improve transistor thermal resistance [55], [56]. This adds process complexity and requires a low thermal resistance interface after transfer, but the potential benefits are large. As an example, semi-insulating 4H-silicon carbide (SiC) substrates have 5.7x higher thermal conductivity than InP. Thermal simulations in [55] predicted a 42% reduction in thermal resistance for a transferred substrate HBT to a SiC substrate compared to a conventional mesa HBT on InP.

C. HBT Modeling and Backend Processes

A robust THz IC design environment requires accurate transistor models and a wiring stack that can support low-loss single-mode transmission lines operating up to the frequencies of interest. InP HBT performance in strongly influenced by nonequilibrium electron transport in the collector space charge region [57]. Large-signal III-V HBT models have been developed that capture velocity modulation effects and other phenomenon associated with the base-emittter and base-collector heterojunctions [58]. Since accurate transistor measurements at THz frequencies are difficult, we perform model extraction at frequencies below 100 GHz. The fidelity of the model at high frequencies is supported by the good agreement observed between measured and simulated IC performance at frequencies approaching the transistor's cutoff frequencies.

Many III-V IC processes utilize the semiconductor substrate as the dielectric medium for microstrip or grounded coplanar waveguide (CPW-G) transmission lines. As frequencies increase, this requires aggressive substrate thinning. For HEMT amplifiers operating to 1 THz in [6], the substrate has been thinned to 18 μm. In addition to the fabrication challenge of wafer thinning, substrate-based transmission lines require through-substrate vias that are of comparable dimensions to the substrate thickness (T_{sub}) and lines should be spaced by more than ~ T_{sub} to avoid line-to-line coupling, these two factors can limit integration density.

Top-side thin-film dielectric wiring is an excellent alternative for THz transmission lines. Dielectric loading can negatively impact the performance of highly laterally scaled HEMTs and these devices generally use airbridge interconnects for device wiring with a minimal amount of dielectric passivation, although some recent THz amplifier results have been reported using thin-film wiring [59]. Because of their higher intrinsic transconductance and vertical device geometry, HBTs are less susceptible to dielectric loading than HEMTs and are generally integrated with multilevel thin-film wiring. Fig. 6 shows a cross section of thin-film wiring utilized for our highest frequency TMICs. The wiring utilizes a BCB interlayer dielectric (εr = 2.7) and electroplated Au-based metallization. The first two wiring levels (M1, M2) are separated by a 1-μm BCB layer. These layers support narrow lines and fine pitch and can be used for low delay, low parasitic wiring in lumped analog circuit blocks. The upper level metallization (M3) is separated from M1 by a thicker 7-μm BCB layer. These layers can be used to form low-loss microstrip or CPW-G lines using either standard (M3 signal, M1 ground) or inverted (M1 signal, M3 ground) configurations, with the selection depending on the circuit configuration and frequency of operation. Fig. 7 plots the simulated insertion loss of a 50-Ω thin-film microstrip transmission line at 670 GHz and 1.03 THz versus the BCB dielectric thickness. We see that a 7-μm thickness offers a good compromise for circuit compactness (line width) and line loss.

The use of top-side thin-film wiring permits the use of thicker substrates than could be used with substrate-based transmission line wiring with a back-side ground plane. Substrate thinning and through-wafer vias are still required for substrate-mode control in packaged ICs. For

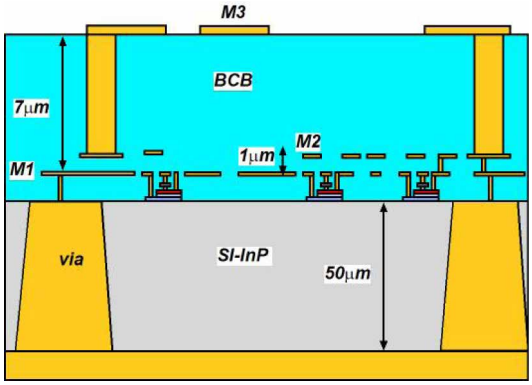

Fig. 6. *Schematic cross section of InP HBT IC thin-film wiring environment.*

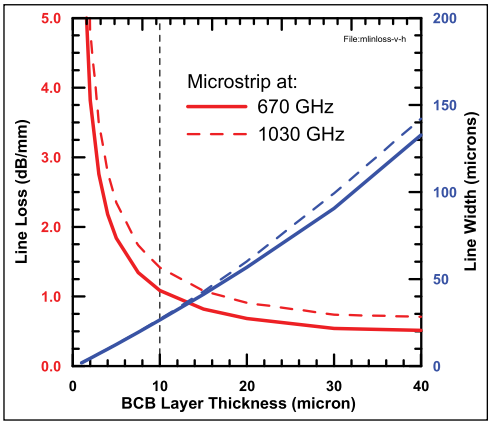

Fig. 7. ***Simulated insertion loss and required line width versus dielectric thickness for realization of 50-Ω thin-film microstrip transmission line with BCB interlayer dielectric.***

our 600-GHz TMIC process, wafers are thinned to 50 μm and through-substrate vias are formed using an elevated temperature inductively coupled plasma (ICP) etch process. To facilitate waveguide packaging, this etch process is also used for die singulation. This process permits the formation of narrow InP extensions that can support waveguide probes (waveguide-to-chip transitions) that extend into rectangular waveguide channels. The extension minimizes the break in the waveguide sidewall, and the etch process can be used to remove the substrate immediately beneath the probe improving probe performance.

III. MILLIMETER-WAVE AND SUBMILLIMETER-WAVE PAS

Given their high bandwidths and power handling, a valuable application for THz HBTs is in the area of PAs operating above 100 GHz at the low-loss operation "windows" (140, 220, 330, 670, and 850 GHz) in the Earth's atmosphere. Here, radiation can travel substantial distances, and thus has motivated research and the development of a wide variety of systems, including: very high data rate point-to-point links; personal imaging systems for detecting concealed weapons; and synthetic aperture radar (SAR) systems operating with multiple frame rates per second which can track maneuvering targets and image scenes on the battlefield.

Even at lower millimeter-wave frequencies such as V-band (40–75 GHz), E-band (60–90 GHz) [60], [61], and W-band (75–110 GHz), InP HBT PAs can generate significant RF power; comparable in linear (W/mm-device periphery) and areal (W/mm^2-chip area) power density to those obtained in high-voltage gallium nitride (GaN) HEMT designs. High-capacity, low-cost, mobile data links have been under extensive development at E-band (71–76 GHz and 81–86 GHz) and W-band frequencies (92–95 GHz) for use in military and commercial platforms. The 102–109.5-GHz band in the United States has recently been petitioned [62] for similar use, with 10-Gb/s wireless data transmission a key application. In platforms or devices with limited available prime/source power, PAs with the highest possible efficiency are very beneficial. Additionally, for systems that utilize multiple frequency bands, having a single PA that operates across those bands reduces system complexity—a PA covering both 71–76- and 81–86-GHz bands is an example.

Our high-frequency PA development has been focused on our 250-nm HBT node that offers high RF figures of merit ($f_t/f_{\max}$ 370 GHz/750 GHz) with good breakdown voltage ($BV_{CEO} = 4.5$ V). Compared to 250-nm InP HBTs, competing GaAs pHEMT and GaN HEMT millimeter-wave PA technologies have higher breakdown and operating voltages. Despite this, InP HBTs can achieve similar operating power densities due to the high current density supported by the devices. Because the bias currents of the InP HBT PA designs will be much higher, careful consideration of the direct current (dc) bias network is required. Through novel design and layout, CE and cascode PA cells have been developed to overcome the challenges of high-current distribution, and 4-, 8-, and 16-way combined PAs have been demonstrated. This has led to the development of state-of-the-art PA's operation between 70 and 260 GHz [60], [63].

In this section, we review PA topology considerations for a given operating frequency in our 250-nm HBT technology. State-of-the-art PAs covering G-band and H-band will be reviewed. These amplifiers ICs have been packaged and power combined into larger solid-state PA (SSPA) modules and are being used to drive diode-based frequency multipliers to increase broadband THz source power.

A. PA Unit Cell Design

Key design decisions for the HBT unit-cell design in SSPA MMICs include: identifying the appropriate geometry and layout for a single HBT cell, choice of PA cell topology, and how to combine PA cells for a given output power objective. Considerations associated with the HBT geometry and layout have been reported in [64]; for this paper, we will focus discussions on the PA cell topology and how the cells are combined. For a given operating frequency, it is important to consider not just the small-signal gain of the HBT at the dc quiescent point, but also how much gain it has over its designated operating load line. At a given static quiescent dc bias, the gain may be high, but under large-signal operation, the gain at I-V points away from the dc bias can be modulated to lower values, leading to "soft" gain compression and lower saturated output power from the transistor.

Fig. 8 shows gain simulations for a 250-nm InP HBT, in CE and common-base (CB) configuration generated using our large-signal HBT model. In the graphs, either the maximum available gain (MAG) or the maximum stable gain (MSG) are plotted depending on the stability factor at the bias condition. The bias points corresponded to the load line that is superimposed on the graphs. Plots are shown at 90, 140, 220, and

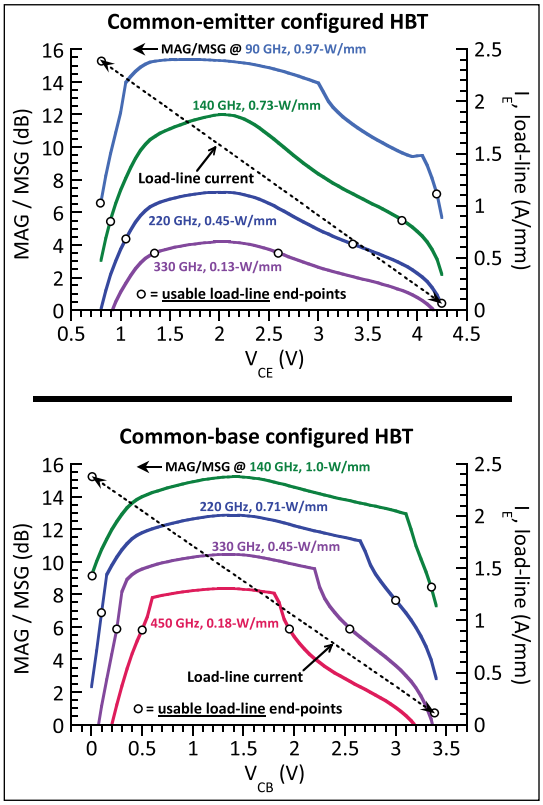

Fig. 8. ***Simulations of the HBT gains at the voltage–current pairs along a class-A PA load line for a multifinger 24-μm 250-nm InP HBT. The plots show HBT CE MAG/MSG (top) and CB MAG/MSG (bottom) across multiple operating frequencies.***

330 GHz, along with the simulated values of saturated output power density under optimum load match conditions. It is acknowledged that the MAG/MSG values overstate what the actual gain for the PA design would be—these plots are intended to be only a guide for making HBT topology decisions. Examination of the CE plot shows that at 90- and 140-GHz peak gain is 12–15 dB, with significant usable load-line boundaries, set where the gain becomes 5–6 dB. Based on these values, the CE topologies have been used for PA designs through the W-band (110 GHz).

At 220 GHz, the lower CE gain and achievable power density significantly reduce the usefulness of the configuration for a PA, and at 330 GHz, CE configured PAs are not feasible. The load-line plot for a CB configured HBT shows that there is significantly more gain and achievable power density above 220-GHz operation, even up to 450 GHz. For the 220-GHz PAs that we have demonstrated, cascode topologies have been utilized due to challenges of stabilizing multistage CB amplifiers.

B. G-Band and H-Band PAs

For the 220-GHz PAs, the cascode topology satisfies our requirements of high per-stage gain, and high PA output power density. For highest output power from a PA cell, maximizing the HBT periphery is key, and at 220-GHz operation, unit finger length and device self-heating must be considered in its design. Details of the PA cascode unit cell design have been covered elsewhere [9], [65]. Fig. 9 shows a circuit schematic for a typical PA cascode cell utilizing a 20-μm CE HBT (four-finger $\times 5$ μm L_e) and a 24-μm CB HBT (two-finger $\times 12$ μm L_e). The output power match of each PA cell is a 50-Ω impedance.

For 2^n corporate power combining, the losses from the on-chip combiner and path length between PA cells degrade combining efficiency. Once these overall losses reach 1.5–2 dB, spatial power combining must be considered for higher output power. In our designs, power cell combining is accomplished using low-loss 2-way and 4-way structures. Because the combiners have only 0.5-dB insertion loss, up to 16-way PA-cell on-chip combining is feasible and has been demonstrated. Increasing RF output power per MMIC is important due to the challenges associated with power combining of multiple MMICs in a waveguide assembly at submillimeter-wave frequencies. These challenges include identifying PAs having similar gain and phase characteristics, maintaining high RF isolation between PA chips and waveguide blocks, build-to-build variations generating chip-to-chip phase mismatch, and increased dc bias complexity. A circuit layout of a 4-way combined PA is shown in Fig. 9. Higher power is achieved using the four-cell design as a basis and combining two or four of them to accomplish 8-way or 16-way PA-cell combining. Details of the structures designs have been reported in [66].

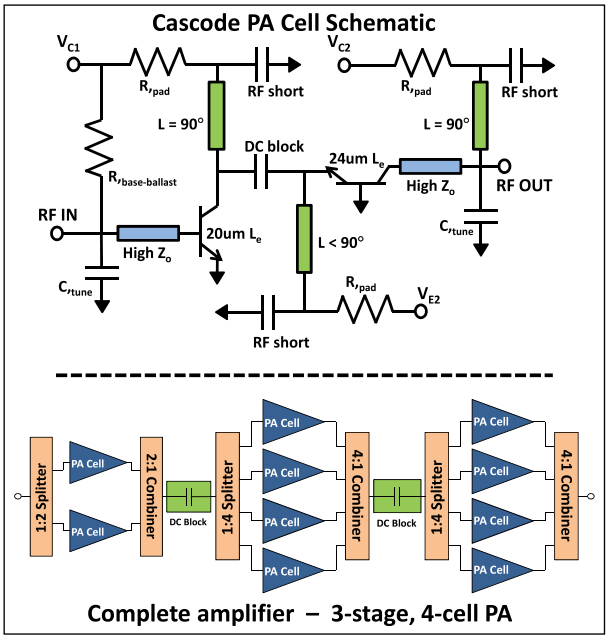

Fig. 9. ***Schematic of the 220-GHz cascode PA cell (top) and a block diagram of the three-stage, 4-PA cell output combined solid-state PA presented (bottom).***

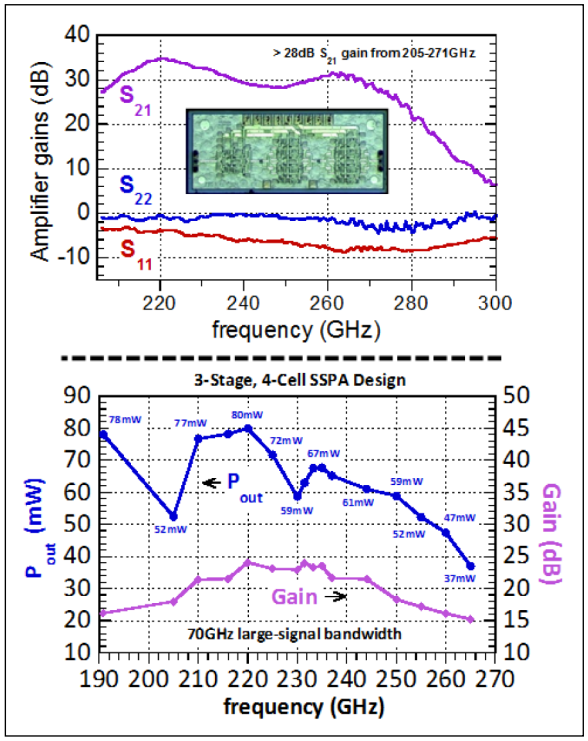

Fig. 10. *IC micrograph and RF summary of the three-stage, 4-PA cell combined G 220-GHz PA design. Dimensions: 1.92mm × 0.80mm. [63]*

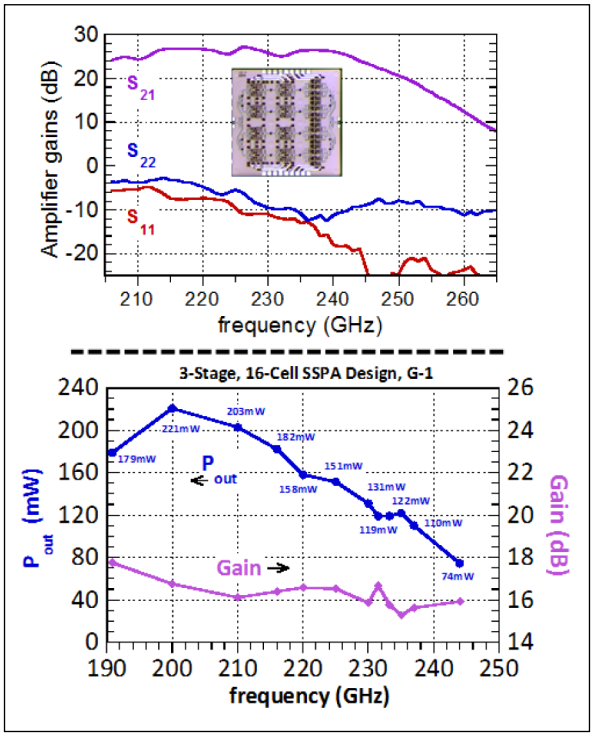

Fig. 11. *IC micrograph and RF summary of the three-stage, 16-PA cell combined 220-GHz PA design. Dimensions: 1.95mm × 1.90mm. [9]*

Amplifier results from a three-stage 4-PA cell amplifier are shown in Fig. 10 [63]. The amplifier dissipates 1.77 W of dc power. The large-signal bandwidth is 70 GHz (190.8–260 GHz) covering most of the WR04 waveguide band. The power peaks to 80 mW at 220 GHz and remains high at 260 GHz where it is 47 mW. Amplifier results from a three-stage 16-PA cell amplifier are shown in Fig. 11 [9]. It dissipates 5.81 W of dc power. The large-signal bandwidth is 45 GHz (190–235 GHz), and the power peaks to record 220 mW at 200 GHz, is 208 mW at 210 GHz, and remains high at 235 GHz where it is 122 mW.

Table 1 provides a performance summary of state-of-the-art SSPAs at the MMIC and module level near 200 GHz. At the MMIC level, InP HBT-based PAs demonstrate the

Table 1 Summary of State-of-the-Art Solid-State PAs Around 200 GHz

Ref	Technology	MMIC/Module	Freq. GHz.	Pout mW	Gain dB	PAE %.
[71]	250 nm InP HBT	3-stage MMIC	191-244	80-50	22-20	4.5-2.8
[63]	250 nm InP HBT	3-stage MMIC	191-244	139-75	20-14.5	-
[9]	250 nm InP HBT	3-stage MMIC	200-235	221-125	15.6-13.2	4-2
[72]	250 nm InP HBT	2-stage MMIC	210-225	90-65	8.2-7.7	-
[73]	250 nm InP HBT	2-stage MMIC	208-220	180-145	11	-
[74]	250 nm InP HBT	1-stage MMIC	220-235	50-40	2.5-1.9	6.7-5.5
[75]	250 nm InP HBT	1-stage MMIC	205-235	90-50	4.5-3	10-5
[75]	250 nm InP HBT	2-stage MMIC	205-235	112-62	6-4	5.1-2.2
[68]	40 nm GaN HEMT	1-stage MMIC	180	23.7	1.8	3.5
[67]	sub-50 nm InP HEMT	Single-MMIC Module	200-230	75-40	11-9.5	3.7[a]
[67]	sub-50 nm InP HEMT	2- MMIC Module	210-225	113-100	12.5-10.5	-
[67]	sub-50 nm InP HEMT	4- MMIC Module	210-225	185-150	8	-
[69]	250 nm InP HBT	32-MMIC Module	230	710	>25	-
[76]	250 nm InP HBT	16-MMIC Module	205-233	450-233	-[b]	-
[70]	250 nm InP HBT	16-MMIC Module	200-230	820-380	-[c]	-

Freq. refers to range over which large signal parameters are reported
Listed ranges of Pout, Gain and PAE are over the entire measured Freq. range and do not necessarily refer to measurements at the min. and max. Freq. Gain and PAE are reported for the given Pout values. When not listed, PAE has not been reported.
[a] PAE only reported at 210 GHz [67]
[b,c] Large-signal gain not reported in [76] and [70]. Reported small-signal gains were 20-10 dB and >10 dB in [76] and [70], respectively.

highest output power level with the only demonstration of >200-mW output power at >200 GHz. The highest reported output power from an individual InP HEMT MMIC is 75mW at 210 GHz from a sub-50-nm InP HEMT technology [67]. This result was reported for a packaged module and includes the loss from the IC-to-waveguide transition. The bandwidths of GaN HEMT devices have been increasing rapidly in recent years and the technology has demonstrated the highest per chip output power levels at W-band (75–110 GHz). To date, the only reported PA result at G-band in GaN is a single-stage amplifier that demonstrates 24 mW of output power with 2-dB associated gain at 180 GHz [68]. In all technologies, power added efficiencies (PAEs) at the MMIC level around 200-GHz remain low (<10%). This is a function of bandwidth limitations and combining losses at these frequencies. Further transistor scaling and bandwidth improvements will increase PAE assuming breakdown voltages are maintained and it is reasonable to assume that PAE values approaching the current state of the art at W-band (20%–30%) can eventually be obtained.

At the module level, only packaged InP HEMT and HBT amplifiers have been reported. In [67], a four-chip combined InP HEMT module was reported with peak 185-mW output power at 210 GHz and demonstrates greater than 150 mW to 225 GHz. Recently, much higher levels of power combining have been demonstrated using Teledyne's 250-nm InP HBT PAs. Raytheon-RRI has demonstrated a 32-PA combined module using three-stage 4-PA cell SSPAs with 710 mW of output power at 230 GHz [69], and in [70], Nuvotronics reported a 16-PA module using two-stage, 8-PA cell SSPAs demonstrating 823 mW of output power at 216 GHz. These results have radically improved upon state-of-the-art output power by 3–4× for solid-state modules at 210–230-GHz operation. As the InP HBT PA MMICs are optimized and output power increases, the power from these modules will exceed 1 W in the near future.

The availability of high-power broadband G-band and H-band PAs is extending the state of the art for THz signal generation using diode multiplier chains. Virgina Diodes Inc. (VDI) has packaged a 220-GHz three-stage, four-cell 250-nm InP HBT PA and demonstrated full WR04 waveguide band operation [77]. This work has led to the development and demonstration of the first ever 1.1–1.5-THz VNA extender system covering the full WR0.65 waveguide band [78]. VDI has also used these PAs to demonstrate a 325–500-GHz doubler source with 0.5–1.0 mW of output power, a 500–750-GHz tripler source with 0.2–0.6 mW of output power, and through subsequent tripling a 1.6–2.2-THz source with 0.1–2.3 μW of output power [77]. Through the use of higher PAs covering the full WR04 band, the THz power achievable from the multiplier sources will increase and become competitive with their narrowband diode-based sources, as well as the solid-state InP HEMT PA results reported at 670 GHz (3 mW) [79] and 850 GHz (1 mW) [80].

IV. THz MONOLITHIC ICS

We now describe HBT ICs operating in the THz frequency spectrum (>0.3 THz). At the 250-nm scaling generation, InP HBT-based ICs have been demonstrated operating above 300 GHz, while amplifier gain and fundamental signal generation have been demonstrated at >600 GHz in the 130-nm HBT technology. THz HBT circuit design principles and circuit demonstrations are reviewed including results from highly integrated transmitter and receiver ICs.

A. THz HBT Amplifiers

1) Amplifier Topologies: At THz frequencies, matching network losses are high and transistors may be operating at a significant fraction of their device f_{max}. The gain per stage of amplifiers can therefore be relatively low and amplifier topologies must be selected with this in mind. For HBT amplifiers, this generally necessitates the use of a CB topology. Due to the reduced Miller capacitance, the maximum available gain of a CB stage is significantly higher than that of a CE configured device. However, the CB configuration is inherently less stable than CE, and its stability and bandwidth are extremely sensitive to any base inductance. This inductance includes extrinsic inductance associated with any grounding connections to the base terminal and intrinsic inductance associated with narrow base-metal contacts along the length of the device. Near 600 GHz, we have observed that even 1 pH of unmodeled base inductance can lead to destabilization of an amplifier stage design.

Various design strategies can be used to mitigate the issues associated with CB ground inductance and stability. In all cases, extensive electromagnetic simulation of designs is required to accurately model wiring parasitics. To reduce intrinsic base inductance, short emitter stripes are preferred. Typical designs near 600 GHz use emitter stripe lengths < 6 μm. Additionally, two base-via contacts on either end of the base finger can be employed to reduce the effective inductance by one-half compared to a standard device with a single base via. Using coplanar waveguide (CPW) transmission line wiring the two base via contacts can be tied directly to a first metal ground plane providing an extremely low inductance ground connection. This has been successfully implemented in amplifier designs operating to >670 GHz [7].

Differential design topologies can also be used to minimize bandwidth reduction and stability issues associated with single-ended ac grounds. A virtual ground is present at the plane of symmetry in a differential design making the designs insensitive to common-mode impedances like those contributed from via inductances and bias circuitry. With sufficiently low common-mode gain, differential designs can be driven with a single-ended signal and remain well balanced, offering high performance, albeit with a 2x dc power penalty over comparable single-ended designs. Balun structures although relatively lossy at THz frequencies are

also compact and can be used for output power combining if desired. The differential amplifier topology also integrates well with differential mixers for transceiver integration.

2) Amplifier Results: 250-nm InP HBTs have been used for amplifier demonstrations around 300 GHz. Using cascode gain stages, 300-GHz driver amplifiers have been reported with 10- and 20-mW saturated output power in [81] and [82], respectively. These results compare favorably to highest reported output powers from InP HEMT technologies at these frequencies. In [83], a 10-mW HEMT module was reported and the MMIC level output power from this part was estimated to be ~13 mW.

Around 300 GHz, HBT LNA noise figures (NFs) of ~11 dB have been reported from on-wafer measurements of cascode and CE HBT amplifiers in [84] and [85], respectively. In [86], a packaged LNA module is reported with ~13-dB NF at 300 GHz. Comparatively, amplifiers have been reported with ~ 6-dB NF at 300 GHz in sub-50-nm [88] and 35-nm [88] InP HEMT and mHEMT processes, respectively. Reported HBT LNAs at these frequencies operate at significantly higher linear current densities (1–2 mA/μm) than comparable HEMT amplifiers (<0.5 mA/μm). The associated shot noise is the largest noise contributor in the device and translates to higher noise figure in the HBT amplifiers. With further scaling, the noise figure of HBT amplifiers can be improved as gain stages can be operated at lower current densities while maintaining adequate per stage gain.

Fig. 12 shows a chip photograph and measured S-parameters for the highest frequency HBT amplifier that has been reported [7]. The nine-stage CB amplifier was fabricated in our 130-nm HBT technology and utilizes inverted grounded coplanar waveguide wiring (CPW-G) with signal

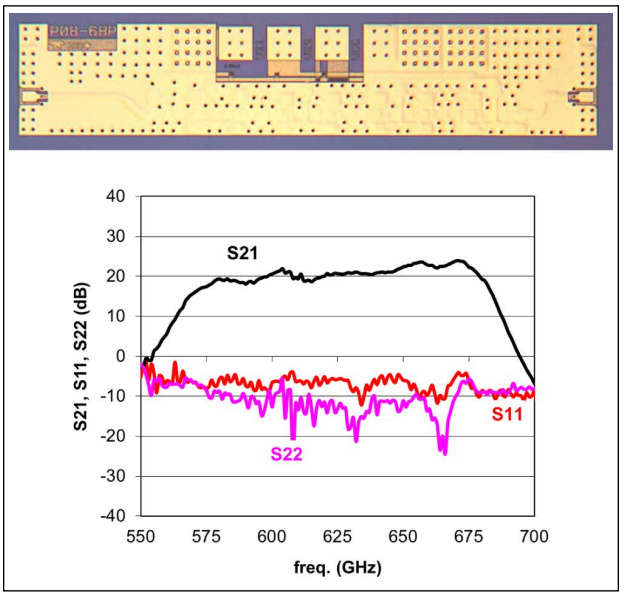

Fig. 12. ***Chip photo of nine-stage 670-GHz CB amplifier and measured S-parameters [7]. Chip dimensions: 1.2 × 0.25 mm².***

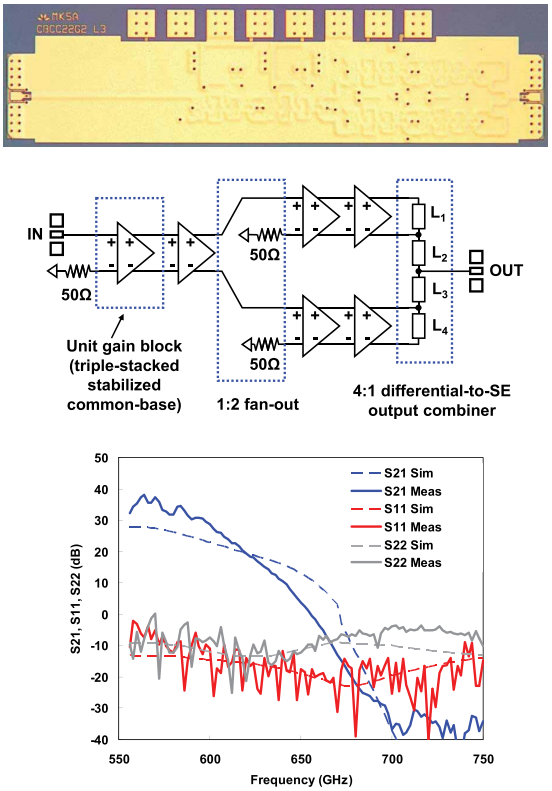

Fig. 13. ***Chip photo, circuit schematic, and measured S-parameters of differential 600-GHz CB amplifier [8]. Chip dimensions: 1.36 × 0.34 mm².***

lines and a coplanar ground planes in M1 metallization and an M3 ground plane that covers the entire circuit area. Amplifier S-parameter measurements were performed on-wafer using Virginia Diodes Inc. (VDI) 500–750-GHz network analyzer extenders and Dominion Microprobes WR-1.5 on-wafer probes. At 670 GHz, the amplifier demonstrates 22-dB gain and the gain is ~20 dB from 600–680 GHz. On-wafer power measurements were performed on the design correcting for output probe losses. The amplifier demonstrated a saturated output power of -4.0 dBm (0.4 mW) at 585 GHz and subsequent testing at 670 GHz gave a saturated output power of -7.5 dBm (0.18 mW). Higher output power levels at a lower frequency (-0.65 dBm at 585 GHz) were achieved using an eight-stage amplifier with a similar topology and larger emitter periphery devices [7].

Corporate power combining to increase amplifier output power level at these frequencies is challenging due to interconnect losses. Fig. 13 shows a chip photograph of a 600-GHz CB amplifier that utilizes a novel dual-branch differential topology that is four-way output power combined to increase amplifier output power [8]. The differential signal provides a convenient way of 1:2 signal splitting without a passive splitter or balun. The four single-ended outputs of the final gain blocks are combined using a passive combining network. Fig. 13 shows measured S-parameters

of the 600-GHz differential amplifier. At 585 GHz, on-wafer power measurements gave a saturated output power of 2.8 dBm (1.9 mW). The power decreases to 1.1 dBm at 620 GHz (1.3 mW).

Other HBT amplifiers operating near 600 GHz were reported in [43] using a 200-nm transferred-substrate InP technology. A nine-stage CE amplifier was reported demonstrating ~9-dB gain at 521 GHz and a five-stage CB design was reported with ~19-dB gain at 576 GHz corresponding to an extremely high gain per stage of 3.8 dB. No output power results were reported from these amplifiers.

The gain per stage of HBT amplifiers near 600 GHz is competitive with those reported from InP HEMT amplifiers near these frequencies (2–3 dB) [89], [59]. HEMT amplifiers have been reported operating to higher frequencies with amplifiers reported at 850 GHz [80] and 1 THz [6]. Packaged HEMT amplifier modules have been demonstrated with NFs of 15 dB and 600 GHz [90] and 13 dB at 670 GHz [89]. The simulated NF of the HBT amplifier in Fig. 11 is 20 dB at 670 GHz. At these frequencies, saturated output power is limited by large-signal gain compression and not by transistor power handling and the higher breakdown voltage of InP HBTs has not benefited PA ICs. A HEMT amplifier TMIC has been reported with 3.8 dBm (2.4 mW) of output power at 643 GHz at the circuit level, and a packaged module combining two such TMICs has been reported with 4.8 dBm (3 mW) of output power at 653 GHz [91].

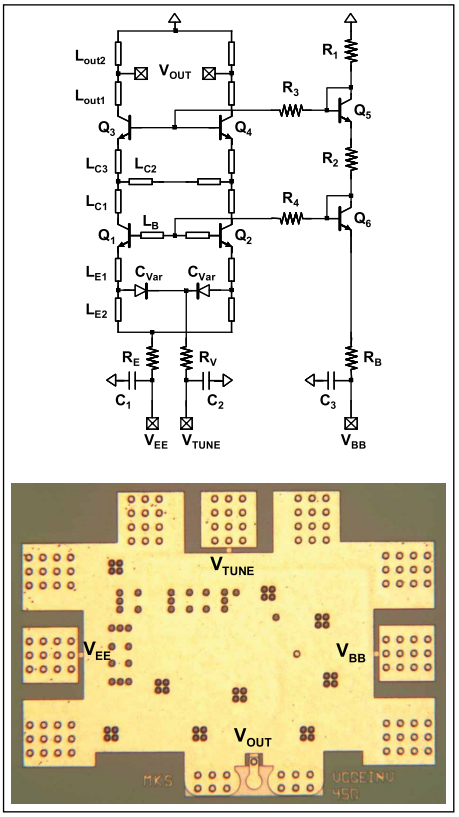

Fig. 14. ***Circuit schematic and chip photograph of differential VCO circuit. Chip dimensions: 0.74 × 0.55 mm².***

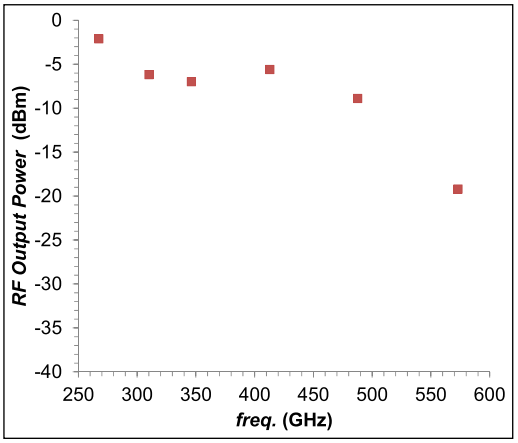

Fig. 15. ***Output power versus frequency of InP HBT THz oscillators [10].***

B. THz HBT Frequency Sources

Local oscillators for THz radio systems can be generated using multiplier chains or on-wafer signal sources. Oscillator circuits can be designed for increased signal power at harmonics enabling RF power generation at close to or beyond the transistor f_{max} [92]. [93], [94], [95], but when possible, fundamental oscillators are generally preferred as they are simpler and more power efficient with no need for filtering subharmonic outputs. Using our InP HBT technologies, we have demonstrated fundamental oscillators operating to >600 GHz with a differential topology that includes an output buffer. Both fixed frequency and voltage controlled oscillators have been realized. This type of oscillator design has been used in phase-locked loop (PLL) circuit designs at 220 GHz [96] and 300 GHz [97] enabling the realization of compact/tunable low phase noise sources.

1) Oscillator Designs: Fig. 14 shows a circuit schematic and chip photograph of a differential oscillator design. The differential topology is advantageous for integration in fully differential transceiver architectures improving common-mode noise rejection and LO leakage cancellation. The schematic in Fig. 14 is shown for a voltage controlled oscillator that utilizes varactor diodes (CVAR) formed with the HBT base-collector junction. Fixed-frequency designs without these varactors have also been fabricated. Typical dc power consumption is between 75 and 115 mW. At the 250-nm HBT scaling generation, oscillators have been realized at frequencies ranging from 220 to 570 GHz [10]. Frequency and power characterization of the oscillators has been performed on-wafer. Fig. 15 summarizes oscillator measured output power versus frequency for fixed-frequency oscillator designs.

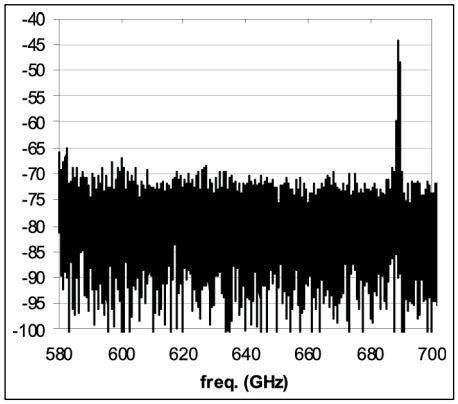

Fig. 16. ***Output spectrum of fixed frequency 688-GHz fundamental oscillator using 130-nm InP HBTs. Measurement is taken on-wafer using Virginia Diodes VNA Extender heads for downconversion. Power measurement is uncalibrated.***

Similar oscillator designs have now been realized in our 130-nm HBT technology. At this scaling node, oscillators have been realized operating to >600 GHz. Fig. 16 shows the output spectrum of a fixed frequency 688-GHz oscillator taken using a VDI VNA extender head for downconversion. The power from this measurement is uncalibrated and at this time power measurements of oscillator designs in the 130-nm technology have not been performed.

2) Phase-Locked Loop Designs: Using voltage controlled oscillator designs we have demonstrated fundamental phase-locked loops (PLLs). Fig. 17 shows a circuit schematic and a chip photograph for a 220-GHz PLL circuit fabricated in our 250-nm HBT process [96]. Along with the voltage controlled oscillator, the circuit consists of 2:1 dynamic frequency divider and a fifth-order subharmonic phase detector. A conventional lag-lead loop filter is included on-wafer and the loop bandwidth is 150 MHz. This design includes a two-stage differential output amplifier to obtain a targeted output power of -1 dBm. The total power consumption is 463.5 mW.

The fabricated PLL IC was characterized on-wafer with the output downconverted by a subharmonic mixer and phase noise was measured by spectrum analyzer. Fig. 18 shows the measured output spectrum (uncalibrated) and phase noise of the PLL. The measured phase noise was -61 dBc and -83 dBc at offset frequencies of 10 and 100 kHz. Beyond 300-kHz offset, the measurement was limited by the spectrum analyzer noise floor.

C. THz HBT Integrated Transmitters and Receivers

With the building block circuits that have been developed integrated THz transmitter and receiver circuits have been realized. Fig. 19 shows a chip photograph of an integrated 570-GHz receiver circuit fabricated in our 130-nm HBT technology. The circuit consists of a 190-GHz voltage controlled oscillator, an LO buffer amplifier, a third-order

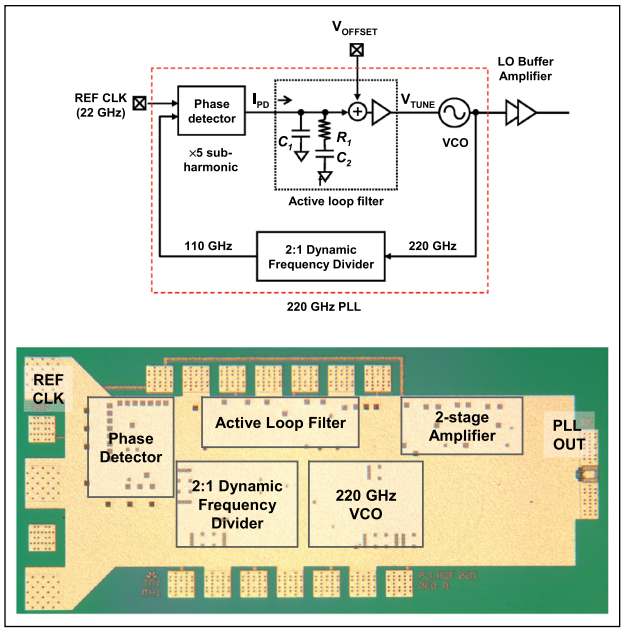

Fig. 17. ***Circuit schematic and chip photograph of 220-GHz PLL circuit. Chip dimensions: 1.57 × 0.7 mm^2.***

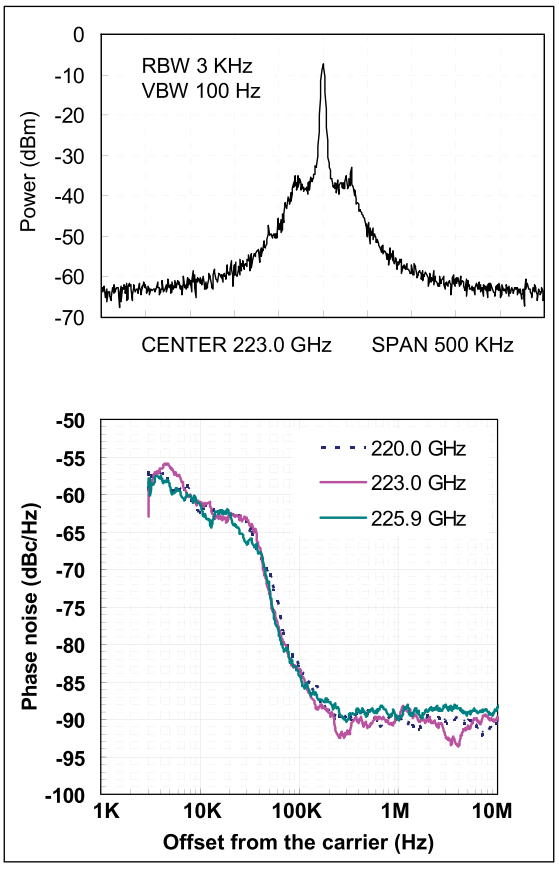

Fig. 18. ***Measurement of close-in output spectrum (power level uncalibrated) and phase noise of 220-GHz PLL output.***

downconverting subharmonic mixer based on a double-balanced architecture and an eight-stage CB CPW-G amplifier similar to that in Fig. 11.

The receiver was characterized on-wafer using a Dominion Microprobe WR1.5 waveguide probe with a WR1.5 horn antenna. A 600-GHz multiplier chain source was coupled into the receiver to identify the LO frequency generated by the VCO. Fig. 19 shows the measured IF output spectrum for a 576-GHz input signal. The LO frequency is 194 GHz. Note, this measurement was not calibrated for source input power. Noise figure and receiver gain measurements were performed using the Y-factor method with a hot and cold source, with the antenna input shuttered between a room temperature (290 K) absorber and a liquid nitrogen bath (77 K). The receiver IF output was fed to a 2-GHz low-noise IF amplifier chain with a 300-MHz bandpass filter and this output was measured with a power detector. Fig. 18 shows the measured receiver gain and noise figure versus frequency. The LO frequency was varied by changing

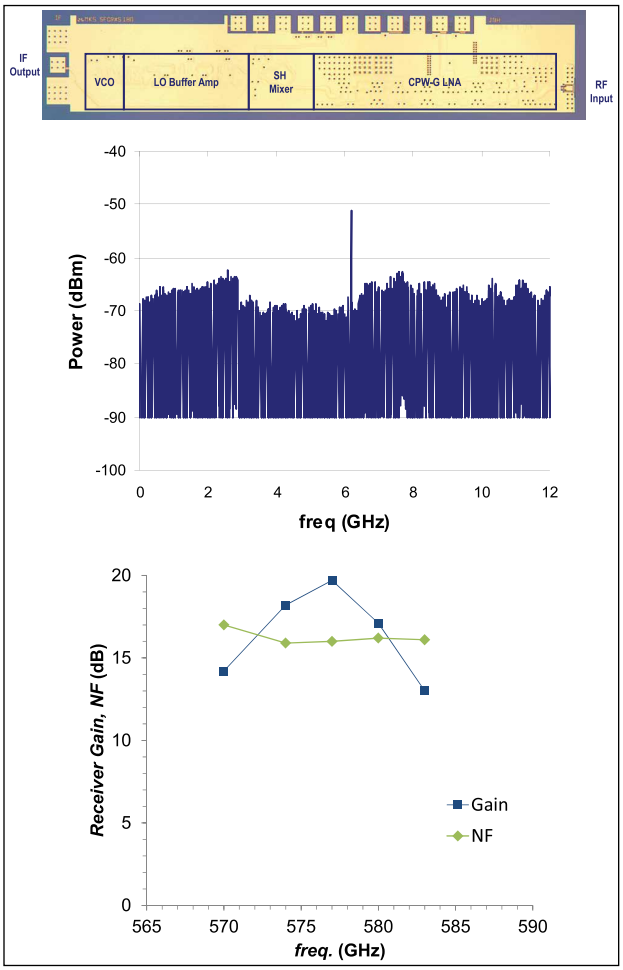

Fig. 19. ***Chip photo of integrated 570-GHz receiver circuit (top). Measured output spectrum of receiver with 576-GHz input signal (middle). Measured receiver gain and noise figure of receiver versus RF frequency (bottom). Chip dimensions: 2.4 × 0.45 mm².***

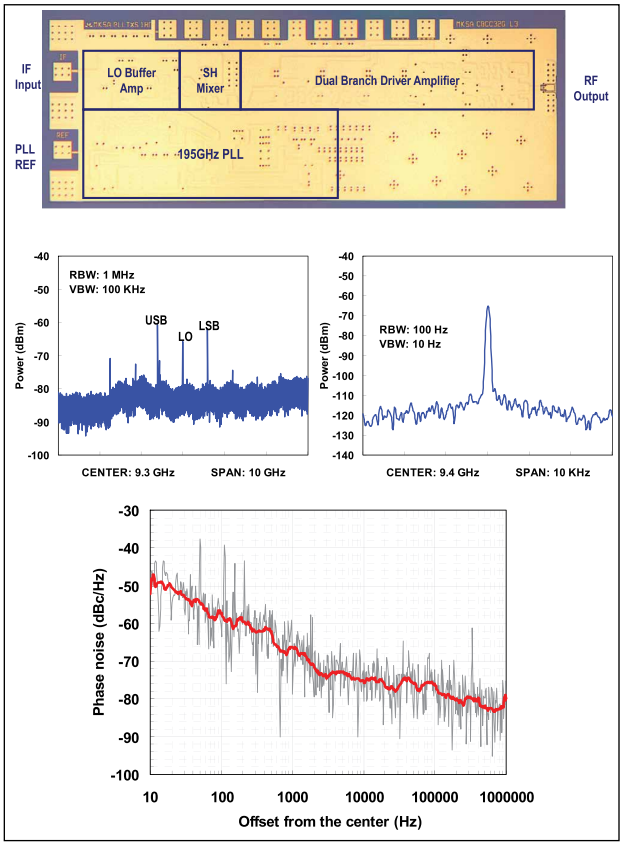

Fig. 20. ***Chip photograph of integrated 590-GHz transmitter circuit with integrated PLL LO source (top). Downconverted transmitter output spectrum (middle). Measured transmitter phase noise (bottom). Chip dimensions: 1.95 × 0.7 mm².***

the VCO control voltage and identified using the 600-GHz multiplier source. For these measurements, the input probe loss was deembedded based on S-parameter measurements of the loss. At 577 GHz, the receiver shows a peak gain of 19.7 dB and a measured noise figure of 16 dB. The total dc power consumption of the circuit is 500 mW.

Phase-locked sources have also be utilized as local oscillators for the integrated transmitter and receiver circuits. In [18], we reported a single-chip 630-GHz transmitter that integrated a 210-GHz PLL local oscillator with a third-order subharmonic mixer. Fig. 20 shows an integrated 590-GHz transmitter circuit that integrates a 195-GHz PLL for the LO, an LO buffer amplifier, a third-order subharmonic transmit mixer and the dual-branch differential CB amplifier design shown in Fig. 12. The circuit consists of 167–130-nm HBTs and consumes 1.08 W of dc power. The transmitter was characterized on-wafer using the same measurement setup as described in [18].

A typical measured downconverted output spectrum of the transmitter is shown in Fig. 19. For this measurement, the PLL reference frequency was 19.69 GHz (f_{LO} = 196.9 GHz) and the IF frequency was 1 GHz. The output spectrum measurement from the downconverting mixer

($f_{LO,mixer}$ = 600 GHz) is uncalibrated. A waveguide coupler was used to sample the output power to an Erikson PM-4 power meter. Correcting for probe and coupler loss a transmitted output power of −2.0 dBm was measured. The measured phase noise of the transmitter is also shown in Fig. 19 (f_{LO} = 197.2 GHz, f_{IF} = 20 GHz). The phase noise measurement was performed on the upper sideband at 611.6 GHz. The measured phase noise is −75 dBc at a 100-kHz offset. Efforts are currently underway to package both integrated transmitter and receiver circuits for the laboratory demonstration of THz communication links.

Other demonstrations of integrated THz transmitter and receiver circuits have been demonstrated around 300 GHz in the 250-nm InP HBT technology [15], [17]. The wide available bandwidth at THz frequencies can potentially be exploited for high data rate communications. A 300-GHz ASK receiver used for 24-Gb/s data transmission over a 0.3-m distance was demonstrated in [16] and a 300-GHz quadrature phase-shift keying (QPSK) modulator and demodulator circuits were demonstrated operating at 50 Gb/s showing a path for achieving even higher data rate communications [14].

V. CONCLUSION

Highly scaled InP HBTs are capable of fundamental circuit operation in the THz frequency regime. IC technologies with accurate transistor models and the necessary backend-of-line processes have been developed to enable fully integrated transceiver circuits operating to 600 GHz. The availability of single-chip THz sources and receivers will open new opportunities for applications in the THz spectrum; opportunities that could be further exploited with the development of low-cost packaging solutions.

THz bandwidth transistors can also provide improved system performance at sub-THz frequencies. This is evidenced by the record levels of solid-state output power now achievable around 200 GHz. Further applications include: broadband high efficiency mm-wave PAs, ultralow-power millimeter-wave beamformer circuits for phased arrays and high-resolution microwave and millimeter-wave mixed-signal ICs such as digital-to-analog converters (DACs) and analog-to-digital converters (ADCs). Recent developments of heterogeneous integration technologies are enabling the intimate integration of InP and Si complementary metal–oxide–semiconductor (CMOS) technologies. The addition of CMOS for low-power digital logic, memory, and calibration circuitry further expands the application space for THz transistor technologies. The performance of InP HBTs can also be further extended with continued transistor scaling. No fundamental barriers exist to prevent HBT scaling to 32-nm feature sizes, a technology node where IC demonstrations at >1 THz could be realized. ■

ACKNOWLEDGMENT

The authors would like to acknowledge the contributions of colleagues at Teledyne Scientific Company in technology development and circuit demonstrations (R. Pierson, P. Rowell, K. Shinohara, J. Bergman, A. Young, E. Regan, Cleanroom Operations staff, and B. Brar). Significant support for THz metrology and integrated circuit testing was provided Dr. A. Skalare, R. Lin, and A. Perralta at Jet Propulsion Labs. The guidance and support of Dr. A. Hung (Army Reseach Lab), Dr. M. Rosker (Raytheon, formerly DARPA), Dr. J. Albrecht (Michigan State University, formerly DARPA), and Dr. D. Palmer (DARPA) through the course of the THz Electronics program is gratefully acknowledged as is the support of B. Wallace (DARPA) under the DARPA ViSAR program.

REFERENCES

[1] R. Lai *et al.*, "Sub 50nm InP HEMT device with fmax greater than 1THz," in *Proc. IEEE Electron Devices Meeting*, Washington, DC, USA, Dec. 2007, pp. 609–611.

[2] D. H. Kim, J. A. del Alamo, P. Chen, W. Ha, M. Urteaga, and B. Brar, "50-nm E-mode $In_{0.7}Ga_{0.3}As$ PHEMTs on 100-mm InP substrate with fmax > 1 THz," in *Proc. IEEE Electron Devices Meeting*, San Francisco, CA, USA, Dec. 2010, pp. 30.6.1–30.6.4.

[3] M. Urteaga, R. Pierson, P. Rowell, V. Jain, E. Lobisser, and M. J. W. Rodwell, "130nm InP DHBTs with ft >0.52THz and fmax >1.1THz," in *Proc. 69th Annu. Device Res. Conf.*, Santa Barbara, CA, USA, Jun. 2011, pp. 281–282.

[4] V. Jain *et al.*, "1.0 THz fmax InP DHBTs in a refractory emitter and self-aligned base process for reduced base access resistance," in *Proc. 69th Annu. Device Res. Conf.*, Santa Barbara, CA, USA, Jun. 2011, pp. 271–272.

[5] J. C. Rode *et al.*, "Indium phosphide heterobipolar transistor technology beyond 1-THz bandwidth," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2779–2785, Aug. 2015.

[6] X. Mei *et al.*, "First demonstration of amplification at 1THz using a 25-nm InP high electron mobility transistor process," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 229–327, Apr. 2015.

[7] J. Hacker, M. Urteaga, M. Seo, A. Skalare, and R. Lin, "InP HBT amplifier MMICs operating to 0.67 THz," in *IEEE MTT-S Microw. Symp. Dig.*, Seattle, WA, USA, Jun. 2013, pp. 1–3.

[8] M. Seo *et al.*, "A 600 GHz InP HBT amplifier using cross-coupled feedback stabilization and dual-differential power combining," in *IEEE MTT-S Microw. Symp. Dig.*, Seattle, WA, USA, Jun. 2013, pp. 1–3.

[9] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "A 23.2dBm at 210GHz to 21.0dBm at 235GHz 16-Way PA-cell combined InP HBT SSPA MMIC," in *Proc. IEEE Compound Semiconductor IC Symp.*, La Jolla, CA, USA, Oct. 2014, pp. 1–4.

[10] M. Seo *et al.*, "InP HBT IC technology for terahertz frequencies: Fundamental oscillators up to 0.57 THz," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2203–2214, Oct. 2011.

[11] M. Seo, M. Urteaga, A. Young, and M. Rodwell, "A 305-330+ GHz 2:1 dynamic frequency divider using InP HBTs," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 8, pp. 468–470, Aug. 2010.

[12] M. Seo, J. Hacker, M. Urteaga, A. Skalare, and M. J. W. Rodwell, "A 529 GHz dynamic frequency divider in 130 nm InP HBT process," *IEICE Electron. Exp.*, vol. 12, no. 3, p. 20141118, Feb. 2015.

[13] Y. Karandikar, H. Zirath, Y. Yan, and V. Vassilev, "A compact 340 GHz 2 × 4 patch array with integrated subharmonic gilber core mixer as a building block for multi-pixel imaging frontends," in *Proc. IEEE Compound Semiconductor IC Symp.*, La Jolla, CA, USA, Oct. 2014, pp. 1–4.

[14] H.-J. Song, J.-Y. Kim, K. Ajito, N. Kukutsu, and M. Yaita, "50-Gb/s direct conversion QPSK modulator and demodulator for terahertz communications at 300 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 3, pp. 600–609, Mar. 2014.

[15] Y. Yan, Y. B. Karandikar, S. E. Gunnarson, M. Urteaga, R. Pierson, and H. Zirath, "340 GHz integrated receiver in 250nm InP DHBT

technology," *IEEE Trans. THz Sci. Technol.*, vol. 2, no. 3, pp. 306–314, May 2012.

[16] H.-J. Song, J.-Y. Kim, K. Ajito, M. Yaita, and N. Kukutsu, "Full integrated ASK receiver MMIC for terahertz communications at 300 GHz," *IEEE Trans. THz Sci. Technol.*, vol. 3, no. 4, pp. 445–452, Jul. 2013.

[17] S. Kim *et al.*, "300 GHz Integrated heterodyne receiver and transmitter with on-chip fundamental local oscillator and mixers," *IEEE Trans. Terahertz Sci. Technol.*, vol. 5, no. 1, pp. 92–101, Jan. 2015.

[18] M. Seo *et al.*, "A single-chip 630 GHz transmitter with 210 GHz sub-harmonic PLL local oscillator in 130 nm InP HBT," in *Int. Microw. Symp. Dig.*, Montreal, Canada, Jun. 2012, pp. 1–3.

[19] M. J. W. Rodwell *et al.*, "Submicron scaling of HBTs," *IEEE Trans. Electron Devices*, vol. 48, no. 11, pp. 2606–2624, Nov. 2001.

[20] M. J. W. Rodwell, M. Le, and B. Brar, "InP bipolar ICs: Scaling roadmaps, frequency limits, manufacturable technologies," *Proc. IEEE*, vol. 96, no. 2, pp. 271–286, Feb. 2008.

[21] C. R. Bolognesi, M. M. W. Dvorak, P. Yeo, X. G. Xu, and S. P. Watkins, "InP/GaAsSb/InP double HBTs: A new alternative for InP-based DHBTs," *IEEE Trans. Electron Devices*, vol. 48, no. 11, pp. 2631–2639, Nov. 2001.

[22] H. J. Zhu *et al.*, "GaAsSb-based HBTs grown by production MBE system," in *Proc. 16th Int. Conf. Indium Phosph. Rel. Mater.*, May 2004, pp. 338–341.

[23] C. R. Bolognesi, R. Flückiger, M. Alexandrova, W. Quan, R. Lövblom, and O. Ostilleni, "InP/GaAsSb DHBTs for THz applications and improved extraction of their cutoff frequencies," in *Proc. IEEE Electron Device Meeting*, San Francisco, CA, USA, Dec. 2016, pp. 723–726.

[24] W. Liu, *Handbook of III-V Heterojunction Bipolar Transistors*. New York, NY, USA: Wiley, 1998, pp. 143–144.

[25] C. Nguyen, T. Liu, M. Chen, H.-C. Sun, and D. Rensch, "AlInAs/GaInAs/InP double heterojunction bipolar transistor with a novel base-collector design for power applictions," *IEEE Electron Device Lett.*, vol. 17, no. 3, pp. 133–135, Mar. 1996.

[26] H.-W. Chiang, J. C. Rode, P. Choudhary, and M. J. W. Rodwell, "Optimization of direct current performance in terahertz InGaAs/InP double-heterojunction bipolar transistors," *J. Appl. Phys.*, vol. 116, p. 164509, Oct. 2014.

[27] M.-C. F. Chang *et al.*, "AlGaAs/GaAs heterojunction bipolar transistors fabricated using a self-aligned dual lift-off process," *IEEE Electron Device Lett.*, vol. 8, no. 7, pp. 303–305, Jul. 1987.

[28] H. Masuda *et al.*, "Novel self-aligned sub-micron emitter InP/InGaAs HBT's using T-shaped emitter electrode," in *Proc. IEEE Indium Phosph. Rel. Mater.*, Hokkaido, Japan, May 1995, pp. 644–647.

[29] G. He *et al.*, "Self-aligned InP DHBT with ft and fmax over 300GHz in a new manufacturable technology," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 520–522, Aug. 2004.

[30] K. Nagata, O. Nakajima, Y. Yamauchi, T. Nittono, H. Ito, and T. Ishibashi, "Self-aigned AlGaAs/GaAs HBT with low emitter resistance utilizing InGaAs cap layer," *IEEE Trans. Electron Devices*, vol. 35, no. 1, pp. 2–7, Jan. 1998.

[31] M. Urteaga, R. Pierson, P. Rowell, M. Choe, D. Mensa, and B. Brar, "Advanced InP DHBT process for high speed LSI circuits," in *Proc. 20th Int. Conf. Indium Phosph. Rel. Mater.*, May 2008, pp. 1–5.

[32] N. Kashio, K. Kurishima, M. Ida, and H. Matsuzaki, "Over 450-GHz ft and fmax InP/InGaAs DHBT with a passivation ledge fabricated by utilizing SiN/SiO_2 sidewall spacers," *IEEE Trans. Electron Devices*, vol. 61, no. 10, pp. 3423–3428, Oct. 2014.

[33] E. Lind *et al.*, "560GHz ft, fmax InGaAs/InP DHBT in a novel dry-etched emitter process," in *Proc. IEEE Device Res. Conf.*, South Bend, IN, USA, Jun. 2007, pp. 18–20.

[34] A. Baraskar, A. C. Gossard, and M. J. W. Rodwell, "Lower limits to specific contact resistivity," in *IPRM Tech. Dig.*, Aug. 2012, pp. 196–199.

[35] A. Baraskar *et al.*, "High doping effects on *in-situ* Ohmic contacts to n-InAs," in *Proc. IEEE Indium Phosph. Rel. Mater.*, Kagawa, Japan, May 2010, pp. 1–4.

[36] A. Baraskar, V. Jain, M. A. Wistey, B. J. Thibeault, A. C. Gossard, and M. J. W. Rodwell, "*in-situ* and *ex-situ* Ohmic contacts to heavily doped p-InGaAs," in *Proc. 16ht Int. Conf. Molecular Beam Epitaxy*, Berlin, Germany, Aug. 2010.

[37] D. F. Williams, A. C. Young, and M. Urteaga, "A prescription for sub-millimeter-wave transistor characterization," *IEEE Trans. THz Sci. Technol.*, vol. 4, no. 3, pp. 433–439, Apr. 2013.

[38] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high frequency characterization," in *Proc. IEEE Bipolar/BiCMOS Technol. Meeting*, Minneapolis, MN, USA, Sep. 2001, pp. 188–191.

[39] M. Urteaga *et al.*, "InP HBT integrated circuit technology for terahertz freqeuncies," in *Proc. IEEE Compound Semiconductor IC Symp.*, Monterey, CA, USA, Oct. 2010, pp. 1–3.

[40] E. Lobisser *et al.*, "InGaAs/InP DHBTs with emitter and base defined through electron-beam lithography for reduced C_{cb} and increased RF cut-off frequency," in *Proc. 39th Int. Symp. Compound Semiconductors*, Santa Barbara, CA, USA, Aug. 2012.

[41] J. C. Rode *et al.*, "An InGaAs/InP DHBT with simulataneous f_T/f_{max} 404/901 GHz and a 4.3 V breakdown voltage," *IEEE J. Electron Devices Soc.*, vol. 3, no. 1, pp. 54–75, Jan. 2015.

[42] Z. Griffith *et al.*, "Sub-300 nm InGaAs/InP type-I DHBTs with 150 nm collector, 30 nm base demonstrating 755 GHz f_{max} and 416 GHz f_T," in *Proc. IEEE Indium Phosph. Rel. Mater. Conf.*, May 2007, pp. 403–406.

[43] V. Radisic *et al.*, "InP HBT transferred substrate amplifiers operating to 600 GHz," in *Int. Microw. Symp. Dig.*, Phoenix, AZ, USA, May 2015, pp. 1–3.

[44] V. Radisic, D. W. Scott, A. Cavus, and C. Monier, "220-GHz high-efficiency InP HBT power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3001–3005, Dec. 2014.

[45] R. Flückiger, R. Lovblom, M. Alexandrova, O. Ostinelli, and C. R. Bolognesi, "Type-II InP/GaAsSb double-heterojunction bipolar transistors with f_{max} >700GHz," *Appl. Phys. Exp.*, vol. 7, no. 3, p. 034105, Mar. 2014.

[46] H. Xu, B. Wu, A. Winoto, and M. Feng, "Advanced process and modeling on 600+ GHz emitter ledge type-II GaAsSb/InP DHBT," in *Proc. IEEE Compound Semiconductor IC Symp.*, La Jolla, CA, USA, Oct. 2014, pp. 1–5.

[47] N. Kashio, T. Hoshi, K. Kurishima, M. Ida, and H. Matsuzaki, "Improvement in high-frequency characteristics of InGaAsSb-base double heterojunction bipolar transistors by inserting a highly doped GaAsSb base contact layer," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 657–659, Jul. 2015.

[48] P. Chevalier *et al.*, "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320GHz f_T/ 370GHz f_{max} HBT and high-Q millimeter-wave passives," in *Proc. IEEE Int. Electron Devices Meeting*, San Francisco, CA, USA, Dec. 2014, pp. 3.9.1–3.9.3.

[49] Q. Z. Liu *et al.*, "SiGe HBTs in 90nm BiCMOS technology demonstrating f_T/f_{max} 285GHz/475GHz through simultaneous reduction of base resistance and extrinsic capacitance," *ECS Trans.*, vol. 64, no. 6, pp. 285–294, Aug. 2014.

[50] V. Jain *et al.*, "Device and circuit performance of SiGe HBTs with 130nm BiCMOS process with ft/fmax of 250/330GHz," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Coronado, CA, USA, Sep. 2014, pp. 96–99.

[51] J. Bock *et al.*, "SiGe HBT and BiCMOS process integration optimization within HTE DOTSEVEN project," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Boston, MA, USA, Oct. 2015, pp. 121–124.

[52] B. Heinemann *et al.*, "SiGe HBT with fT/fmax of 505 GHz/720 GHz," in *Proc. IEEE Electron Device Meeting*, San Francisco, CA, USA, Dec. 2016, pp. 51–54.

[53] W. R. Deal, K. Leong, W. Yoshida, A. Zamora, and X. B. Mei, "InP HEMT integrated circuits operating above 1,000 GHz," in *Proc. IEEE Electron Device Meeting*, San Francisco, CA, USA, Dec. 2016, pp. 707–710.

[54] K. Shinohara *et al.*, "Scaling of GaN HEMTs and Schottky diodes for submillimeter-wave MMIC applications," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 2982–2996, Oct. 2013. DOI: 10.1109/TED.2013.2268160.

[55] D. W. Scott *et al.*, "InP HBT transferred to higher thermal conductivity substrate," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 507–509, Apr. 2012.

[56] A. Thiam *et al.*, "InP HBT thermal management by transferring to high thermal conductivity silicon substrates," *IEEE Electron Device Lett.*, vol. 35, no. 10, pp. 1010–1012, Oct. 2014.

[57] T. Ishibashi, "Nonequilibrium electron transport in HBTs," *IEEE Trans. Electron Devices*, vol. 48, no. 11, pp. 2595–2605, Nov. 2001.

[58] M. Iwamoto *et al.*, "Large-signal HBT model with improved collector transit time formulation for GaAs and InP technologies," in *Proc. IEEE Int. Microw. Symp.*, Philadelphia, PA, USA, Jun. 2003, pp. 635–638.

[59] A. Tessmann, A. Leuther, M. Ohlrogge, and H. Massler, "Submillimeter-wave amplifier circuits based on thin film microstrip line front-side technology," in *Proc. IEEE Compound Semiconductor IC Symp.*, New Orleans, LA, USA, Oct. 2015, pp. 1–4.

[60] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "340-440 mW broadband, high efficiency E-band PA's in InP HBT," in *Proc. IEEE Compound Semiconductor IC Symp.*, New Orleans, LA, USA, Oct. 2015.

[61] H.-C. Park, S. Daneshgar, Z. Griffith, M. Urteaga, B.-S. Kim, and M. J. W. Rodwell,

"Millimeter-wave series power combining using sub-quarter wavelength baluns," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2089–2102, Oct. 2014.

[62] *102-109.5 GHz Operational Waiver Request*. [Online]. Available: https://www.fcc.gov, 102-109.5 GHz operational waiver request.

[63] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "190-260 GHz high-power, broadband PA's in 250-nm InP HBT," in *Proc. IEEE Compound Semiconductor IC Symp.*, New Orleans, LA, USA, Oct. 2015, pp. 1–4.

[64] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "Multi-finger 250-nm InP HBTs for 220-GHz mm-wave power," in *Proc. IEEE Indium Phosph. Rel. Mater. Conf.*, Santa Barbara, CA, USA, Aug. 2012, pp. 1–4.

[65] Z. Griffith and T. Reed, "Cascode cell having a DC blocking capacitor," U.S. Patent 9165894 B2, Oct. 1, 2015.

[66] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "A 227.5GHz InP HBT SSPA MMIC with 101mW Pout at 14.0dB compressed gain and 4.04% PAE," in *Proc. IEEE Compound Semiconductor IC Symp.*, Monterey, CA, USA, Oct. 2013, pp. 1–4.

[67] V. Radisic *et al.*, "220-GHz solid-state power amplifier modules," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2291–2297, Oct. 2012.

[68] A. Margomenos *et al.*, "GaN technology for E, W and G-band applications," in *Proc. IEEE Compound Semiconductor IC Symp.*, La Jolla, CA, USA, Oct. 2014, pp. 1–4.

[69] D. Gritters, K. Brown, E. Ko, Z. Griffith, and M. Urteaga, "200–260 GHz solid-state amplifier with 700-mW of output power," in *Proc. IEEE-Int. Microw. Symp. Dig*, Phoenix, AZ, USA, May 2015.

[70] J.-M. Rollin, D. Miller, M. Urteaga, Z. Griffith, and H. Kazemi, "DC-240 GHz polystrata combining architecture for high efficiency and compact SSPAs," in *Proc. IEEE Compound Semiconductor IC Symp.*, New Orleans, LA, USA, Oct. 2015, pp. 1–4.

[71] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "A 50–80mW SSPA from 190.8–244GHz at 0.5mW pin," in *Proc. IEEE Int. Microw. Symp.*, Tampa, FL, USA, Jun. 2014, pp. 1–4.

[72] T. B. Reed, M. J. W. Rodwell, Z. Griffith, P.Rowell, A. Young, and M. Field, "A 220 GHz InP HBT solid-state power amplifier MMIC with 90 mW Pout at 8.2 dB compressed gain," in *Proc. IEEE Compound Semiconductor IC Symp.*, San Diego, CA, USA, Oct. 2012, pp. 1–3.

[73] T. B. Reed, Z. Griffith, P. Rowell, M. Field, and M. Rodwell, "A 180mW InP HBT power amplifier MMIC at 214 GHz," in *Proc. IEEE Compound Semiconductor IC Symp.*, Monterey, CA, USA, Oct. 2013, pp. 1–3.

[74] V. Radisic, D. W. Scott, and C. Monier, "50 mW 220 GHz InP HBT power amplifier MMIC," in *Proc. IEEE Int. Microw. Symp.*, Tampa, FL, USA, Jun. 2014, pp. 1–3.

[75] V. Radisic, D. W. Scott, A. Cavus, and C. Monier, "220-GHz high-efficiency InP HBT power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3001–3005, Dec. 2014.

[76] H. Kazemi *et al.*, "350 mW G-band medium power amplifier fabricated through a new method of 3D-copper additive manufacturing," in *Proc. IEEE Int. Microw. Symp.*, Phoenix, AZ, USA, May 2015, pp. 1–3.

[77] E. Bryerton, J. Hesler, and S. Retzloff, "Broadband tunable supra-THz test sources," in *Proc. Int. Conf. Infr., Millim. THz Waves (IRMMW-THz)*, Hong Kong, Aug. 2015, pp. 1–2.

[78] [Online]. Available: http://vadiodes.com/index.php/en/news/24-2015-news/601-july-2015-news-leading-edge-vna-extenders-from-virginia-diodes

[79] V. Radisic, K. Leong, X. Mei, S. Sarkozy, W. Yoshida, and W. R. Deal, "Power amplification at 0.65 THz using InP HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 1–58, Mar. 2012.

[80] K. M. K. H. Leong *et al.*, "A 0.85 THz low noise amplifier using InP HEMT transistors," *IEEE Microw. Wireless Compon. Letts.*, vol. 25, no. 6, pp. 397–398, Jun. 2015.

[81] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "A 6-10 mW power amplifier at 290-307.5GHz in 250 nm InP HBT," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 9, pp. 597–599, Sep. 2015.

[82] J. Kim, S. Jeon, M. Kim, M. Urteaga, and J. Jeong, "H-band power amplifier integrated circuits using 250-nm InP HBT technology," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 2, Mar. 2015.

[83] V. Radisic *et al.*, "A 10-mW sub-millimeter-wave solid-state power-amplifier module," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 4, pp. 1903–1909, Jul. 2010.

[84] J. Hacker *et al.*, "THz MMICs based on InP HBT technology," in *Proc. IEEE Int. Microw. Symp.*, Anaheim, CA, USA, May 2010, pp. 1126–1129.

[85] K. Ericksson, S. E. Gunnarsson, V. Vassilev, and H. Zirath, "Design and characterization o H-band (223-325 GHz) amplifiers in a 250 nm InP DHBT technology," *IEEE Trans. THz Sci. Technol.*, vol. 4, no. 1, pp. 56–64, Jan. 2014.

[86] K. Ericksson, P. J. Sobis, S. E. Gunnarsson, J. Hanning, and H. Zirath, "InP DHBT amplifier modules operating between 150–300 GHz using membrane technology," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 433–439, Feb. 2015.

[87] W. Deal, X. B. Mei, K. M. K. H. Leong, V. Radisic, S. Sarkozy, and R. Lai, "THz monolithic integrated circuits using InP high electron mobility transistors," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 25–32, Sep. 2011.

[88] A. Leuther, A. Tessmann, M. Dammann, H. Massler, M. Schlechtweg, and O. Ambacher, "35 nm mHEMT technology for THz and ultra low noise applications," in *Proc. IEEE Indium Phosph. Rel. Mater. Conf.*, Kobe, Japan, May 2013, pp. 1–2.

[89] W. R. Deal *et al.*, "Low noise amplification at 0.67 THz using 30 nm InP HEMTs," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 7, pp. 270–368, Jul. 2011.

[90] A. Tessman *et al.*, "A 600 GHz low-noise amplifier module," in *IEEE Int. Microw. Symp. Dig.*, Tampa, FL, USA, Jun. 2014, pp. 1–3.

[91] V. Radisic, K. M. K. H. Leong, X. B. Mei, S. Sarkozy, W. Yoshida, and W. R. Deal, "Power amplification at 0.65 THz using InP HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 724–728, Mar. 2012.

[92] R. Wanner, R. Lahner, G. Olbrich, and P. Russer, "A SiGe monolithically integrated 278 GHz push-push oscillator," in *IEEE Int. Microw. Symp. Dig.*, Honolulu, HI, USA, Jun. 2007, pp. 333–336.

[93] Y. Baeyens *et al.*, "Highly efficient harmonically tuned InP D-HBT push-push oscillators operating up to 287 GHz," in *IEEE Int. Microw. Symp. Dig.*, Honolulu, HI, USA, Jun. 2007, pp. 333–341.

[94] E. Seok *et al.*, "A 410GHz CMOS push-push oscillator with an on-chip patch antenna," in *Proc. IEEE Int. Solid-State Circuit Conf.*, San Francisco, CA, USA, Feb. 2008, pp. 472–629.

[95] D. Huang, T. LaRocca, L. Samoska, A. Fung, and M.-C. Chang, "324 GHz CMOS frequency generator using linear superposition technique," in *Proc. IEEE Int. Solid-State Circuit Conf.*, San Francisco, CA, USA, Feb. 2008, pp. 476–629.

[96] M. Seo *et al.*, "A 220-225.9 GHz InP HBT single-chip PLL," in *Proc. IEEE Compound Semiconductor IC Symp.*, Waikoloa, HI, USA, Oct. 2011, pp. 1–4.

[97] M. Seo, M. Urteaga, M. Rodwell, and M.-J. Choe, "A 300 GHz PLL in an InP HBT technology," in *Proc. IEEE/MTT-S Int. Microw. Symp. Dig.*, Baltimore, MD, USA, Jun. 2011, pp. 1–4.

ABOUT THE AUTHORS

Miguel Urteaga (Senior Member, IEEE) received the M.S. and Ph.D. degrees in electrical engineering from the University of California Santa Barbara, Santa Barbara, CA, USA, in 2001 and 2003, respectively.

He is the Manager of Teledyne Scientific Company's advanced device development group. His research is focused on the development of ultrahigh-speed transistor technologies, primarily in the InP material system. He has led the development of Teledyne's high-performance InP HBT IC technologies. These technologies have been used to demonstrate state-of-the-art integrated circuits ranging from high-speed mixed-signal and digital ICs to mm-wave and THz monolithic integrated circuits. He served as the program manager at Teledyne for the DARPA THz Electronics and Diverse Accessible Heterogeneous Integration (DAHI) programs. He has authored or coauthored over 100 conference and journal publications.

Zach Griffith (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of California Santa Barbara (UCSB), Santa Barbara, CA, USA, in 2005.

From 2005 to 2008, he was a Project Scientist at UCSB designing and fabricating record bandwidth InP HBTs. He is currently a mm-wave and THz IC Design Engineer with the Teledyne Scientific Company, Thousand Oaks, CA, USA. Since joining Teledyne Scientific in 2008, his efforts shifted to InP-transistor-based MMIC and PA design. For over 16 years he has participated in the development of InP HBT technology and high-frequency MMICs which employ it. His design accomplishments include mm-wave op-amps for highly linear low-GHz amplification, efficient broadband E-, W-, D-, and G-band high power amplifiers, and other benchmark circuits having demonstrated state-of-the-art performance. He has authored and coauthors over 125 publications and holds six patents associated with this work.

Munkyo Seo (Senior Member, IEEE) received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, South Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical engineering from the University of California Santa Barbara (UCSB), Santa Barbara, CA, USA, in 2007.

From 1997 to 2002, he was an RF Engineer with LG Electronics Inc., Anyang, South Korea, designing microwave subsystems for wireless communication. He was an Assistant Project Scientist with UCSB from 2008 to 2009. In 2009, he joined Teledyne Scientific Company, Thousand Oaks, CA, USA, where he worked on the design of various millimeter-wave, terahertz, and high-speed mixed-signal circuits. Since 2013, he has been with Sungkyunkwan University, Suwon, South Korea, as an Assistant Professor.

Jonathan Hacker (Fellow, IEEE) received the Ph.D. degree in electrical engineering from California Institute of Technology (Caltech), Pasadena, CA, USA, in 1994.

Currently, he is the Department Manager of the High Frequency Sources and Sensors Department at Teledyne Scientific, Thousand Oaks, CA, USA. He has spent 19 years at Teledyne as a highly creative leader pushing the technological edge of millimeter-wave and submillimeter-wave solid-state technology to realize cost-effective and high-performance phased array sensors that can enable fantastic new capabilities for seeing and communicating. In the pursuit of this vision, he has captured programs worth collectively over $100 million from government agencies such as the Defense Advanced Research Projects Agency (DARPA), the Air Force Research Laboratory (AFRL), ARL, and others, through his ability to conceive and convincingly explain a path forward to realize technological solutions worthy of this scale of investment. He has performed pioneering research on quasi-optical power combining and frequency multiplication techniques, as well as demonstrating MMIC amplifiers operating up to 670 GHz.

Dr. Hacker was recognized as Teledyne§s 2011 Technologist of the Year. He has served as an elected member of the IEEE Microwave Theory and Techniques Society Administrative Committee (AdCom), and Chair of the IEEE MTT-S Technical Coordinating Committee on Terahertz Technology and Applications. He was the lead author on the 2013 winning paper _A 325 GHz InP Differential-Mode Amplifierfi for the Tatsuo Itoh Award that is given annually to the best paper published in the IEEE Microwave and Wireless Components Letters in the previous calendar year.

Mark J. W. Rodwell (Fellow, IEEE) received the Ph.D. degree from Stanford University, Stanford, CA, USA, in 1988.

He holds the Doluca Family Endowed Chair in Electrical and Computer Engineering at the University of California Santa Barbara (UCSB), Santa Barbara, CA, USA. He also manages the UCSB Nanofabrication Lab. His research group develops nanometer and THz transistors, and millimeter-wave and sub-millimeter-wave integrated circuits.

Dr. Rodwell, together with his group and collaborators, received the 2010 IEEE Sarnoff Award, the 2012 IEEE Marconi Prize Paper Award, the 1997 IEEE Microwave Prize, the 1998 European Microwave Conference Microwave Prize, and the 2009 IEEE IPRM Conference Award