An Ultra-Low-Power Dual-Polarization Transceiver Front-End for 94 GHz Phased Arrays in 130-nm InP HBT

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***Abstract*— We present a fully integrated 94-GHz transceiver front-end in a 130-nm/1.1-THz f_{max} InP HBT process. Low power is obtained through low-voltage design and high transistor gain. The IC is designed for multi-function, dual-polarization phased arrays. At 1.5-V collector bias, in dual-polarization simultaneous receiving mode, the IC has 21-dB gain, <9.3-dB noise figure, and consumes 39 mW, while in transmitting mode with time-duplexed vertical and horizontal outputs, the transceiver front-end achieves 5-dBm output power, 22-dB gain, and consumes 40 mW. At 1-V collector bias, in dual-polarization simultaneous receiving mode, the IC has 22.7-dB gain, <8.9-dB noise figure, and consumes 26 mW, while in transmitting mode, it has 22-dB gain and the saturated output power of 1.4 dBm with 29-mW power consumption.**

***Index Terms*— InP HBT, millimeter-wave integrated circuits, phased arrays, receivers, transceivers, transmitters.**

I. Introduction

MILLIMETER-WAVE systems are used for high-speed wireless communications and high-resolution radar/imaging [1]–[4]. There are key design trade-offs, in particular performance (gain and radiated power) versus dc power consumption and die area. Many millimeter-wave systems are designed in SiGe and CMOS RF integrated circuit technologies. They require large dc power consumption to achieve the required system performance. The targeted radar application (Fig. 1) is a 94-GHz phased array with c.a. 10 000 elements. Previously reported SiGe ICs designed for such a system consume more than 100-mW dc power per-element [5], [6]; with 10 000 elements, 100-mW per-element dissipation would result in more than 1 kW overall dc power consumption. This large dc power consumption would require extremely large, heavy, and expensive power-supplies and heat-sinks.

In addition, packaging many elements is also a significant obstacle at millimeter-wave frequencies. A tiled package approach, in which a unit cell element is repeated in the X and Y dimensions, can integrate a large number of elements. Therefore, RF front-end should have smaller die area [3], [5]–[7]. Low-speed control DACs and memory registers for the array phase, polarization, and transmit (Tx)/receive (Rx) states will be implemented on separate low-speed CMOS ICs. Using the technologies of [8], [9], the CMOS control ICs can be placed below the InP array ICs. Packaged this manner, the control circuits do not increase the RF element spacing's.

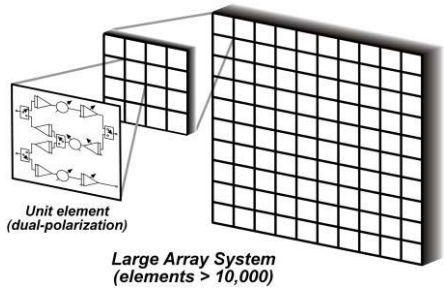

Fig. 1. Phased-array system with a large number of elements.

Here we report an ultra-low-power dual-polarization transceiver front-end. The transceiver transmits on vertical (V) or horizontal (H) polarizations, while it receives both V and H polarizations. Tx and Rx modes are switched in time [3], [5]–[7]. Ultra-low-power consumption is achieved using an advanced InP HBT technology and low-power millimeter-wave design. Section II describes the technology and design techniques. Design details and measurements of building blocks are described in Section III. Section IV describes the measurements of the integrated transceiver front-end and conclusions are presented in Section V.

II. Ultra-Low-Power mm-Wave Design

The low power 94-GHz design was obtained through low-power IC design techniques (Fig. 2) and transistors in an InP HBT process with very high gain.

A. 130-nm InP HBT Process

The transceiver front-end was designed into a 130-nm InP HBT process [10]. This process provides 50-Ω/square thin film resistors, 0.3-fF/μm^2 metal-insulator-metal capacitors, and three levels of gold interconnects (M1–M3) with 1-μm thickness. M1 is used as a ground and signal lines are

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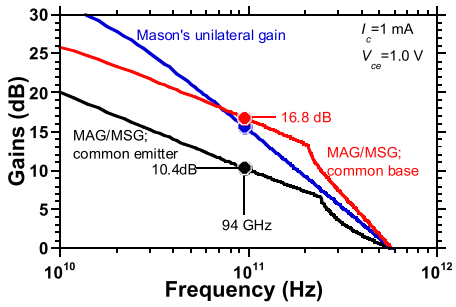

Fig. 2. Gains of CE and CB configurations ($0.13\times3\ \mu\text{m}^2$ HBT at $I_C = 1$ mA and $V_{CE} = 1$ V).

implemented with M3, which has a 7-μm separation from M1. By using these microstrip lines with 50-Ω characteristic impedance and 0.63-dB/mm loss at 94 GHz were designed for matching networks and interconnections.

Advanced 130-nm InP HBTs enable design of low-power circuits at millimeter-wave frequencies. At a high-power bias, $I_C = 6.9$ mA and $V_{CE} = 1.6$ V, a $0.13\times2\ \mu\text{m}^2$ HBT exhibits a current gain cutoff frequency $f_\tau = 520$ GHz and a maximum frequency oscillation $f_{max} = 1.1$ THz. Critically, at a low-power bias, $I_C = 1$ mA and $V_{CE} = 1$ V (Fig. 2), at 94 GHz the same HBT provides 10-dB (10 dB/mW) common-emitter (CE) and 17-dB (17 dB/mW) common-base (CB) maximum stable gain. With high gain and low power per stage, the IC power can be kept low. We used the CE configuration for low-noise amplifiers (LNAs) and low-gain stages because it can provide simultaneous noise and 50-Ω input matching easily. Since it has higher gain and better input–output isolation, the CB configuration is used for high-gain stages, phase shifters, variable-gain amplifiers (VGAs), and active switches. Moreover, the input impedance of the CB configuration with $I_C = 1$ mA is almost 50 Ω; therefore, it is easy to implement 50-Ω input matching.

The InP HBT IC technology is a research and development process. Details of the technology are described in [11]–[13]. In this technology, ICs have been reported at frequencies as high as 650 GHz, with as many as 150 HBTs, and with die areas as large as 4.7 mm^2. The ICs of the present paper were designed using HBT models earlier developed to support 650-GHz IC design [11] in the same technology.

Low noise figure is required to increase range/data-rate and improve sensitivity. The minimum noise figure of an HBT is derived in [14]

$$F_{MIN} = 1+\frac{n}{\beta_0}+\frac{f}{f_\tau}\sqrt{\frac{2I_C}{V_T}(r_E+r_B)\left(1+\frac{f_\tau^2}{\beta_0 f^2}\right)+\frac{n^2 f_\tau^2}{\beta_0 f^2}} \quad (1)$$

where r_E and r_B are the emitter and base resistances, and β_0 is the dc current gain, and n is the collector current ideality factor. Low noise figure requires high f_τ, low bias current (I_C), high dc current gain, and low base resistance. Because both f_τ and β_0 decrease at low current densities, F_{min} passes through a minimum as I_C is decreased. Unfortunately, at 94 GHz, the associated noise-matched gain is low at the I_C associated with the minimum F_{min}. Consequently, in the LNAs we here

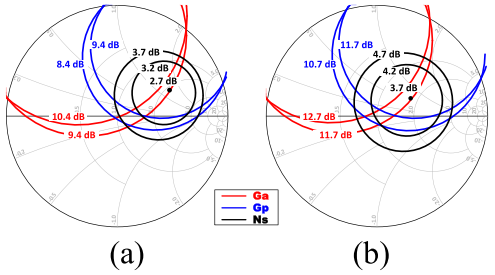

Fig. 3. Gain and noise circles of the CE configuration ($0.13\times3\ \mu\text{m}^2$ HBT at $V_{CE} = 1$ V): (a) $I_C = 1$ mA and (b) $I_C = 3$ mA.

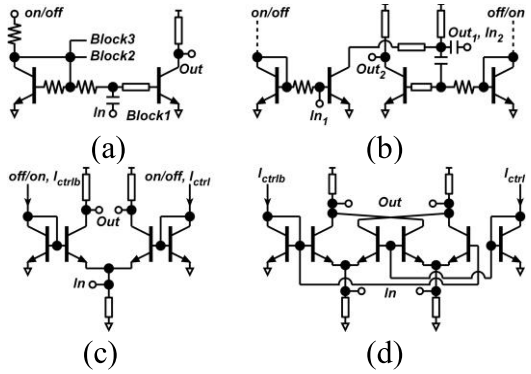

Fig. 4. Low-power design. (a) RF stage current mirror biasing to permit 1-V collector bias and stage on/off switching. (b) Tx/Rx switching at low-power points by stage dc power switching. (c) Mirror as switch or VGA. (d) Multiplier for mixers, modulators, and phase shifters.

report, the HBT bias current is set higher than that associated with the minimum F_{min}, compromising between gain and noise. Fig. 3 shows simulated gain and noise circles of the $0.13\times3\ \mu\text{m}^2$ HBT with $I_C = 1$ and 3 mA. At $I_C = 3$ mA, the HBT has $F_{min} = 3.7$ dB, with 11.7 dB associated gain G_A, while at $I_C = 1$ mA, the noise is lower ($F_{min} = 2.7$ dB), yet the associated gain remains high at 9.4 dB. At 1-mA bias, the 0.13 μm × 3 μm HBTs have concurrent low noise, low-power consumption, and reasonable gain. Given that large impedance transformation ratios introduce increased matching network losses and hence add noise, in LNAs the HBT optimum noise source resistance should be at most ~2:1 times the system source impedance. At $I_C = 1$ mA, Z_{opt} of the 0.13 μm × 3 μm HBT is $\sim(2+j1.5)\cdot50\ \Omega$. Because F_{min} and G_A are a function of the emitter current density, a smaller 0.13 μm × 2μm HBT biased at a proportionally smaller $I_C = 2/3$ mA will provide a similar F_{min} and G_A and yet will consume less dc power. Unfortunately, Z_{opt} is also proportionally increased, and once matching network losses are considered, the LNA noise figure will be increased.

B. Low-Power IC Design

For low power, RF stages are biased as current mirrors [Fig. 4(a)] with 1.5 or 1 V collector bias (the latter for lower dc power), and with a 1.5-V mirror reference supply. When feasible, smaller HBTs are used in the mirror references than in the main circuit to minimize bias circuit current. The mirror reference is shared between several blocks to minimize power

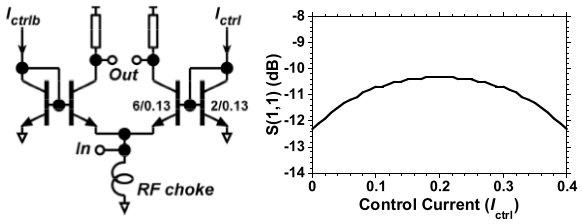

Fig. 5. Input reflection coefficient of the variable-gain CB stage as the control current is swept ($I_{\text{ctrl}} + I_{\text{ctrlb}} = 0.4$ mA).

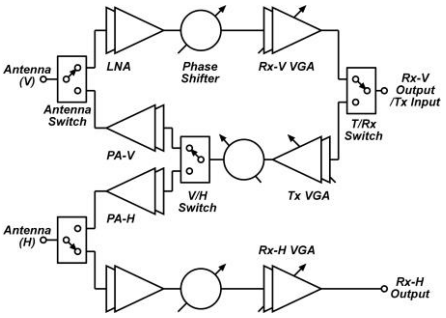

Fig. 6. Block diagram of the transceiver front-end.

consumption, and is also the ON/OFF switch for Tx/Rx modes and V/H polarizations.

At the RF backplane (Fig. 6), the output port of the receiver in the vertical polarization path is shared with the input port of the transmitter in the transceiver front-end. Therefore, a single-pole double-throw (SPDT) RF switch is required. This is simply implemented by switching OFF unused gain stages [Fig. 4(b)] while ensuring that the RF port impedance remains 50 Ω. This can reduce power consumption and die area by eliminating an explicit switch sub-circuit.

CB stages biased by current mirrors provide variable gain and switch signal paths [Fig. 4(c)], while mirror-based analog multipliers [Fig. 4(d)] form mixers which are then used as in-phase/quadrature (I/Q) modulators within the analog phase shifters. When the total bias current is maintained constant, the input impedance of the CB stage has only a small variation as gain is varied (Fig. 5). These current mirror-based designs enable precisely controlled bias current without a tail current source and allow for low supply voltage. This then reduces dc power consumption.

III. Building Blocks: Design and Results

The block diagram of the transceiver front-end is shown in Fig. 6. The base architecture will transmit on vertical or horizontal polarizations, while receiving simultaneously both V and H polarizations. The transceiver consists of LNAs, power amplifiers (PAs), VGAs, Tx/Rx switches, and phase shifters. Each of building blocks was designed to have low-power consumption and die area. In this section, design details and simulation and measurement results are presented. The fabricated chips were characterized by on-wafer probing. S-parameters were measured with an Agilent PNA-X network analyzer and OML VNA extension modules. Measurements were referenced to the probe tips using line-reflect-reflect-match calibration

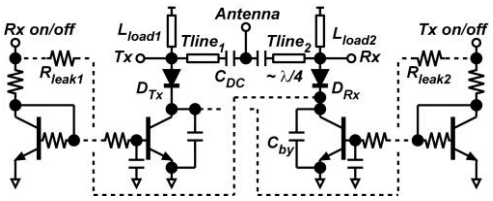

Fig. 7. Schematic of the antenna switch.

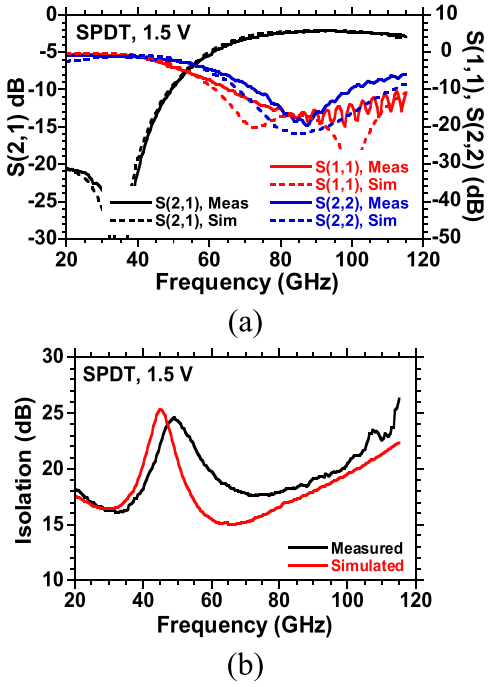

Fig. 8. Antenna switch measurements. (a) Insertion loss and return losses. (b) Isolation.

with Cascade Microtech impedance standard substrate. Power measurements were conducted with an Agilent waveguide power sensor (W8486A) and losses of cables and probes were de-embedded. Circuits were biased at 1.5 V for both the current mirror reference and the supply voltage. Each breakout IC test circuit has an individual biasing current mirror.

A. Antenna Switch

The antennas are shared between the transmitters and receivers; therefore, an SPDT switch is required to connect the antenna to either the transmitter or the receiver. The switch uses current-switched base–collector diodes, with these isolated by $\lambda/4$ lines ($T_{\text{line1,2}}$). $\lambda/4$ lines also provide sufficient space between the transmitter and receiver paths to integrate the transmitter and receiver (Fig. 7). When the receiver is ON, the diode D_{Tx} is turned on, therefore the transmitter input is connected to ground and the input impedance from the Antenna to the transmitter port becomes high due to the isolation line. For low switch loss, the diode on-resistance is made low by using a relatively large dc current through the diode. This increases power consumption. 2.6-mA bias current is chosen as a compromise between dc power consumption and

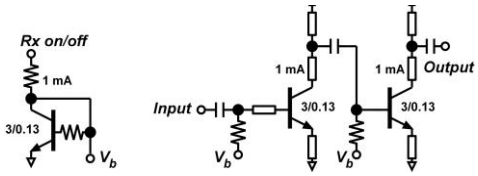

Fig. 9. Schematic of the LNA.

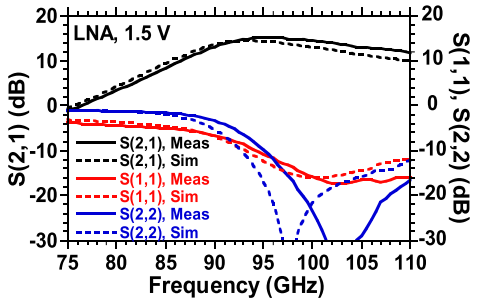

Fig. 10. Measured and simulated S-parameters of the LNA.

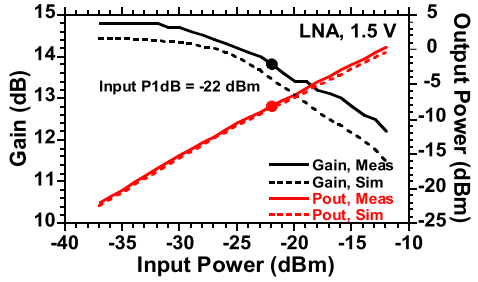

Fig. 11. Measured input–output power characteristics of the LNA, from which the input 1-dB compression point is determined.

loss. Diode parasitic capacitance is resonated out with $L_{\text{load1,2}}$. Large resistors $R_{\text{leak1,2}}$ hold the switch diodes in reverse bias when they are in the OFF-state.

Measured switch S-parameters are shown in Fig. 8 and agree well with simulations. The input impedance of each port is matched to 50 Ω. The switch has 2-dB insertion loss and 20-dB isolation with 4.8-mW power consumption from 1.5-V collector supply voltage.

B. LNA

The LNA is composed of two CE stages with inductive emitter degeneration for simultaneous input and noise matching (Fig. 9). Each stage consumes 1-mA bias current and is biased with a receiver current mirror reference. The bipolar junction transistor size is chosen to have low minimum noise figure, high-gain, and low-impedance transformation ratio for the input network. The bias current is 1 mA.

The LNA has 15.1-dB gain at 94 GHz (Fig. 10) and −22-dBm input 1-dB compression point (Fig. 11). Excluding the current mirror, the LNA consumes 3.5 mW with 1.5-V collector supply voltage. The noise figure was measured with a 94-GHz noise source (Micronetics NSI-9095W), noise figure analyzer (NFA: Agilent N8972A), and an external W-band down-conversion mixer by using system downconverter

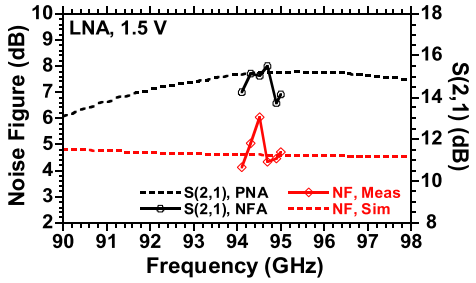

Fig. 12. Noise and gain measurements of the LNA.

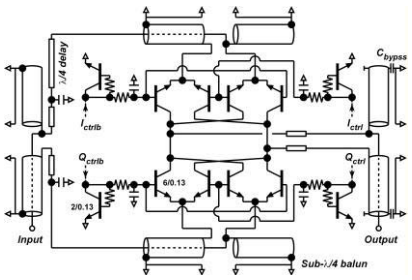

Fig. 13. Schematic of the phase shifter.

measurement option of NFA. Gains measured with the network analyzer and NFA are matched well. The measured noise figure is close to simulations, though it shows ripples with frequency arising from the scalar (versus vector) measurement calibration. The noise figure is less than 6 dB (Fig. 12).

C. Phase Shifter

Passive RF phase shifting promises higher linearity and low-power consumption but high-resolution phase shifting with low loss and small die area is difficult, therefore an active phase shifter is adopted in this paper. The phase shifter uses an active I/Q vector modulator (Fig. 13) [4]. A sub-λ/4 balun [15] and λ/4 delay line generate I/Q signals. The λ/4 delay line with a 50-Ω characteristic impedance has 0.6-dB loss. Two further such baluns generate differential I/Q input signals to the Gilbert cell mixer/modulator core, and a final balun converts the differential output signal to single-ended format. By using sub-λ/4 baluns, loss and die area are reduced; the largest balun in the phase shifter has 0.8-dB simulated insertion loss and its size is 225×700 μm^2. I/Q signal amplitudes are controlled by current mirrors as discussed in Section II. The sum of I_{Ctrl} and I_{Ctrlb} is set to 0.4 mA, as is the sum of the currents $Q_{\text{Ctrl}} + Q_{\text{Ctrlb}}$. By keeping the total HBT bias current constant, the phase shifter input match has only small variation with variations in gain or phase as shown in Fig. 5. The emitter area ratio between the current mirror and the main circuit is 1:3 to reduce power consumption due to the mirror reference. Current mirrors consume 0.8 mA; therefore, HBTs in the signal path consume 3.5 mA. This is about 3:1 larger than the current in the reference branches of the current mirrors controlling the phase shifter. In the target system, the bias currents would be controlled by simple external-bit PMOS current digital-to-analog converters on a separate CMOS die.

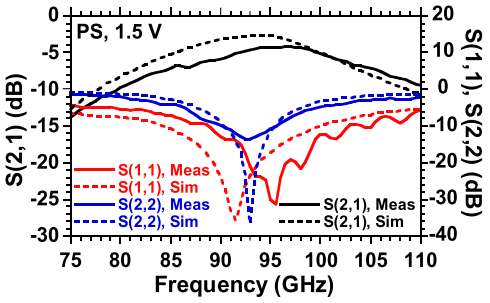

Fig. 14. Measured and simulated S-parameters of the phase shifter with $I_{\text{ctrl}} = Q_{\text{ctrl}} = 0$ mA.

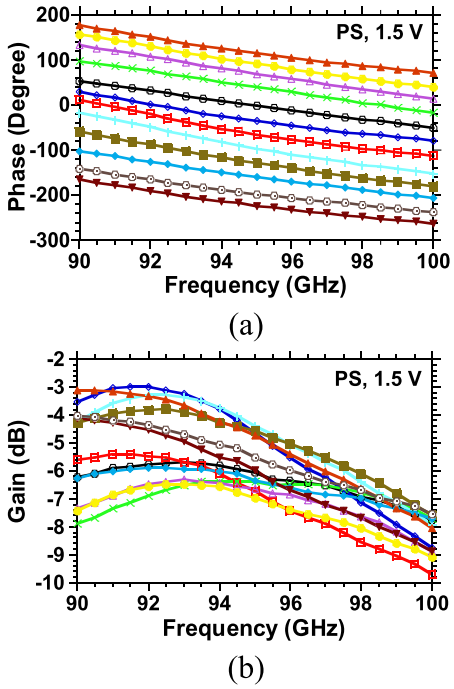

Fig. 15. Measured (a) phase and (b) gain variations of the phase shifter.

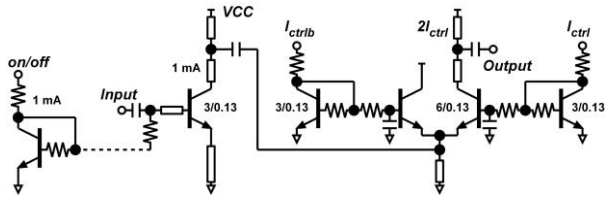

Fig. 16. Schematic of the VGA.

The phase shifter consumes 6.5 mW with 1.5-V collector supply voltage including current mirrors. Measured S-parameters are close to simulations (Fig. 14), and measurements of the phase shifter show that it can provide 360° phase shift, but with ~4 dB associated gain variation (Fig. 15).

D. VGAs and Output Tx/Rx Switch

Fig. 16 shows the VGA used in the transmitter and receiver. The first stage of VGA has the same topology as the LNA. The second stage uses current steering [Fig. 4(c)] to control the gain [16]. The gain is controlled by control currents I_{Ctrl} and I_{Ctrlb}, with their sum held constant at 1 mA. The output port of the vertical-polarization receiver is also used as the transmitter input port; therefore another SPDT switch is functionally required. The switch function is implemented by turning the unused amplifier OFF (Fig. 17). As no additional switch is needed, power consumption and chip area are both saved. The receiver VGA output is matched to 50 Ω including the effect of the input capacitance of the transmitter VGA in the OFF-state. Similarly, the transmitter VGA input matching network includes the output capacitance of the receiver VGA in the OFF-state. By this means, the switch ports remain matched to 50 Ω in both Tx and Rx modes.

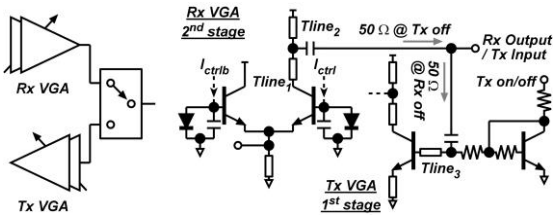

Fig. 17. Tx/Rx signal Backplane switch incorporated into the transmitter VGA.

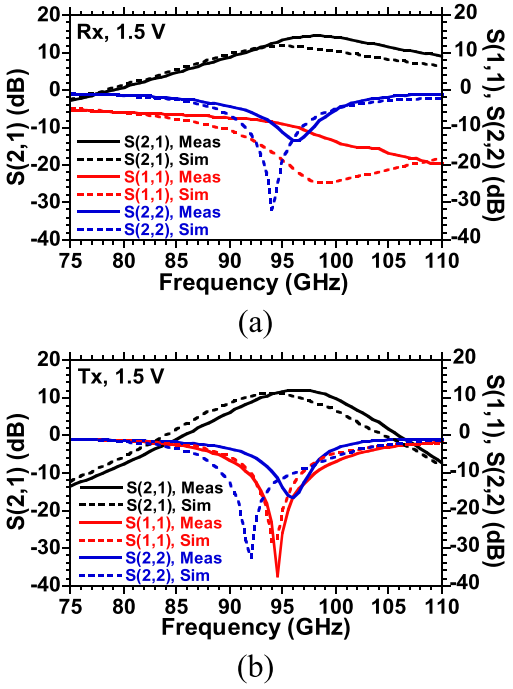

Fig. 18. Measured and simulated S-parameters of (a) receiver VGA, and (b) transmitter VGA.

Measured S-parameters of the transmitter and receiver VGAs with the highest gain setting are shown in Fig. 18. The transmitter and receiver VGAs have a peak gain of 12.5 dB, and is 10.9 dB at 94 GHz. Each VGA consumes 7 mW with the unused path turned off. Measurements agree well with simulation. The amplifiers are well-matched to 50 Ω, and have over 7-dB gain adjustment (control current: 0.3–0.8 mA) with an associated 2° variation in phase shift (Fig. 19). Variation of

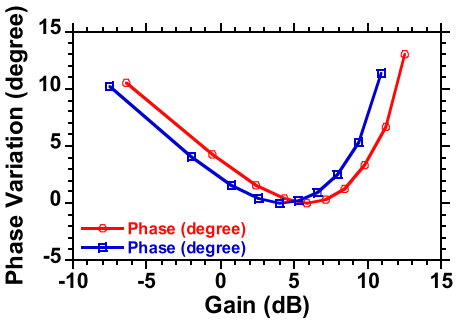

Fig. 19. Measured gain and phase variation for different control current settings of the transmitter and receiver VGAs.

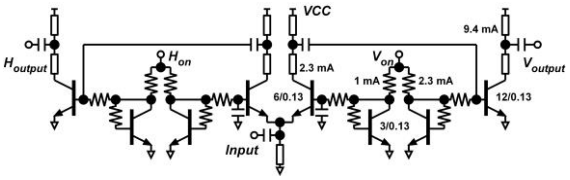

Fig. 20. Schematic of the PA and V/H switch.

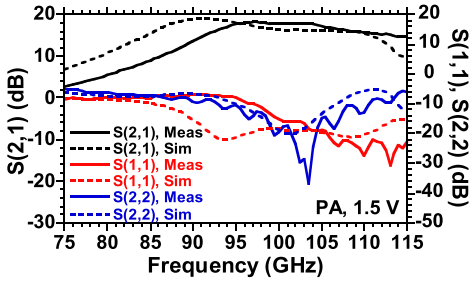

Fig. 21. Measured and simulated S-parameters of the PA.

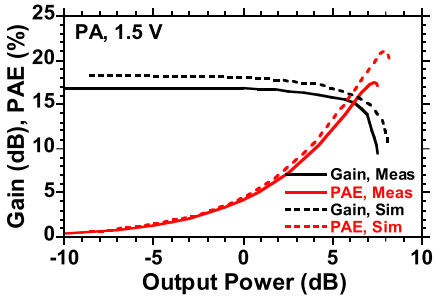

Fig. 22. Measured and simulated gain and PAE versus output power with 1.5-V collector supply voltage.

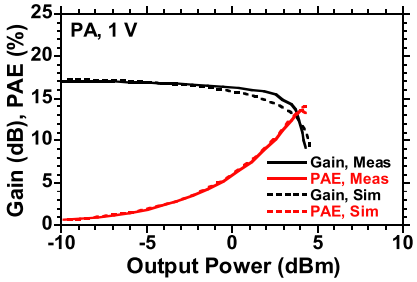

Fig. 23. Measured and simulated gain and PAE versus output power with 1-V collector supply voltage.

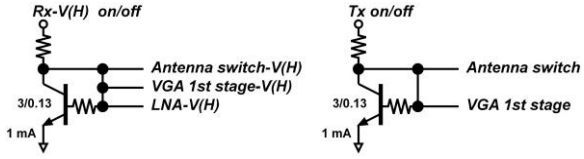

Fig. 24. Bias network for the transceiver.

the VGA phase shift with gain is made small by the variation in the second stage input impedance (Fig. 5), together with the small transistor parasitic capacitances. The VGA can therefore compensate for gain variation arising from the phase shifter. Because the VGA in the horizontal-polarization receiver does not share its output port with the transmitter, it has slightly higher gain than the VGA in the vertical receiver.

E. PA and V/H Switch

The PA is composed of a class-A CE output stage and a CB preamplifier with vertical and horizontal polarization outputs. These are switched and biased by current mirrors, with total control current set to 1 mA (Fig. 20). Even before impedance-matching, with the selected bias conditions, the CB stage has an input impedance close to 50 Ω. The input network therefore requires only minor tuning. The preamplifier provides high isolation between the vertical and horizontal polarization outputs. The CE output stage was designed for $>$ 7-dBm saturated output power.

In measurements, the PA has 17-dB gain at 94 GHz (Fig. 21). The saturated output power is 7 dBm with a power added efficiency (PAE) of 18% at 94 GHz (Fig. 22). Including its bias circuit, the PA consumes 22.5 mW at a 1.5-V collector bias voltage. With a 1-V bias, the PA has 16.5-mW power consumption and 4-dBm saturated output power. Lower supply voltage (1 V) reduces the PA power consumption by 30%, but sacrifices 3-dB saturated output power (Fig. 23).

F. Bias Network and Pad Design

The active circuits are biased by current mirrors (Fig. 24). The current mirror also serves as the ON/OFF switch selecting receive versus transmitter modes. The antenna switch, LNA, and the first stage of the VGA are biased by the same current mirror in the receiver to reduce bias network power consumption. In the transmitter, the antenna switch and the first stage of the VGA shares the same current mirror. The PA has an individual current mirror because they consume large current, and their reference voltage shifts as the PA input power is varied. The fully integrated transceiver front-end IC has only five current mirror references, these controls the V-polarization receiver, the H-polarization receiver, the V-polarization PA, the H-polarization PA, and the transmitter.

Single-ended stages, rather than differential stages, are used throughout the IC, as this reduces the IC power consumption. Single-ended RF stages have poor power supply immunity. Quarter-wave short-circuited lines at 94 GHz within the power

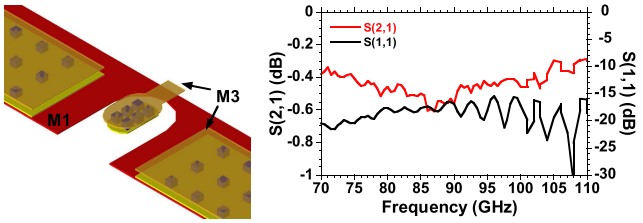

Fig. 25. Layout of the IC probe pad and measured performance of a back–back pair of pads.

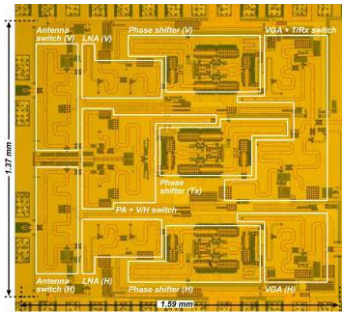

Fig. 26. Integrated transceiver front-end (chip size including pads: $1770 \times 1550\ \mu m^2$).

supply network are used extensively to isolate the individual circuit blocks from the main power supply feed. At the time of design, the IC was simulated including electromagnetic models of the entire power supply network.

On-wafer probing is also a consideration: Fig. 25 shows the mask layout of the IC probe pad. The pad was designed for a 50-Ω interface and converts from the coplanar waveguide ground-signal-ground probe footprint to a microstrip line. On-wafer measurements of a pair back-to-back connected pads shows 0.4-dB insertion loss and better than −15 dB return loss.

IV. Transceiver Front-End

Fig. 26 shows the chip photograph of the integrated transceiver front-end; its block diagram is shown in Fig. 6. The front-end was characterized using on-wafer probing. The IC is $1770 \times 1550\ \mu m^2$. This chip size is slightly larger than the $\lambda/2$ (1.6 mm) $\times\ \lambda/2$ design target because of the large number of probe pads required for signal and dc control during on-wafer probing. Die area could be reduced using better packaging technologies. The transceiver front-end can receive both vertical and horizontal polarizations simultaneously and can transmit on either vertical or horizontal polarizations. The transmitter is turned off when receiving to save power consumption, and vice versa. In measurements, the transceiver front-end was tested with collector supplies of 1.5 and 1 V, while the bias supply voltages are 1.5 V. Reducing the collector supply voltage to 1 V reduces dc power consumption, but decreases the transmitter maximum output power. The fully integrated transceiver front-end IC was tested with external five switches and twelve external current sources. These switches control current mirror references for the V-polarization receiver, the H-polarization receiver, the V-polarization PA, the H-polarization PA, and the transmitter.

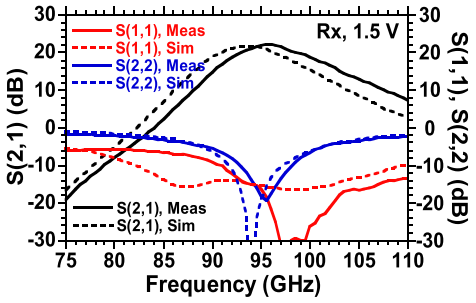

Fig. 27. Measured and simulated S-parameters of the vertical-polarization receiver at the highest gain setting for the VGA and $I_{ctrl} = Q_{ctrl} = 0$ mA for the phase shifter with 1.5-V collector supply voltage.

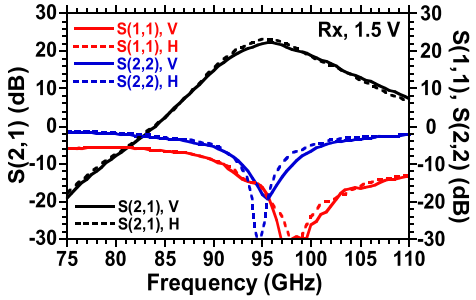

Fig. 28. Comparison of S-parameters of the receiver vertical- and horizontal- polarization receivers at the highest gain setting for the VGA and $I_{ctrl} = Q_{ctrl} = 0$ mA for the phase shifter with 1.5-V collector supply voltage.

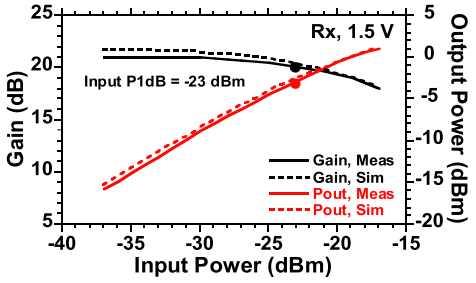

Fig. 29. Measured and simulated output power and gain versus input power of the vertical-polarization receiver at the highest gain setting for the VGA and $I_{ctrl} = Q_{ctrl} = 0$ mA for the phase shifter with 1.5-V collector supply voltage.

Current sources were used instead of current DACs controlling T/Rx VGAs and phase shifters.

The receiver signal path consists of the antenna switch, LNA, phase shifter, and the receiver VGA. Measured and simulated S-parameters of the vertical polarization receiver at the highest gain setting for the VGA and $I_{ctrl} = Q_{ctrl} = 0$ mA with 1.5-V collector supply voltage for phase shifter are shown Fig. 27. The vertical polarization receiver has 21-dB gain at 94 GHz and the gain difference between the vertical and horizontal polarizations is less than 1.4 dB (Fig. 28). The measured input 1-dB compression point is −23 dBm (Fig. 29). The noise figure of the full receiver was measured using the same setup as used to test the LNA, and is less than 9.3 dB (Fig. 30). The receiver was also tested with a reduced 1-V collector supply voltage to further reduce the dc power consumption. Under

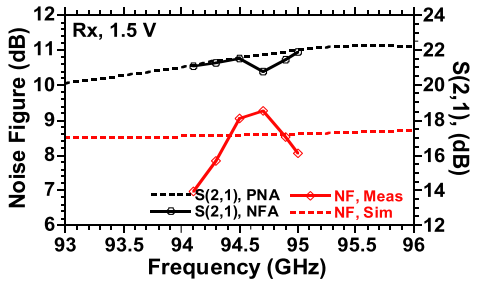

Fig. 30. Noise and gain measurements of the vertical-polarization receiver at the highest gain setting for the VGA and $I_{\text{ctrl}} = Q_{\text{ctrl}} = 0$ mA for the phase shifter with 1.5-V collector supply voltage.

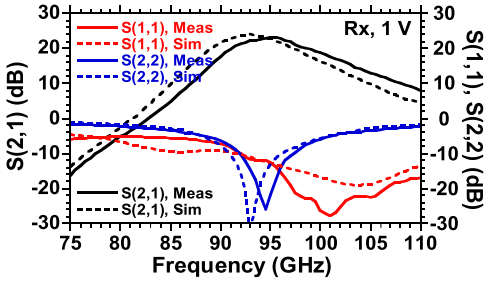

Fig. 31. Measured and simulated S-parameters of the vertical-polarization receiver at the highest gain setting for the VGA and $I_{\text{ctrl}} = Q_{\text{ctrl}} = 0$ mA for the phase shifter with 1-V collector supply voltage.

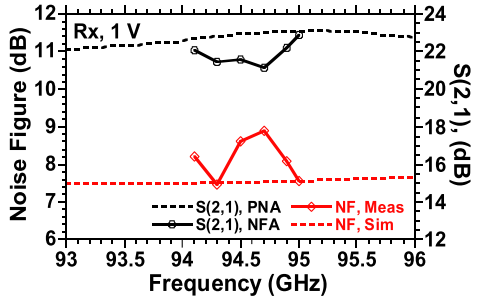

Fig. 32. Noise and gain measurements of the vertical-polarization receiver at the highest gain setting for the VGA and $I_{\text{ctrl}} = Q_{\text{ctrl}} = 0$ mA for the phase shifter with 1-V collector supply voltage.

1-V collector bias, the receiver has slightly higher gain and slightly lower noise figure compared to measurements with 1.5-V collector supply voltage (Figs. 31 and 32). However, with a 1-V bias, the receiver has a 4.5 dB lower input 1-dB compression point (Fig. 33). The vertical- and horizontal-polarization receivers together consume 39-mW dc power with a 1.5-V collector bias and 26 mW with a 1-V collector bias. These results show that, with 1-V collector bias, the receiver retains good performance but consumes significantly less dc power.

Figs. 34 and 35 show measured and simulated S-parameters of the transmitter at the highest gain setting for the VGA and $I_{\text{ctrl}} = Q_{\text{ctrl}} = 0$ mA for the phase shifter with 1.5 and 1-V collector supply voltage. The transmitter has 22-dB gain with either collector supply voltage. The measured P_{sat} is 5 dBm with a 1.5-V collector supply voltage; this is consistent

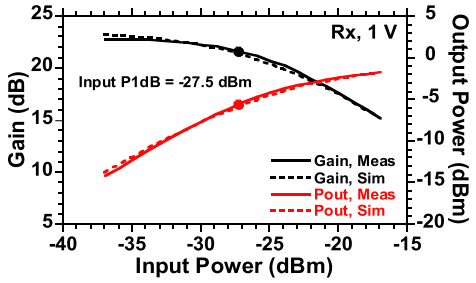

Fig. 33. Measured and simulated output power and gain versus input power of the vertical-polarization receiver at the highest gain setting for the VGA and $I_{\text{ctrl}} = Q_{\text{ctrl}} = 0$ mA for the phase shifter with 1-V collector supply voltage.

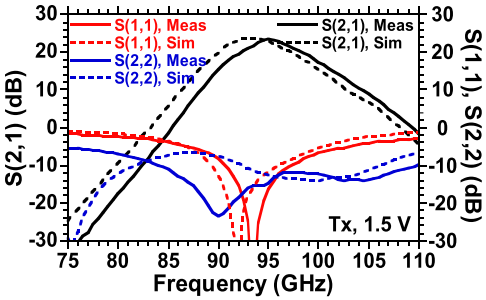

Fig. 34. Measured and simulated S-parameters of the vertical-polarization transmitter at the highest gain setting for the VGA and $I_{\text{ctrl}} = Q_{\text{ctrl}} = 0$ mA for the phase shifter with 1.5-V collector supply voltage.

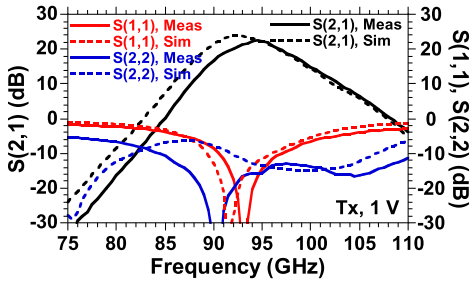

Fig. 35. Measured and simulated S-parameters of the vertical-polarization transmitter at the highest gain setting for the VGA and $I_{\text{ctrl}} = Q_{\text{ctrl}} = 0$ mA for the phase shifter with 1-V collector supply voltage.

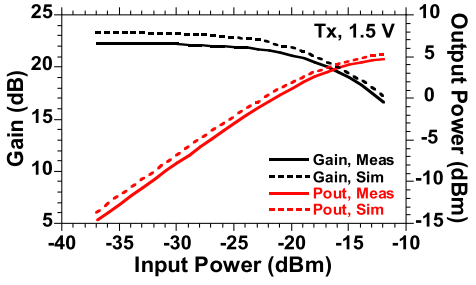

Fig. 36. Measured and simulated gain and output power of the transmitter at the highest gain setting for the VGA and $I_{\text{ctrl}} = Q_{\text{ctrl}} = 0$ mA for the phase shifter with 1.5 V and collector supply voltage.

with the measured 7-dBm P_{sat} of the PA and 2-dB loss in the antenna switch (Fig. 36). With a 1.5-V collector supply, the transmitter consumes 40-mW dc power. The transmitter,

TABLE I
PERFORMANCE COMPARISON

Single-element	[5]	[6]	This Work	
			1.5 V	1 V
Frequency (GHz)	90-102	88-96	92-98	
Architecture	TRx	TRx	TRx	
Rx Gain (dB)	22-25	30	21	22
Rx NF (dB)	9*	8.5	< 9.3	< 8.9
Tx Gain (dB)	13	> 25	22	22
Tx Psat (dBm)	-5	>2	5	1.4
Tx DC Power	137 mW (1 Tx)	116 mW (1 Tx)	40 mW (1 Tx)	29 mW (1 Tx)
Rx DC Power	137 mW (2 Rx)	160 mW (2 Rx)	39 mW (2 Rx)	26 mW (2 Rx)
Area	1.9 mm^2 2 Tx, 2 Rx	1.9 mm^2 2 Tx, 2 Rx	2.7 mm^2 2 Tx, 2 Rx (incl. pads)	
Technology f_t/f_{max} (GHz)	SiGe BiCMOS 200/270	SiGe BiCMOS 200/270	InP HBT 520/1100	

* excl. T/Rx switch

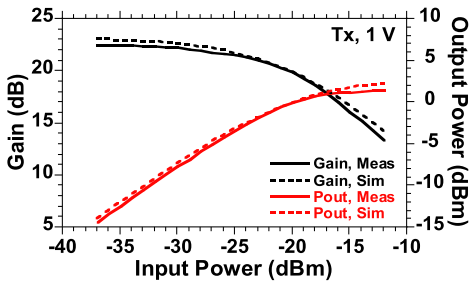

Fig. 37. Measured and simulated gain and output power of the transmitter at the highest gain setting for the VGA and $I_{ctrl} = Q_{ctrl} = 0$ mA for the phase shifter with 1 V and collector supply voltage.

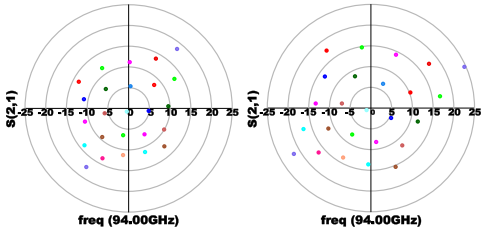

Fig. 38. Phase and gain variation at the highest gain setting for the VGA with 1.5-V collector supply voltage (vertical-polarization). (a) Receiver. (b) Transmitter. The constellation points correspond to $I_{Ctrl} = 0, 0.1, 0.2, 0.3,$ and 0.4 mA, and $Q_{Ctrl} = 0, 0.1, 0.2, 0.3,$ and 0.4 mA.

biased with 1-V collector supply voltage, has 1.4-dBm P_{sat} with 29-mW power consumption (Fig. 37). Measurements of the transmitter signal path, including the transmitter VGA,

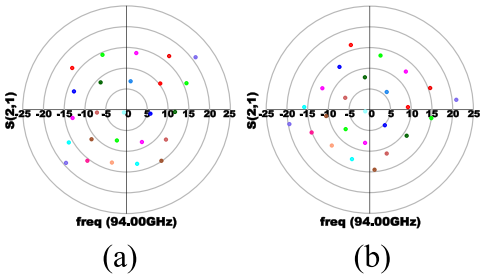

Fig. 39. Phase and gain variation at the highest gain setting for the VGA with 1-V collector supply voltage (vertical-polarization). (a) Receiver. (b) Transmitter. The constellation points correspond to $I_{Ctrl} = 0, 0.1, 0.2, 0.3,$ and 0.4 mA, and $Q_{Ctrl} = 0, 0.1, 0.2, 0.3,$ and 0.4 mA.

phase shifter, PA, and antenna switch, are in good agreement with simulation and measurements of the individual sub-circuits.

Figs. 38 and 39 show measured phase and gain variations of the receiver and transmitter at the highest gain setting of the VGA and sweeping each control current (I_{ctrl}, Q_{ctrl}) from 0 to 0.4 mA for the phase shifter with 1.5 V and with 1-V collector supply voltage, respectively. Measurements show the transmitter and receiver can provide 360° phase shift with almost 20-dB gain.

V. CONCLUSION

An ultra-low-power dual-polarization transceiver front-end for a 94 GHz phased array in a 130-nm InP HBT process is presented. The transceiver front-end is designed for multi-function, dual-polarization phased arrays. The measured performance is summarized and compared to state-of-the-art in

Table I. The fully integrated transceiver front-end demonstrates competitive performance with power consumption of 39 mW at 1.5 V (26 mW at 1 V) and 40 mW at 1.5 V (29 mW at 1 V) in receiving and transmitting modes, respectively. The transceiver front-end with 1.5-V collector supply voltage consumes one third of the dc power consumed by ICs using SiGe BICMOS [5], [6]. When the transceiver front-end is biased with 1-V collector supply voltage, the dc power consumption is further reduced. To the best of the authors' knowledge, this paper presents the lowest power consumption transceiver front-end with competitive performance so far reported at W-band frequencies.

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