A 140 GHz MIMO Transceiver in 45 nm SOI CMOS

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***Abstract*—This paper demonstrates a 140 GHz QPSK transceiver, designed as part of a 4-channel MIMO (multi input multi output) system using 45 nm CMOS SOI technology. A direct conversion architecture is implemented. In the receiver, low noise amplifier (LNA) is followed by a passive double balanced down conversion mixer and baseband amplifier; in the transmitter, an active Gilbert cell IQ modulator is followed by a driver amplifier. The 140 GHz local oscillator (LO) is generated by a ×9 multiplier. The measured receiver conversion gain is 18 dB with a 12 GHz 3-dB bandwidth; a narrowband 145 GHz gain notch, unfortunately, limits the usable bandwidth. 3-dB modulation bandwidth of the transmitter is 6-8 GHz. Total power consumption of the 4-channel receiver is 495 mW from a 1 V supply. The 4-channel transmitter consumes 463 mW power from a 1 V supply. We show preliminary single-channel link measurements at an instrument-limited 800 Mb/s data rate.**

Keywords—Millimeter wave integrated circuits, transceivers, transmitters, receivers, CMOS, MIMO communication.

I. INTRODUCTION

The increasing data consumption of mobile users demands high-data-rate wireless links. Millimeter waves (mm-waves) provide wide unlicensed and unallocated frequency bands, creating an opportunity for wideband and high-speed applications. At these frequencies signal range is limited and attenuation can be severe; signal strength is recovered using phased arrays [1, 2]. The short wavelengths permit many simultaneous independent beams, massive MIMO, even from small antenna apertures. CMOS technologies are preferred for these applications due to their low cost and high integration capability. State of the art CMOS technologies now have power gain (f_{max}) and current gain (f_t) cut-off frequencies in 200-250 GHz range, referenced to the top metal layer [3]. It is now possible to develop mm-wave transceivers and MIMO systems using CMOS [4 - 6].

In this work, a 140 GHz four-channel MIMO transceiver front-end is designed using 45 nm CMOS SOI technology. Details of this technology can be found in [3]. We present measured circuit characteristics of the LNA, LO frequency multiplier, and baseband transimpedance amplifier, and of one full receive channel and one full transmit channel. Finally, we show preliminary 800 Mb/s single-channel link measurements, through an attenuator and over a length of waveguide, using a transmitter/receiver pair, with the data rate limited by the equipment presently available. Full MIMO link demonstration requires IC packaging and systems integration, and will be reported subsequently.

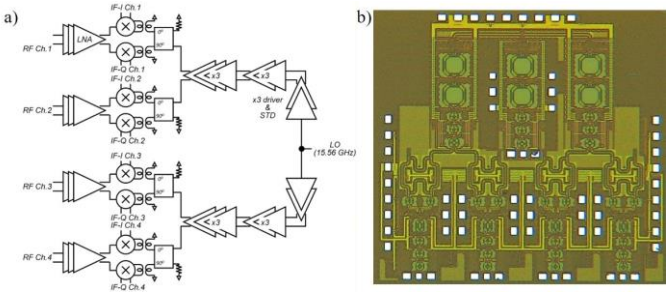

Fig. 1: 140 GHz 4-channel MIMO receiver (a) circuit block diagram and (b) microscope image. Including pads, the die is 1.69 mm × 1.76 mm.

II. RECEIVER ARCHITECTURE AND BUILDING BLOCKS

The four-channel receiver (Fig. 1) is direct conversion, with a three-stage LNA followed by double-balanced passive down-conversion mixers in the in-phase (I) and quadrature-phase (Q) signal paths. The I/Q baseband signals then pass through ~20dB-gain on-wafer transimpedance amplifiers (not shown). A 9:1 frequency multiplier chain and a 90 degree hybrid coupler generate the (I, Q) local oscillator signals. The 4-channel receiver is 1.69 mm × 1.76 mm.

A. 140 GHz LNA

The differential LNA (Fig. 2) uses capacitive cross-coupled neutralization of the gate-drain capacitance to boost the limited transistor maximum available gain at 140 GHz and to reduce interaction between the input and output tuning networks. Transformers match impedances between stages. The transistors use 24 double-contacted gate fingers of 1 μm length, and are biased at ~ 0.3 mA/μm, and V_{DD} = 1 V. The transistor footprint was simulated using the PEX parasitic extraction tool up to metal layer 3, with the remaining metal layers modeled using a 3D full-wave electromagnetic simulator (Ansys HFSS). Matching network elements were also modelled using HFSS.

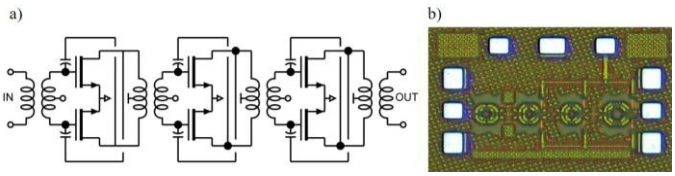

Fig. 2: 140 GHz 3-stage LNA (a) circuit diagram and (b) microscope image. Excluding pads, the die is 0.32 mm × 0.17 mm.

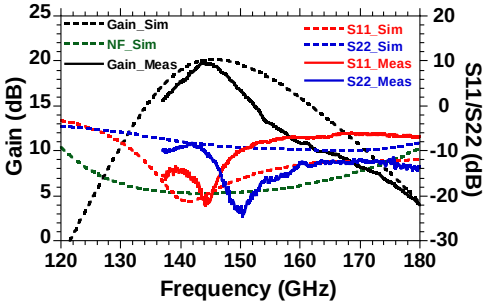

Fig. 3: a) Simulated (dashed) and measured (solid) S-parameters of the LNA

In simulations (Fig. 3), the 3-stage LNA has 19.2 dB gain at 140 GHz, a peak 20 dB gain at 145 GHz, and 20 GHz bandwidth. The simulated noise figure is 5.2 dB, which is low [4-6], but has yet to be measured. S-parameters of the LNA are measured using an Agilent PNA-X network analyzer, G-band OML VNA extension modules, and GGB 140-220 GHz wafer probes. The measured peak gain is 19-20 dB, close to simulation, but the measured 3 dB bandwidth, at 10 GHz, is much smaller than measurement. We ascribe the difference between simulation and measurement to the device models, which, at the time of design, had not been confirmed by 140 GHz on-wafer measurements. LNA consumes 42.4 mW power from a 1 V supply.

B. 140 GHz LO Generation

The 4-channel receiver uses two 9:1 frequency multipliers (Fig. 1) to generate the 140 GHz LO from an external 15.56 GHz reference, with each multiplier serving two channels. Each 9:1 multiplier consists of a digital single-ended to differential converter (Fig. 4b) and cascaded 3:1 multipliers (Fig. 4a). The multipliers are similar in topology to the LNA (Fig. 2a), with transformer-coupling, cross-coupled capacitive neutralization, and differential stages to reduce even harmonic generation. In the transformer-coupled chain (Fig. 4a) the first stage, driven into strong limiting, generates the 3rd harmonic of the 15.6 GHz input, and its output is tuned to 47 GHz. The second transformer-coupled stage operates as a 47 GHz amplifier. The third stage, with its output tuned to 140 GHz, operates as a mixer, while the fourth and fifth stages operate as 140 GHz limiting amplifiers. The multiplier's simulated output power is 5 dBm from 140 to 150 GHz, while the measured output power is 1- 3 dBm from 140 to 160 GHz with a 1.1 V supply (Fig. 5).

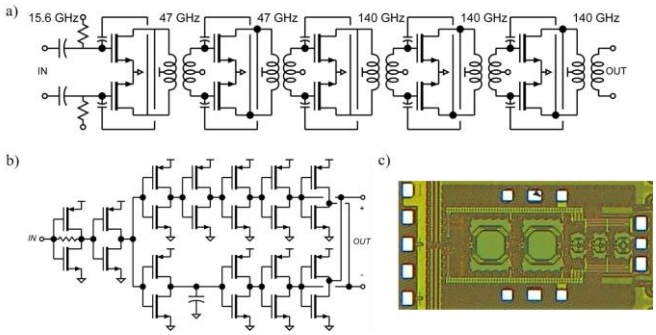

Fig. 4: Circuit schematics of a) cascaded 3:1 multipliers and b) the single ended to differential conversion c) Microscope image of the multiplier. Excluding the pads, the die is 0.65 mm × 0.27 mm.

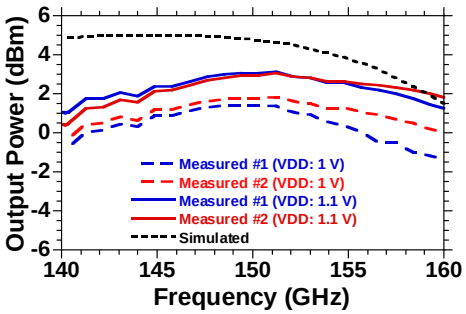

Fig. 5. Simulated and measured output power vs. frequency curves for the LO multiplier breakout with 1 V and 1.1 V supply voltages.

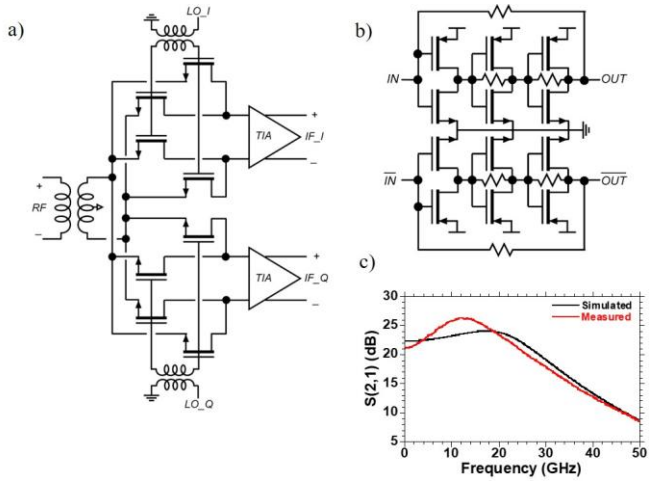

Fig. 6. Circuit diagram of a) the (I, Q) down-conversion mixer and b) the baseband transimpedance amplifier. (c) Shows the simulated (black) and measured (red) gain S_{21} of the transimpedance amplifier.

Multiplier consumes 98 mW from a 1 V supply and 108 mW from a 1.1 V supply

C. Down-Conversion Mixer

For high dynamic range, the (I, Q) down-conversion mixer is passive (Fig. 6a), using double-balanced CMOS switches. The mixers are followed by baseband pseudo-differential transimpedance amplifiers (TIAs, Fig. 6b). Fig. 6c shows the simulated and measured gain (S_{21}) of the TIA.

In simulations, the overall receiver showed 31 dB conversion gain and 5.5 dB double sideband noise figure given a 140 GHz RF and a 1 GHz baseband output signal at 27^0C. Fig. 7 demonstrates the simulated receiver performance at a fixed LO of 139 GHz. (Fig. 7)

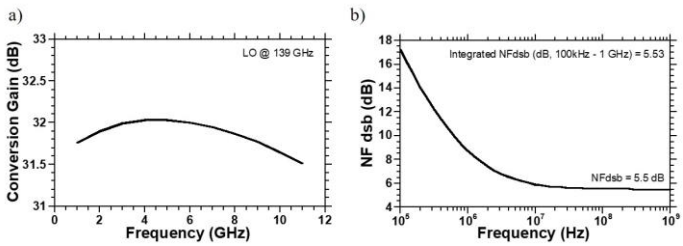

Fig. 7. a) Simulated conversion gain and b) simulated double side band NF of the receive channel

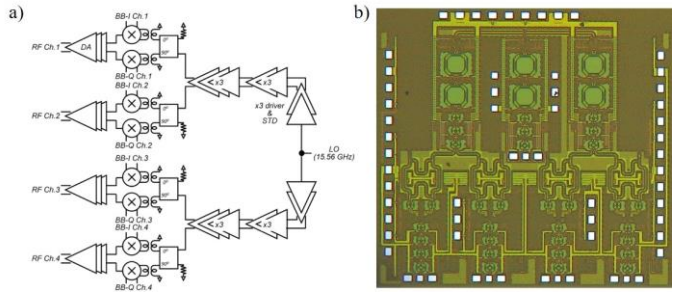

Fig. 8: Circuit block diagram (a) and microscope image (b) of the 4-channel transmitter (Size = 1.67mm × 1.76mm).

III. Transmitter Architecture and Building Blocks

The transmitter design is similar to that of the receiver, except that the up-conversion mixers are active Gilbert cell designs (Fig. 8). The three-stage LNA of the receiver was used, without modification, as the transmitter power amplifier.

A. IQ Modulator

IQ modulator uses double-balanced (Gilbert cell) mixers (Fig. 9a). The baseband inputs are digital, with a digital single-end to differential converter (Fig. 9b). This eases testing, but restricts transmitter operation to simple QPSK, and, further, prevents transmitter spectral shaping with e.g. root-raised-cosine modulation waveforms.

In simulations, the power amplifier showed 4.3 dBm output power (P_{1dB}) at 1-dB gain compression (Fig. 10) in single-tone operation. Similarly, simulated transmitter output power in QPSK operation is ~ 4.2 dBm.

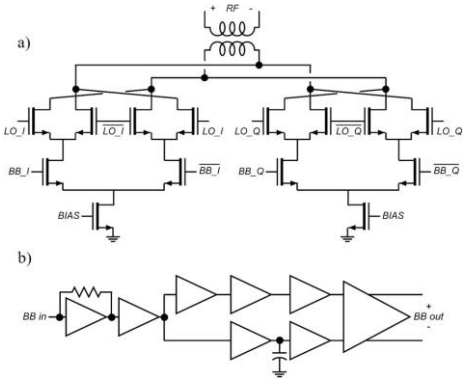

Fig. 9 Circuit diagram of a) Gilbert cell based IQ vector modulator b) baseband input driver

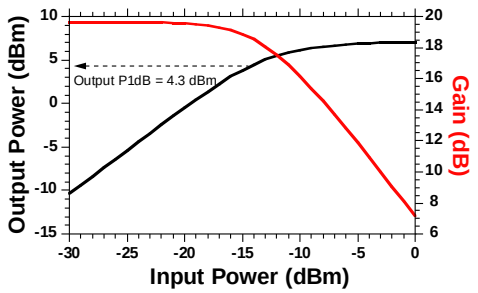

Fig. 10 Simulated output power, and gain vs. input power of the power amplifier

IV. Measurement Results

Transmitter and receiver single-channel characteristics were measured with all four channels biased. Linear S-parameter measurements used the equipment noted earlier; receiver gain characteristics are quoted with one of the two differential baseband outputs terminated in 50 Ω. Fig. 11a show the measured receiver frequency-dependent conversion gain with a fixed 145.9 GHz LO frequency, and with the baseband (and hence RF) frequencies swept. All data are corrected for probe losses and single ended to differential conversion. The measured conversion gain is 18 dB with 12 GHz 3-dB bandwidth. The difference (~30 vs ~18dB) in receiver's simulated and measured performance is a result of the reduced LO multiplier output power (Fig. 5). Fig. 11b show the measured frequency-dependent gain with a fixed 100 MHz baseband frequency and with the RF (and hence LO) frequencies swept. The narrowband 145 GHz zero in the transfer function, possibly the result of a power-supply resonance, will limit the transceiver data rate to 2-4 Gb/s. The 4-channel receiver operates with 1 V supplies for LNA, TIA and multiplier with 163 mA, 109 mA and 223 mA current consumption, hence 495 mW total power consumption for the 4-channel receiver.

The transmitter was tested with modulation on the Q input, with the I input held at a logic zero. Spectral measurements were performed using a mm-wave harmonic mixer and a microwave spectrum analyzer; measurements are corrected for probe losses. To measure the modulation bandwidth, the LO is held at 146 GHz, the baseband input frequency is swept, and the power in the double side band (DSB) modulation sidebands is measured (Fig. 12a). From this measurement, the 3-dB modulation bandwidth is around 6 - 8 GHz. The 4-channel transmitter operates with 1 V power supplies for driver amplifier, mixer and multiplier chain, with 161 mA, 94 mA and 208 mA current consumption, hence 463 mW total power consumption of the 4-channel transmitter.

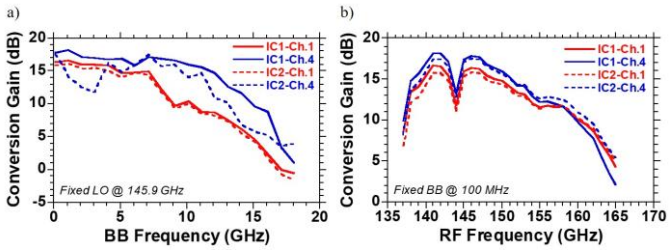

Fig. 11 Measured conversion gain of two different receive channels of two different chips with a) fixed LO at 145.9 GHz b) fixed baseband at 100 MHz

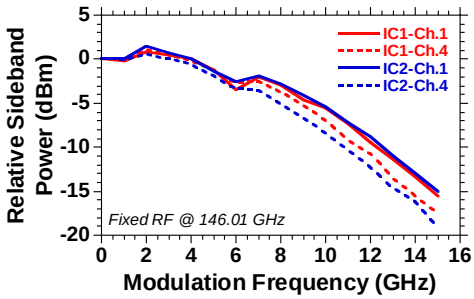

Fig. 12: Measured relative sideband power vs. modulation frequency with fixed RF frequency at 146.01 GHz for two different transmitter channels in two different ICs

Although these chips are designed to support 20 Gb/s QPSK data transmission, due to the notch in RF frequency-gain curve, it is expected to support 2-4 Gb/s QPSK data transmission.

After chip level measurements, transmitter and receiver ICs were mounted on separate printed circuit boards (PCBs), and were provided a common 16.6 GHz LO subharmonic drive signal. The transmitter and receiver ICs communicated between their 140 GHz ports via mm-wave wafer probes, a ~1 meter section of 140-220 GHz waveguide, and a waveguide attenuator (Fig. 13). The total attenuation between IC ports is c.a. 20 dB. Baseband I and Q data streams were generated by an arbitrary waveform generator whose maximum rate was 800 Mb/s, and eye diagrams are captured using a high speed digital oscilloscope. Fig. 14 shows eye diagrams measured at 500, 600 and 800 Mb/s data rates. The mm-wave carrier is at 9×16.6GHz =149.4 GHz. Wireless link measurements, at higher data rates will be measured shortly.

V. Conclusion

A 140 GHz QPSK transceiver front-end is presented, with four channels per IC to support MIMO transmission. We report one channel transceiver measurements in this paper. The measured performance is summarized and compared to the state of the art in Table 1. Initial link measurements have been demonstrated at an instrument-limited 800 Mb/s rate. Wireless link experiments are being prepared.

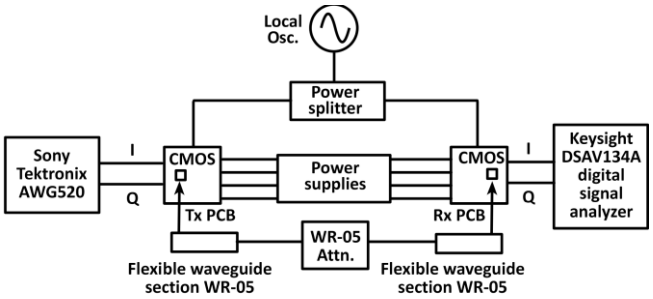

Fig. 13 Experimental setup of the link measurement

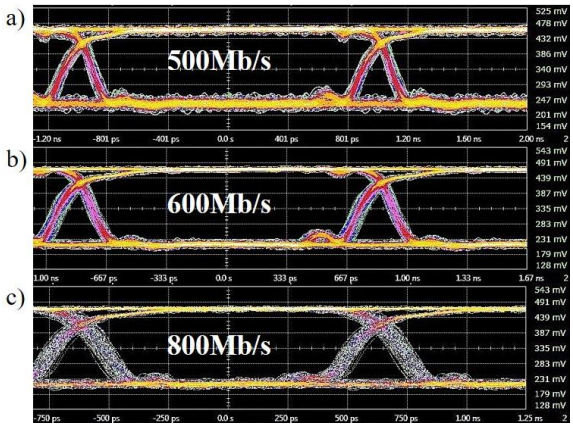

Fig. 14. Eye diagrams captured in Keysight digital oscilloscope DSAV134A for a) 500 Mb/s b) 600 Mb/s c) 800 Mb/s data rate

Table 1. Comparison between state-of-the-art designs

	[4]	[5]	[6]	[7]	**This Work**
Technology	65nm CMOS	28nm CMOS	45nm CMOS	250nm InP DHBT	45nm CMOS
Freq. [GHz]	240	102-128	155	110-170	140
Gain [dB]	25	36-39	23	26	18
NF [dB]	15#	8.4-10.4	20*	9.5	5.5*
Pdc [mW]	260 (1 TRx)	51 (1 Rx)	345 (1 TRx)	357 (1 TRx)	958 (4 TRx)
Area [mm^2]	2 (1 TRx)	0.89 (1 Rx)	3.92 (1 TRx)	3.64 (1 TRx)	5.91 (4 TRx)
Integration	Full	Rx Front End	Tx/Rx	Tx/Rx	Tx/Rx

*simulated, #calculated from measurements

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