100-340GHz Systems: Transistors and Applications

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***Abstract*—** We examine potential 100-340 GHz wireless applications in communications and imaging, and examine the prospects of developing the mm-wave transistors needed to support these applications.

I. Introduction

Wireless networks face exploding demand; the available spectrum is nearly exhausted. Industry is responding by introducing 5G systems at 28, 38, 57-71(WiGig), and 71-86GHz. Research now considers next-generation systems between 100-340 GHz. These will access a much larger spectrum. The short wavelengths provide massive spatial multiplexing in hub and backhaul communications. The short wavelengths will permit high-resolution imaging, from small apertures, to assist driving or flying in foul weather. Such applications will drive THz transistor development.

II. 100-340 GHz Systems

Consider three applications: a wireless communications base station or hub serving 100's of mobile users, a spatially multiplexed point-point backhaul link, connecting such hubs to the internet, and an imaging system, with TV-like resolution, enabling driving in very heavy fog or rain.

Fig. 1 shows a 140GHz spatially multiplexed hub, supporting 512 users. Each of 4 hub faces has 256 antennas, each $0.6\lambda \times 2.4\lambda$, in a 0.35m length phased array. Assume a handset with an 8×8 array at $\lambda/2$ spacing (9mm×9mm), 20 dB margins for packaging, manufacturing, aging, and partial beam obstruction, and uncoded QPSK modulation at 10^{-3} error rate. A 45 mW transmitter output power per element and 3 dB handset noise figure can then support 128 users, at up to 100m range, and 10Gb/s downlink rate per user, even in 50mm/hr. rain. At 75GHz, the same parameters would provide 160m range, but the arrays would have 4:1 larger areas.

Fig. 2 shows a spatially multiplexed backhaul link. N transmitters, carrying independent data, form an array of length L. The receiver, at distance R, has a similar array but uses MIMO [1] beamforming. If the array angular resolution λ/L is smaller than the element apparent angular separation L/NR, then the signals can recovered with high SNR. Link capacity is increased N:1. Short wavelengths are of great advantage, as a short array can then carry many channels; at 500m range, an 8-element array must be 1.6m long at 340GHz, 2.6m at 140GHz, and 3.5m at 75GHz. At 340GHz, if each array element is an 8×8 subarray of 7λ by 7λ elements (for small beam angle adjustment) then, with 20 dB total margins and QPSK at 10^{-3} error rate, transmitting 640Gb/s over 500m range in 50mm/hr. rain requires only 80 mW/element output power and 4dB receiver noise figure. Using two polarizations, the capacity is 1.2Tb/s in the same length array. At 140GHz, only 2mW/element is required, but the array is longer.

The third example (Fig. 3) is 340GHz imaging radar, for driving in e.g. heavy fog, providing a TV-like 64×512 pixel image refreshed at 60Hz. A linear 1×64 array steers the beam vertically, while frequency scanning and a frequency-selective Fresnel lens steers it horizontally. Given a 35cm×35cm aperture, 10% pulse duty factor, and 10dB SNR from a 1 ft^2 target at 300m range in heavy fog, the necessary peak output power is 50mW/element given 6.5dB receiver noise. The high 340GHz carrier permits a sharp 0.14 degree resolution from an array that can fit behind a car's radiator grille.

III. THz Transistors

These and similar systems will drive THz transistor development. CMOS VLSI can provide the baseband and mm-wave signal processing, with a few *application specific mm-wave transistors* (SiGe, InP, GaN) providing the low-noise amplifiers (LNAs), efficient power amplifiers (PAs), and, for >200GHz system, signal conversion to the final carrier frequency. GaN [2] provides very high power and efficiency at 94GHz, while SiGe HBTs have reached 720GHz f_{max} [3]. Here we consider the prospect for further improvement in InP THz transistors, serving applications to 340GHz and above.

InP HBTs serve in mm-wave frequency converters and PAs [4]; 130nm node InP HBTs attain 1.1THz f_{max}. Though 650GHz InP HBT transceivers have been demonstrated [4], even at 220GHz, PA efficiency is impaired by limited gain. Higher-bandwidth HBTs are desirable for efficient 220 and 340GHz PAs, and for 650GHz systems. Bandwidth is increased by scaling, decreasing semiconductor thicknesses, reducing junction widths, increasing current densities, and decreasing contact resistivities; [5] gives scaling laws and roadmaps. Yet, further improving f_{max} is difficult.

One challenge is parasitics distributed along the emitter stripe (Fig. 4); as with FETs, base metal resistance [6] decreases f_{max}. If the emitter length is reduced to reduce metal resistance, then capacitances from the base pad and the emitter ends become more significant, and f_{max} is again reduced. The base metal must be made thicker, and the base pad and inactive regions at the emitter ends made smaller

A second challenge is obtaining adequately low base contact resistance. Though base contacts of resistivity sufficiently low for the 32nm (3THz f_{max}) node have been demonstrated (Fig. 5) [7] in TLM test structures, it is difficult

realize such contacts in a processed transistor, where the contact is deposited on a surface exposed to several prior process steps. Refractory base contacts penetrate negligibly into even an 18nm thick base, and have shown excellent resistivity in TLMs [7]. Unfortunately, their resistivities in processed HBTs has been high, possibly due to their failure to penetrate residual surface oxides. Addressing this Rode [6] (Fig. 6, Fig. 7) used a 1nm Pt surface contact metal layer below a refractory Ru barrier. The Pt reacts with the base semiconductor and penetrates 2.7nm into it. This contact cannot be used for the 64 and 32nm nodes: the resistivity is too high. Further, the base doping is graded, being extremely high at the surface for low contact resistivity, but moderate towards the collector for reduced Auger recombination. As the base is made thinner with scaling, less base contact penetration can be tolerated if the metal is to contact heavily-doped semiconductor.

The first step in developing 90nm node HBTs was developing the scaled emitter junction and its tall contact via (Fig. 8). This uses a sputter-deposited, REI-etched $Ti_{17\%Wt}W_{83\%}$ alloy. Device images, and DC data, are shown in Fig. 9 and Fig. 10. RF data was poor due to a process failure during isolation. Given the difficulties with base contact, scaled emitter and base widths will not alone provide further increased f_{max}. We are therefore exploring regrowth processes.

Extrinsic base regrowth (Fig. 11) can indirectly provide the low base contact resistivity required for increased f_{max}. After forming the emitter-base junction, an extrinsic base is regrown upon the intrinsic base. Here, the motivation for regrowth differs from earlier work [8]; the extrinsic base can be very heavily doped ($\sim 2\cdot10^{20}$ cm^{-3}) (Fig. 5) for low contact resistivity, yet the intrinsic base can be more lightly doped ($\sim 5\cdot10^{19}$ cm^{-3}) for low Auger recombination hence acceptable β. The extrinsic base can be made moderately thick (~30nm), permitting a thicker Pt layer to penetrate more deeply through surface oxides for low contact resistivity, yet the intrinsic base can be made thin (10-15nm) for low base transit time. β will also increase because of reduced Auger recombination in the intrinsic base and reduced electron diffusion to the base contacts. High β improves noise figure in LNAs and improves DC precision in ADCs and DACs.

Regrowth can also bury dielectrics into the base-collector junction, as is common in SiGe HBTs [3] (Fig. 12). This permits wide base contacts for low base resistance, yet a narrow collector junction for low collector capacitance. Such structures can be formed by template assisted selective epitaxy (TASE) [9]. A dielectric template is first formed on the N+ subcollector. Upper portions of the N+ subcollector, plus the N– drift collector, are then grown within the template. The template top is removed, and the HBT base and emitter grown on the drift collector. The emitter-base junction is formed normally. Fig. 13 shows wide InP lateral overgrowth on a (111) InP wafer. This structure can be combined with extrinsic base regrowth to further enhance bandwidth.

Among transistors, InP FETs have the lowest noise, and serve in LNAs. For lower noise or higher frequencies, the cutoff frequencies must be increased. For this, the gate length must be reduced, but the g_mR_{ds} product must remain constant, and, given the fixed parasitic source-gate and gate-drain capacitances, the transconductance per unit gate width must be increased. These factors require a thinner channel and a thinner gate-channel insulator. In present InP HEMTs, this insulator, ~6nm InAlAs, cannot be made much thinner without unacceptably increasing the gate leakage. This gate dielectric scaling limit impairs further bandwidth improvements.

High-K ZrO_2 gate dielectrics can now be deposited with low interface trap density onto InAs. Using these, even 2.5nm ZrO_2 provides low gate leakage and 4.8:1 greater capacitance density than a 6nm InAlAs layer [10,11]. This will permit further scaling of mm-wave InAs MOS-HEMTs. Unlike in III-V MOSFETs, where the source and drain lie close to the gate, in a THz HEMT, for low parasitic capacitances, high-mobility modulation-doped spacers separate the gate from the source and drain. Fig. 14 shows a target device, formed using multiple MOCVD regrowths. Fig. 15 and Fig. 16 show DC and RF data of a preliminary device fabrication effort [11].

ACKNOWLEDGMENT

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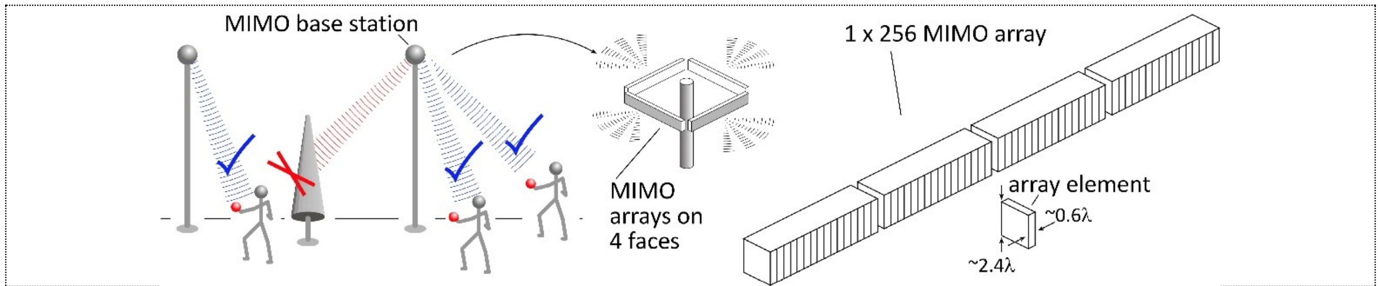

Fig. 1: Spatially multiplexed network hub. The hub has 4 faces, each a 256-element MIMO array, providing up to 128 independent signal beams. Link SNR analysis suggests that, with a 140GHz carrier at 100m range, 10Gb/s transmission per beam is feasible.

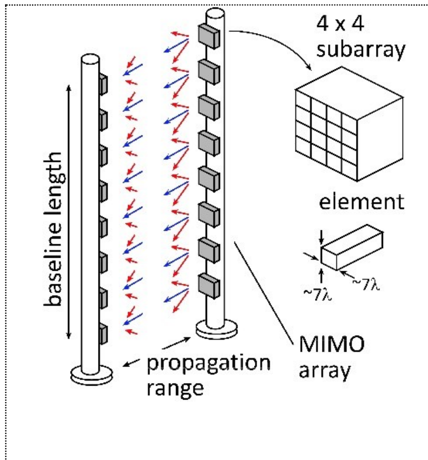

Fig. 2: Spatially multiplexed wireless backhaul link, using linear transmitter and receiver array, with each element being a 4×4 subarray.

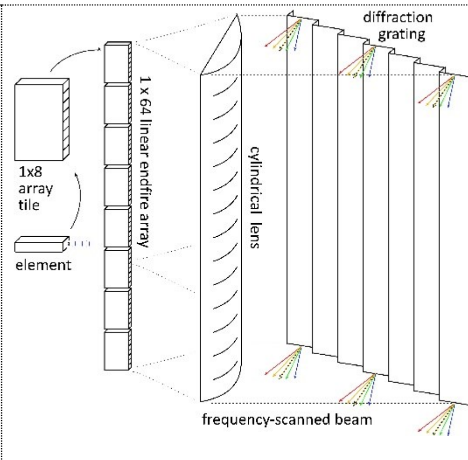

Fig. 3: 340 GHz frequency-scanned imaging radar for driving in foul weather. The figure shows a separate imaging lens and diffraction grating for lateral beamsteering; these can be combined into a Fresnel lens.

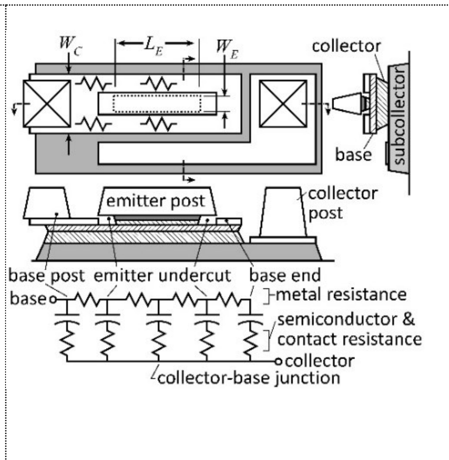

Fig. 4: Parasitic metal resistance and the junction capacitances of inactive device regions are both distributed along the length of the emitter stripe. These significantly reduce the f_{max} of THz HBTs.

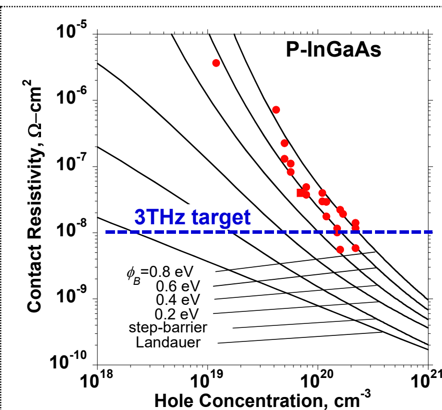

Fig. 5: Measured (dots) and computed (lines) contact resistance to P-InGaAs as a function of doping and barrier height. 10^{-8} Ω-cm^2 is sought for the 32nm (3THz f_{max}) node, and has been demonstrated in TLM test structures but not in HBTs.

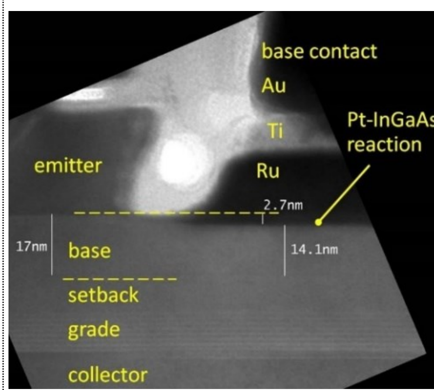

Fig. 6: FIB/SEM cross section of the emitter-base junction of an HBT nominally at the 130nm node. The HBT base contacts are 1nm Pt below refractory Ru, and have penetrated 2.7nm into the base.

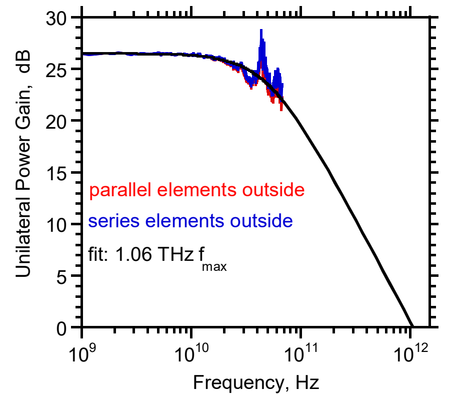

Fig. 7: Measured unilateral power gain of the HBT of figure 6, with the open- and short-circuit pads de-embedded in either order. A least-squares fit to the data de-embedded with the parallel elements outside yields slightly more than 1THz f_{max}.

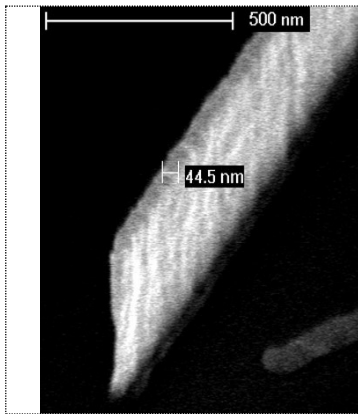

Fig. 8: InP HBT technology at the 65nm node: a ~400nm height, 44nm width dry-etched TiW emitter contact/via.

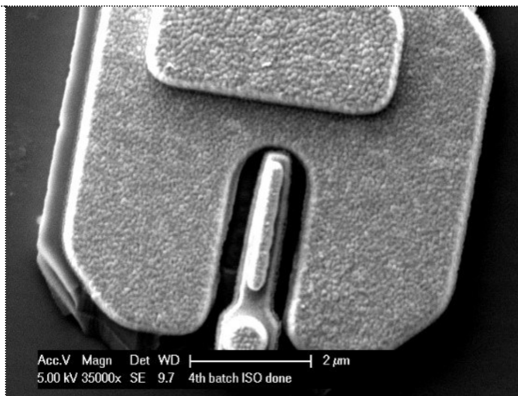

Fig. 9: InP HBT nominally at the 65nm node. This particular device has a 90nm emitter junction width.

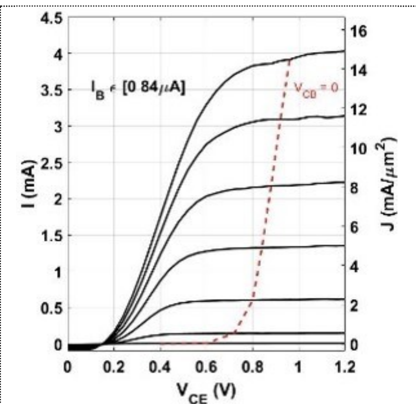

Fig. 10: DC common-emitter characteristics of an InP HBT with a 90nm emitter. The DC current gain is 45.

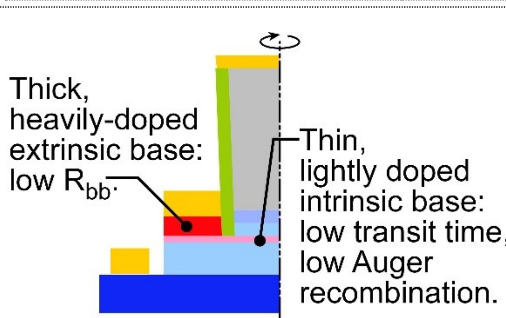

Fig. 11: Regrowth can provide a extrinsic base thicker and much more heavily-doped than the intrinsic base, enabling reduced contact resistance.

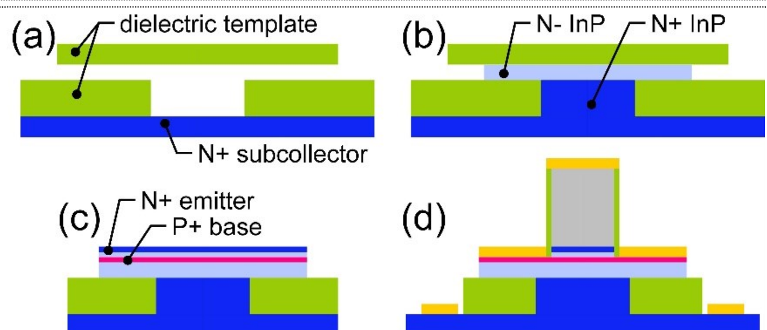

Fig. 12: Process flow for fabrication of THz HBTs with dielectrics buried within the base-collector junction: (a) dielectric template, (b) regrowth, (c) emitter and base growth, and (d) completed device.

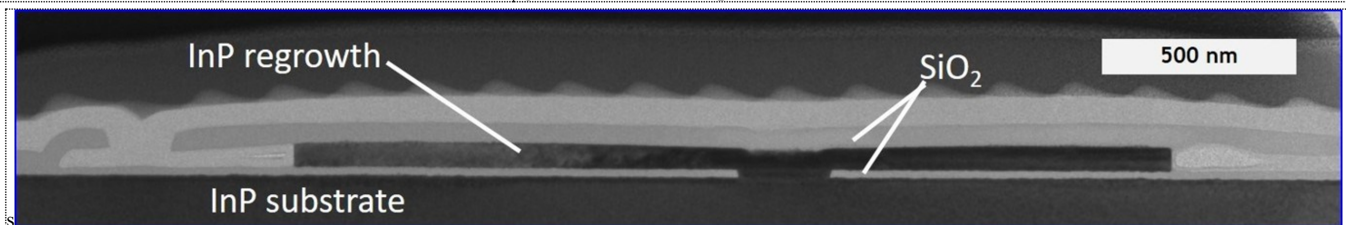

Fig. 13: FIB/TEM image of a ~100nm thick InP film grown by TASE on a (110) InP substrate.

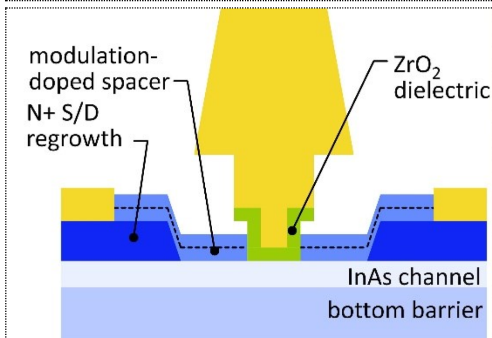

Fig. 14: THz InP MOS-HEMT with a ZrO2 gate dielectric and high-mobility modulation-doped source-gate and gate-drain spacers.

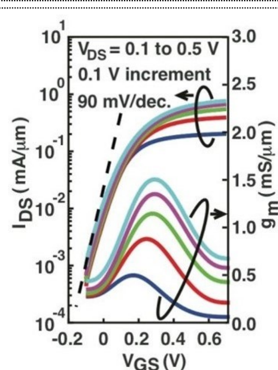

Fig. 15: DC characteristics of a InAs-channel MOSFET at 30nm gate length.

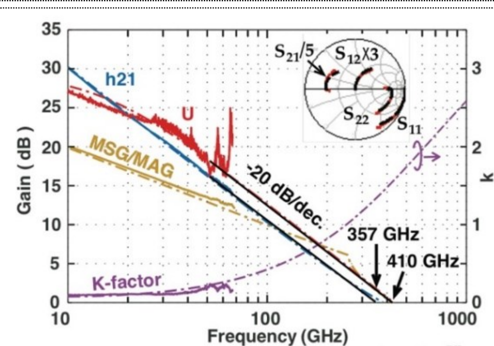

Fig. 16: RF characteristics of a InAs-channel MOSFET at 30nm gate length.