Materials for nm Transistors: 2D or 3D ?

Mark Rodwell,
University of California, Santa Barbara

2D or 3D Semiconductors ?

2D or 3D: which for future electron devices ?

VLSI

high-frequency wireless

power conversion

What are the challenges ?

...and how best to solve them ?

How should materials community best direct its efforts ?

A plea from a transistor & IC design guy:

Please focus on atomic-scale techniques in 3D materials

Goals:
Transistors for Computers
Transistors for Radios

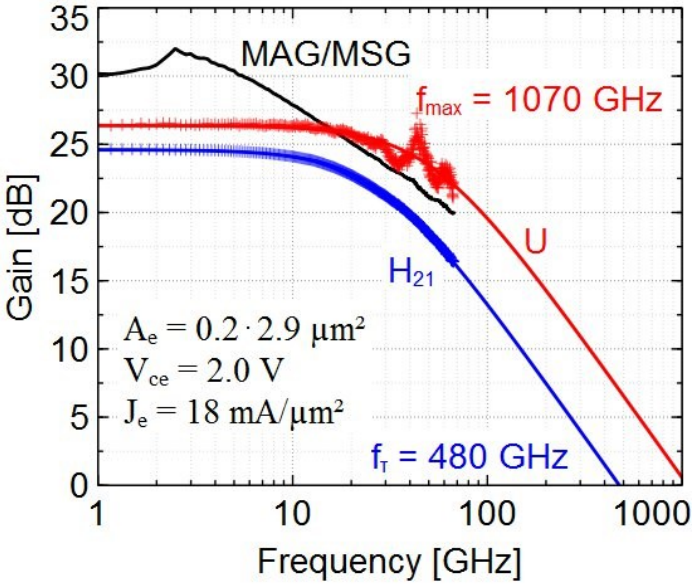
Transistor design: high-frequency wireless

Bipolar transistor cutoff frequencies:
transit times, RC charging times, CV/I delays

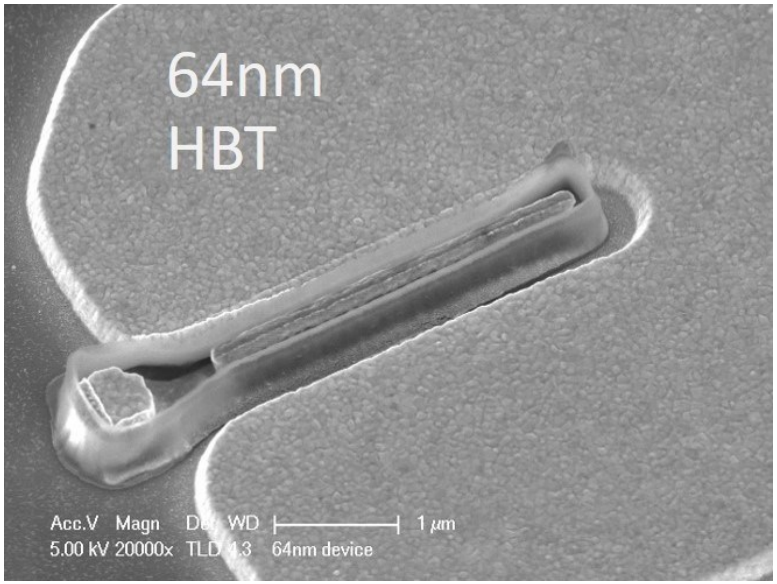
High-frequency scaling
narrow junctions, thin epi layers, high electron velocity
high current density, **ultra low resistivity contacts**

Are 2D materials relevant ?

130 nm result
Rode (UCSB), IEEE TED, 2015



64 nm in development
Yihao Fang, UCSB, unpublished



Transistor design: high-frequency wireless

Field-effect transistor cutoff frequencies:

Transconductance. Output conductance

Gate-channel capacitance. Gate end capacitances.

Source and drain access resistance

Need **thin channel** and **thin gate dielectric**

For low output conductance.

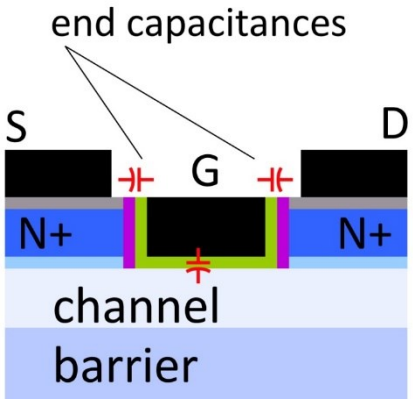
For high transconductance → low C_{end}/g_m time constant.

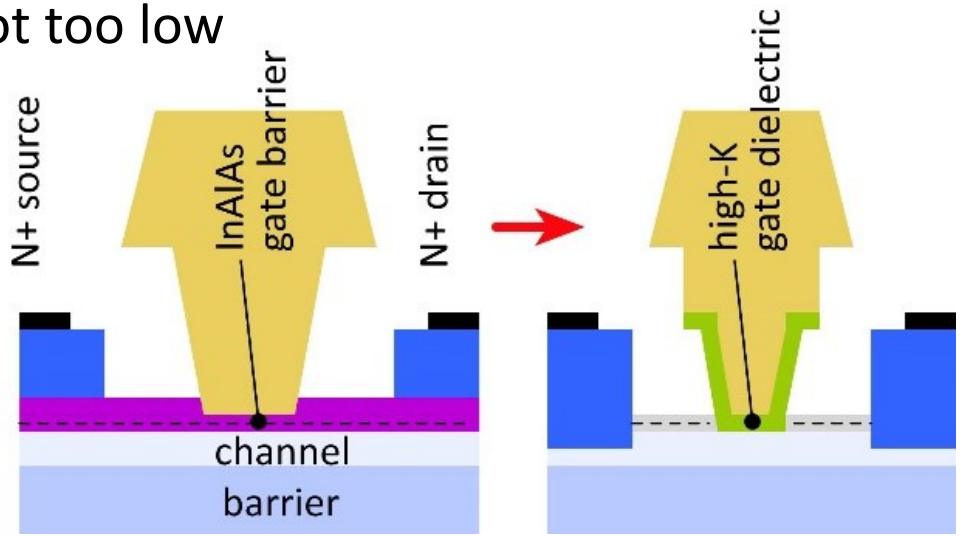
Need low access resistivities

regrown N+ source / drain interfaces to channel

very low resistivity metal-semiconductor contacts

Channel **m*, DOS**: not too high, not too low





Transistor design goals: VLSI

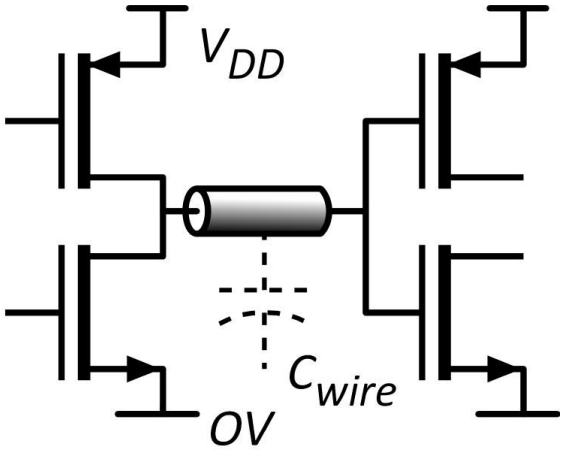
Small transistors: plentiful, cheap

Small transistors→ short wires

small delay CV_{DD}/I

low energy $CV_{DD}^2/2$

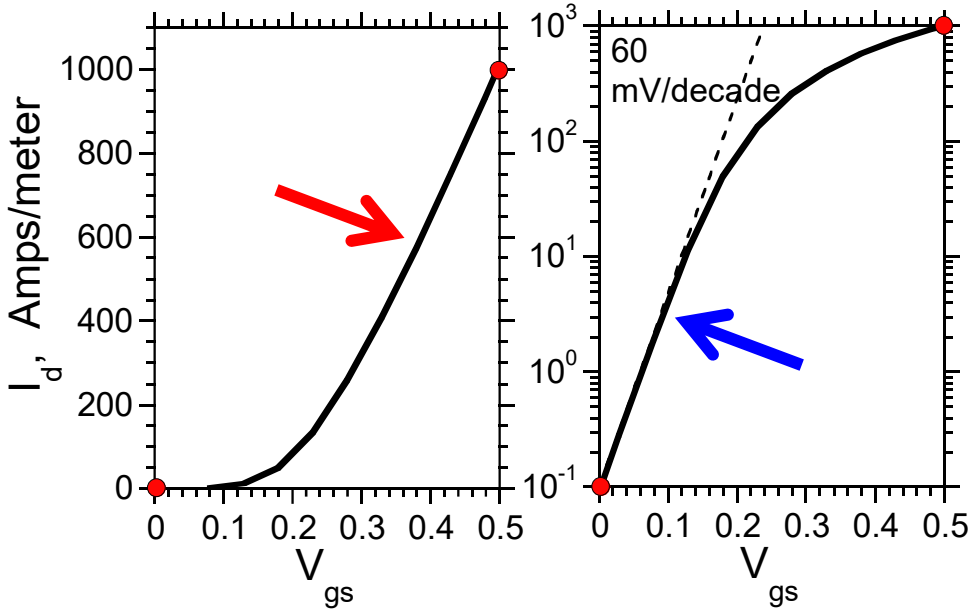
Small transistor footprint is key



Low leakage current

thermal: $I_{off} > I_{on}*\exp(-qV_{DD}/kT)$

want low V_{DD} yet low I_{off}.



Want:

Large *dI/dV* above threshold

Large on current (mA/micron^2)

If possible, subthreshold swing steeper than thermal→ low V_{DD}

Transistor design: challenges and solutions

VLSI FETs: Electrostatic scaling limits

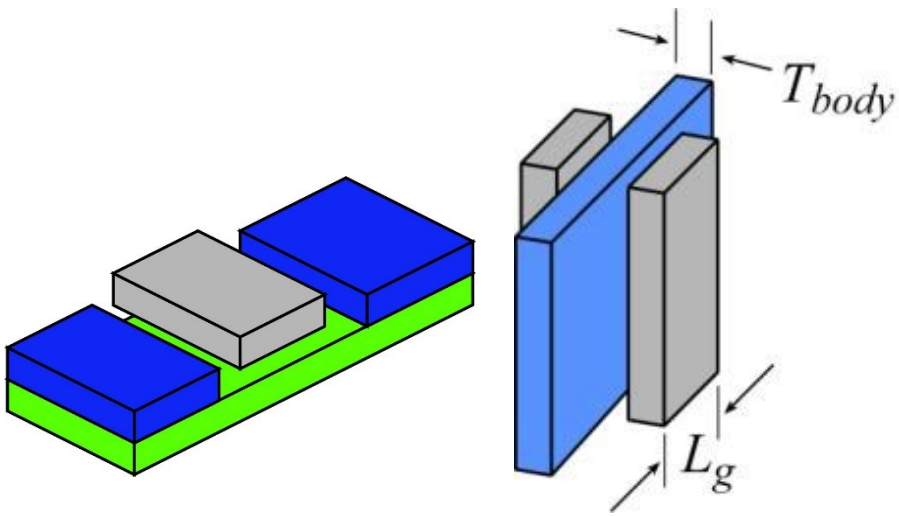
Low subthreshold swing:

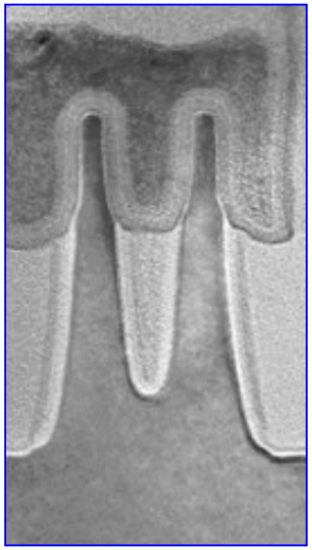
Need large gate-channel capacitance
much larger than drain-channel capacitance.

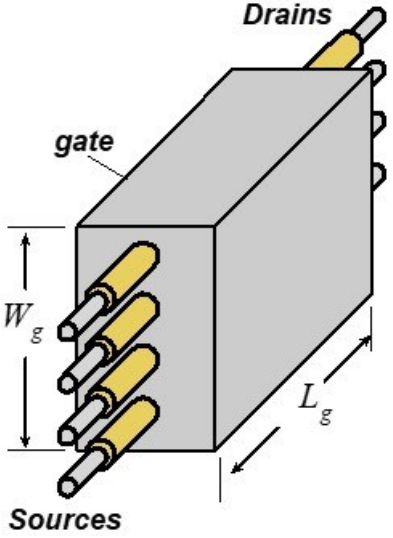
Scaling = shorter gate: **need thinner dielectric, thinner channel**

Tunneling leakage: **minimum dielectric thickness**

→ **finFETs, gate-all-around FETs**.







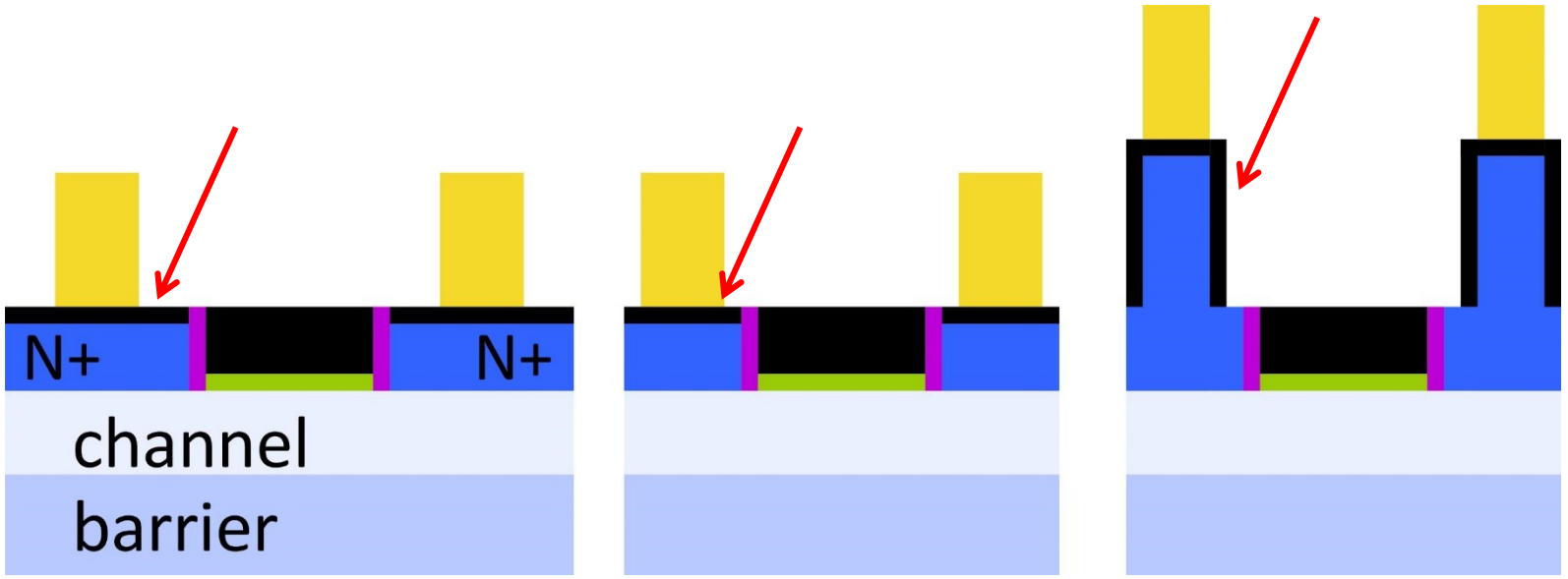
VLSI FETs: S/D access resistivity

7nm node: contacts are substantial fraction of FET footprint

Source/drain access resistance = $\rho_{contact}$/Area

Need extremely low contact resistivity, ~3× 10^{-9} Ω-cm^2.

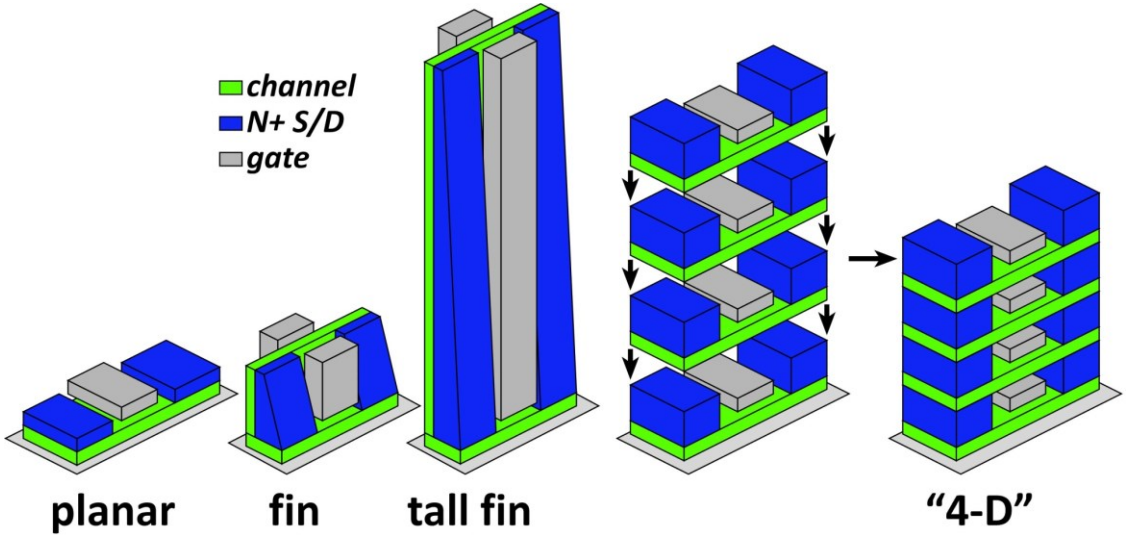
or: **corrugated or vertical contacts**



VLSI FETs: increasing drive current density

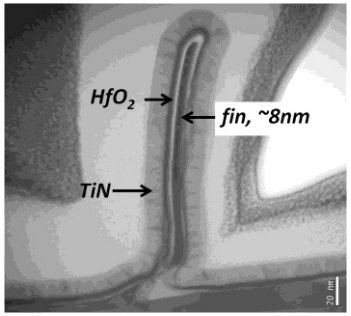
more current per IC area→ smaller IC area→ shorter wires

→ **3D integration**

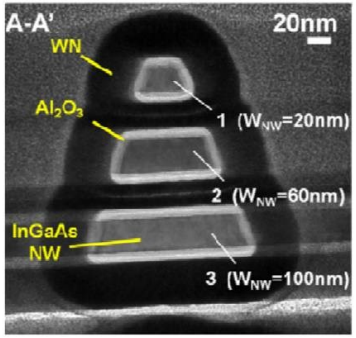


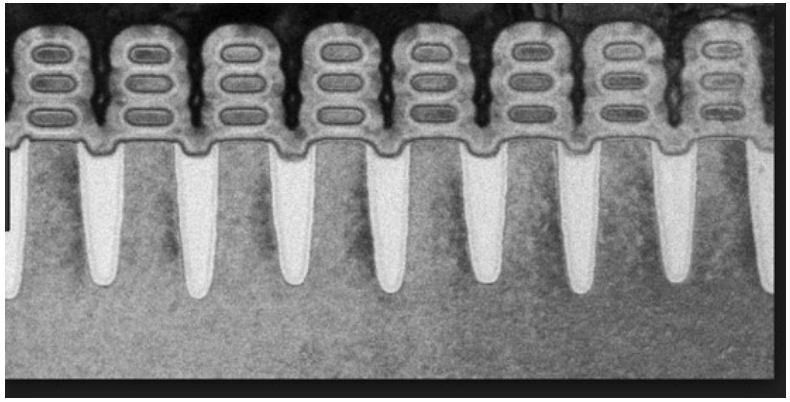
stacked nanosheet FET

Cohen-Elias *et al.*,
UCSB
2013 DRC



J .J. Gu *et al.*, 2012 DRC,
Purdue (P. Ye group_
2012 IEDM





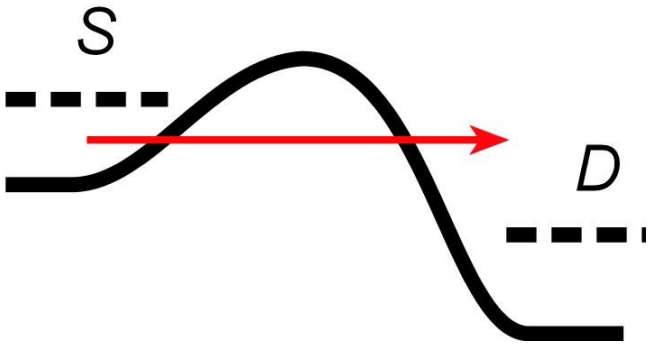
https://www-03.ibm.com/press/us/en/pressrelease/52531.wss

VLSI FETs: S/D tunneling

Source-drain tunneling leakage:

$$I_{off} \propto \exp(-2\alpha L_g), \quad \text{where } \alpha \cong \hbar\sqrt{(qV_{th})}$$

imposes minimum gate length



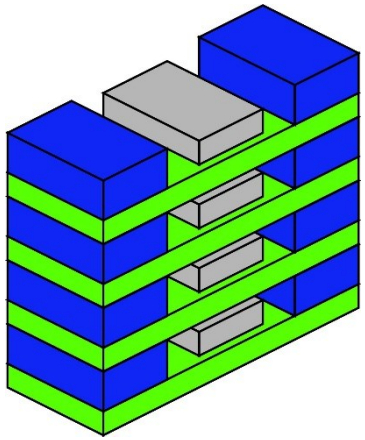
Solution 1: **increased transport mass** (Lundstrom)

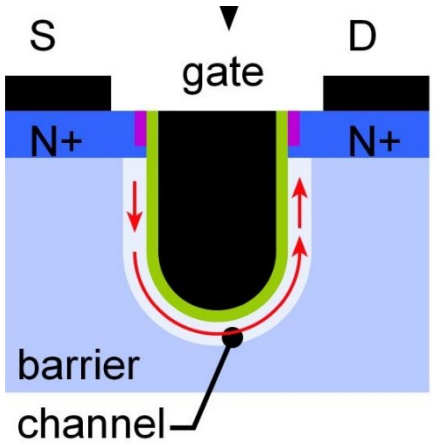
anisotropy, strain

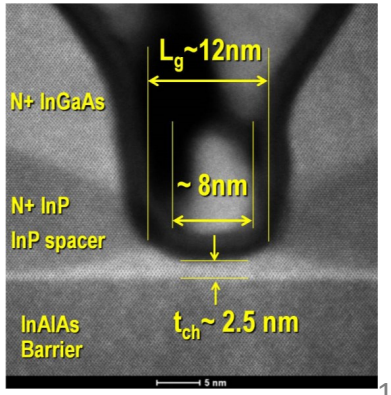
Reduces mA/μm with 2DEG FETs. Not so in nanowires

Favors stacked **stacked nanosheet**, **stacked nanowire**

Solution 2: **Corrugation. U-shaped device**.







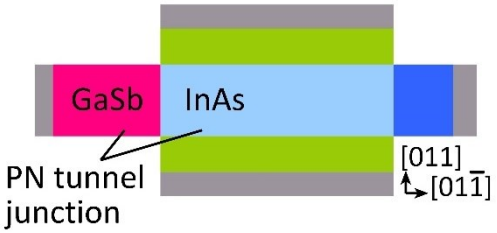
VLSI FETs: power density & supply voltage

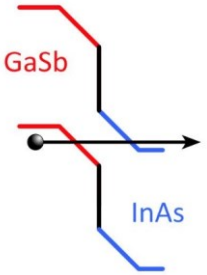
TFETs (and FerroFETs): steep subthreshold swing

TFET: truncates source thermal distribution.

TFETs are hard to build !

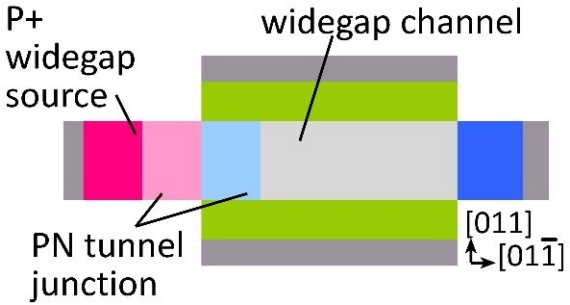
Requires **PN, heterojunction perpendicular to channel**
needs **ultra thin channel** for high junction field

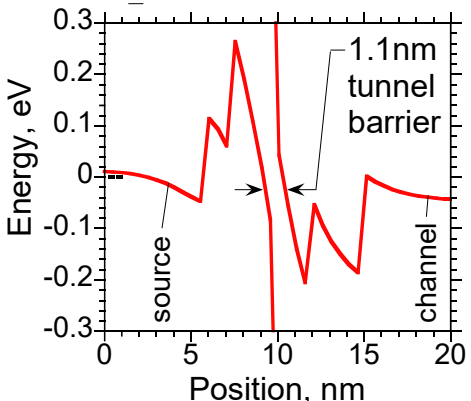




UCSB triple-heterojunction TFET designs.

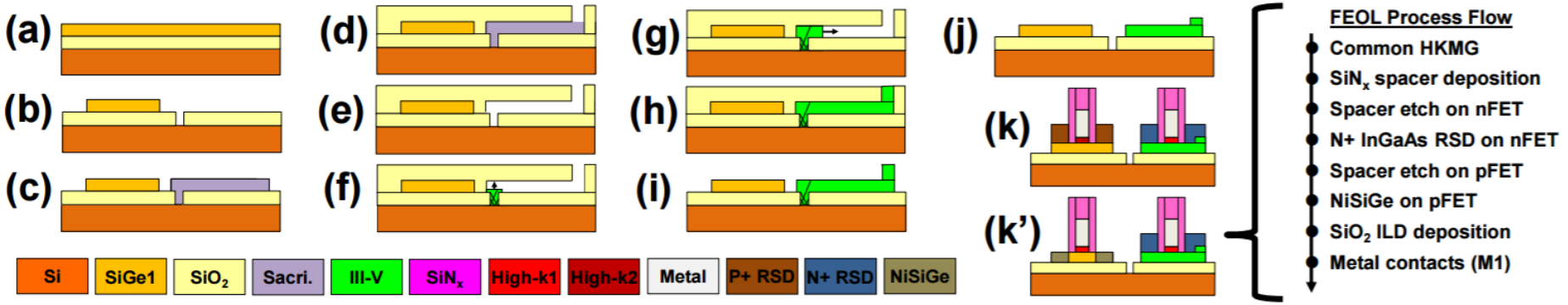
simulations: about 30:1 more on-current, **30:1 faster** logic
even harder to build ! Working on these now.





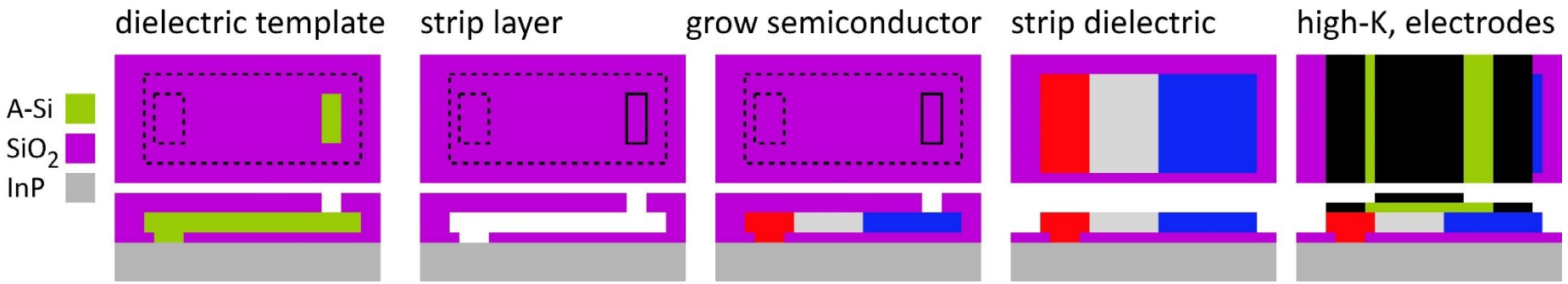
Template assisted selective epitaxy

L. Czornomaz et al. (IBM Zurich), 2015 & 2016 VLSI Symposia



Can make **PN and HJ perpendicular to channel**
Can **control thicknesses to near-atomic precision**.

We are trying to use this to make 3HJ TFETs.



Do 2D materials help ?

Do 2D materials aid nm transistor scaling ?

The argument often presented:

Thinner channel→ thinner (channel+dielectric)→ shorter $L_{g,min}$

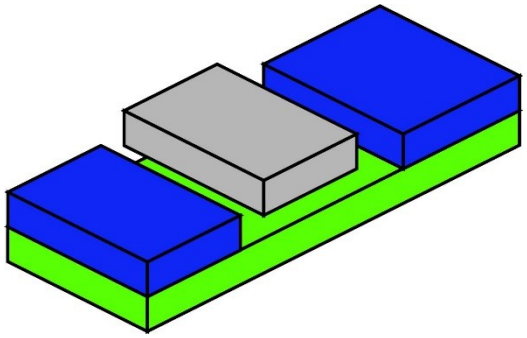
The counter-argument:

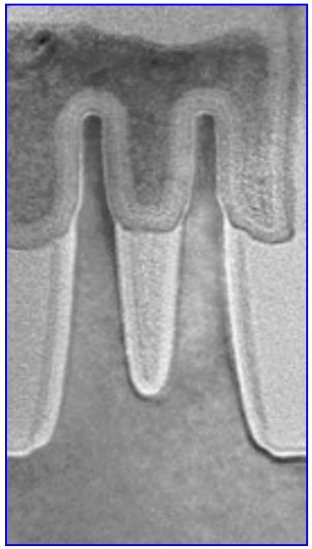
It is the sum (channel+dielectric) thickness that matters

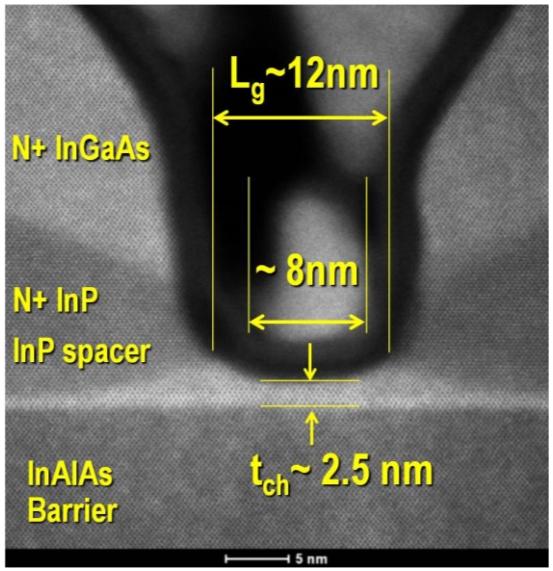
Dielectric: minimum ~0.5nm EOT

Little benefit for channels thinner than 2 nm

and...we can make 2nm channels with 3D semiconductors







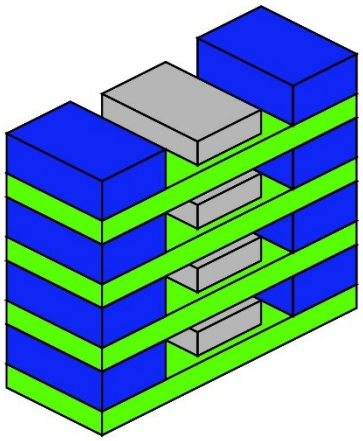
2D materials: other problems

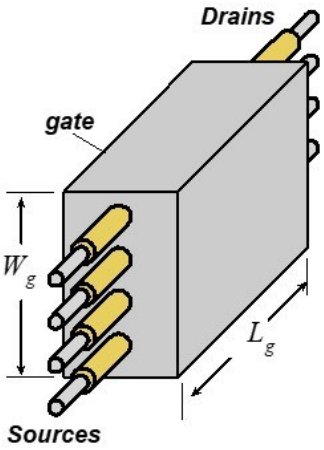
VLSI: large required areas, low defect density.
Exfoliation/transfer→ creases:

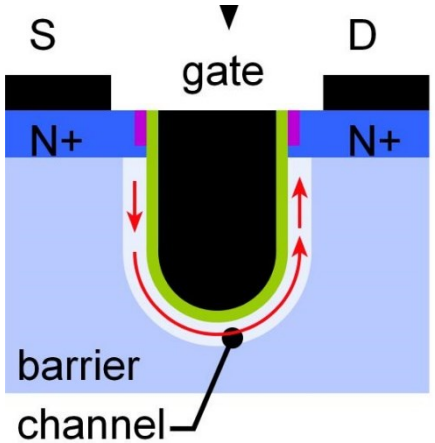
Can I make **finfets** ?
or **stacked nanosheet FETs** ? or **stacked nanowires** ?

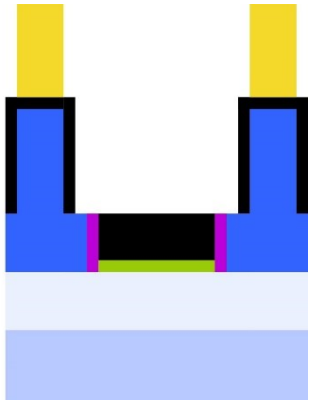
Can I introduce **corrugation** ? increase S/D **contact** area ?

Can I get **contact resistivity below 10^{-8} Ω-cm²** ?









A plea to the materials community

When it gets crowded, build vertically

Los Angeles: sprawl

Manhattan: dense

2-D integration:
wire length $\propto$ # gates$^{1/2}$

3-D integration:
wire length $\propto$ #gates$^{1/3}$

LA is interconnect-limited

1) Chip stacking (skip...different community)
2) 3D transistor integration

What should we do? **3D/2D/3D** electronics

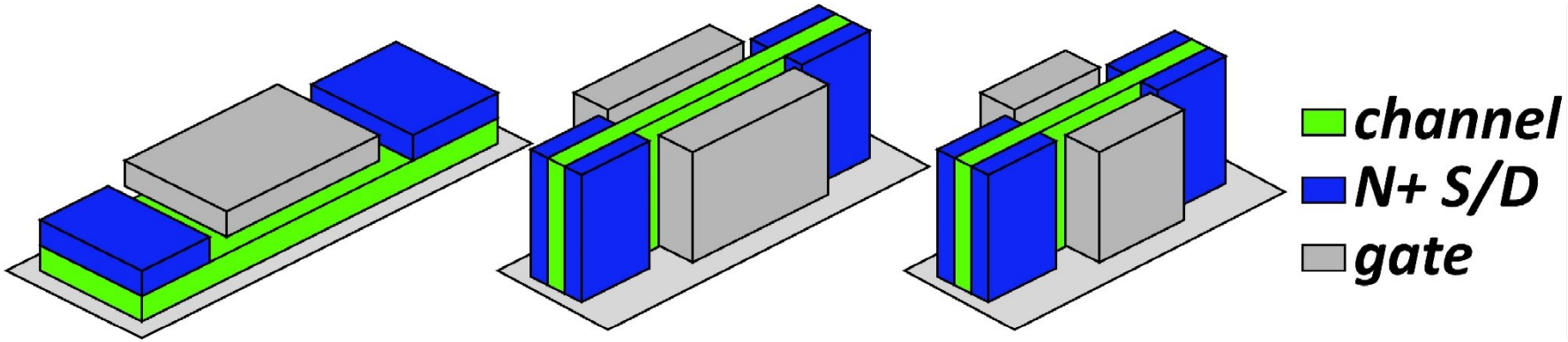
Vertically integrated **3-Dimensional transistors**
using
nearly 2-Dimensional channels (1nm or thinner)
made from
3-Dimensional materials

Vertically stacked horizontal nm MOSFETs

Laterally packed vertical nm MOSFETs and TFETs

...with near-atomic control of semiconductor layer thicknesses

What integration density must we beat ?



finFETs permit somewhat shorter gate length than planar FETs

But 7nm node uses 15nm gate*; can't get much shorter.

*http://ieeexplore.ieee.org/document/7838334/

What should we do? nm stacked horizontal FETs

Vertical nanosheets: 1 nm channel easier than in finFETs

thin the channel to 0.7-1nm

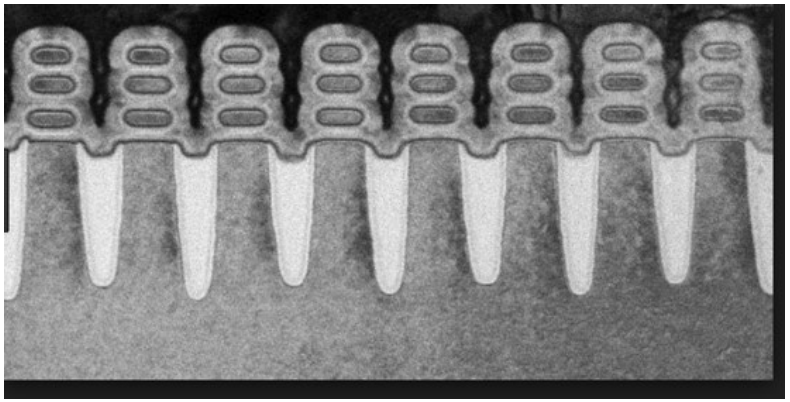
precision growth: Atomic Layer Epitaxy .

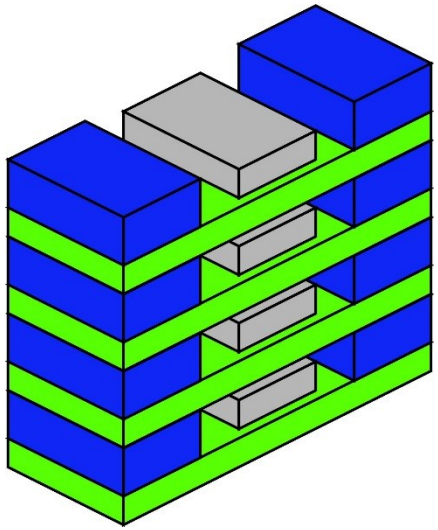
precision surface etching: Atomic Layer ETching

But:

only helps electrostatics when body dominates over high-K

only helps S/D tunneling given high transport m*.

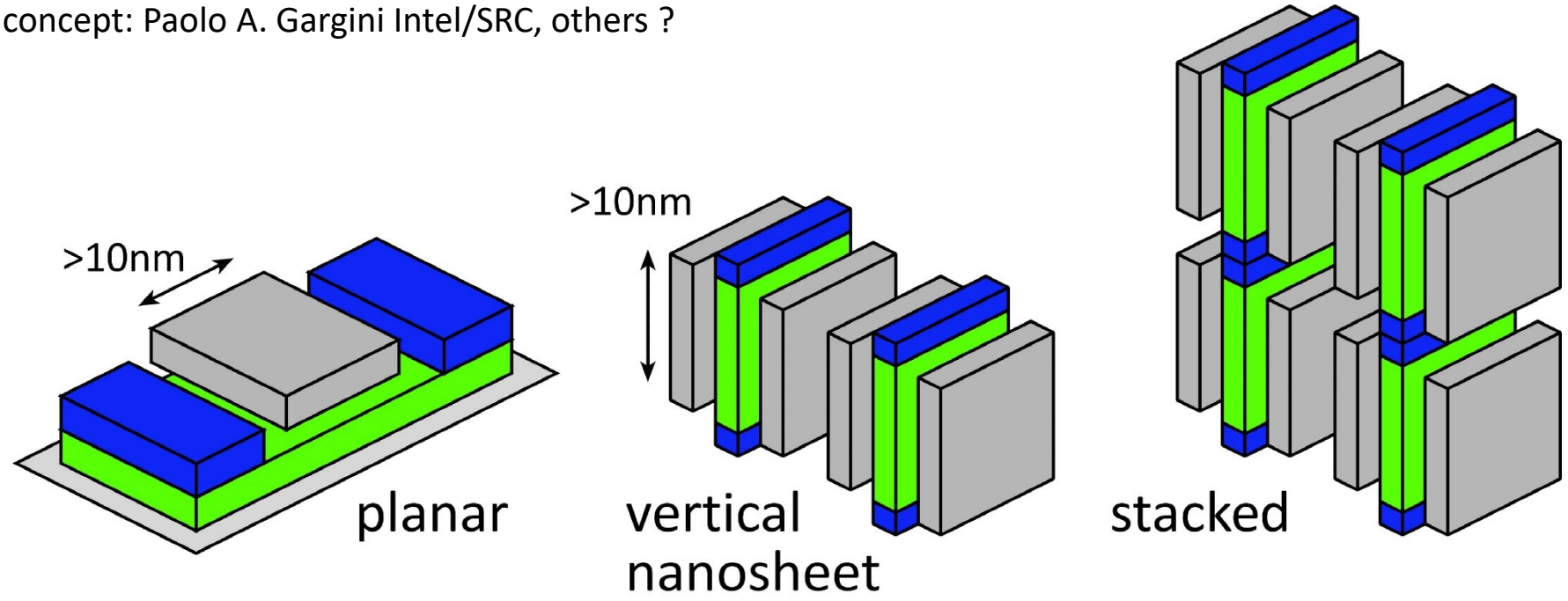




https://www-03.ibm.com/press/us/en/pressrelease/52531.wss

What should we do? nm-channel vertical integration

concept: Paolo A. Gargini Intel/SRC, others ?

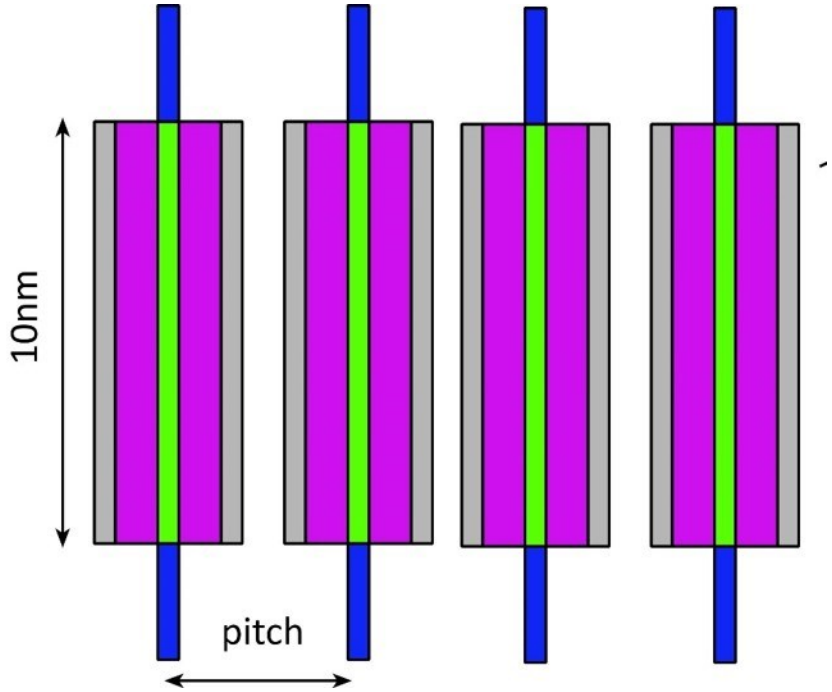


Vertical devices:

gates can be long (~10nm),
yet devices can be packed at <10nm spacing
→ increased integration density

What integration density can be achieved ?

3D: what density can be reached ?

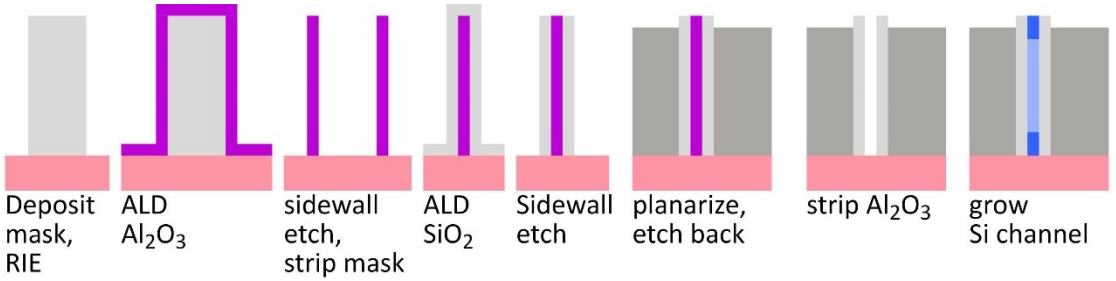


Gate dielectric:	1nm - limited by tunneling
FET-FET spacing:	1nm - limited by tunneling
Semiconductor channel:	1nm
Gate metal:	0.5 nm
device pitch (?)	5nm

Physics limits: ***Integration density can be significantly increased***

Technology limits: ***1nm-thickness fabrication feasible?***

nm-scale fabrication



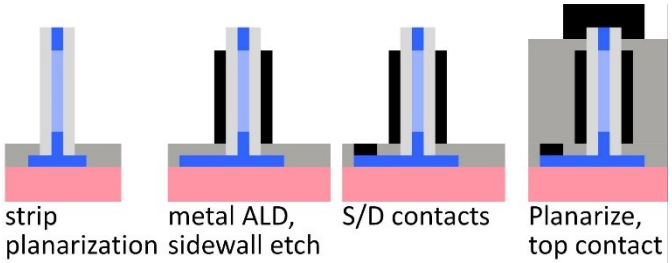
*V. Djara et al, 2015 VLSI Symposium

nm-scale semiconductor growth: template assisted epitaxy*

form ~2-atom-thick Si layer (not 2D semiconductor)

technique: selective growth in ALD-defined sacrificial template

ALD has single-atom thickness control



nm-scale metallization and contacts

ALD metal processes, sidewall etch processes

TFETs can be also fabricated by this technique