Microwave Dual-Conversion Front-Ends for 2-20 GHz Reconfigurable Transceivers

Seong-Kyun Kim[1,2], Rob Maurer[1], M.J.W. Rodwell[1]
[1]ECE Department,
University of California,
Santa Barbara, CA 93106
rodwell@ece.ucsb.edu

Miguel Urteaga[2]
[2]Teledyne Scientific Company
1049 Camino Dos Rios,
Thousand Oaks, CA 93021
Seongkyun.Kim@Teledyne.com

***Abstract*— We report upconversion and downconversion ICs designed as components for a dual-conversion microwave receiver using a 100GHz 1st IF and a target 2-20GHz RF tuning range. The IC have high dynamic range, with the upconversion IC having 20-25 dB IIP3 and 5-7dB conversion loss, hence 5-7dB predicted noise figure. 2nd-generation ICs, in fabrication, target a 2-40GHz spurious-free tuning range.**

Keywords—Dual conversion, wideband receivers, microwave receivers, InP HBT

I. Introduction

The DARPA ACT program goal seeks to reduce the cost and time required to design microwave transmitters and receivers operating at any specified DOD-relevant frequency in the 2-20GHz bandwidth. To this end, the program seeks to develop transmitter and receiver ICs that operate with useful dynamic range over the entire 2-20GHz bandwidth. A transceiver operating at any particular frequency channel within this large bandwidth can then be quickly developed by combing the broadly-tunable transceiver with application-specific PA, LNA, and filters designed for the specific target frequency band of operation. Custom microwave systems can then be developed quickly and cheaply.

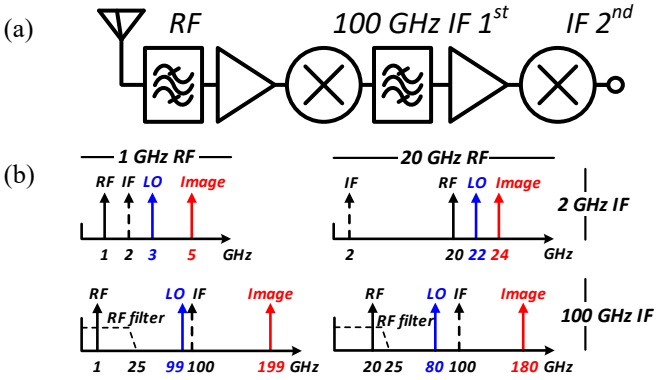


Fig. 1: Dual-conversion receiver (a) with a 100GHz first IF frequency. Frequency plans (b) of a 1-20GHz receiver using either a 2 GHz or 100GHz 1st IF. With a 2GHz 1st IF, image responses fall within the receiver passband; with a 100GHz 1st IF, they do not.

Such broadband receivers can be constructed from a ~40 GS/s sample rate ADC, combined with an input LNA and filter, plus output digital filtering. This, however requires that the ADC, and the subsequent digital filter, have both high sample rates (for 2-20GHz coverage) and high resolution (for high receiver dynamic range). Here we demonstrate a complementary approach, a dual-conversion superheterodyne receiver with a 100GHz first intermediate frequency (IF). Dual-conversion is an established broadly-tunable RF transceiver architecture wherein upconversion to a 1st IF frequency much higher than the input RF frequency places the receiver image response well outside the target tuning bandwidth (Fig. 1). We extend the design to microwave frequencies, with a target 2-20GHz RF tuning range, by placing the 1st IF at 100GHz [1]. Such high IF frequencies are made feasible by THz semiconductor process technologies. In particular, at the 128nm node, InP HBTs show 1.1THz f_{max} [2]; this allows high dynamic range mixers and amplifiers to be realized at the 100GHz 1st IF frequency.

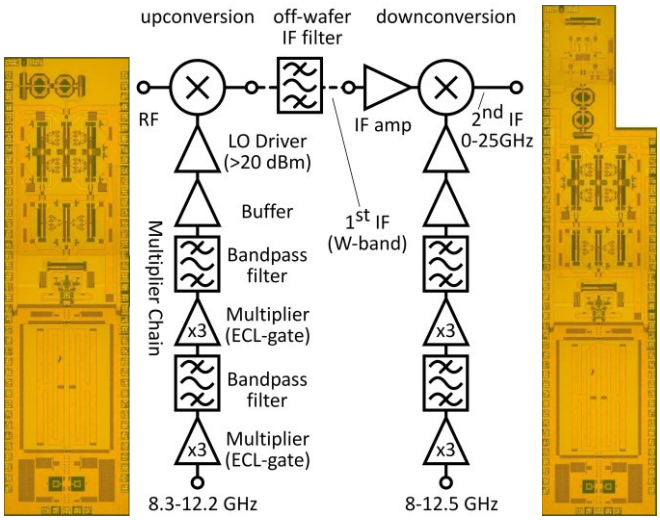
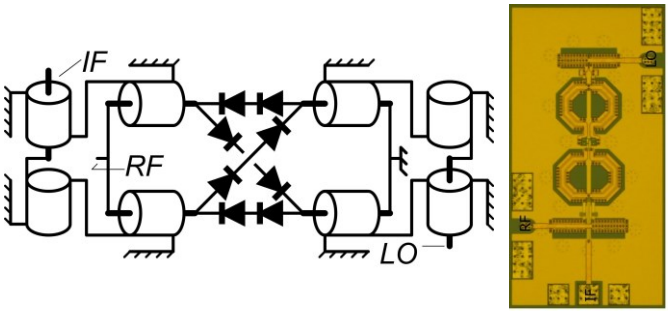


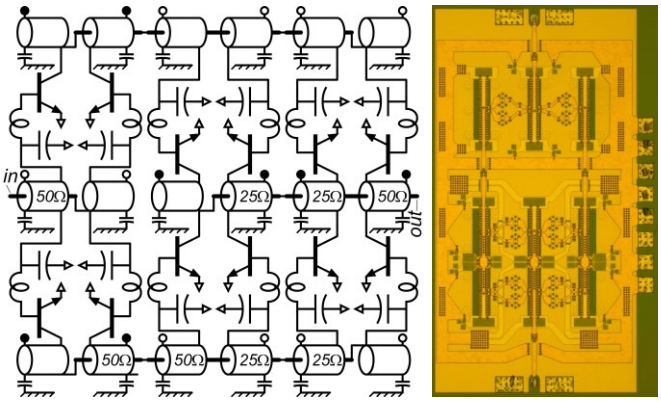
Fig. 2. IC photographs and block diagrams of the upconversion and downconversion ICs within the dual-conversion receiver (the upconversion IC is 4.3 mm × 1.1 mm).

II. IC Designs and Results

In the receiver (Fig. 2), an upconversion IC converts the signal from RF to the 1st IF. As low phase noise is necessary for RADAR, instead of a PLL, a 9:1 multiplier generates the LO. The signal passes through a compact off-wafer W-band waveguide bandpass filter to the downconversion IC, consisting of an IF amplifier, a downconversion mixer, and a second 9:1 LO multiplier chain. The user can set the 2nd IF between DC and 25GHz.



(a)



(b)

Fig. 3: Broadband, high-IP3 upconversion mixer (a) and broadband high-power LO driver (b).

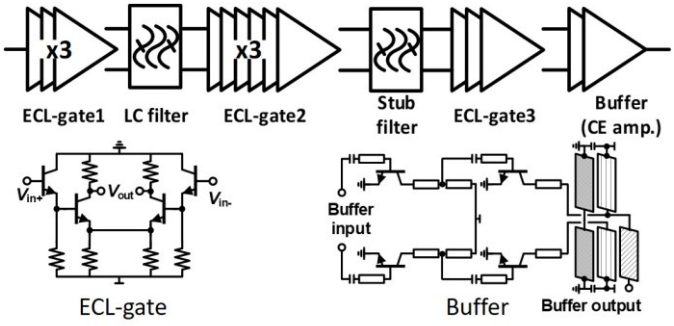


Fig. 4: LO multiplier chain: block diagram (top), ECL gate (bottom left) as 3:1 multipliers/amplifiers, and output buffer (bottom right).

The ICs have several novel features for high dynamic range, wide tuning range, and high IF frequency (Fig. 2, Fig. 3). The diode mixers use broadband baluns, Schottky-like InP DHBT base-collector junction diodes, and high ~20 dBm LO power. The LO driver provides >20 dBm P_{sat} over 55-100GHz. The LO multiplier chain uses *logic gates* as both compact broadband multipliers and amplifiers, even at 100GHz. The IF amplifiers have 6dB gain, 8dB noise figure and 20dBm OIP3 at 94GHz. Over a 1-20GHz RF bandwidth (Fig. 5), the upconversion IC has 20-25 dB IIP3 and 5-7 dB conversion loss, hence (since the mixer is passive) 5-7dB noise figure. Without the IF amplifier, the downconversion IC has similar performance. Each IC consumes ~2W. Given this measured performance, used with a 2dB-noise-figure LNA with 12 dB gain, the dual conversion receiver is expected show 6.7dB noise figure and 11dBm IIP3; with 18 dB LNA gain, we would expect 3.8dB noise figure and 5dBm IIP3

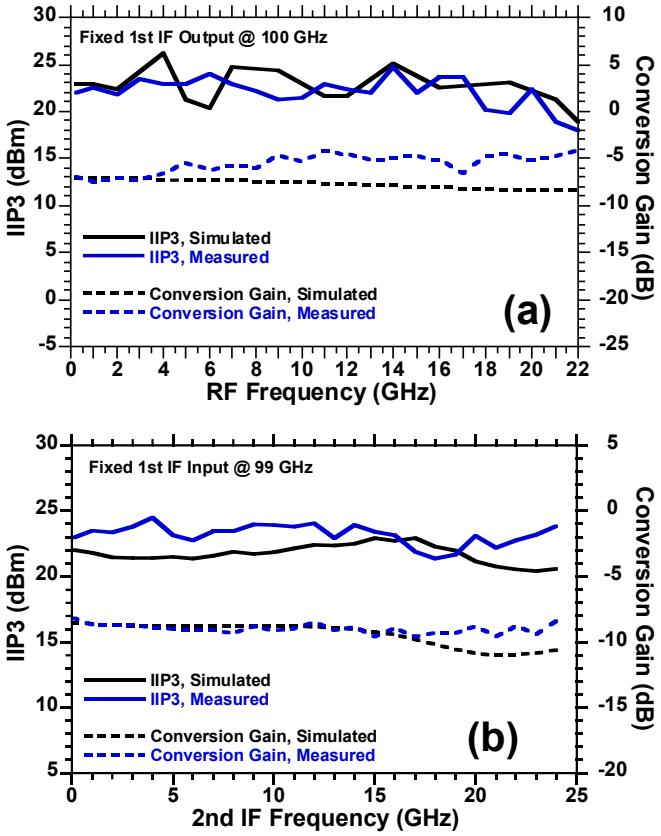


Fig. 5: Performance of the upconversion IC as a function of RF frequency (a), and of the downconversion IC (without IF amp) as a function of the 2nd IF frequency (b).

III. Future Work

2nd-generation ICs, presently in fabrication, use a new digital frequency multiplication architecture to suppress spurious harmonics, easing multiplier harmonic filtering requirements and improving the receiver spurious-free tuning range. These designs also use novel mixer architectures to maintain spurious-free dynamic range while reducing the required DC power.

[1] S. K. Kim, R. Maurer, M. Urteaga and M. J. W. Rodwell, "A High-Dynamic-Range W-Band Frequency-Conversion IC for Microwave Dual-Conversion Receivers," 2016 IEEE Compound Semiconductor Integrated Circuit Symposium, Austin, TX, October 23–26,

[2] M. Urteaga, *et al.*, "A 130 nm InP HBT integrated circuit technology for THz electronics" 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, December.