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L_g = 30 nm InAs Channel MOSFETs Exhibiting f_{max} = 410 GHz and f_t = 357 GHz

Jun Wu, Yihao Fang, Brian Markman, Hsin-Ying Tseng, and Mark J. W. Rodwell

***Abstract*—We report L_g = 30 nm InAs-channel MOSFETs exhibiting 420 GHz f_{max}, record for a III-V MOSFET, and 357 GHz f_t. The device incorporates a 5 nm strained InAs channel grown on an InP substrate. To reduce the parasitic gate-source and gate-drain capacitances, regrow lateral access regions increase the separations between the gate and the N+ source and drain; modulation doping within these access regions provides a low associated series resistance, enabling high g_m. The 30 nm L_g device shows an 1.5 mS/μm DC peak extrinsic g_m at V_{DS} = 0.5 V and V_{GS} = 0.3 V, 91% of the value (1.65 mS/μm) extracted from 10 MHz RF measurements, indicating a low DC-RF dispersion.**

***Index Terms*—InAs, MOSFETs, MOSHEMTs, RF, ft, fmax**

I. Introduction

Transistors using narrow band-gap III-V semiconductors are promising candidates for future high-speed electronics, particularly in mm-wave applications [1] [2]. Although III-V MOSFETs have been investigated primarily for VLSI applications [3]-[6], they are also of potential interest in mm-wave applications [6]-[9], because at a given gate leakage current density, the high-k ZrO_2 or HfO_2 gate dielectric can be made with a smaller equivalent oxide thickness [6] than that of the InAlAs gate barrier in a HEMT [10], thereby increasing the intrinsic transconductance $g_{m,i}$ and reducing the output conductance. Further, in HEMTs, source and drain access resistances are increased by the InAlAs barrier layer lying between the channel and the N+ source and drain regions; this barrier need not be present in III-V MOSFETs [3] [4] [7].

Despite this, reported InAs-based MOSFETs show far lower f_t and f_{max} than InAs HEMTs [1]. Degraded channel mobility from the semiconductor-dielectric interface [11] may be one cause. Further, in many reported III-V MOSFETs [3] [4] [7] [8], close proximity to the gate of the source and drain N+ regions increases the gate-source and gate-drain capacitances. In contrast, in HEMTs, modulation-doped access regions increase the separations between the gate and the N+ source and drain. Doping of the access regions is selected to balance between low access resistance (hence high extrinsic transconductance $g_{m,ex}$) and low capacitive parasitics [12].

Here we report InAs-channel MOSFETs exhibiting 420 GHz f_{max}, record for a III-V MOSFET, and 357 GHz f_t. In these, regrown modulation-doped access regions increase the separations between the gate and the N+ source and drain. The N+ source and drain are formed by a second regrowth [3] [4]. The regrowth technique involves no dry-etching steps that can potentially damage the channel or its interface to the high-k dielectric. At L_g = 30 nm, the minimum subthreshold swing is 90 mV/dec. and the measured peak $g_{m,ex}$ shows only a small difference between DC (1.5 mS/μm) and 10 MHz (1.65 mS/μm), both factors indicating a good quality of the high-k/InAs gate stack.

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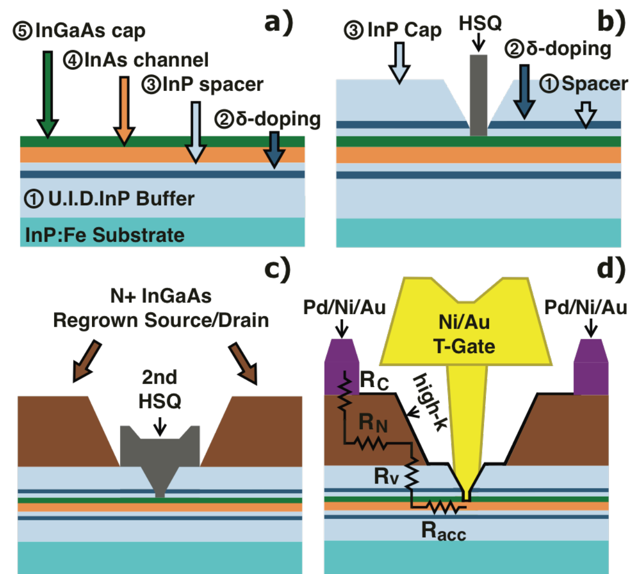

Fig. 1. Schematic of the MOSFET processing. R_C, R_N, R_v, and R_{acc} in (d) denote contact resistance, regrown N+ contact film resistance, vertical resistance through the InP layer, and access resistance, respectively.

II. Device Fabrication

Devices were fabricated on a semi-insulating InP (100) substrate, on which the following epitaxial structures, Fig. 1(a), were first grown using metalorganic vapor phase epitaxy (MOVPE): a 10 nm U.I.D. InP buffer, a 2 nm Si-doped modulation doping layer (target $5\times10^{12}\ cm^{-2}$), a 2 nm U.I.D. InP vertical spacer, a 5 nm strained InAs channel, and a 3 nm U.I.D. $In_{0.53}Ga_{0.47}As$ cap. The growth of strained InAs on InP was managed by using a low growth temperature of 500 ^oC, and a low V/III ratio of 7.8 [13]. After the channel growth, the first dummy gate was defined by hydrogen silesequioxane (HSQ) and electron beam lithography (EBL). After one cycle

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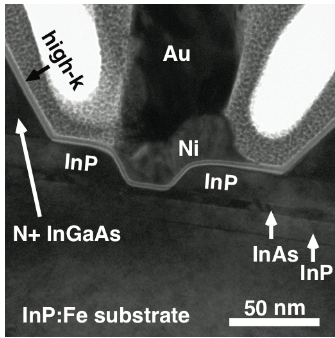

Fig. 2. TEM cross-section of a L_g= 30 nm device

of digital-etch cleaning in dilute HCL [3], samples were re-loaded into the MOVPE chamber. An InP HEMT structure was grown at 550 ^oC, Fig.1 (b), which consisted of a 2 nm U.I.D. InP vertical spacer, a 2 nm Si-doped modulation doping layer (target $5\times10^{12}\ cm^{-2}$), and a 10 nm U.I.D. InP cap. Hall measurement was performed on a sample with the same epitaxial structure grown by MOVPE but without the dummy gate processing interruption. The measured electron mobility and carrier density are 6000 $cm^2/V\cdot s$ and $5.6\times10^{12}cm^{-2}$, respectively, verifying the quality of the strained InAs channel but indicating a doping level somewhat below the target value. The dummy gate was then removed in HF, followed by the second dummy gate definition, which was made wider than the first dummy gate to provide 50 nm access regions from gate to source and drain, Fig. 1(c). 80-nm highly doped N+ InGaAs ($4\times10^{19}\ cm^{-2}$) was then regrown for source and drain contacts.

Post-growth processing, Fig. 1(d), consisted of mesa isolation, removal of the second dummy gate, 2-cycle digital etching of the InGaAs cap on channel by HF, follow immediately by atomic layer deposition (ALD). In the ALD chamber, the sample was first passivated by 9 cycles of exposure to a N_2-plasma and tri-methyl-aluminum, and subsequently, 3-nm ZrO_2 was deposited at 300 ^oC [4]. After ALD, the sample was annealed for 15 min in forming gas at 400 ^oC. Vias were opened in source and drain contact regions, and after removing the high-k inside these vias, 5/30/100 nm Pd/Ni/Au source and drain contacts, together with the RF probing pads, were deposited by thermal evaporation, followed by lift-off. Processing was finalized by T-gate formation. A two-step EBL was used to realize sub-100 nm gate foot. CSAR 62:anisole 1:1 was first spun-on, exposed at high dose and developed in amyl acetate to define the T-gate foot. Then samples were coated with UV-6, exposed at low dose, and developed in MIF for the T-gate head. A small T-gate foot without overlapping the regrown source and drain contacts is of crucial importance in reducing the parasitic capacitances. Finally, 30/300 nm Ni/Au gate metal was deposited by thermal evaporation, followed by lift-off. Fig. 2 shows the TEM cross-section of a L_g = 30 nm device. It can be clearly seen that the gate metal is well aligned with the channel, without overlapping the N+ InGaAs regrown contacts. The aggregation of metal towards the source side resulted from the photoresist shadowing during the gate metal evaporation. This will be removed if the sample holder can rotate during the step.

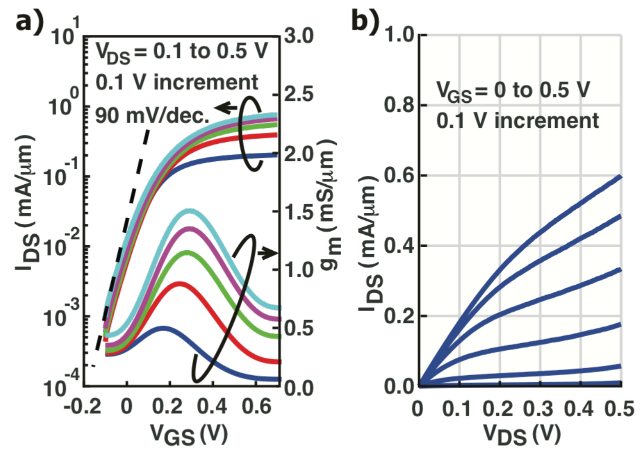

Fig. 3. Transfer (a) and output (b) characteristics of the device with gate length L_g= 30 nm

III. DC Performance

Fig. 3(a) shows the measured transfer characteristics of the device of L_g = 30 nm, which exhibits a DC peak extrinsic transconductance, $g_{m,ex}$, of 1.5 mS/μm at V_{DS} = 0.5 V and V_{GS} = 0.3 V, and a minimum subthreshold slope, SS_{min}, of 90 mV/decade under the same V_{DS} bias. $g_{m,ex}$ evaluated from the measured y_{21} parameter at 10 MHz is 1.65 mS/μm. Such a

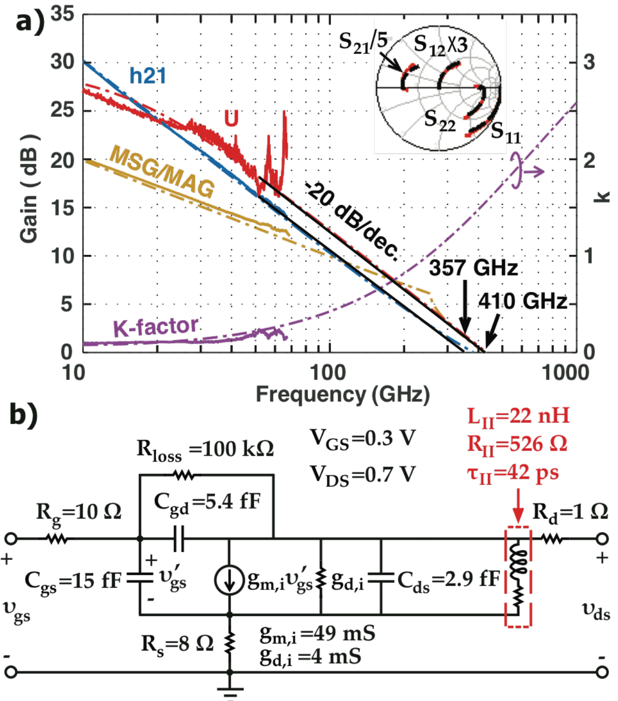

Fig. 4. (a) Measured (solid curves) and modeled (dashed curves) current gain, unilateral power gain, maximum stable/available gain and stability factor of the same device in Fig. 3 at V_{GS} = 0.3 V and V_{DS} = 0.7 V. The device has 2 gate fingers, each of 10 µm length, i.e. total gate width W_g = 2×10 µm. The solid black lines indicate the -20 dB/decade extrapolations from the 30-50 GHz regions that are used to determine f_t and f_{max}. The inset shows the measured (red) and modeled (black) S-parameters. (b) Small signal equivalent circuit model to fit the measured data in (a).

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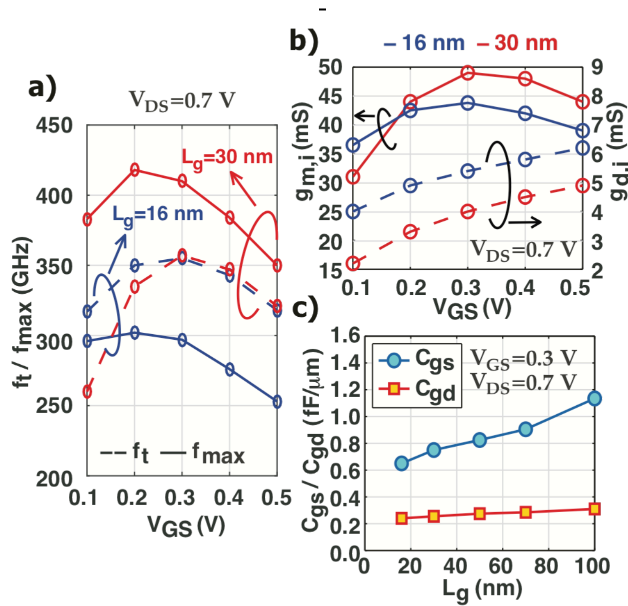

Fig. 5. (a) Comparison of the extracted f_t and f_{max} between the L_g = 30 and = 16 nm devices. (b) The fitted intrinsic transconductance $g_{m,i}$ and intrinsic output conductance $g_{d,i}$ at various gate biases for the two devices. (c) Extracted gate-source C_{gs} and gate-drain C_{gd} capacitances as a function of the gate length L_g at V_{GS} = 0.3 V and V_{DS} = 0.7 V.

small deviation of $g_{m,ex}$ at DC and 10 MHz confirms that a good quality of high-k dielectric and high-k/semiconductor interface is maintained even after the complex processing flow. Further, the measured SS_{min} here is also consistent with the result reported in Ref [3] (86 mV/decade) with the same channel material, high-k deposition scheme and similar device dimensions, but fabricated with a far simpler process. The off-state current of the device is high, 0.9 μA/μm at V_{DS} = 0.5 V and V_{GS} = -0.1 V, and is independent of V_{DS} at negative biases. We believe that the off-state current is dominated by drain-to-source parallel conduction in the InP buffer. The off-state leakage could be reduced by using an InAlAs bottom barrier, as this has a greater conduction band offset to the channel.

Fig. 3(b) shows the output characteristics of the same device. The measured R_{on} at V_{GS}= 0.8 V is 495 $\Omega \cdot \mu m$. Two sets of TLM were fabricated: one measures the regrown contact film; the other measures the modulation-doped access regions. The computed contribution to R_S, Fig 1(d), consists of 14 $\Omega \cdot \mu m$ contact resistance (R_C), 86 $\Omega \cdot \mu m$ regrown N+ contact film resistance (R_N), 130 $\Omega \cdot \mu m$ vertical resistance (R_v) through the InP layer, and 14 $\Omega \cdot \mu m$ access resistance (R_{acc}). As compared with our previous work [3] [4], the 14 nm thick lightly-doped InP layer between the InAs channel and the N+ InGaAs source and drain, together with the conduction-band offsets at the heterointerfaces, adds a large vertical component to the parasitic source and drain resistances. The source and drain resistances are further increased by a large (5 μm) separation between the source/drain contact metals and the gate edges.

IV. RF Performance

S-parameters were measured from 10 MHz to 67 GHz using on-wafer probing and a port power of -27 dBm. An off-chip load-reflect-reflect-match calibration was performed before measurements, and the device under test was de-embedded using on-chip open and short pad structures. Fig. 4 (a) shows the measured current gain h_{21}, unilateral power gain U, maximum stable/available gain MSG/MAG and stability factor k of the L_g = 30 nm device at V_{DS} = 0.7 V and V_{GS} = 0.3 V. The device has 2 gate fingers, each of 10 μm length, i.e. total gate width W_g = 2×10 μm. A small signal equivalent circuit was fitted to the measured S-parameters, Fig. 4 (b). A series L-R network fits to y_{22} and models the frequency-dependent source-drain conductance arising from the parasitic bipolar current gain combined with either impact ionization or band-to-band tunneling at high V_{DS}. The fitted *L/R* time constant is 40 ps, similar to that reported in [7] [9]. Above 30 GHz, both h_{21} and U roll off at -20 dB/decade. The extracted f_t and f_{max} are 357 and 410 GHz. Note that all f_t and f_{max} values shown in this paper are extracted from the -20 dB/decade extrapolations from the 30-50 GHz regions of the measured h_{21} and U (the black solid lines in Fig. 4(a)). As compared with the asymmetric drain engineering approach reported in Ref [9], the fitted $g_{m,i}$ (49 mS) of this work is higher, but the capacitances and intrinsic output conductance $g_{d,i}$ are similar or smaller, which explains the improved f_t and f_{max}. The highest f_{max} (420 GHz) is measured at V_{DS}= 0.7 V and V_{GS}= 0.2 V and the best balance between f_t and f_{max} is at V_{GS}= 0.3 V, Fig. 5.

Fig. 5 (a) compares the performance of the L_g = 30 and 16 nm devices. As L_g decreases to 16 nm, f_{max} degrades, while f_t remains relatively unchanged. Figs. 5 (b) and (c) show key extracted device parameters. The simultaneous reduction of $g_{m,i}$ (b) and gate-source C_{gs} and gate-drain C_{gd} capacitances (c) explains the unchanged f_t for the 16 nm device. The increased $g_{d,i}$ due to the short-channel effect causes f_{max} to degrade.

V. Conclusion

In this work, we demonstrate an InAs MOSFET, targeted at high-speed applications, with regrown access regions and contacts. The results demonstrate improved f_t and f_{max} over previously reported III-V MOSFETs. The improvement is attributed to the reduced parasitic capacitances and the maintained high $g_{m,i}$, thanks to the use of the modulation doped access regions. The small dispersion of $g_{m,ex}$ measured at DC and 10 MHz highlights the preserved InAs/high-k quality even after the complex process. Transistor bandwidth can be improved by reducing the source resistance and by improving the alignment between the gate and the channel recess.

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