Transistors:
mm-Wave and Low-Power VLSI

Mark Rodwell, UCSB

Low-voltage devices
B. Markman, H.-Y. Tseng, S. Brunelli, S. Choi, A. Goswani, C. Palmstrøm, J. Klamkin: ***UCSB***
P. Long, J. Huang, E. Wilson, S. Mehrotra, C.Y.-Chen, M. Povolotskyi, G. Klimeck: ***Purdue***

InP HBT:
Y. Fang, J. Rode:* ***UCSB***

InP MOS-HEMT
J. Wu: ***UCSB***

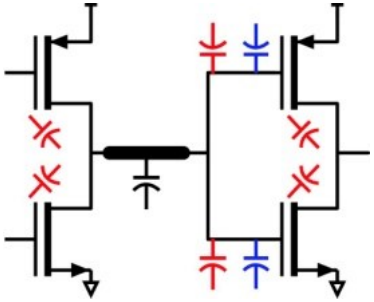
Millimeter-wave systems design, mm-wave ICs.
M. Abdelghany, A. Farid, A. Ahmed, U. Madhow : ***UCSB***
A. Niknejad: ***UC Berkeley***

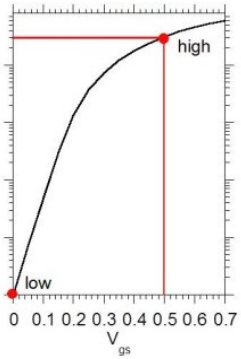
*Now with *Intel*

VLSI Transistors

Why is Moore's law scaling nearly over ?

Power density: becoming excessive

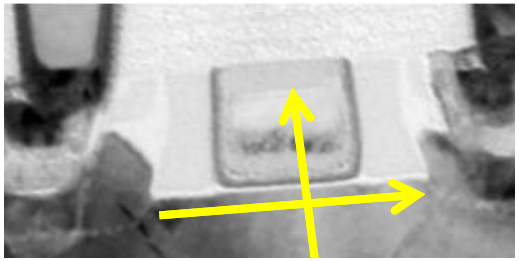




$C_{wire}V_{DD}^2$ switching energy:
→ want low V_{DD}

Static leakage $I_{off} > I_{on}exp(-qV_{DD}/kT)$
→ want high V_{DD}

Cannot make FET gates much shorter



Oxide tunneling: minimum oxide thickness
→ minimum gate length given electrostatics

Source-drain tunneling: minimum gate length

Reducing gate length reduces power:

integration density ↑, wiring capacitance ↓, switching energy ↓.

Reduce power by reducing voltage or increasing density

3D: increasing integration density

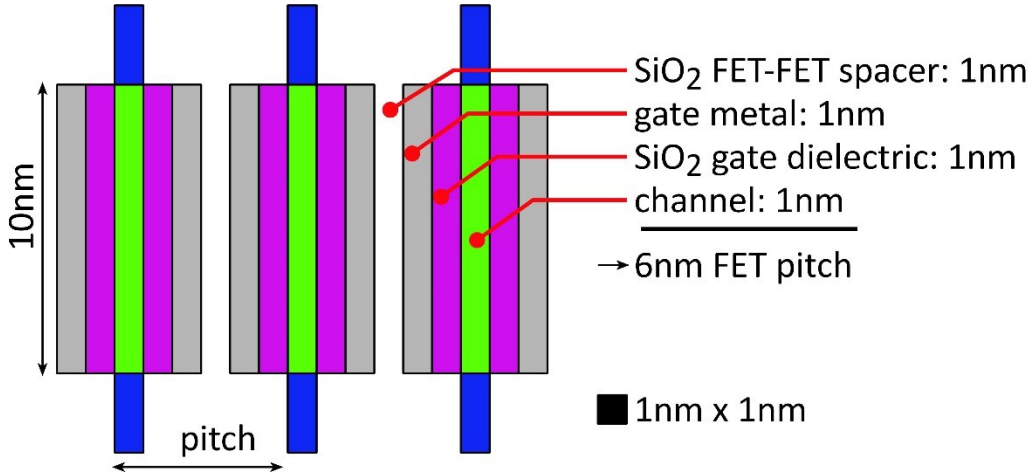
Planar FETs: 7nm node uses 15nm gate; can't get much shorter

> 15nm minimum transistor pitch.

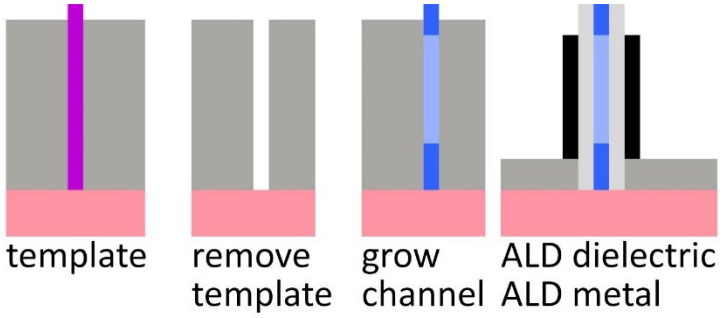
R. Xie *et al.*, 2016 IEDM

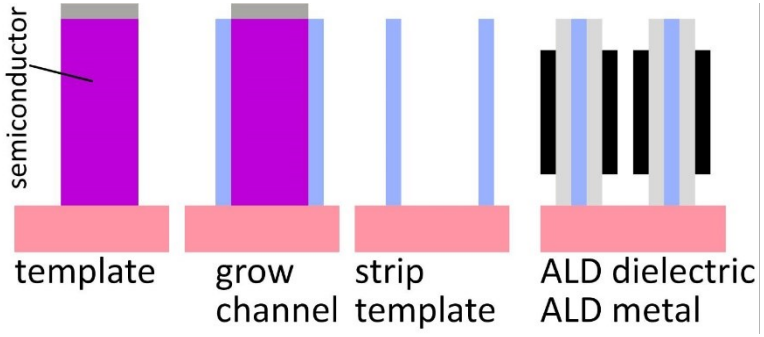
If oriented vertically, minimum transistor pitch is ~6nm

physical limit; fabrication might be difficult/impossible



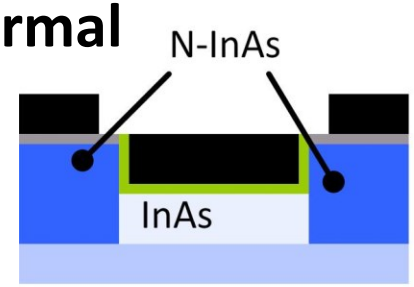
Perhaps it can be done ?

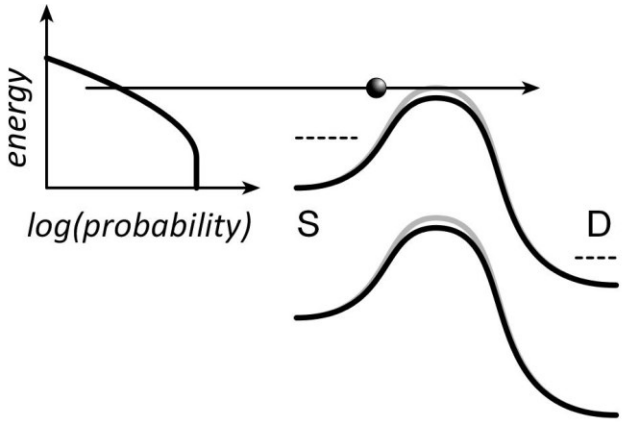


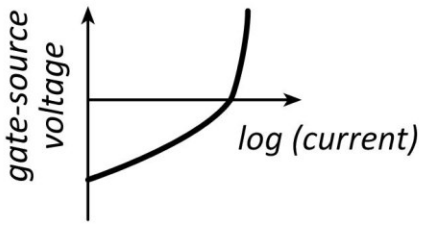


Tunnel FETs: truncating the thermal distribution

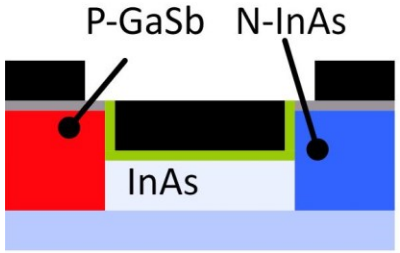
Normal

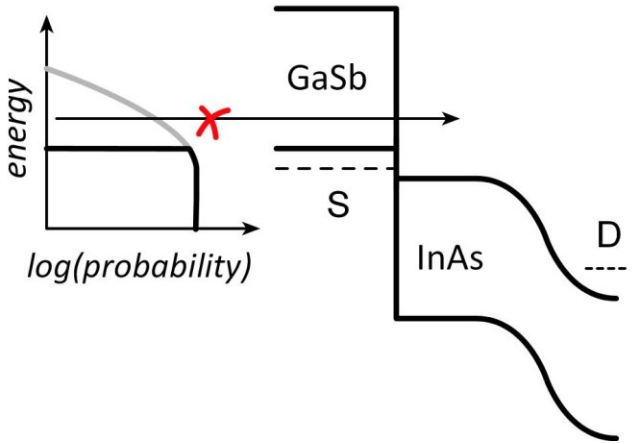


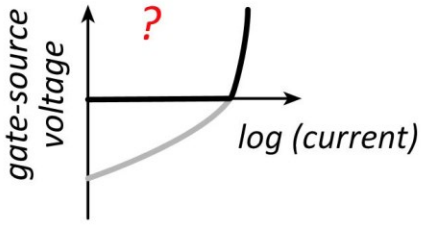




T-FET







J. Appenzeller *et al.*,
IEEE TED, Dec. 2005

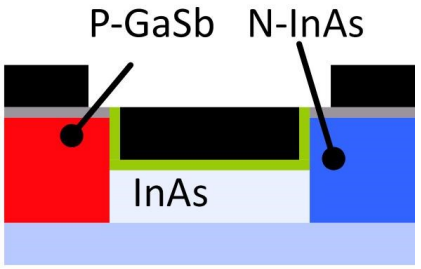
Source bandgap truncates thermal distribution ✓

Must cross bandgap: tunneling ✗

Fix (?): GaSb/InAs broken-gap heterojunction

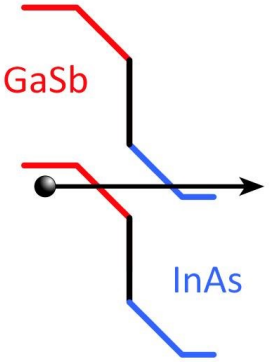
Tunnel FETs: are prospects good ?

Real TFET
nonzero barrier energy: quantization
nonzero barrier thickness: electrostatics



Transmission Probability (WKB, square barrier)

$$P \cong \exp(-2\alpha T_{\text{barrier}}), \text{ where } \alpha \cong \frac{\sqrt{2m^* E_{\text{barrier}}}}{\hbar}$$



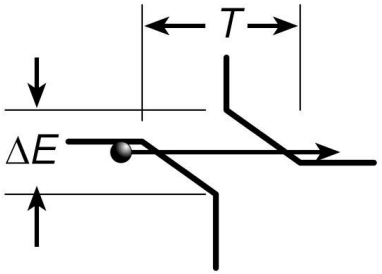
$$\text{Assume}: m^* = 0.06 \cdot m_0,\ E_b = 0.2\ \text{eV}$$

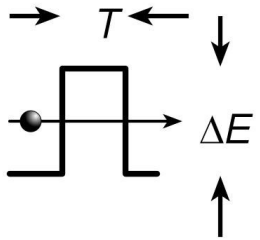
Then :

$P \cong 33\%$ for a 1nm thick barrier

$\cong 10\%$ for a 2nm thick barrier

$\cong 1\%$ for a 4nm thick barrier



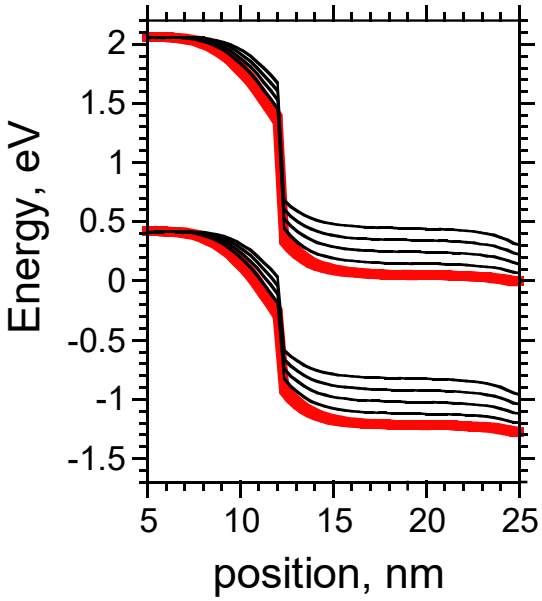


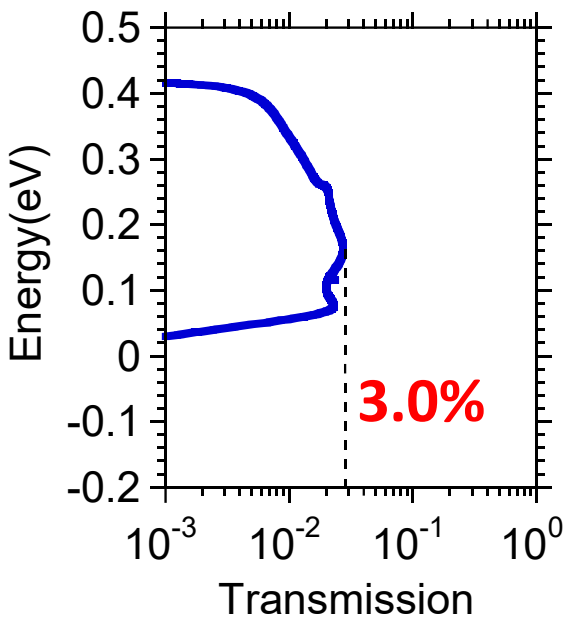
For high I_{on}, tunnel barrier must be *very* thin.

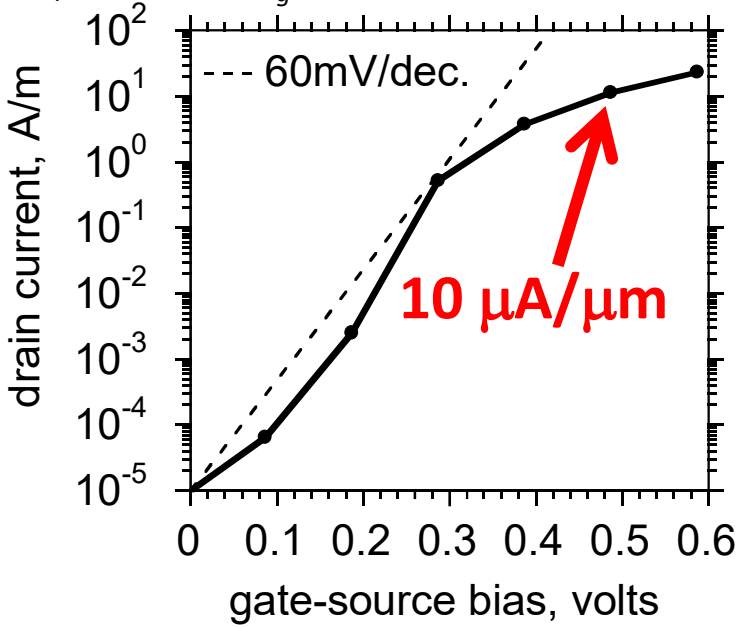
TFET on-currents are low, TFET logic is slow

NEMO simulation:

GaSb/InAs tunnel finFET: 2nm thick body, 1nm thick dielectric @ ε_r=12, 12nm L_g







Experimental:

Tabulation from Zhao et al., MIT, IEEE EDL, 7/2017

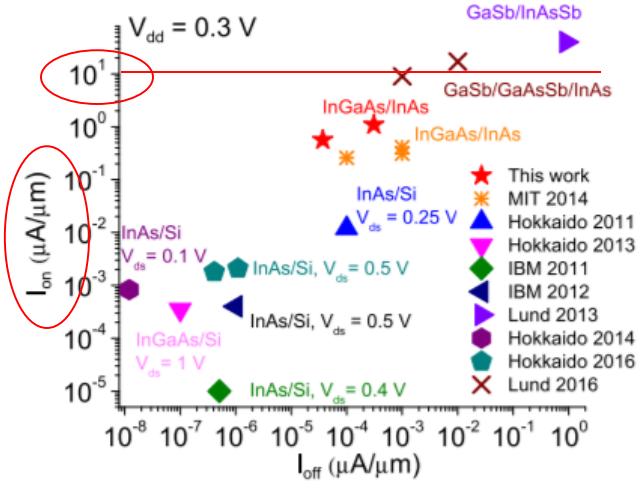
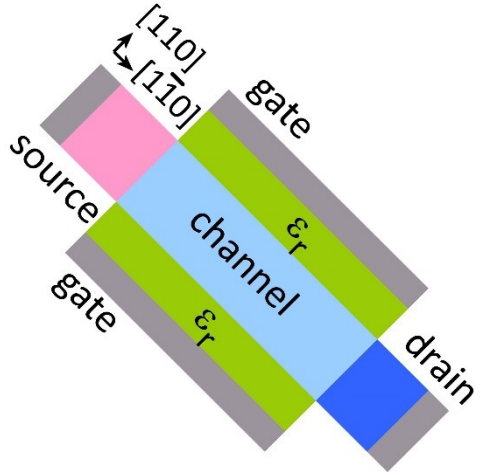


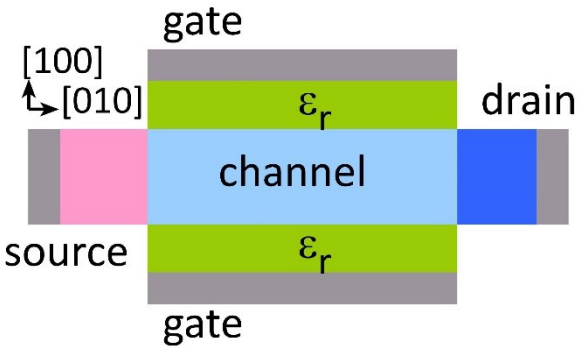
Fig. 5. I_{on} vs. I_{off} at V_{dd} = 0.3 V (V_{ds} = 0.3 V, ΔV_{gs} = 0.3 V with exceptions marked next to data points) for recently published vertical III-V NW TFETs. All devices but the present ones are fabricated through bottom-up techniques.

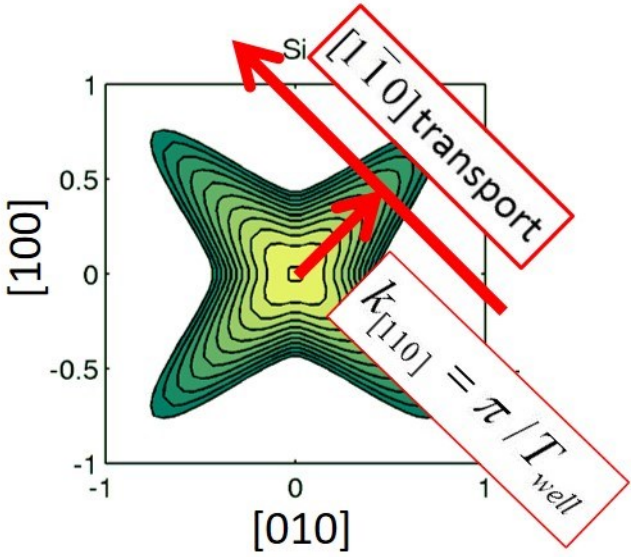
Low current → slow logic

[110] gives more on-current than [100]

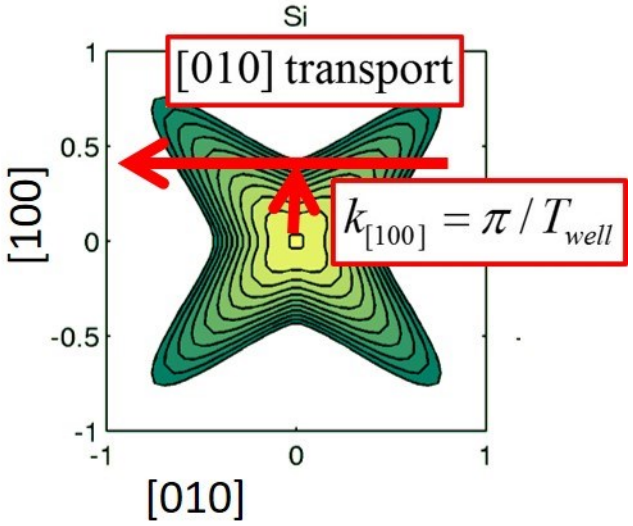
P. Long *et al.*, EDL 3/2016







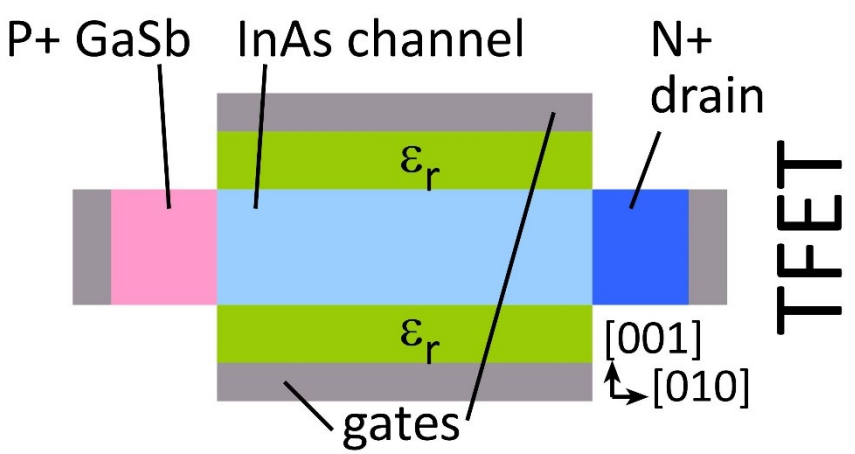
high confinement mass
low transport mass

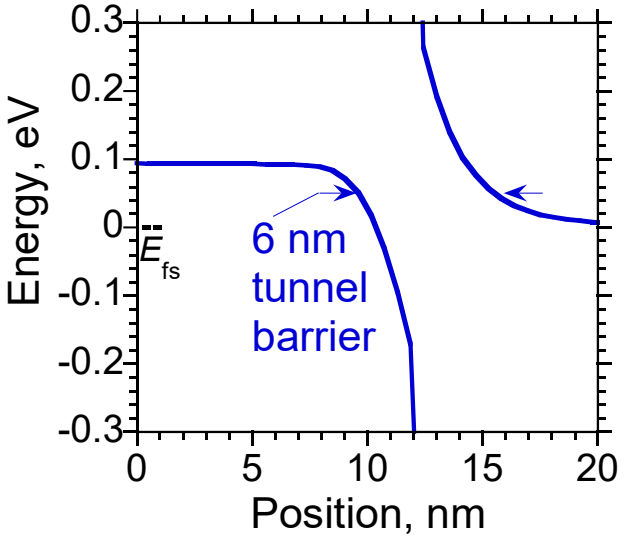


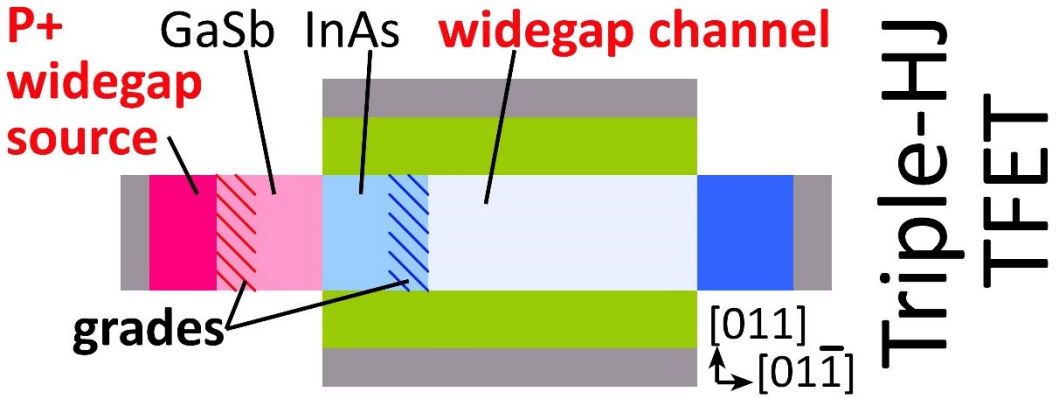
low confinement mass
high transport mass

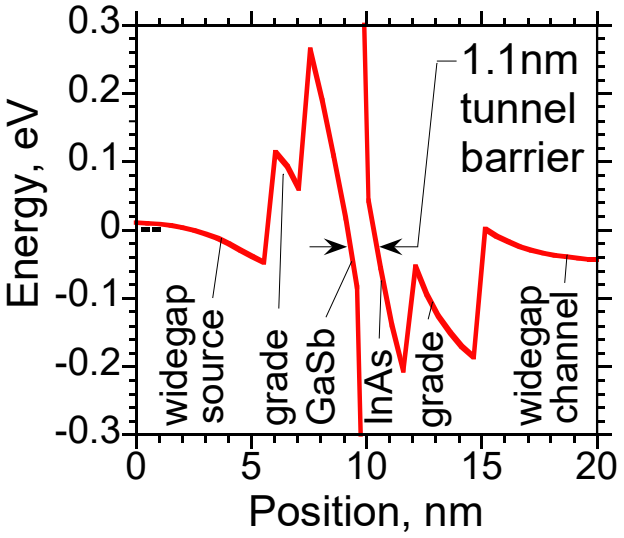
Heterojunctions increase the junction field.

Source HJ: S. Brocard, *et al*., EDL, 2/2014; Channel HJ: P. Long *et al*., EDL 3/2016







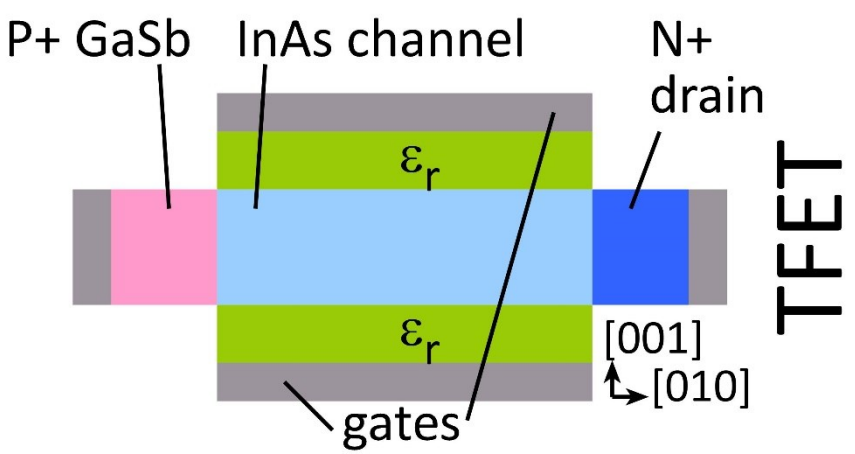


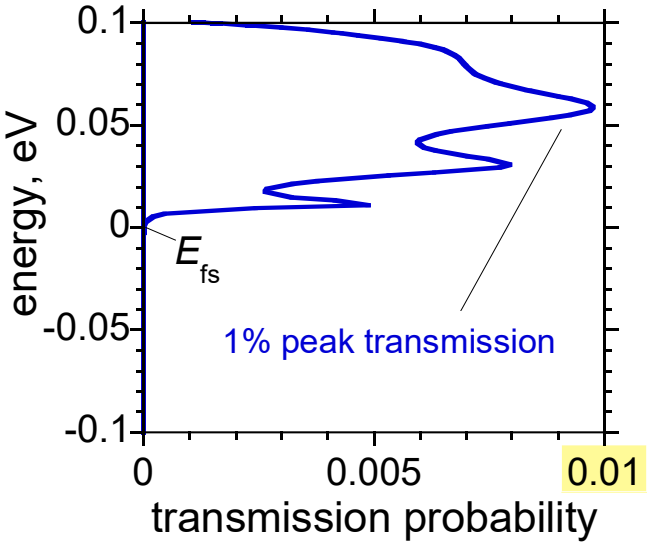
Added heterojunctions→ greater built-in potential→greater field→ thinner barrier

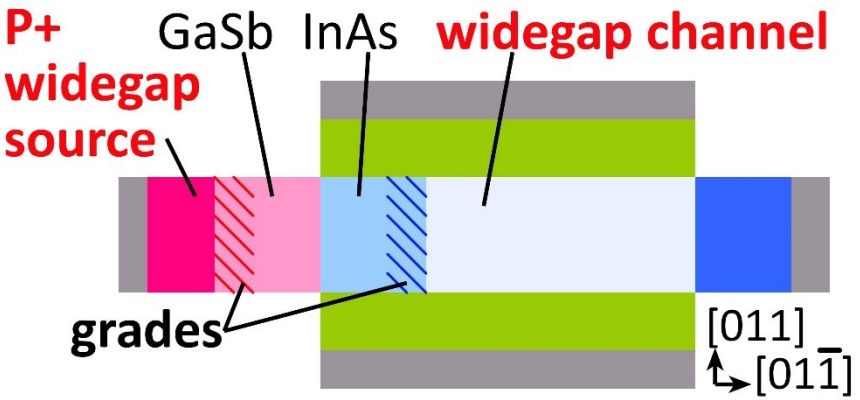
Key facts: 2nm thick channel, design for V_{DD}=70mV.

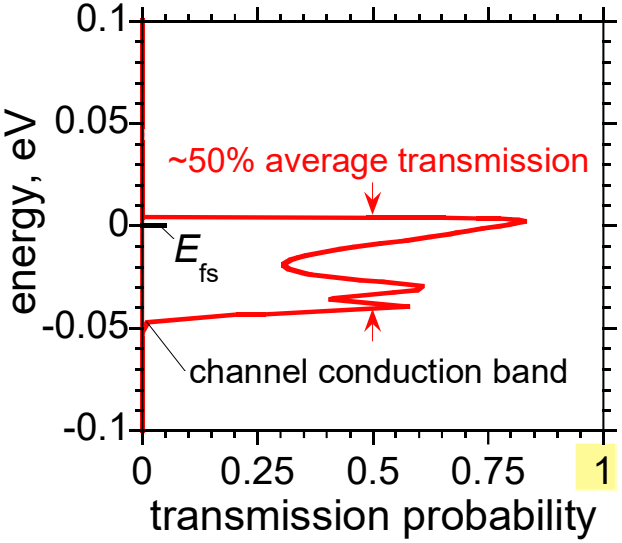
Heterojunctions increase the tunneling probability

Source HJ: S. Brocard, *et al*., EDL, 2/2014; Channel HJ: P. Long *et al*., EDL 3/2016







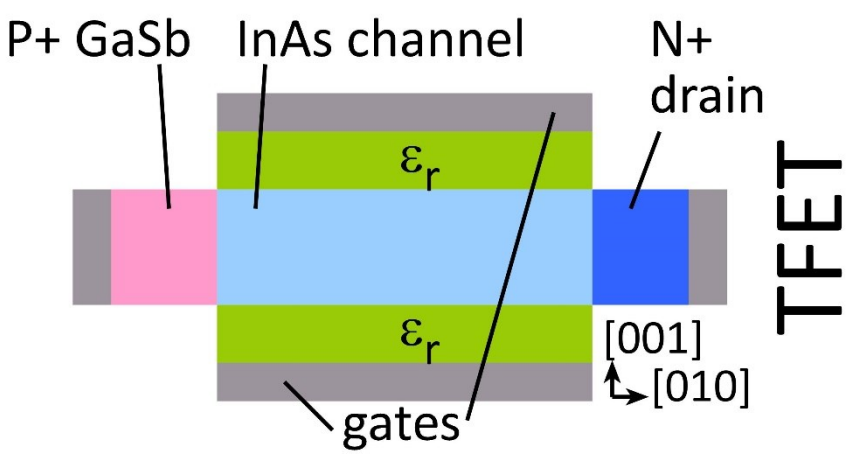


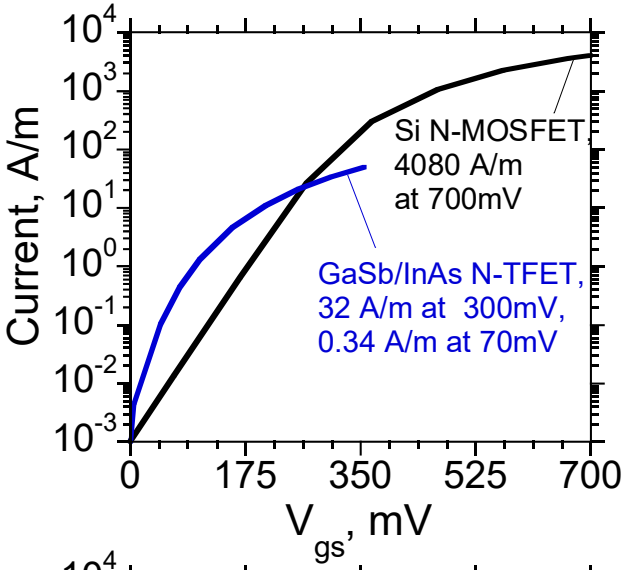
Added heterojunctions→ greater built-in potential→greater field→ thinner barrier

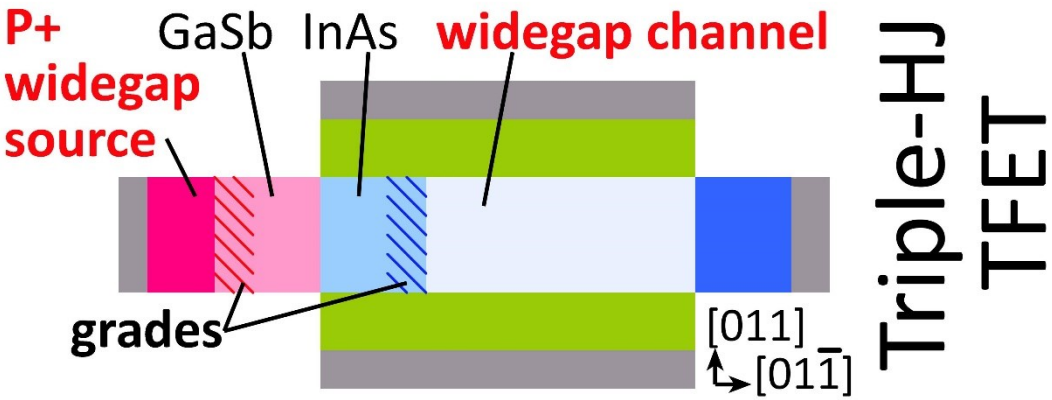
Key facts: 2nm thick channel, design for V_{DD}=70mV.

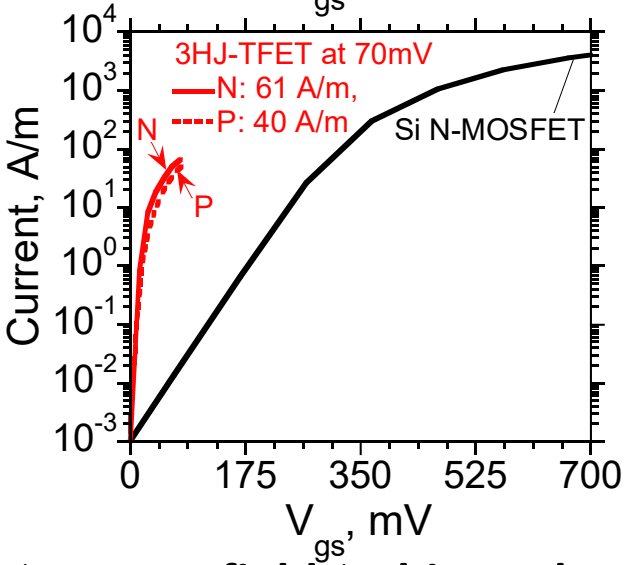
Heterojunctions increase the on-current

Source HJ: S. Brocard, *et al*., EDL, 2/2014; Channel HJ: P. Long *et al*., EDL 3/2016







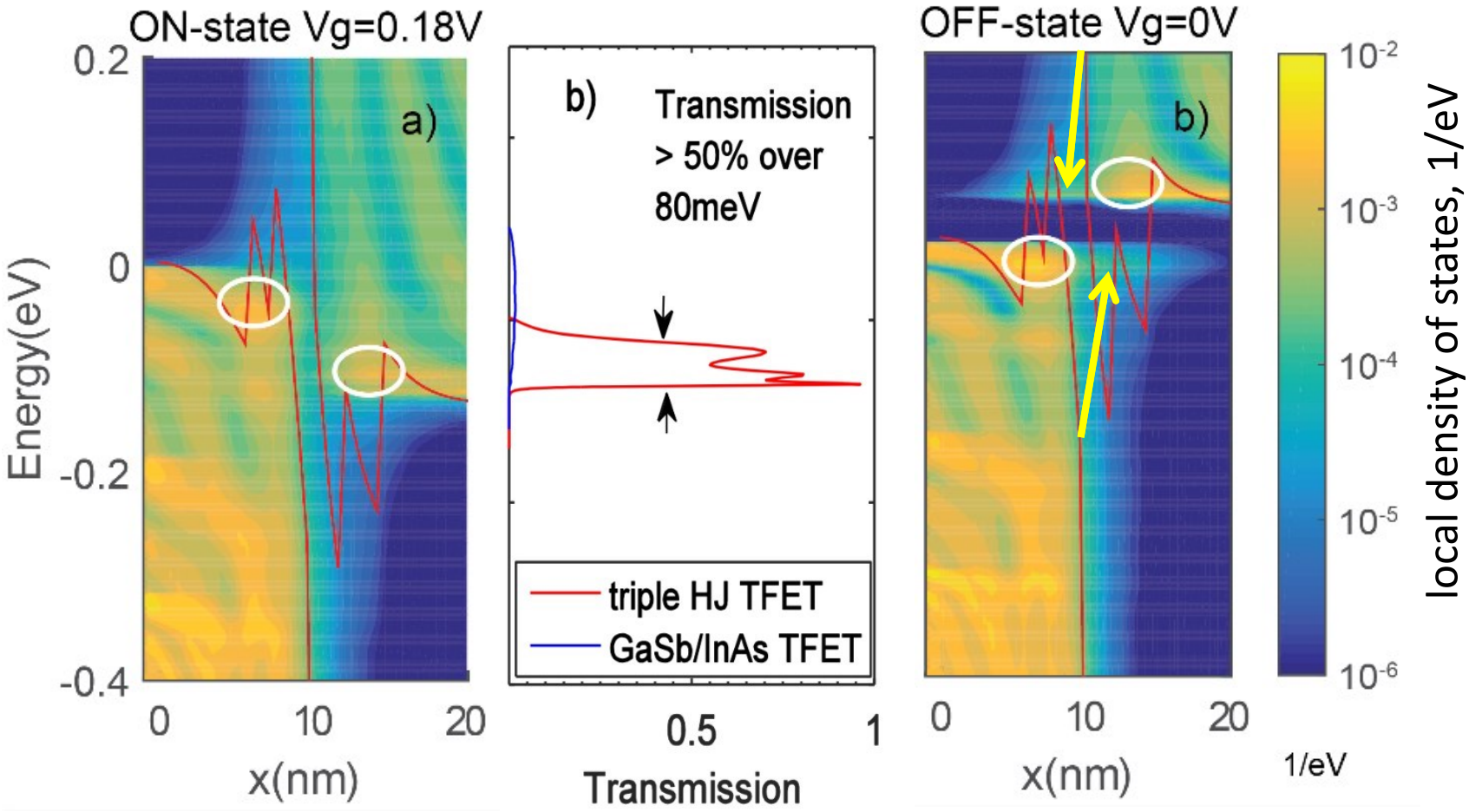


Added heterojunctions→ greater built-in potential→greater field→ thinner barrier

Key facts: 2nm thick channel, design for V_{DD}=70mV.

Role of the resonant bound states

P. Long *et al.*, 2016 IEDM: **Resonances in TFETs: Avci & Young (Intel) 2013 IEDM**



On-state: bound states increase transmission

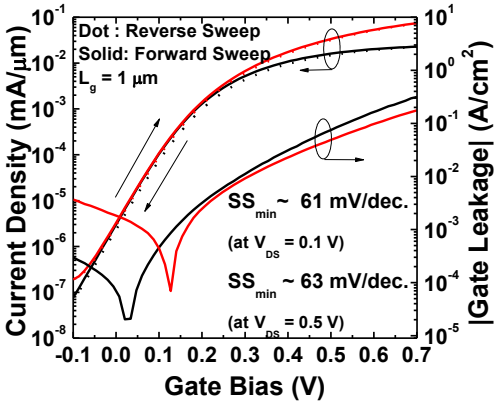
Off-sate: evanescent tails of bound states increases leakage

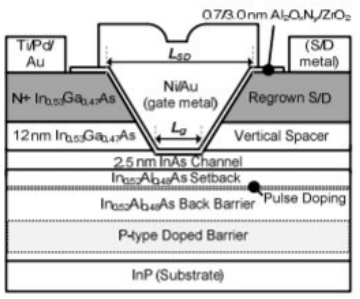
→ Keep the bound state energies near the well edge energies

Preferred semiconductors under gate dielectric

InAs: 61mV/dec.

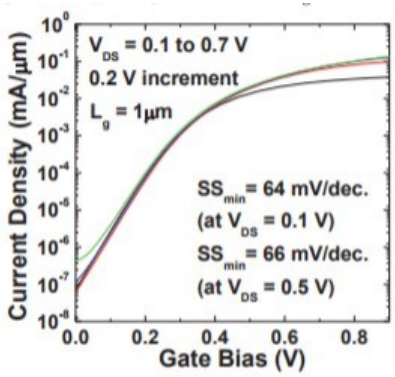
Lee *et al.*, 2014 VLSI Symposium

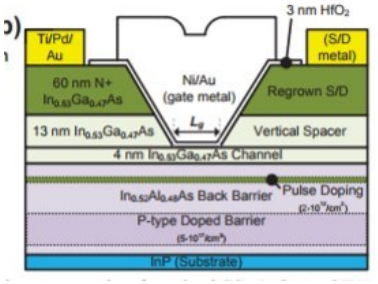




InGaAs: 64mV/dec.

Lee *et al.*, 2014 DRC

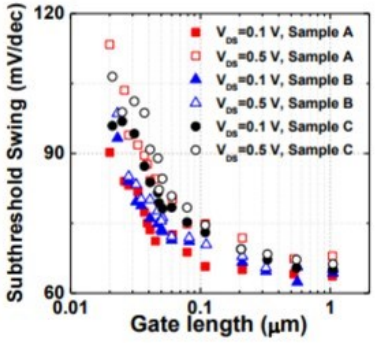


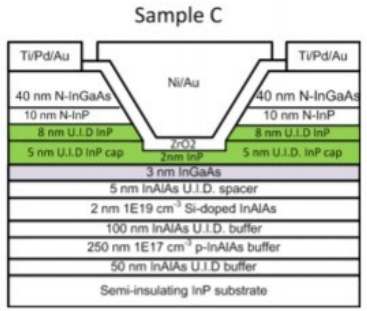


InP: 67*mV/dec.

*Note InP/InGaAs band offset

Huang *et al.*, 2014 Lester Eastman Conference

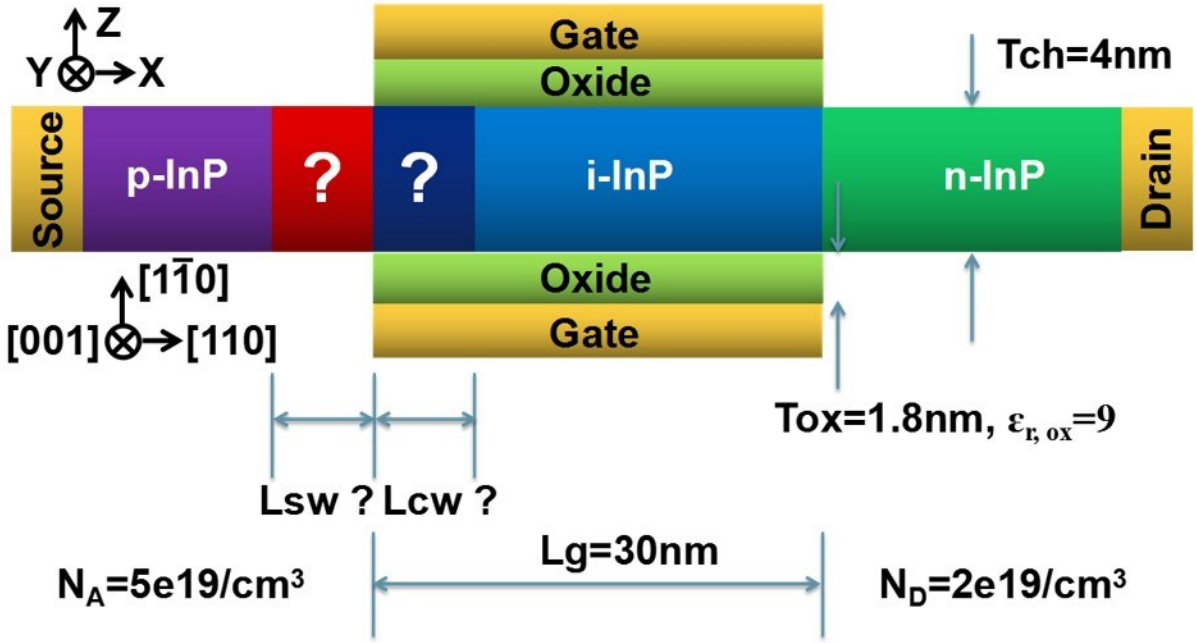




Gate dielectrics: Chobpattana *et al.* (Stemmer), APL 5/2014, APL 10/2014, Carter *et al.* (Rodwell) Applied Physics Express 8/2011

Target 3HJ tunnel transistor design

Long *et al.*, 2017 DRC



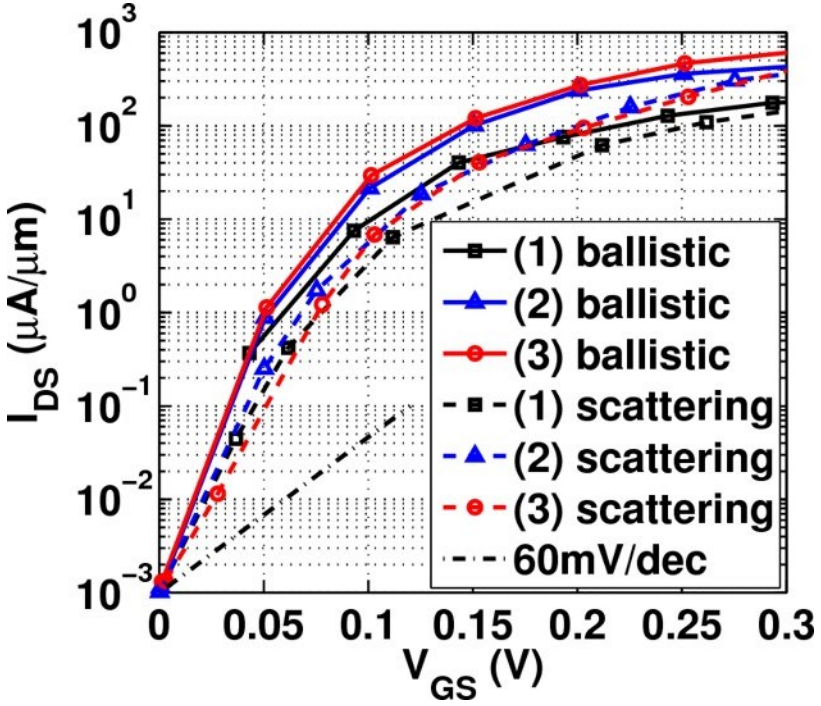
Design	Source well (N_A=5×10^{19}/cm^3)	Channel well
1)	4.0nm p-$Ga_{0.47}In_{0.53}As$	4.5nm i-$Ga_{0.47}In_{0.53}As$
2)	4.0nm p-$Ga_{0.74}In_{0.26}As$, 1.9% tensile strain	4.0nm i-$Ga_{0.23}In_{0.77}As$, 1.6% compressive strain
3)	**4.0nm p-GaAs,** 3.8% tensile strain	**3.5nm i-InAs**, 3.1% compressive strain

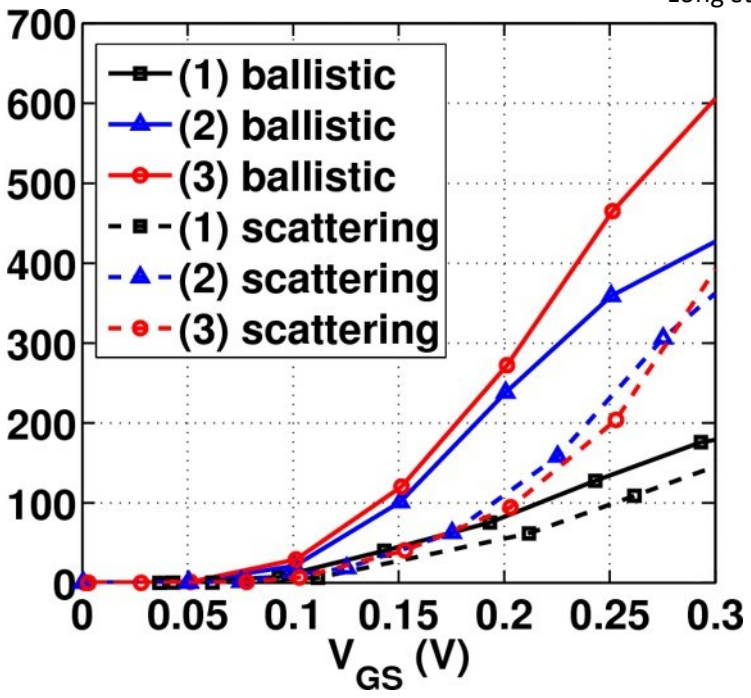
Design 3: highest current, no semiconductor alloys.

Need design revision: P-InP → P-InAlAs in source

Target 3HJ tunnel transistor design: simulations

Long *et al.*, 2017 DRC





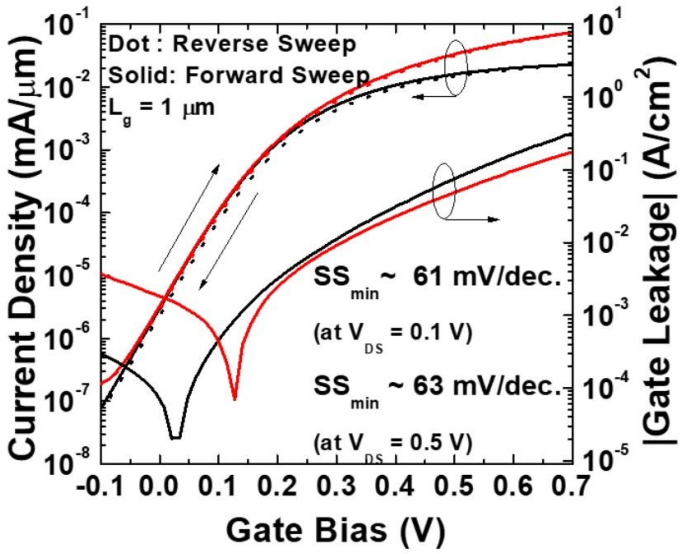
Design	Ballistic (SS, I_{on} @ I_{off}=1nA/μm, V_{DD}=0.3V)	**With phonon-assisted tunneling**
1)	15mV/dec., 0.18mA/μm	20mV/dec., 0.14mA/μm
2)	14mV/dec., 0.43mA/μm	26mV/dec., 0.36mA/μm
3)	14mV/dec., 0.61mA/μm	**34mV/dec., 0.39mA/μm**

Design 3: highest current, no semiconductor alloys.

Base III-V MOS Technology at UCSB

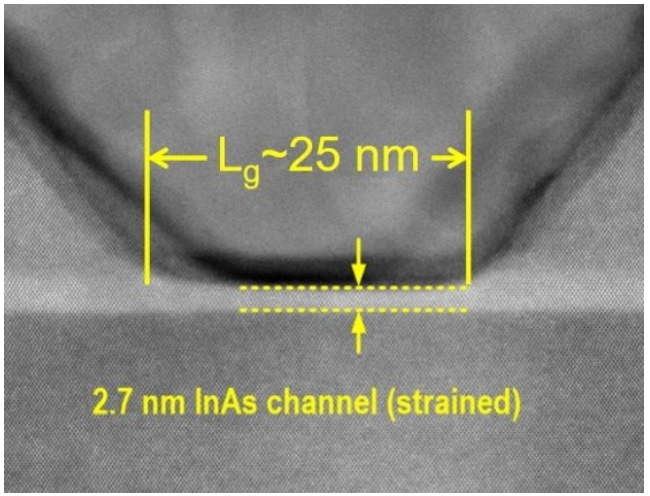
Gate dielectrics with very low trap density

V. Chobpattanna, S. Stemmer
FET data: S Lee, 2014 VLSI Symp.



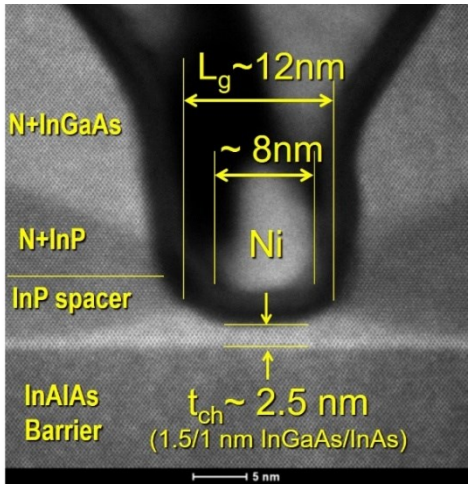
22nm L_g: 0.5 mA/μm I_{ON} @ 100nA/μm I_{OFF} & 0.5V V_{DD}

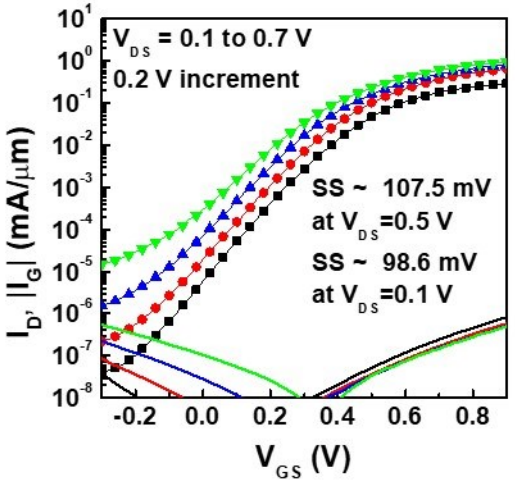
S. Lee et al., VLSI 2014

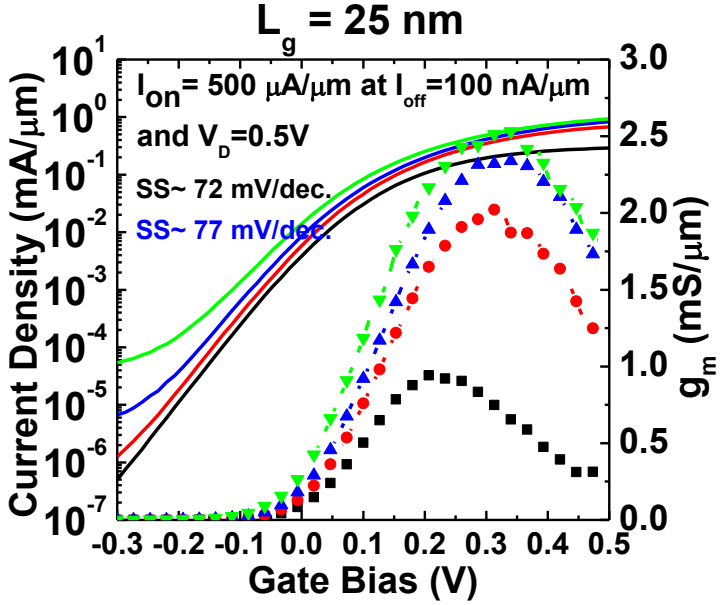


Good DC MOSFET with 12nm L_g, 2.5 nm thick channel

C. Y. Huang et al., DRC 2015





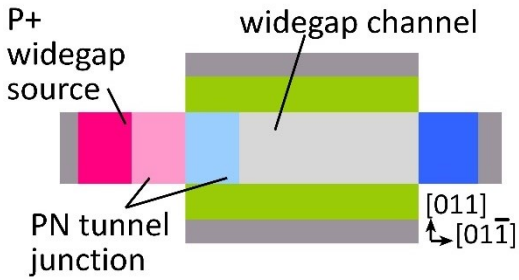


How to build the device? No easy approach.

All TFETs:

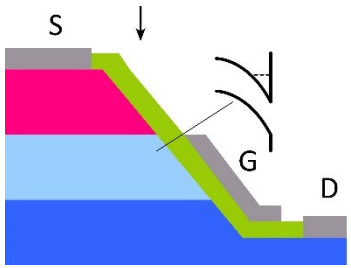
need junction perpendicular to gate dielectric.

how ?

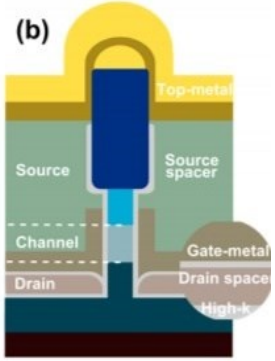


Example processes:

gated mesa edge



nanowire



Memišević, et al
2016 IEEE Silicon Nanoelectronics Workshop

vertical etched ridge

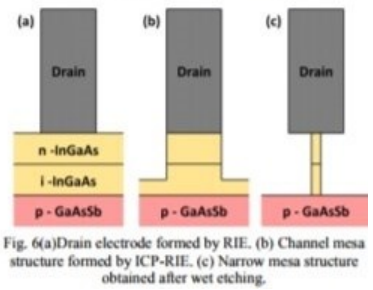


Fig. 6(a)Drain electrode formed by RIE. (b) Channel mesa structure formed by ICP-RIE. (c) Narrow mesa structure obtained after wet etching.

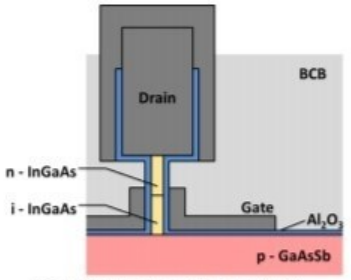
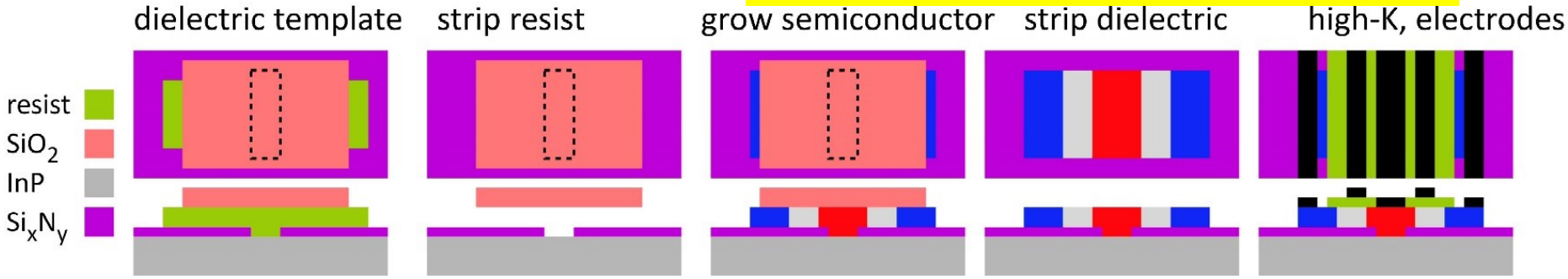


Fig. 5 Schematic image of fabricated TFET.

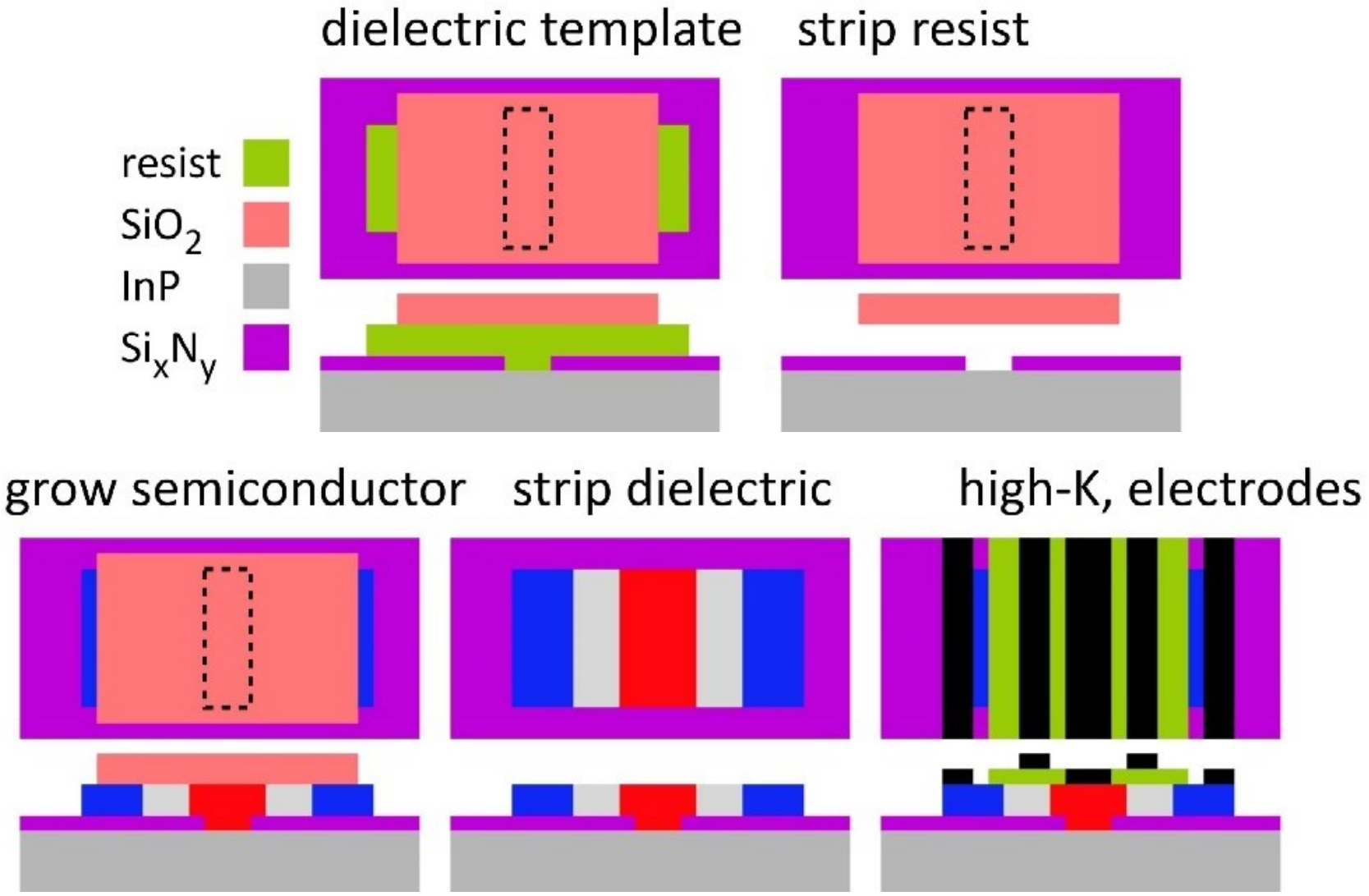
Fujimatsu, Saito, Miyamoto, 2012 IEEE IPRM

Target growth & process flow: Template Assisted Selective Epitaxy (TASE)

L. Czornomaz et al. (IBM Zurich), 2015 & 2016 VLSI Symposia



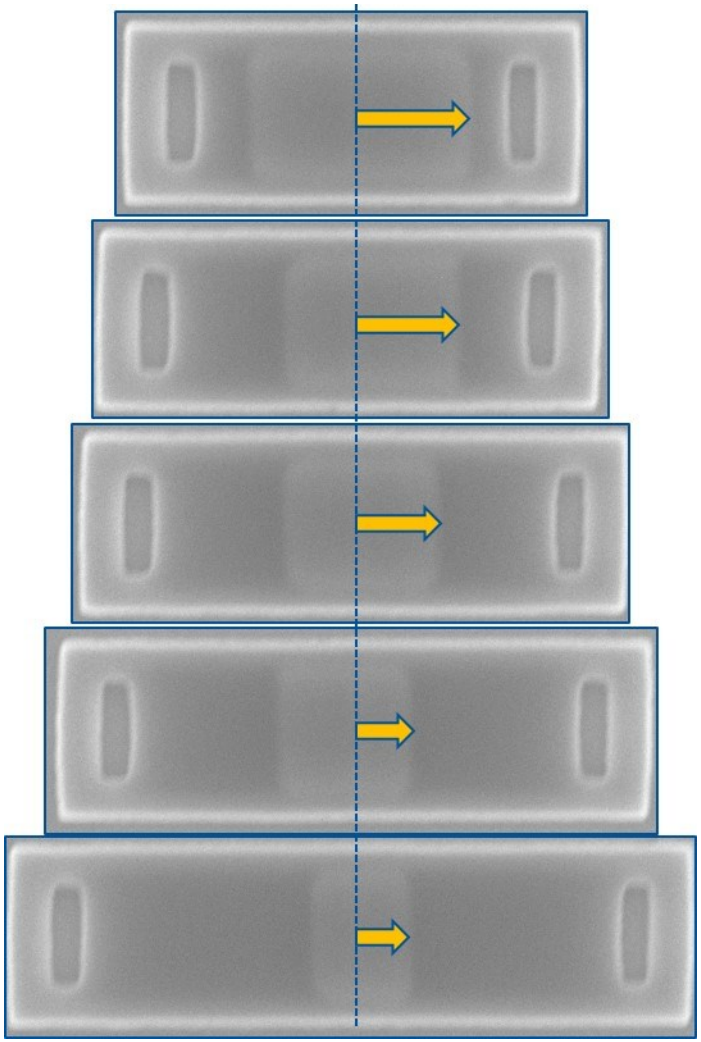
TFETs by template-assisted epitaxy



TASE: L. Czornomaz et al. (IBM Zurich), 2015 & 2016 VLSI Symposia

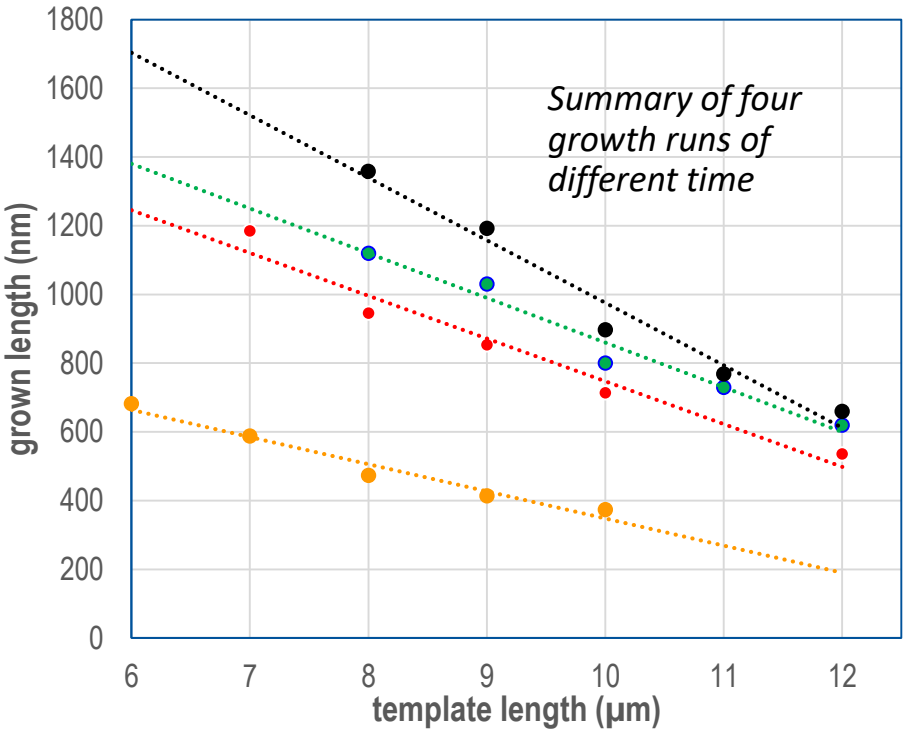
This conference: see paper Fr2B7, Nanostructures session, S. Brunelli *et al.*, Towards Horizontal Heterojunctions ...

MOCVD TASE



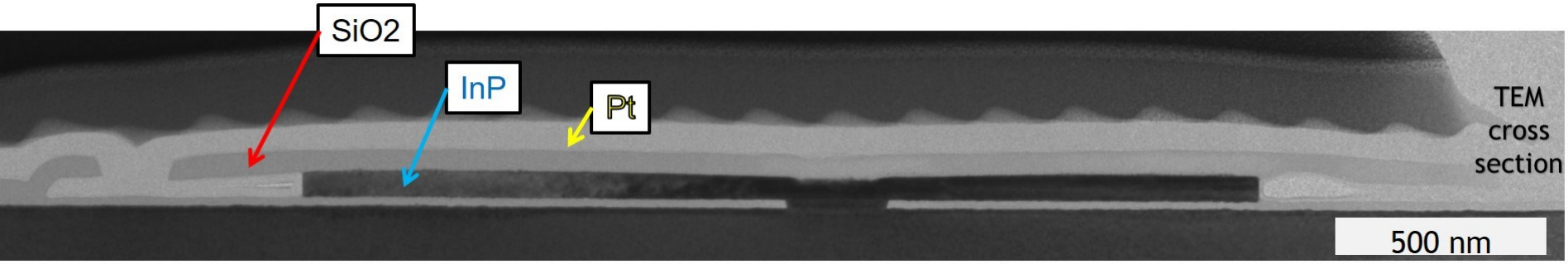
Growth in the template cavity appears to be limited by diffusion mechanisms

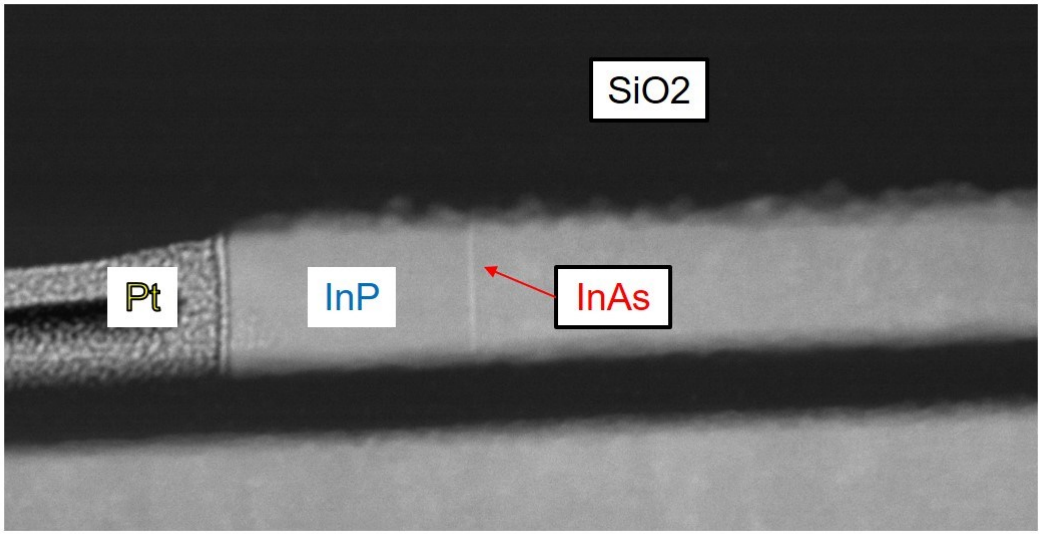
Template length influences growth rate with inverse proportionality

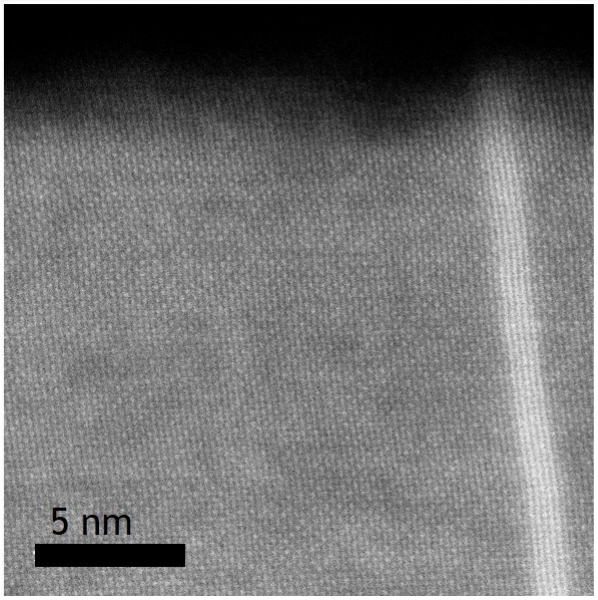


This conference: see paper Fr2B7, Nanostructures session, S. Brunelli *et al.*, Towards Horizontal Heterojunctions ...

TFETs: horizontal heterojunctions by TASE







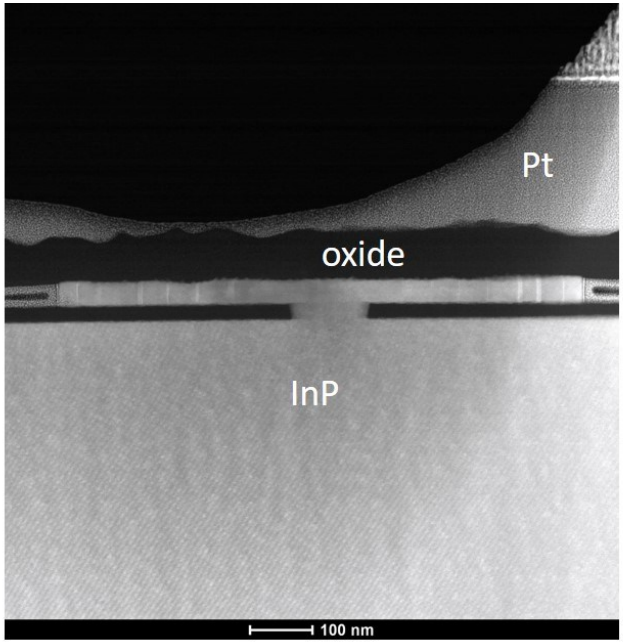
Heterojunctions by pseudo-ALE

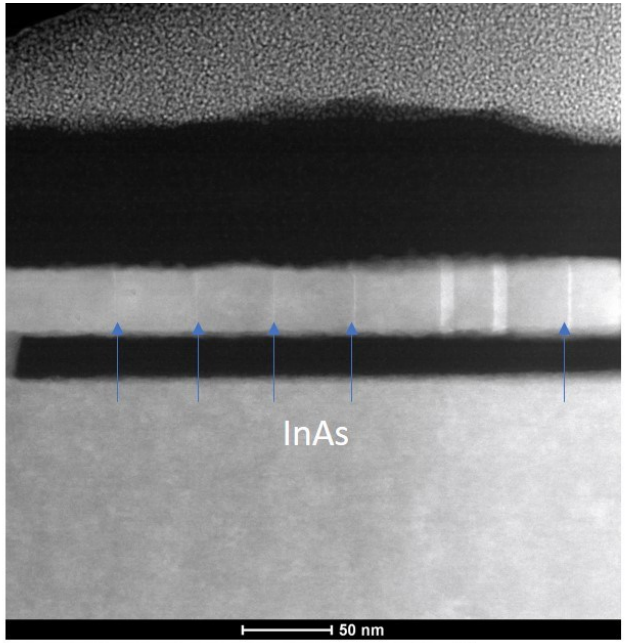
InP with ~1.25nm strained InAs layers

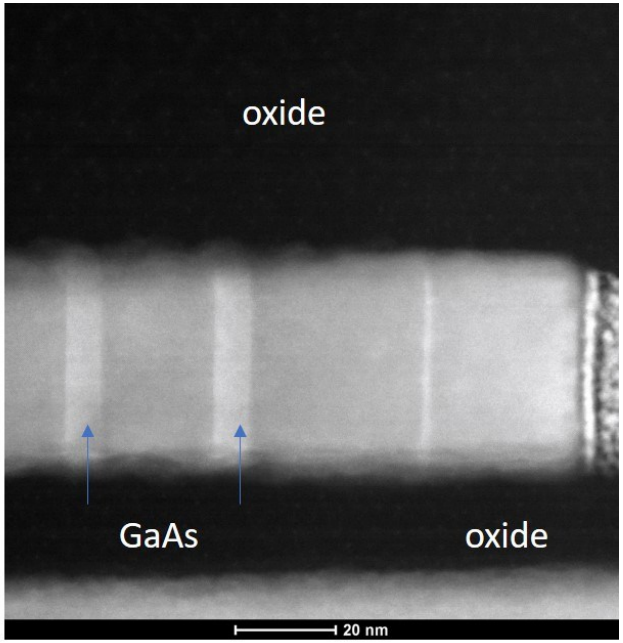
110 wafer, clean $1\bar{1}0$ growth facets

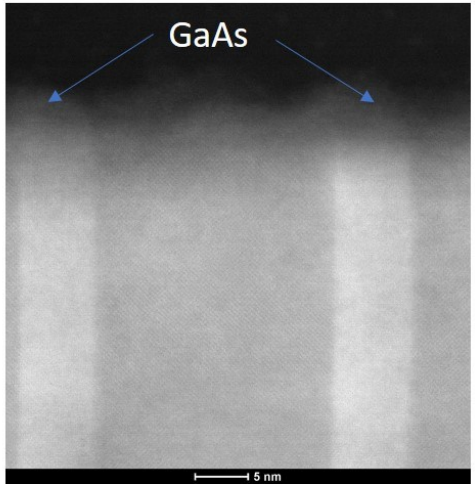
This conference: see paper Fr2B7, Nanostructures session, S. Brunelli *et al.*, Towards Horizontal Heterojunctions ...

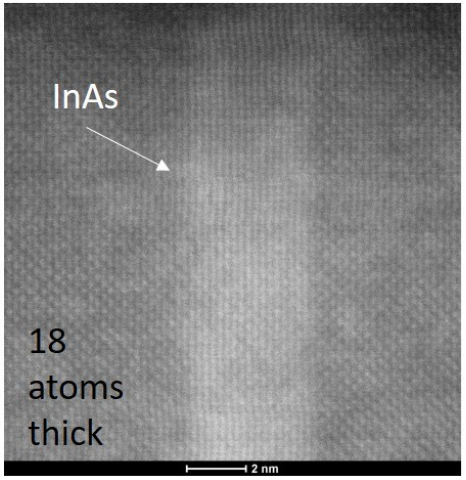
Horizontal InAs & GaAs heterojunctions in InP

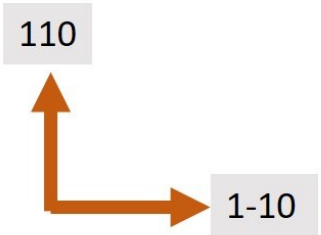










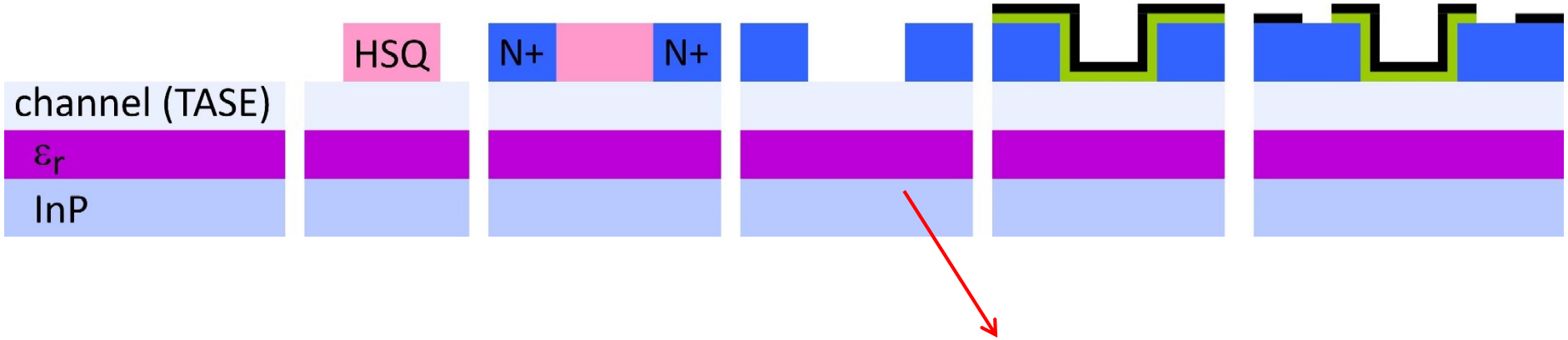


Working now on better control of the layer thicknesses...

Towards a TASE-fabricated TFET

First step: simple MOSFET with regrowth S/D contacts

ALE-deposited gate dielectric and metals

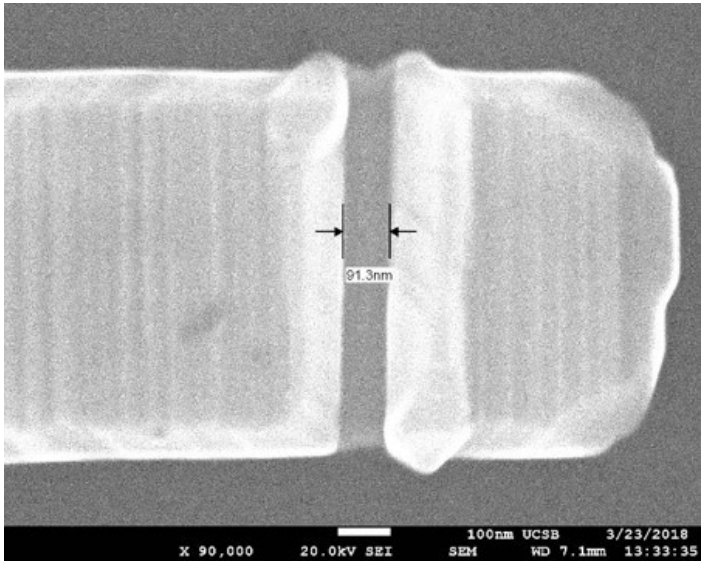


Remaining steps for 3HJ-TFET

horizontal GaAs/InAs/InP HJ

P+ InGaAs doping

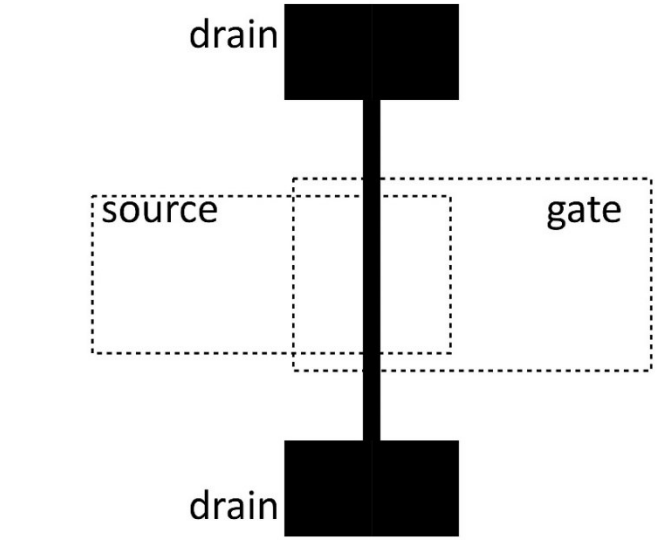
...growth & fabrication

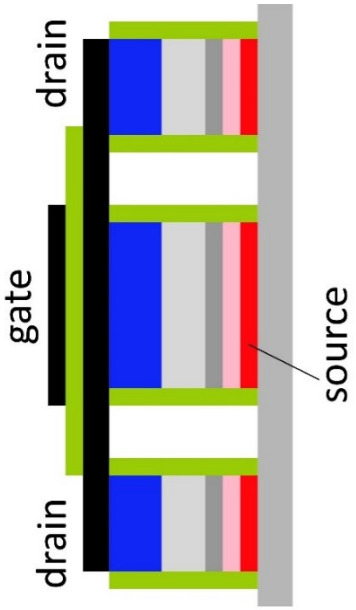


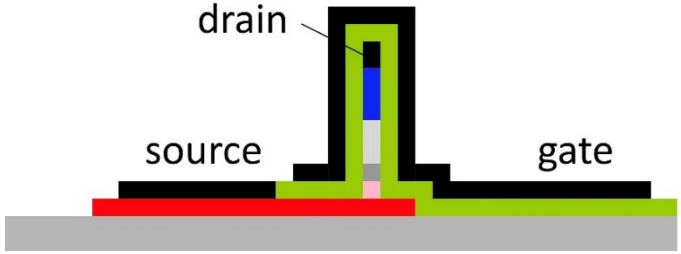
Alterative process: vertical ridge

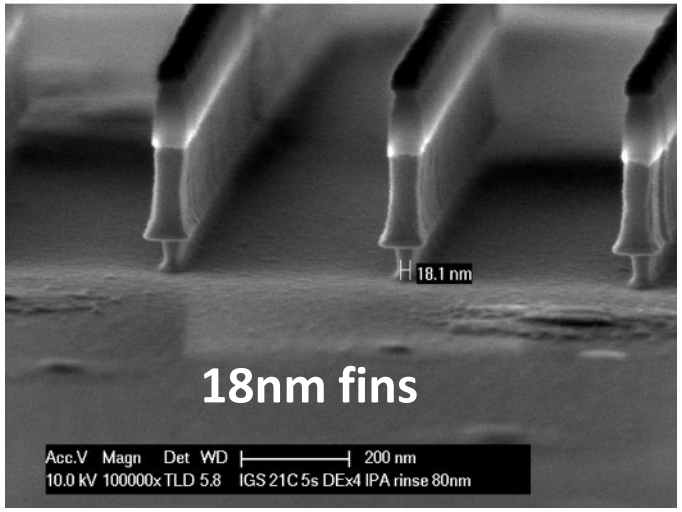
Drain pads
support narrow vertical ridge
→ target 5-10 nm ridge

Wrap-around gate
wraps over drain
no need for planarization









THz transistors

Transistors for mm-wave, sub-mm-wave wireless

Massive growth in use of radio communication

sub-5GHz spectrum almost used up

Next generation 5G, coming soon.

28, 38, 57-71(WiGig), and 71-86GHz.

Some degree of spatial multiplexing (multiple beams)

Research now explores the next generation (6G?).

100+ GHz carriers: 140, 220, 340GHz

maybe 650GHz

massive spatial multiplexing

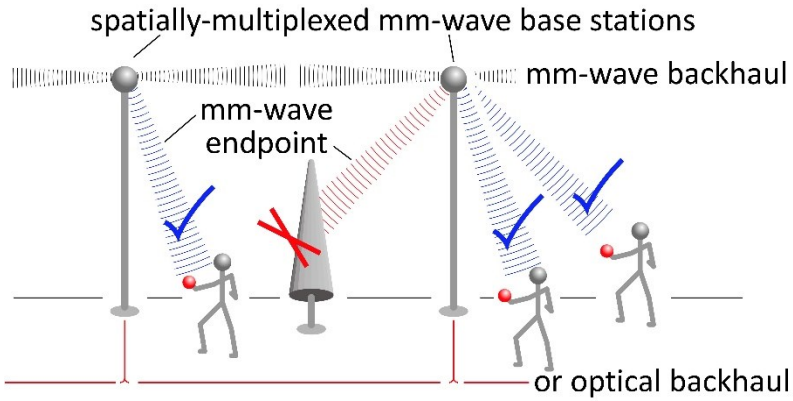
This will drive transistor development:

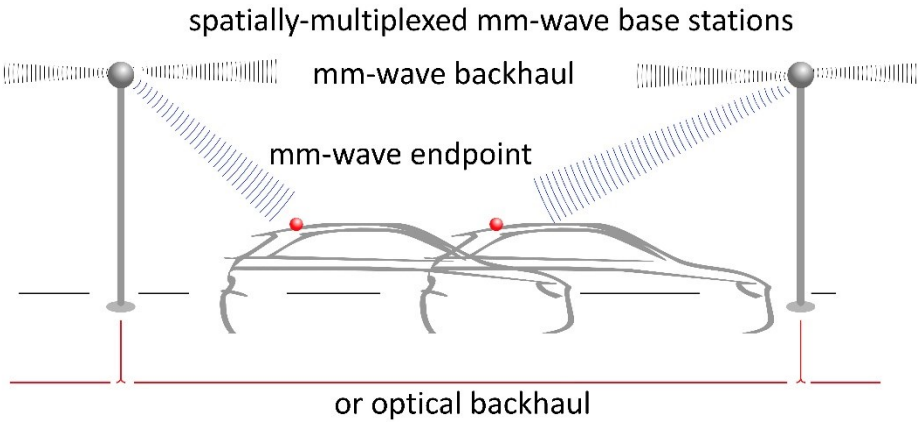
PAs for transmitters, **GaN**, **InP HBT**, SiGe HBT

LNAs for receivers: **InP HEMT**, **InP MOS-HEMT**

100-340GHz wireless communications

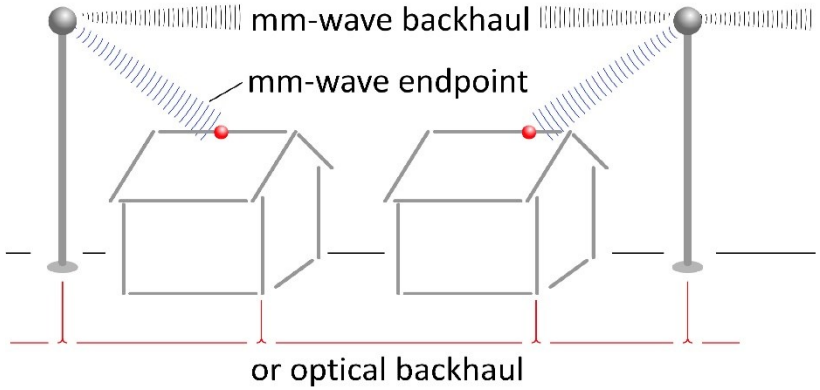
Gigabit mobile communication.

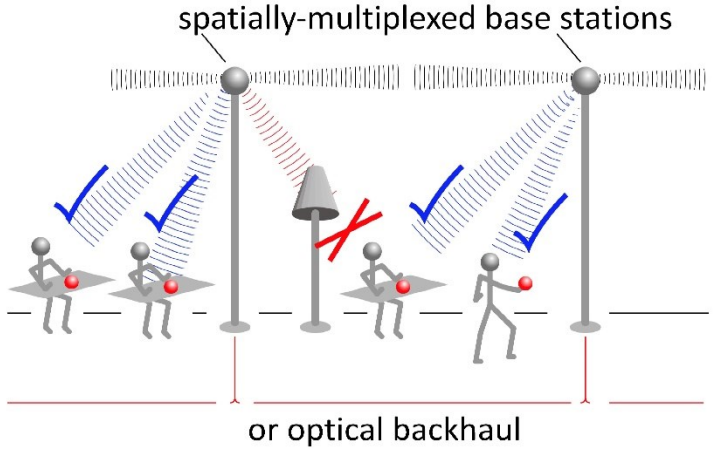




Information anywhere, any time, without limits

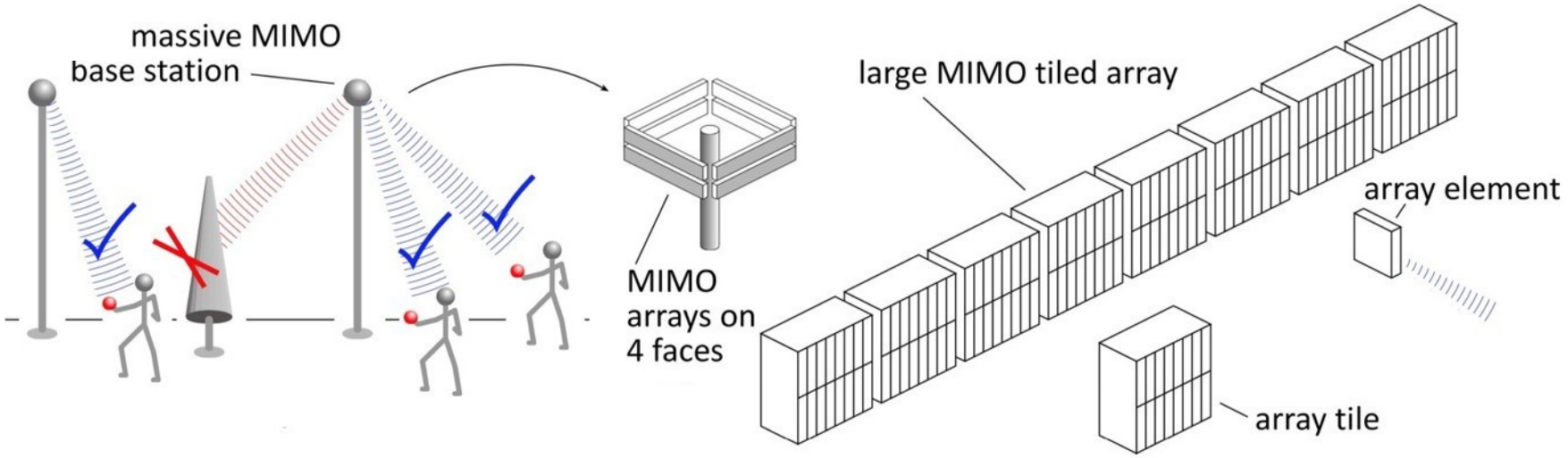
Gigabit residential/office communication.





Cellular/internet convergence: competition, low cost, broader deployment

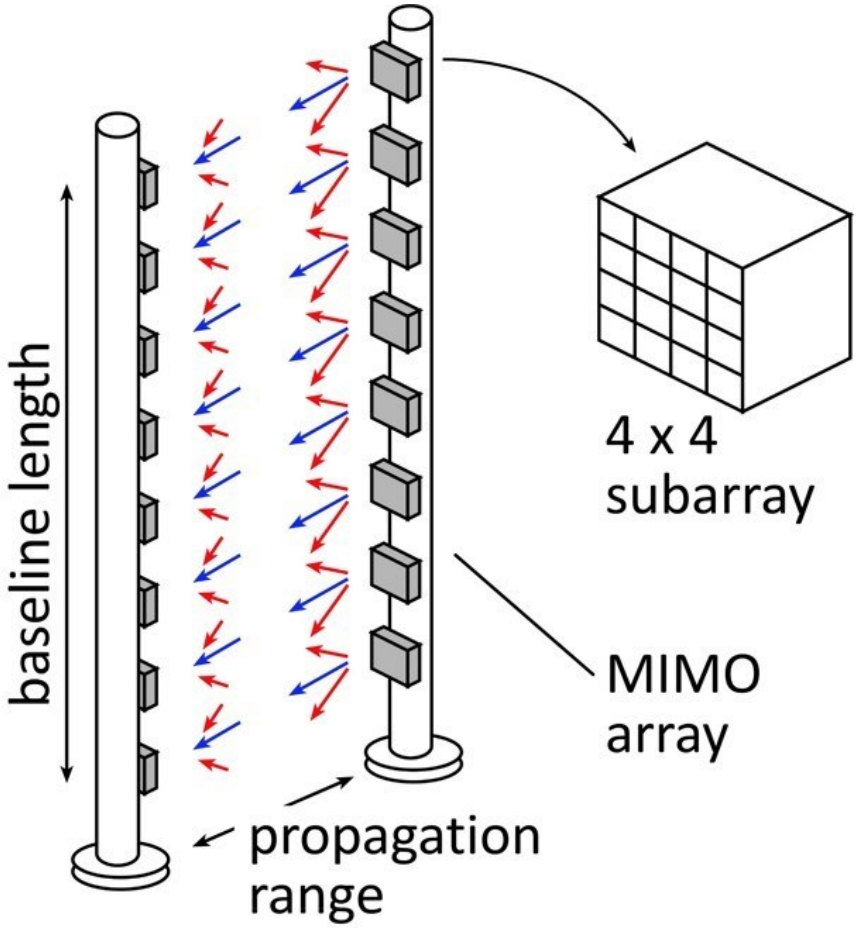
140/220 GHz spatially multiplexed base station



10 Tb/s spatially-multiplexed base station
Each face supports 256 beams @ 10Gb/s/beam.
100 meters range in 50 mm/hr rain
Realistic packaging loss, operating & design margins

Key device specifications:
140 GHz: PAs: P_{sat}=21.5 dBm: LNAs: F=4 dB
220 GHz: PAs: P_{sat}=25 dBm: LNAs: F=4 dB

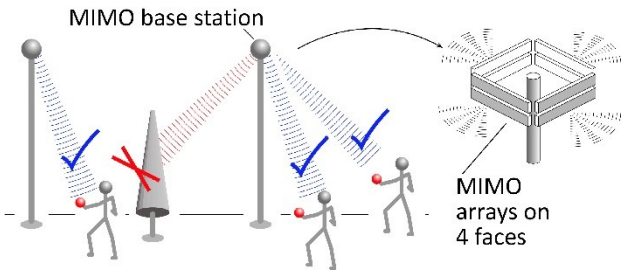
340 GHz, 650 GHz spatially-multiplexed backhaul

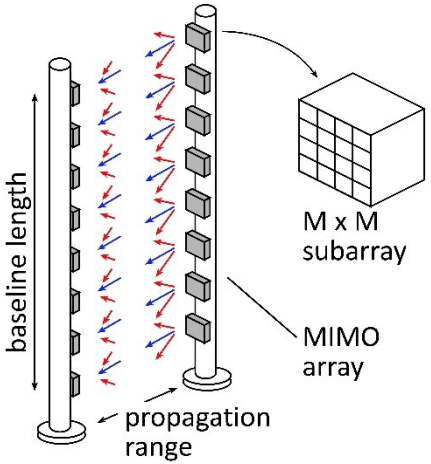


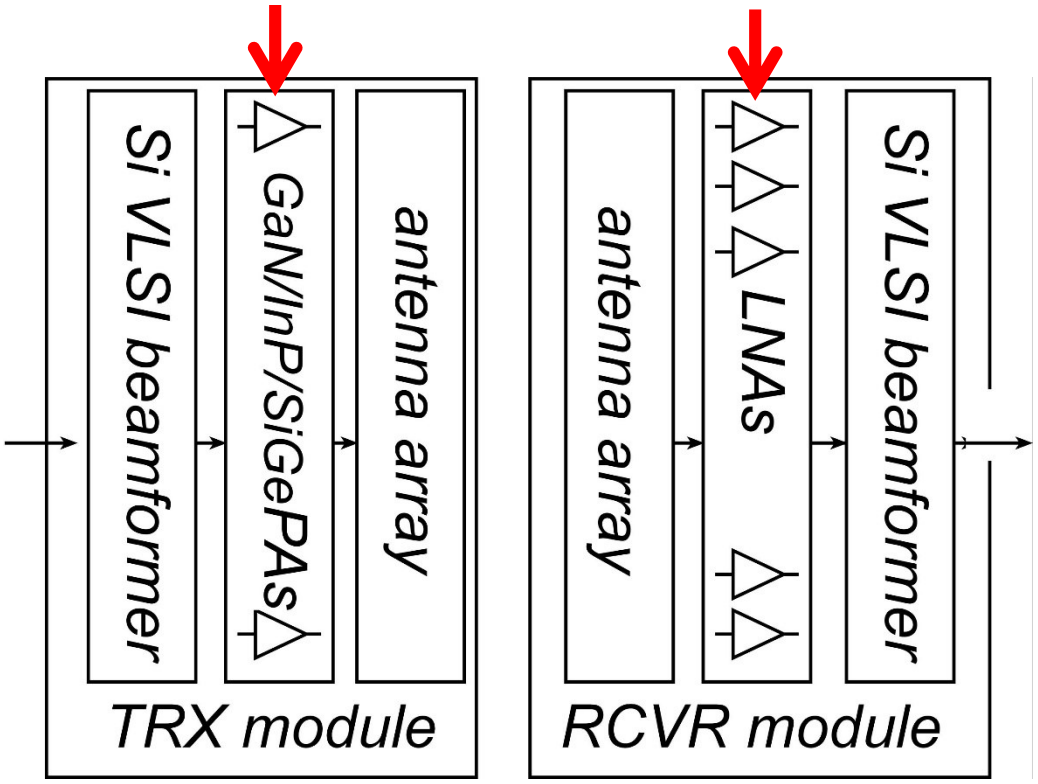
340 GHz:
640Gb/s @ 240 meters;
1.2 meter, 8-element array
F= **4dB**, P_{sat}≅**14dBm**

650 GHz:
1.28Tb/s @ 240 meters;
1.2 meter, 16-element array
F= **4dB**, P_{avg}=14.5dBm, P_{sat}≅**18.5dBm**

mm-Wave Wireless Transceiver Architecture







custom PAs, LNAs → power, efficiency, noise
Si CMOS beamformer→ integration scale

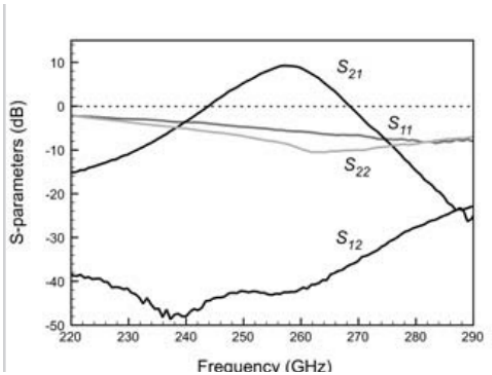
...similar to today's cell phones.

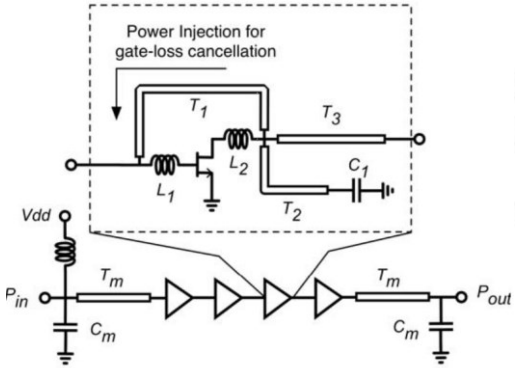
mm-wave CMOS (examples)

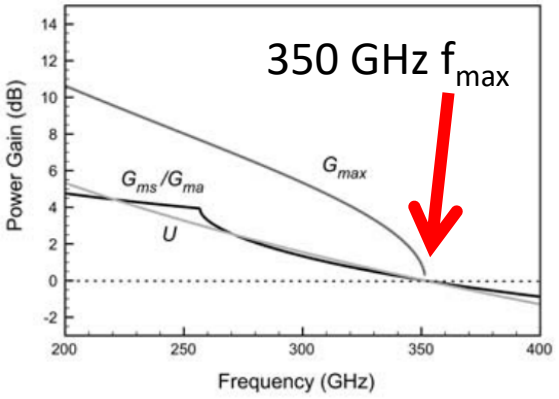
260 GHz amplifier, Feedback-enhanced-gain:

65nm bulk CMOS, 2.3 dB gain per stage (350GHz f_{max})

Momeni ISSCC, March 2013



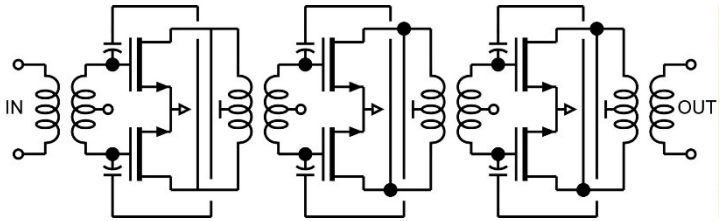


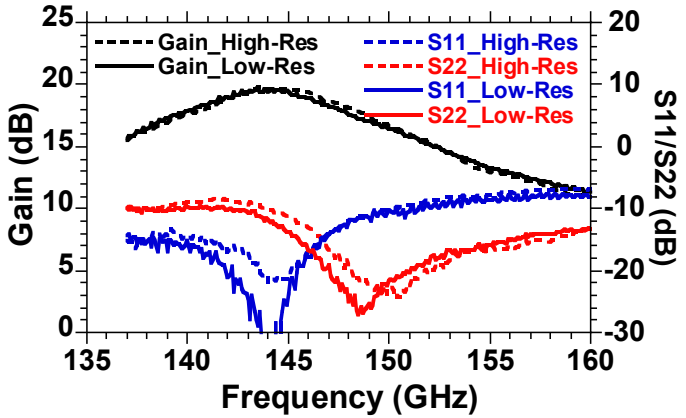


145 GHz amplifier, conventional neutralized design:

45 nm SOI CMOS, 6.3 dB gain per stage, ~1.5mW P_{sat}

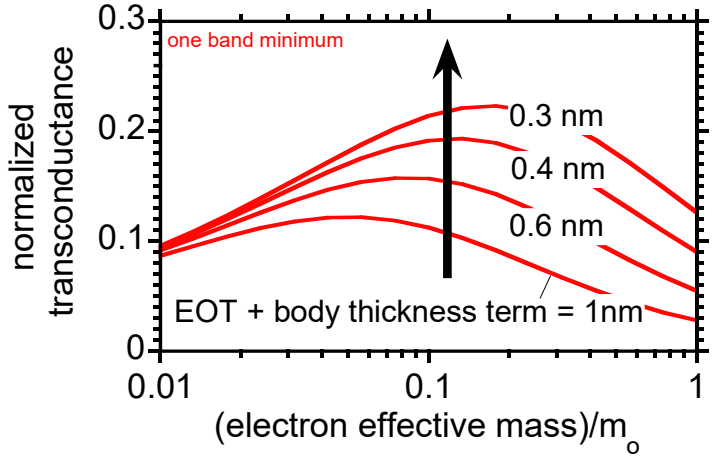
Kim et al. (UCSB), submitted



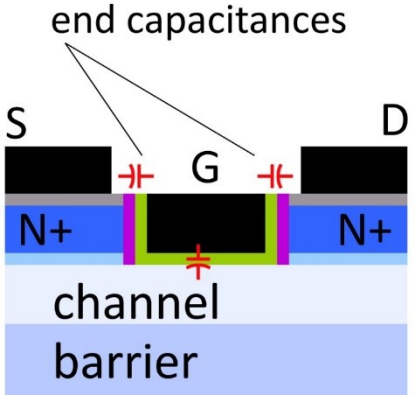


mm-Wave CMOS won't scale much further

Gate dielectric can't be thinned
→ on-current, g_m can't increase



Shorter gates give no less capacitance
dominated by ends; ~1fF/μm total

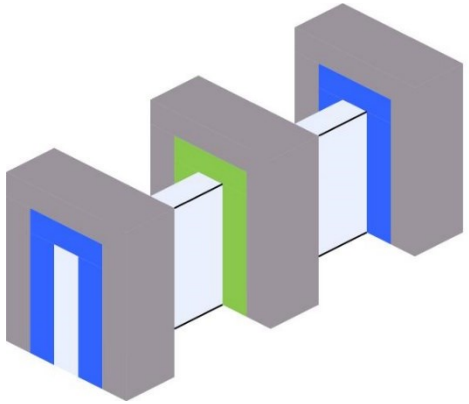


Maximum g_m, minimum C→ upper limit on f_τ.
about 350-400 GHz.

Tungsten via resistances reduce the gain

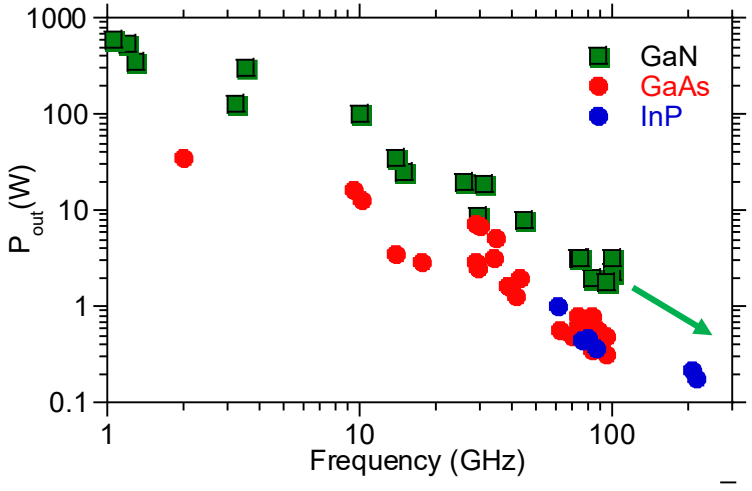
Inac et al, CSICS 2011

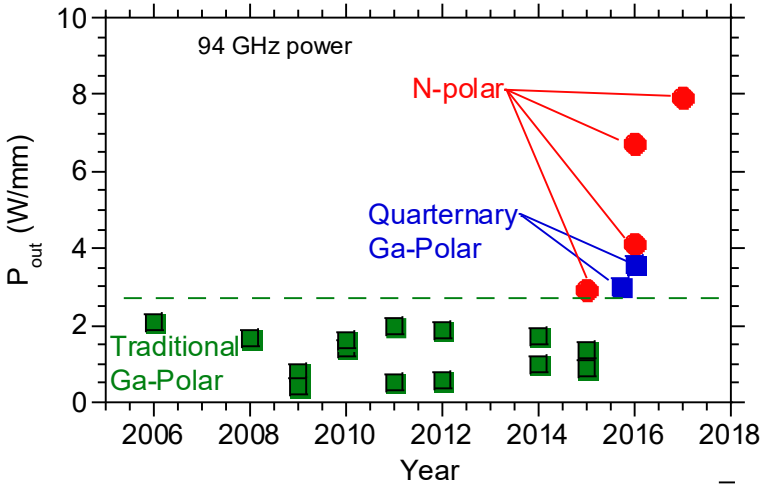
Present finFETs have yet larger end capacitances



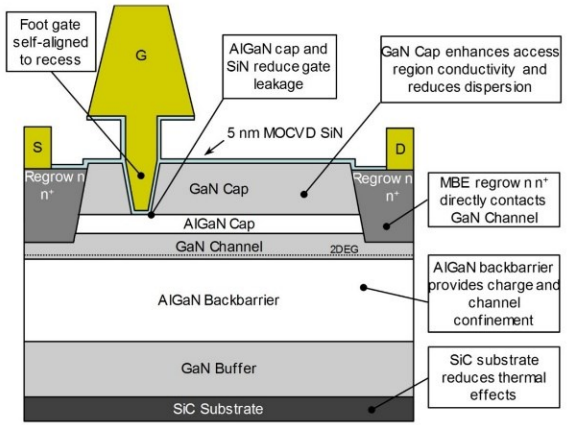
Gallium nitride mm-wave power

GaN is the leading high-frequency power technology

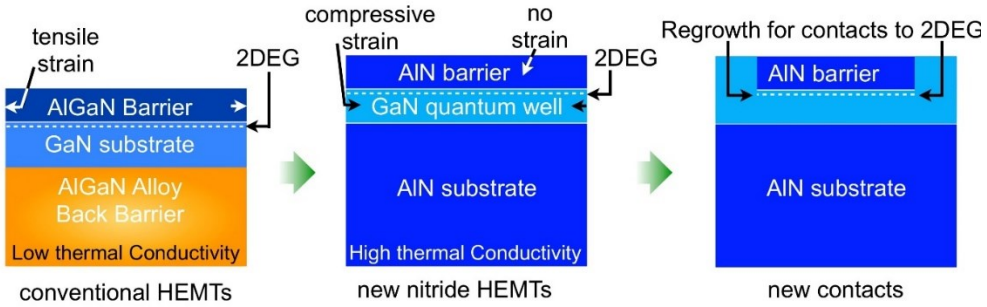




N-polar GaN: Mishra

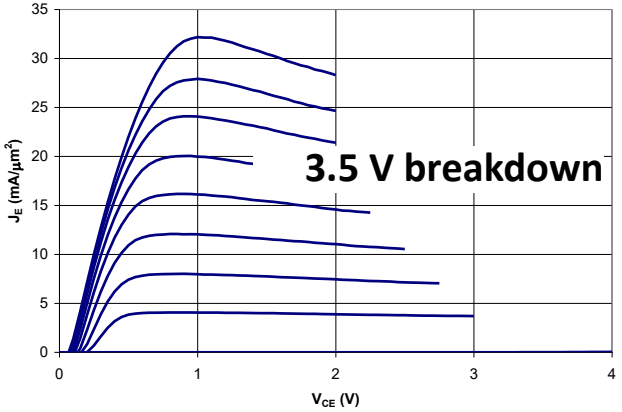


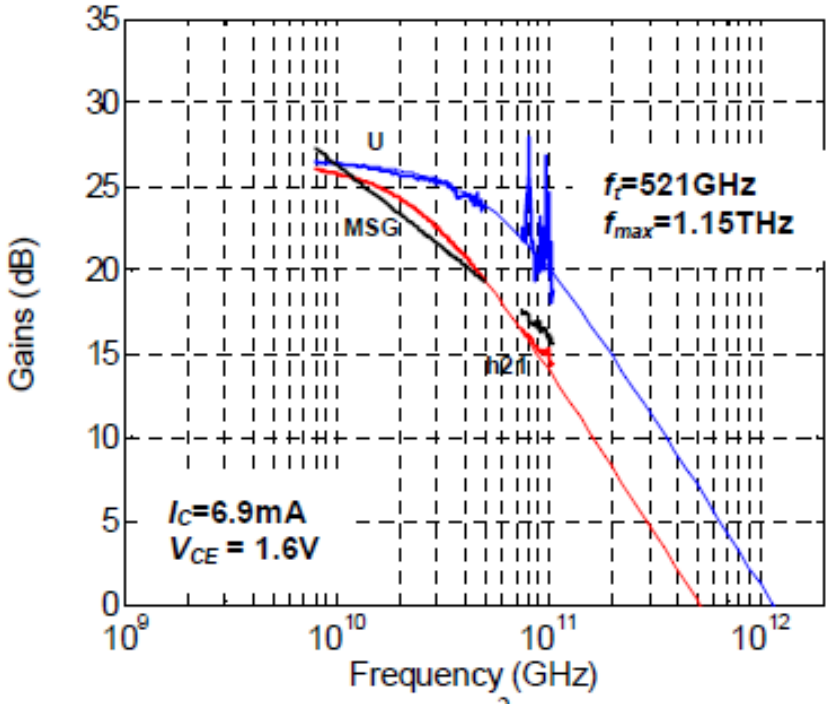
nm AlN/GaN: Xing/Jena



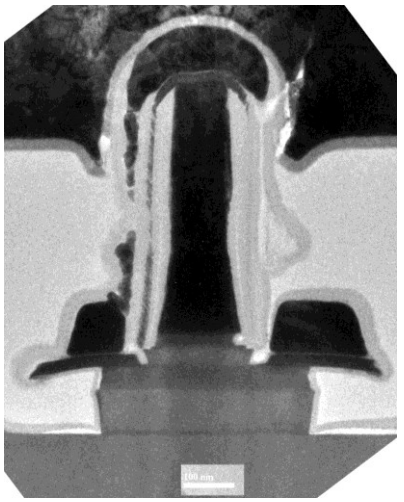
130nm / 1.1THz InP HBT Technology

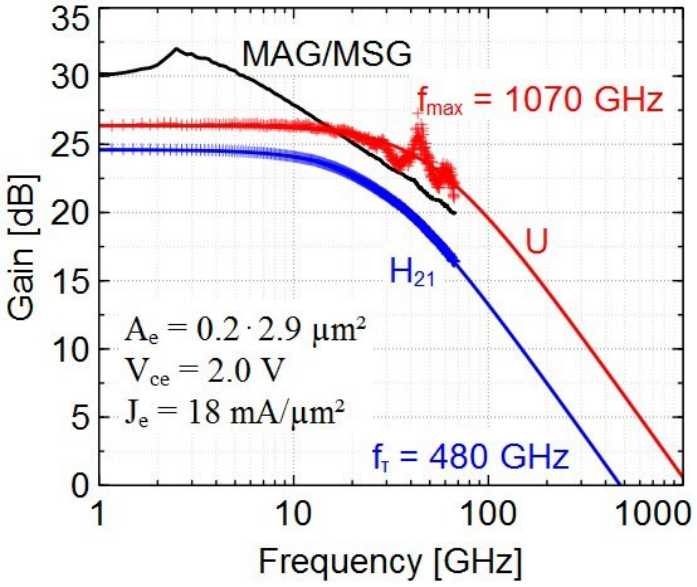
Teledyne: M. Urteaga *et al*: 2011 DRC





Rode (UCSB), IEEE TED, 2015

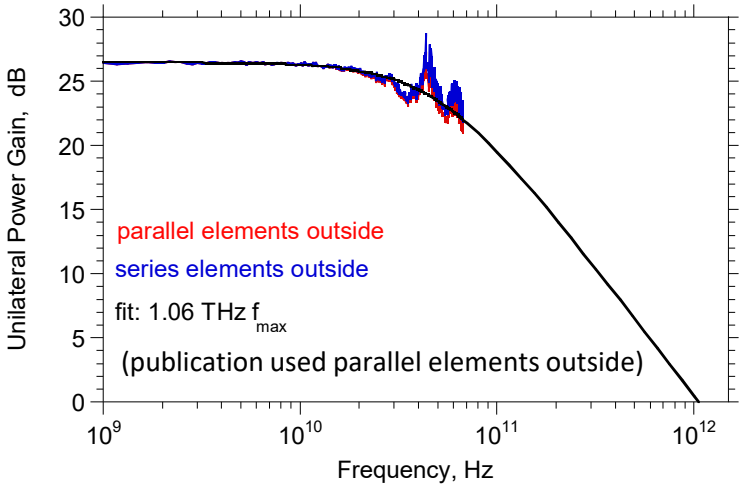


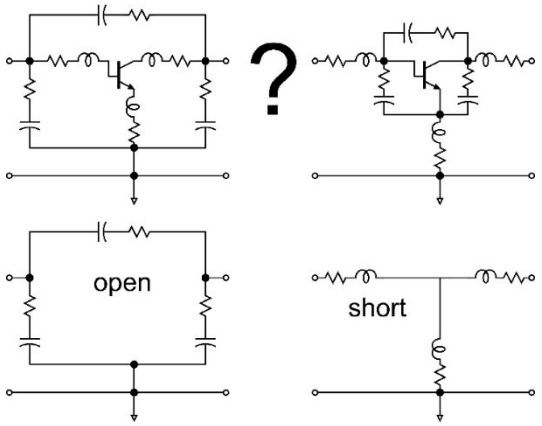


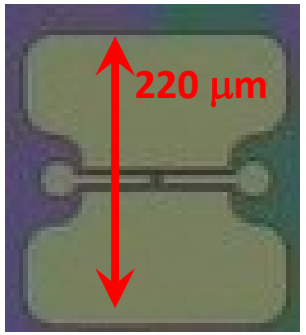
THz transistor measurements

Problems with simple pads:

Substrate resonances @ >35 GHz → make pads small, grounds close(!)
Ambiguity in series-first or shunt-first pad stripping.
Our present HBTs, stripping order makes only a minor difference.

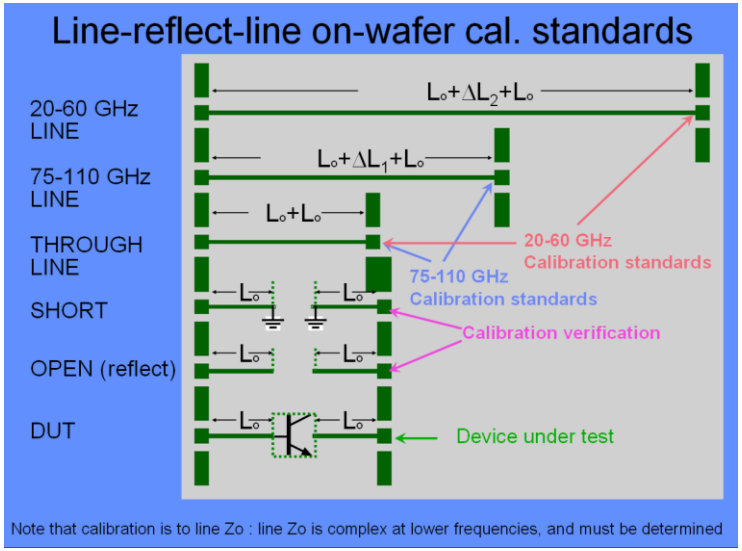






On-wafer LRL is much better

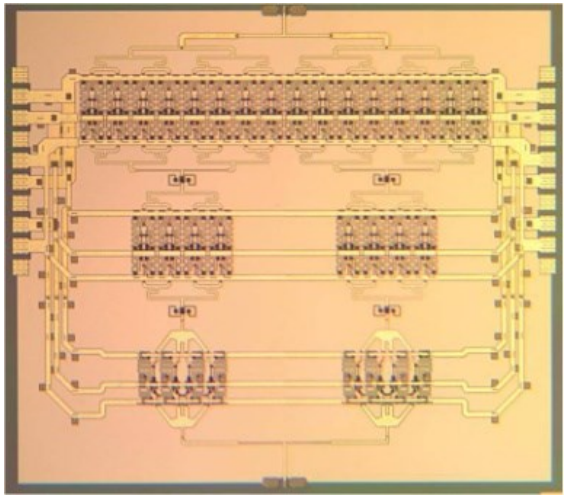
No pad-stripping.
Still must avoid substrate resonances
thinned substrate with TSV's
or thin-film microstrip wiring



130nm / 1.1THz InP HBT: IC Examples

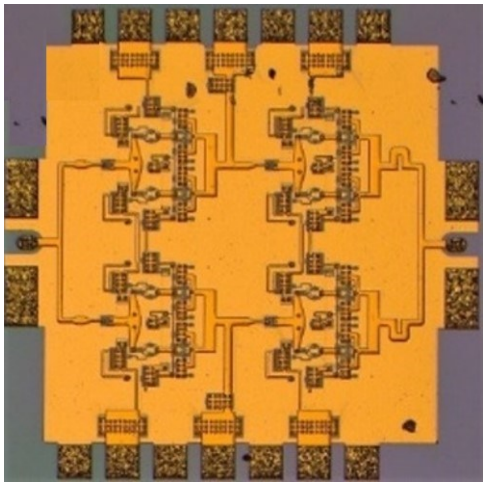
220 GHz 0.18W power amplifier

UCSB/Teledyne: T. Reed *et al*: 2013 CSICS



325 GHz, 16mW power amplifier

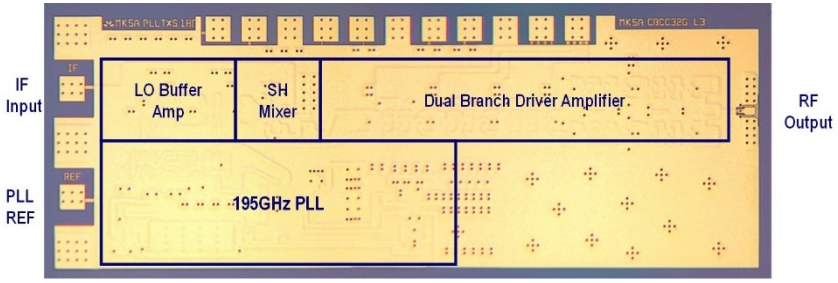
UCSB/Teledyne: (A. Ahmed, submitted)

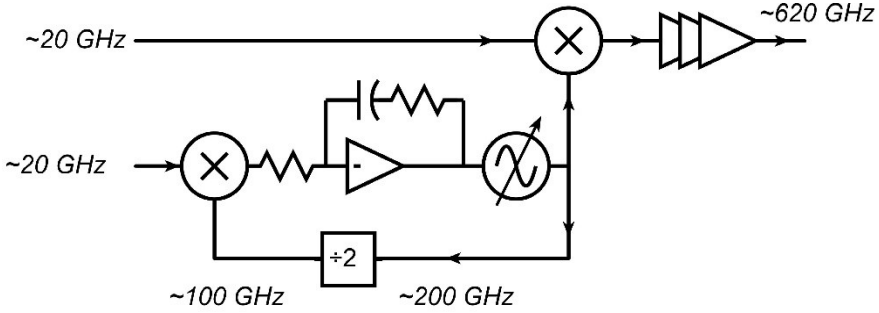


Integrated ~600GHz transmitter

Teledyne: M. Urteaga *et al*: 2017 IEEE Proceedings

but, only ~1 mW output power

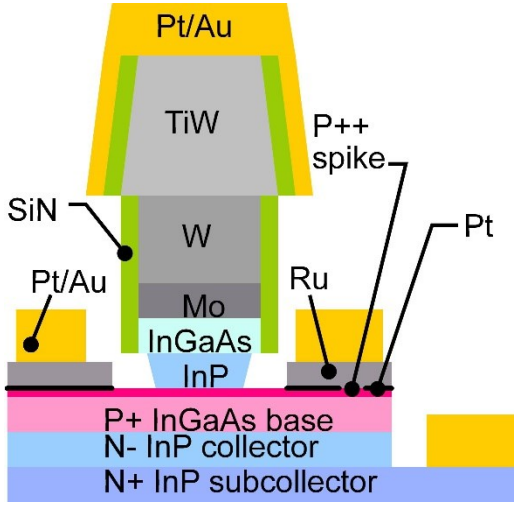




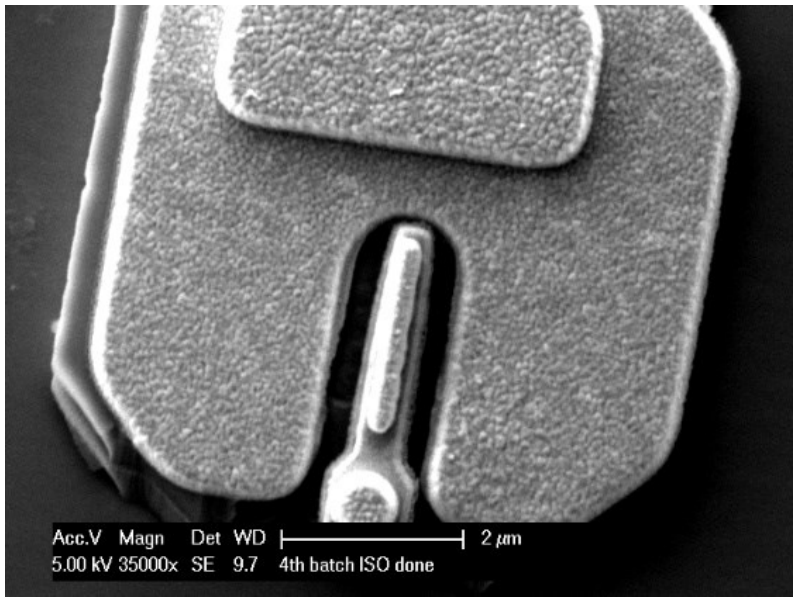
InP HBT: Towards the 2 THz / 64nm Node

Thin semiconductor layers (transit time)
High current density (CV/I)
Narrow junctions (heat)
Ultra low resistivity contacts (RC)
Low base metal resistance (RC)

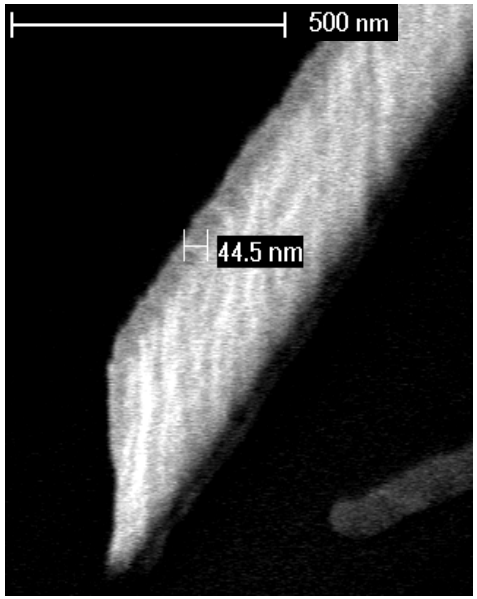
5nm P+ spike: low-ρ_c contacts, good β.



90 nm HBT



45 nm emitter

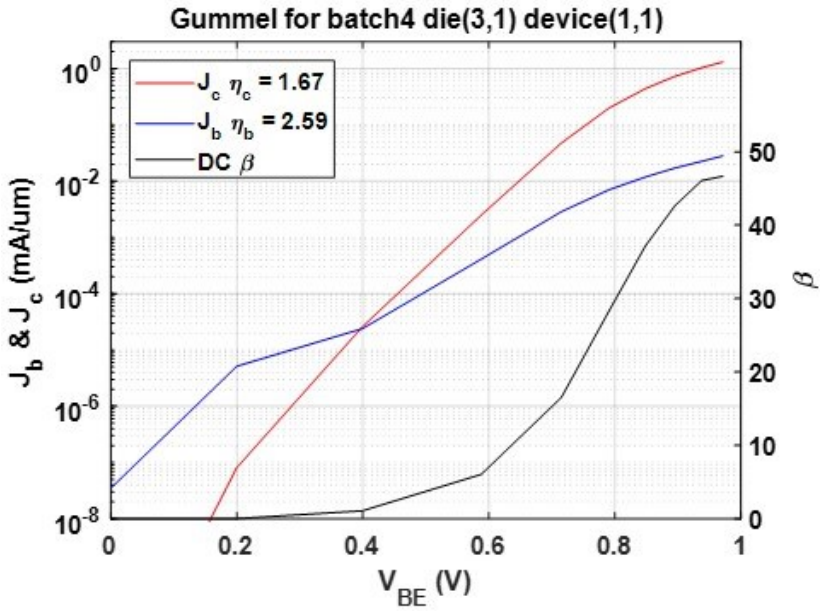


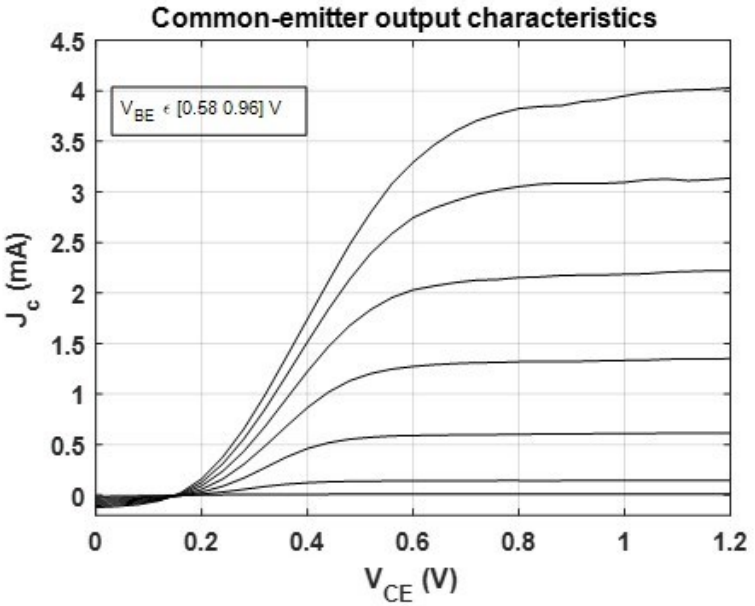
Yihao Fang, UCSB, to be submitted

InP HBT: Towards the 2 THz / 64nm Node

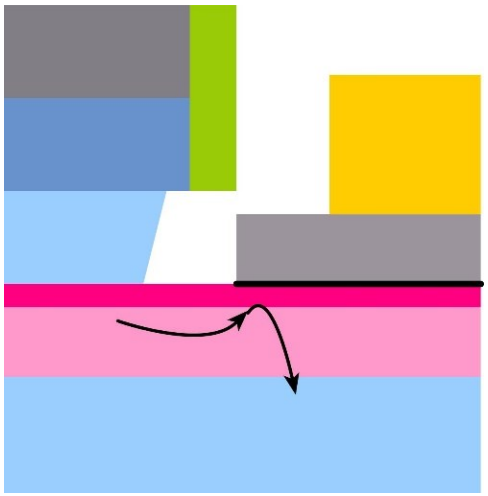
Good β, even at 90nm.

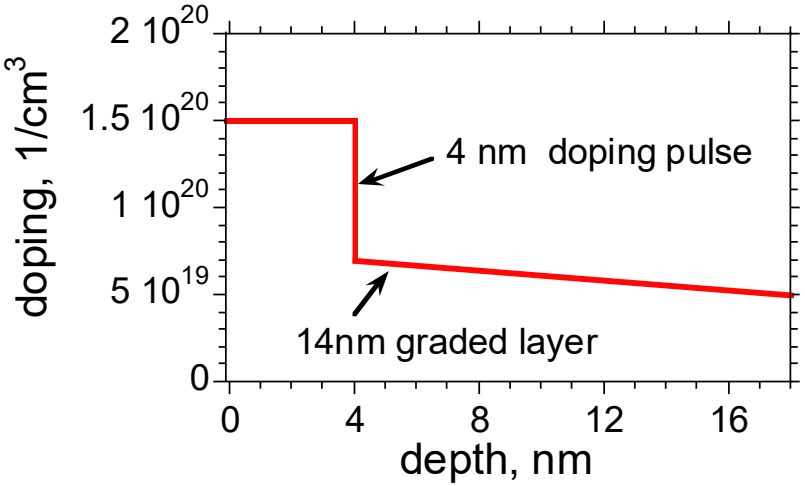
Yihao Fang, UCSB, to be submitted





...because of doping pulse, grade

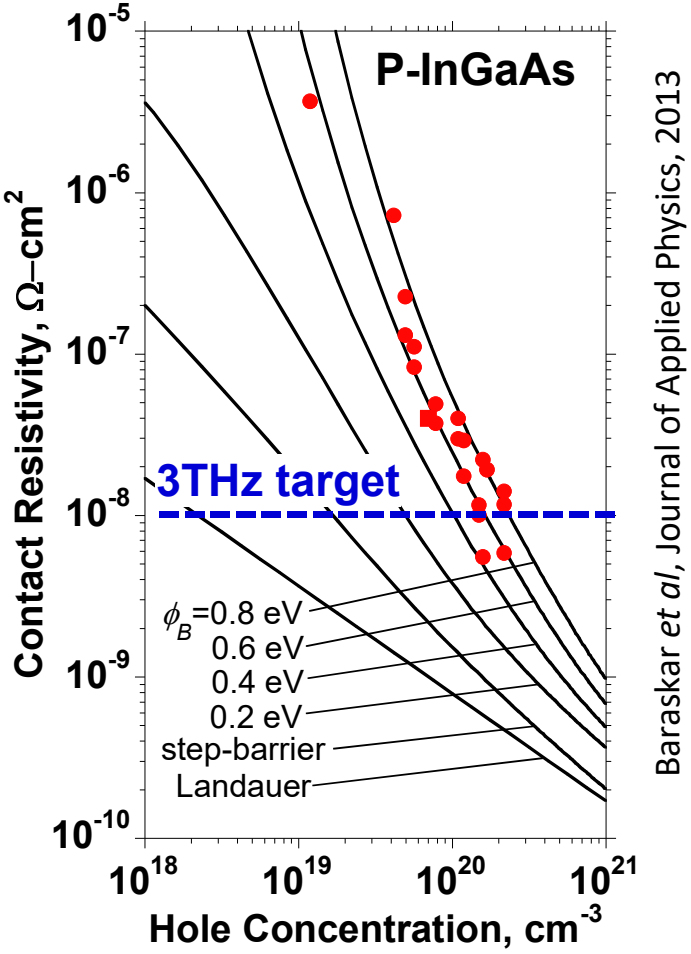




Challenges at 65nm: base contacts, base metal

Obtaining good base contacts

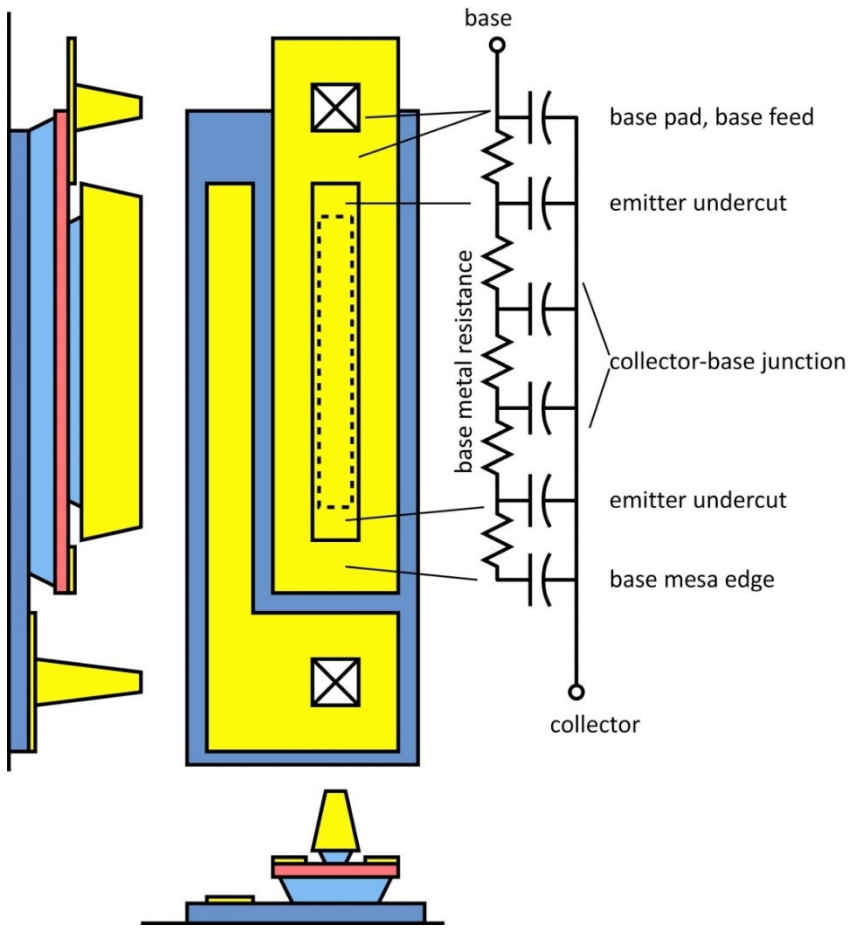
in HBT vs. in contact test structure
(emitter contacts are fine)



Baraskar *et al*, Journal of Applied Physics, 2013

RC parasitics along finger length

metal resistance, excess junction areas



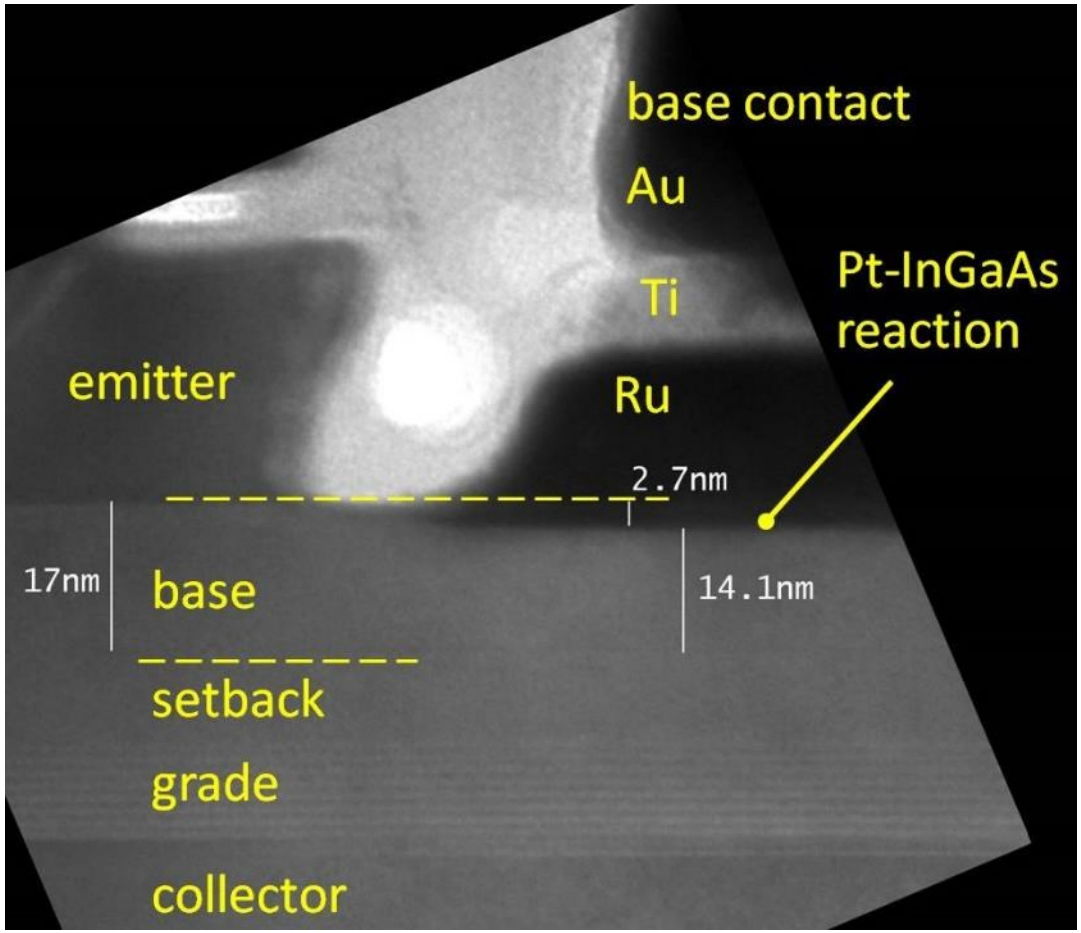
Rode et al., IEEE TED, Aug. 2015

Challenges at 65nm: Base contact penetration

TLM test samples:
ultra-clean surfaces
non-penetrating contacts
refractories: Ru, Mo, Ir, W
→ ~6×10^{-9} Ω-cm^2 resistivity

HBT emitter:
first process step
ultra-clean surfaces
refractory Mo contacts
~$1\text{-}2\times10^{-8}$ Ω-cm^2 resistivity

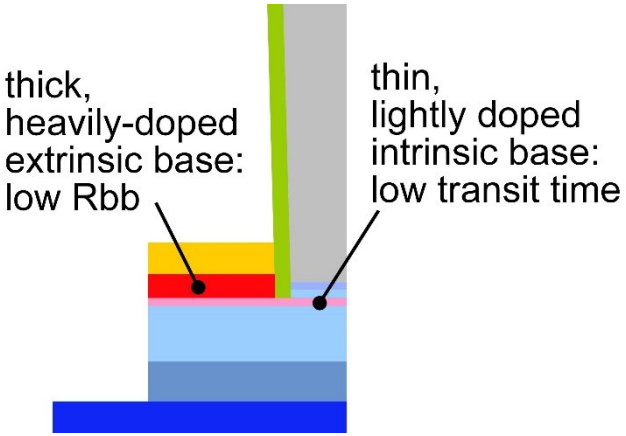
HBT base:
late process step
UV-O_3/HCl cleaning not enough
controlled-penetration contacts: 1nm Pt→ 3nm reaction depth
→ incompatible with thin & pulse-doped base designs



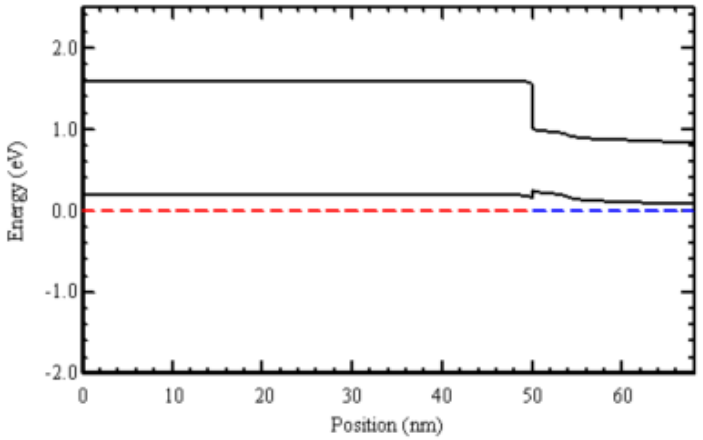
Rode et al., IEEE TED, Aug. 2015

Next: regrowth instead of scaling

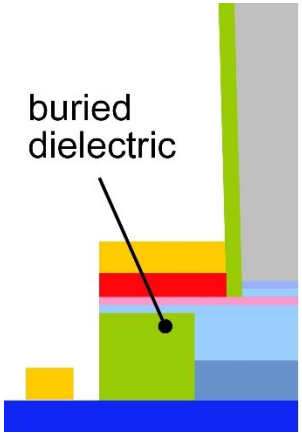
Goal: regrown-base HBT
increased β, f_{max}



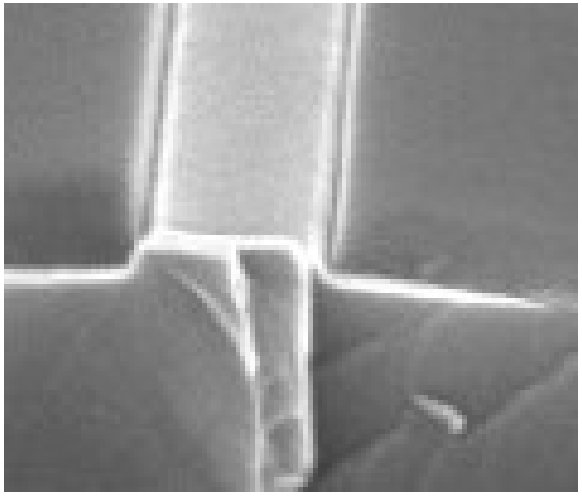
Intrinsic/extrinsic base junction
metamorphic p-GaAs/p-InGaAs
electron barrier→ high β
low intrinsic doping→ low Auger→ high β



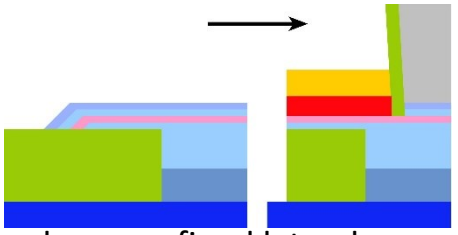
Goal: pedestal-collector HBT
increased f_{max}



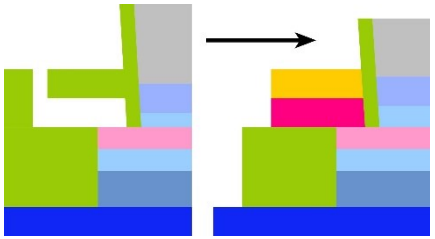
1st step :
collector growth in dielectric window



Next step:
base lateral overgrowth,



or base confined lateral overgrowth

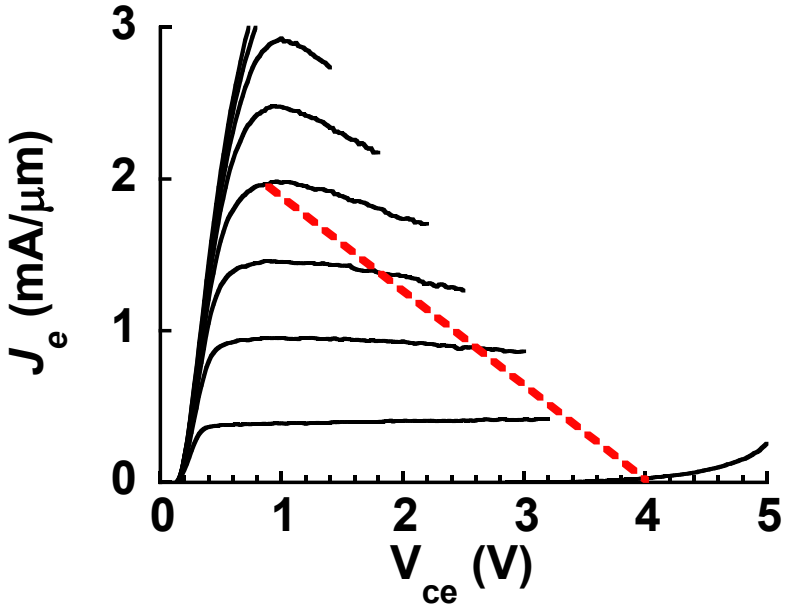


mm-wave PAs: need higher current density

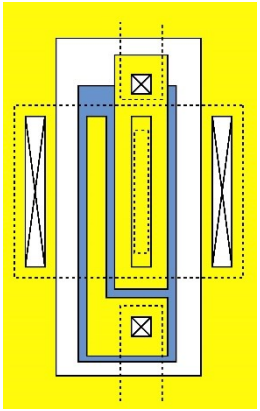
3 μm max emitter length (> 1 THz f_{max})
2 mA/μm max current density
I_{max}= 6 mA

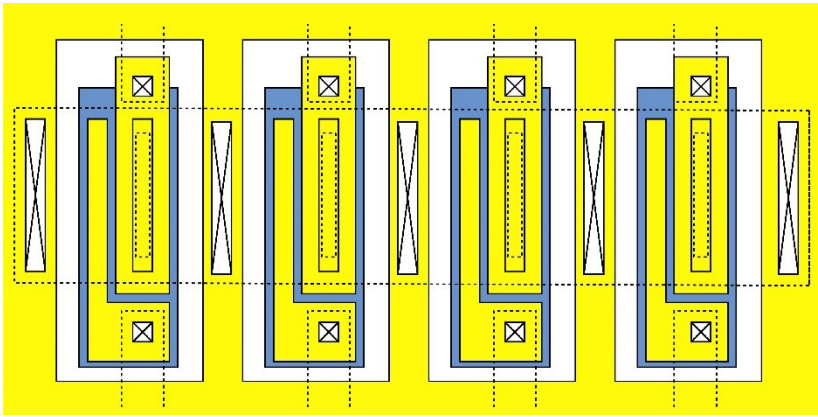
Maximum 3 Volt p-p output

Load: 3V/6mA= 500 Ω

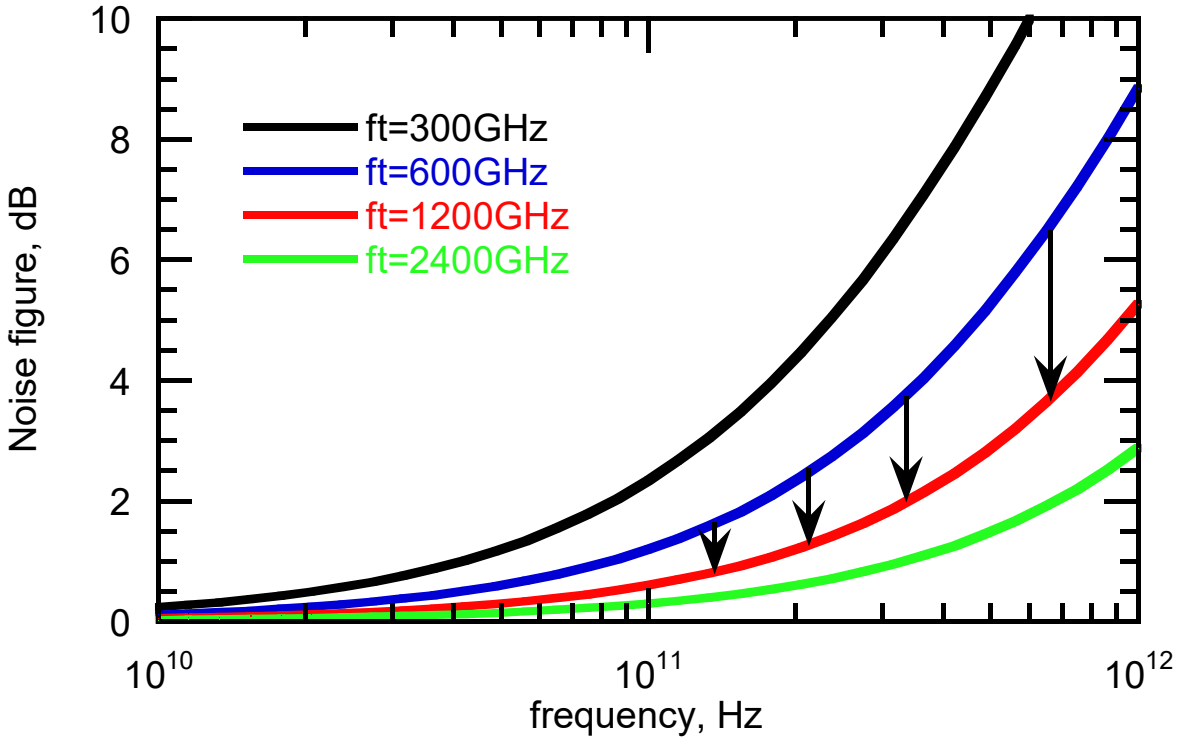


1) Transmission-line combiner: cannot provide 500 Ω loading
2) Lumped multi-finger layouts: parasitics, reduced gain, f_{max}





HEMTs: key for low noise



$$F_{\min} \approx 1 + 2\sqrt{g_m(R_s + R_g + R_i)\Gamma} \cdot \left(\frac{f}{f_\tau}\right) + 2g_m(R_s + R_g + R_i)\Gamma \cdot \left(\frac{f}{f_\tau}\right)^2$$

$$\Gamma \approx 1$$

Hand-derived modified Fukui Expression, fits CAD simulation extremely well.

2:1 to 4:1 increase in f_τ → improved noise

→ less required transmit power→ easier PAs, less DC power

or enable higher-frequency systems

Towards faster HEMTs

Scaling limit: gate insulator thickness

HEMT: InAlAs barrier: tunneling, thermionic leakage

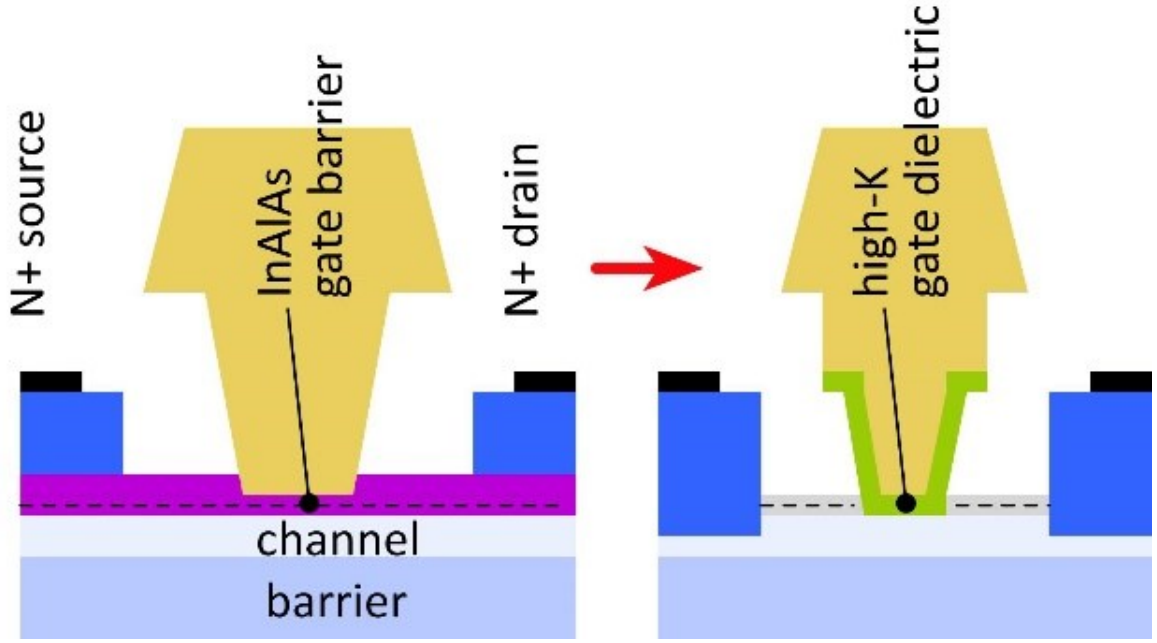
solution: replace InAlAs with high-K dielectric

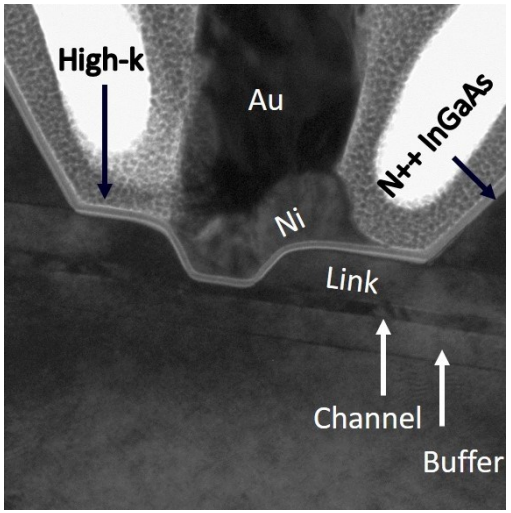
2nm ZrO_2 (ε_r=25): adequately low leakage

Scaling limit: source access resistance

HEMT: InAlAs barrier is under N+ source/drain

solution: regrowth, placing N+ layer <u>on</u> InAs channel

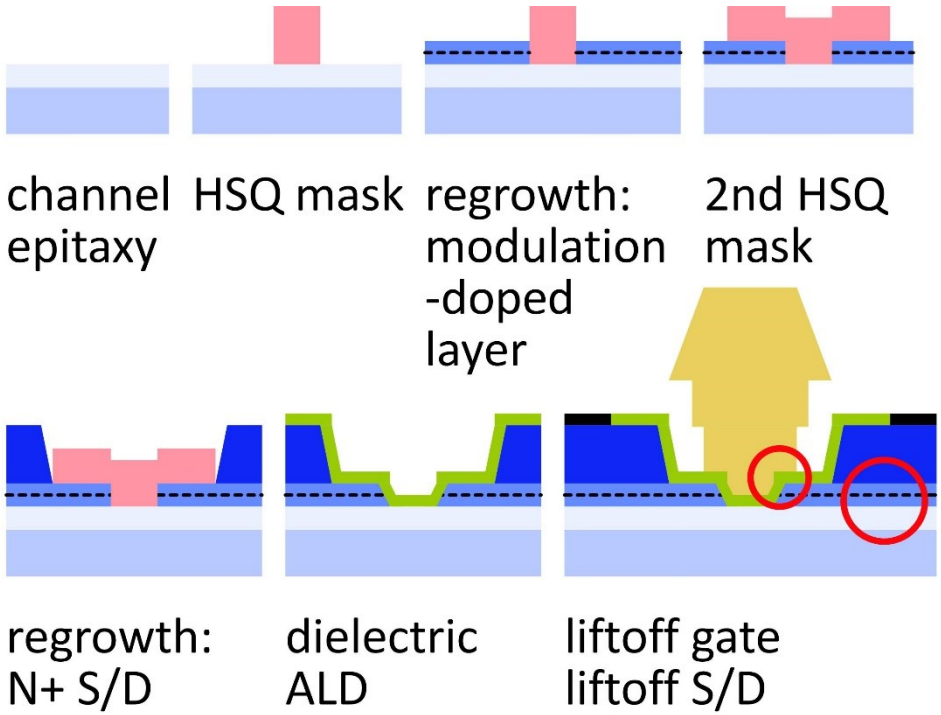


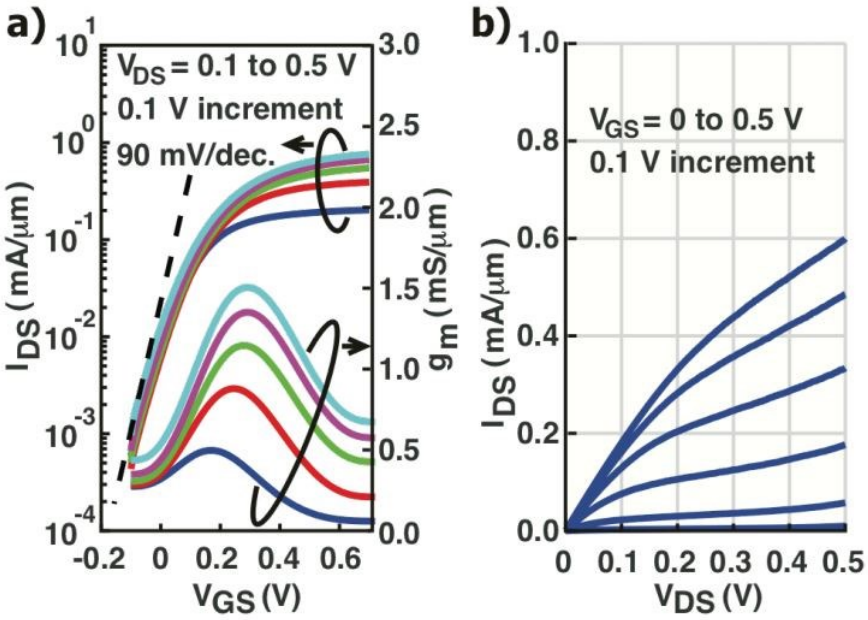


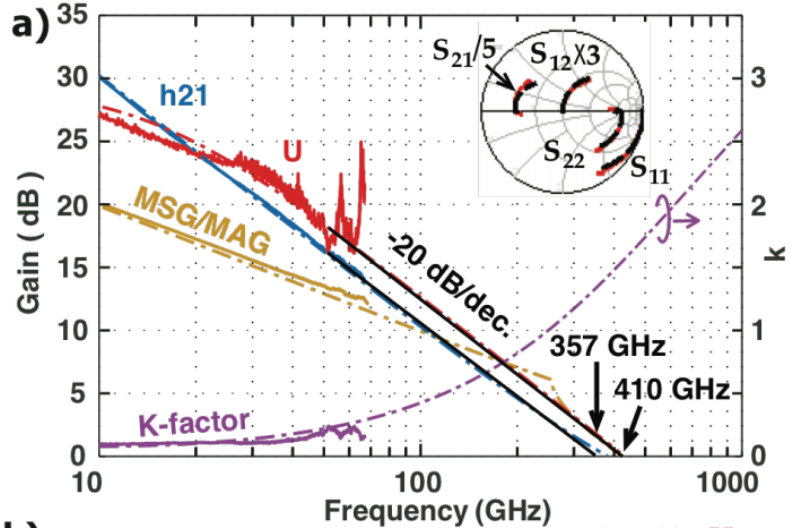
Jun Wu, UCSB, IEEE EDL

Towards faster HEMTs

Jun Wu, UCSB, IEEE EDL, 2018





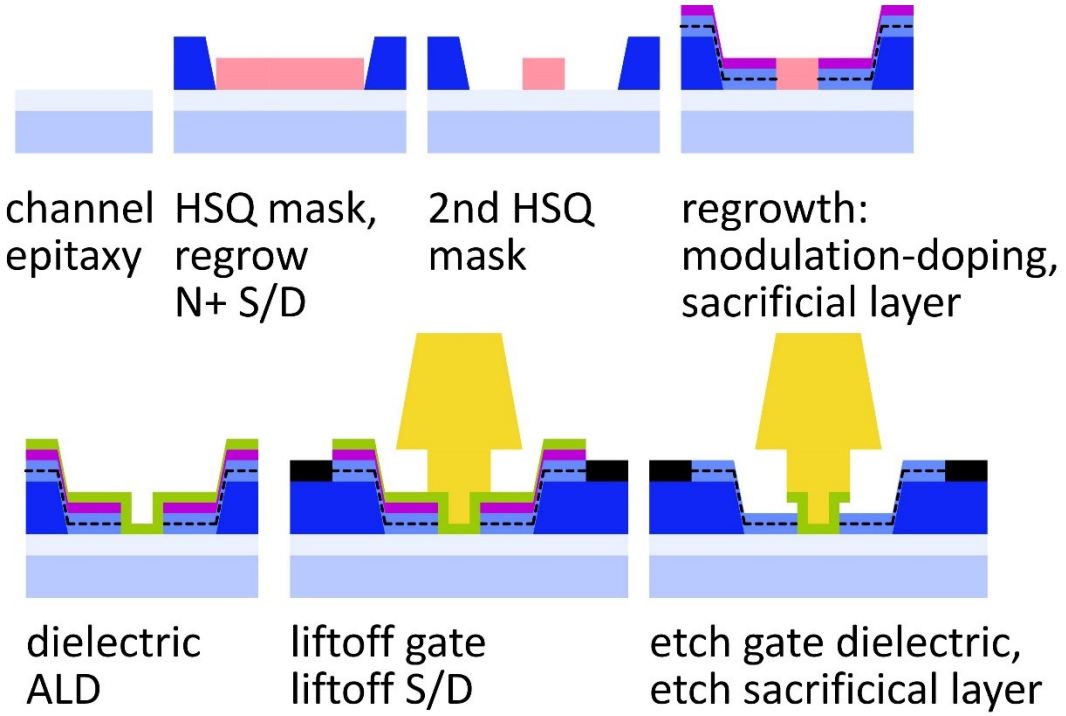


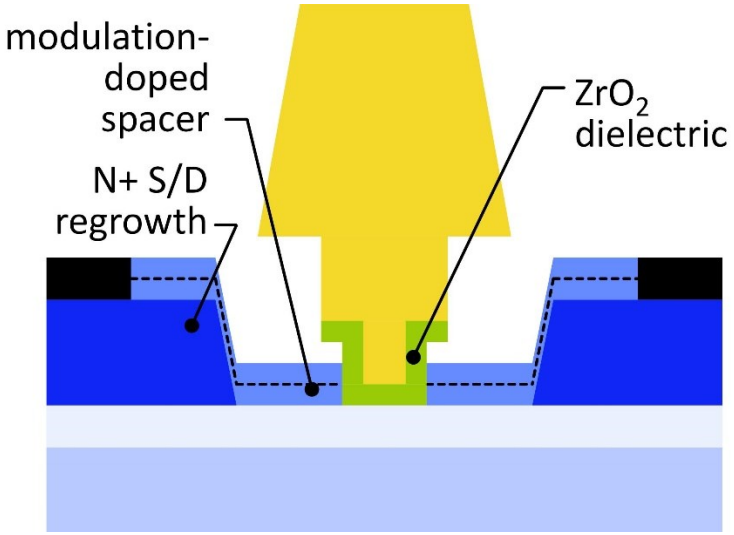
Double regrowth
modulation-doped access regions
N+ contacts

High-K gate dielectric: 3 nm ZrO2.

Highly scaled
5nm InAs channel
10-30nm gate lengths

Towards faster HEMTs: next step





Revised process: no N- material between channel and contacts
reduced source/drain access resistance

Revised process: sacrificial layer
reduces parasitic gate-channel overlap: less gate-source capacitance

Thinner gate dielectric (2nm ZrO_2), thinner channel (3nm InAs)
higher g_m , lower g_{ds}

Transistors: mm-Wave Low-Power VLSI

Electron devices for VLSI

Low-voltage transistors

low voltage → low CV^2 → low switching power.

NC FETs.

high-current TFETs.

3D integration

more transistors/cm^2→smaller IC→ shorter wires→ less power

process-intensive: can universities contribute ?

nm-scale memory

easier than nm logic: don't need good I_{on}, I_{off} at low V_{DD}.

just need to change a physical state, then measure it.

nm and THz Transistors

The transistor was demonstrated 70 years ago.

most easy things have been done.

nm technologies need advanced tools: hard for universities.

what should we do next ?

VLSI

low voltage logic: **NCFETs**, **high-current TFETs**

3D integration.

atomic-scale memory.

High-frequency transistors: 100-340GHz

power transistors: **GaN HEMT, InP HBT**

low-noise transistors: **InP HEMT**

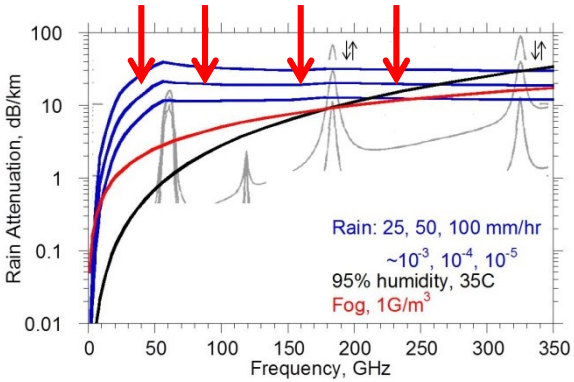
Beyond-220GHz transistors: **InP HBT & HEMT**

Power conversion and control.

(backup slides follow)

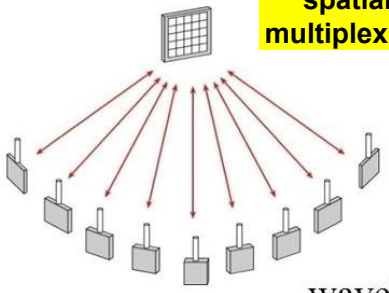
100-340 GHz: benefits & challenges

Large available spectrum



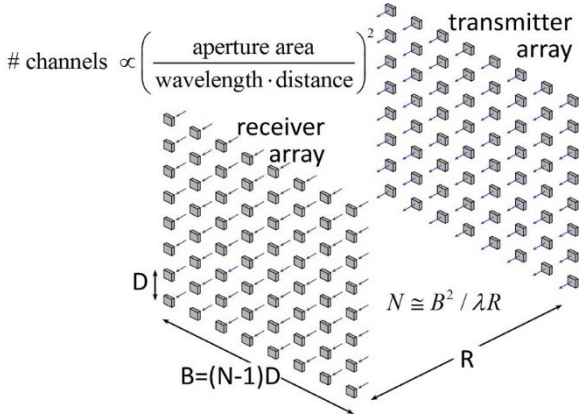
(note high attenuation in foul or humid weather)

Massive # parallel channels



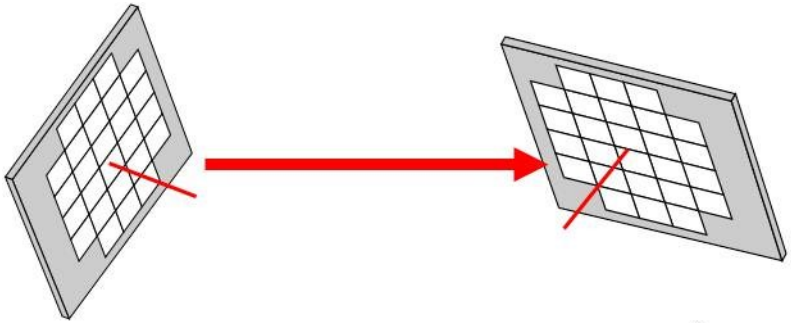
spatial multiplexing

$$\text{angular resolution} \approx \frac{\text{wavelength}}{\text{array widt h}}$$



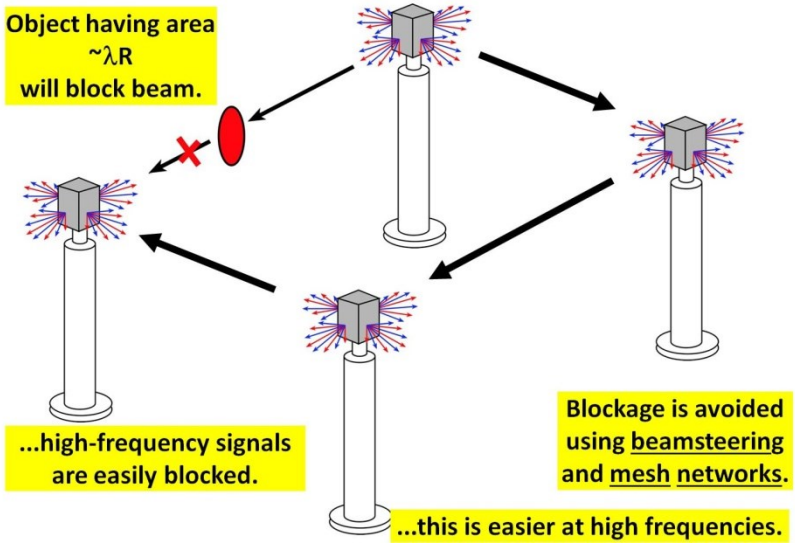
line-of-sight MIMO

Need phased arrays (overcome high attenuation)

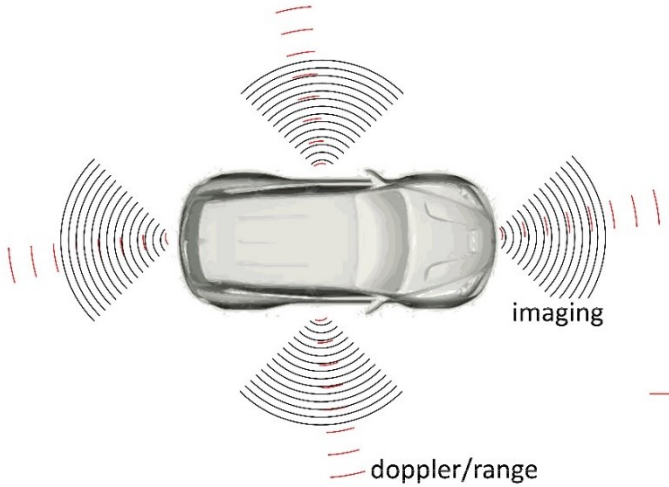


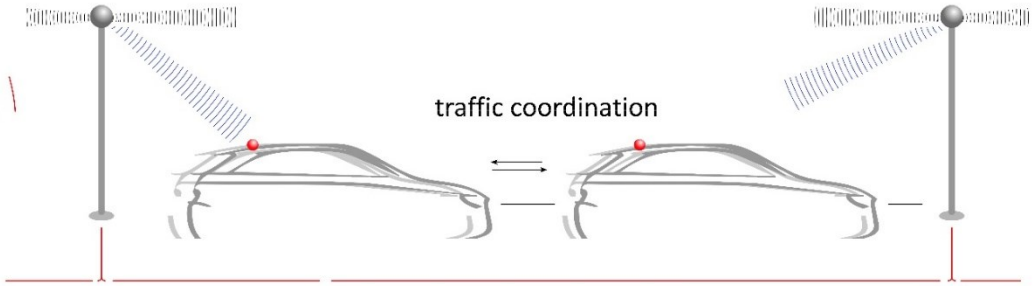
$$\frac{P_{received}}{P_{transmit}} \propto N_{receive} N_{transmit} \frac{\lambda^2}{R^2} e^{-\alpha R}$$

Need mesh networks



100-340GHz: radar and imaging





340 GHz TV-resolution radar: see through fog and rain.

drive safely in fog at 100 km/hr

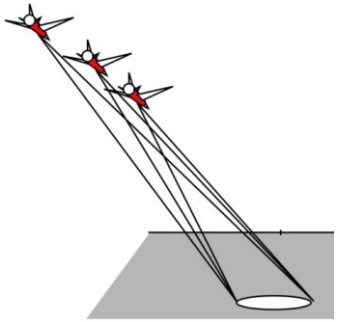
self-driving: complements LIDAR, but works in bad weather

60 GHz Doppler / ranging radar.

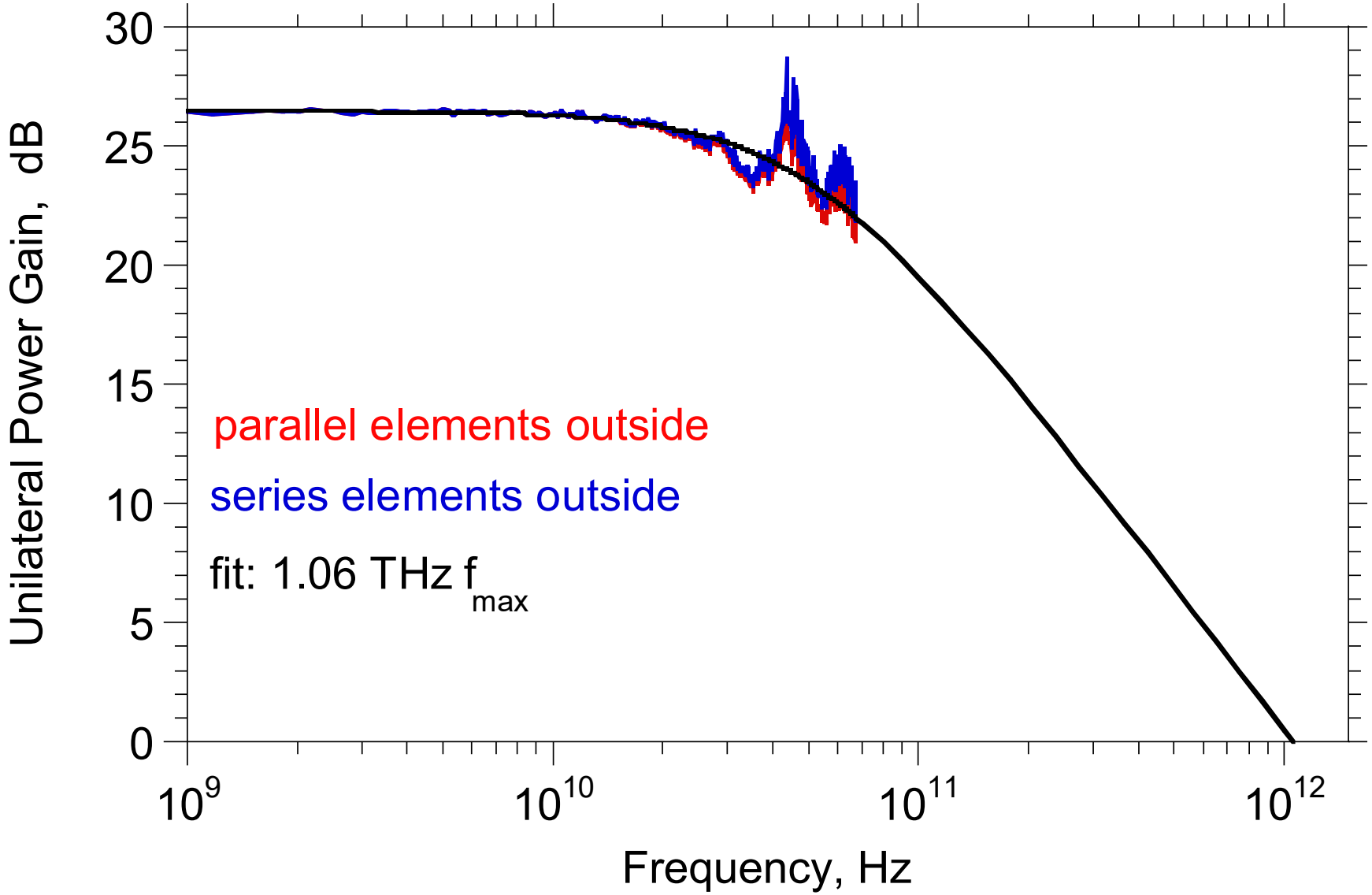
long-range but low-resolution: detects objects, but can't recognize them .

Imaging for drones, small aircraft

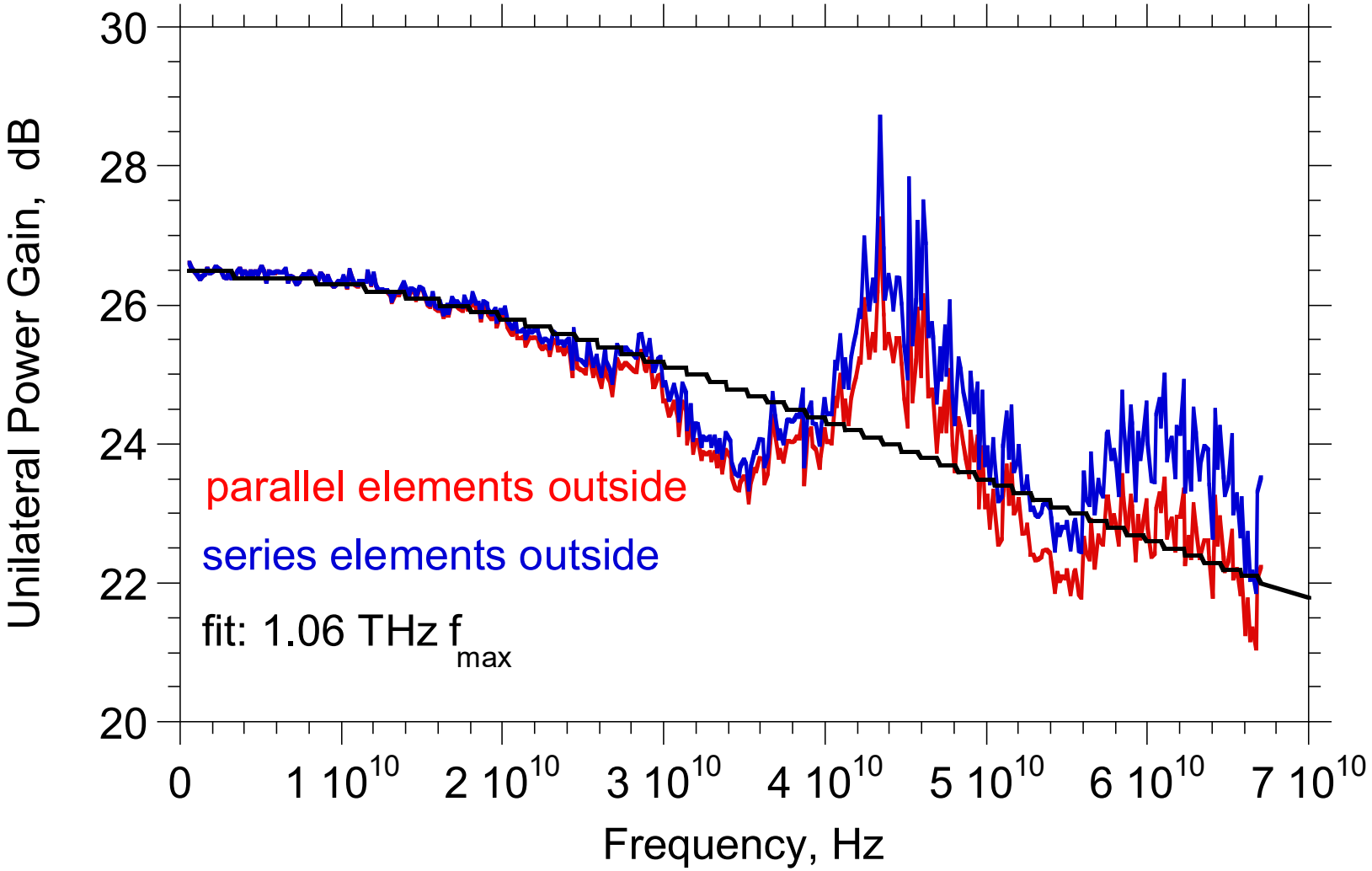
small, light aperture, high resolution.



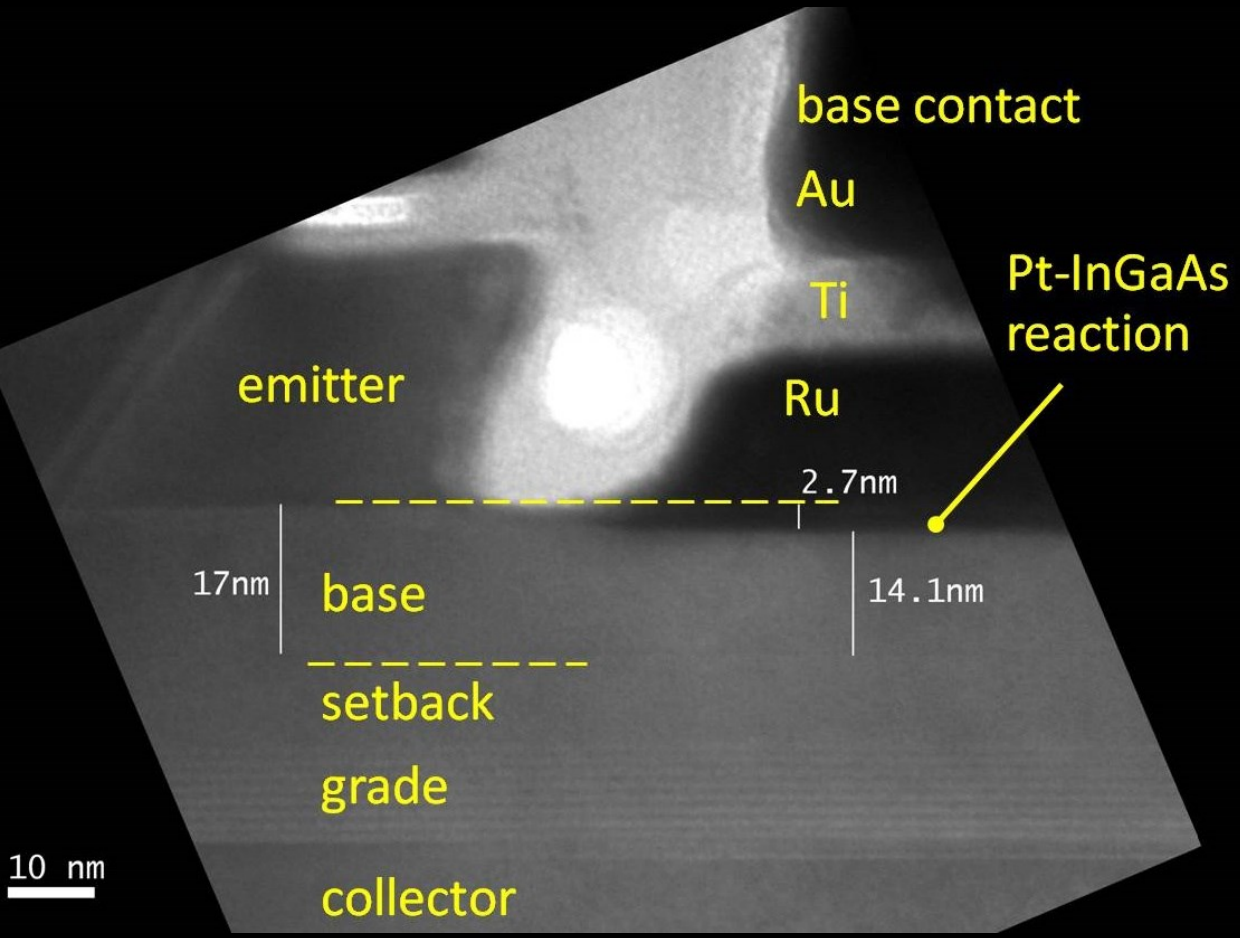
Effect of order of pad stripping

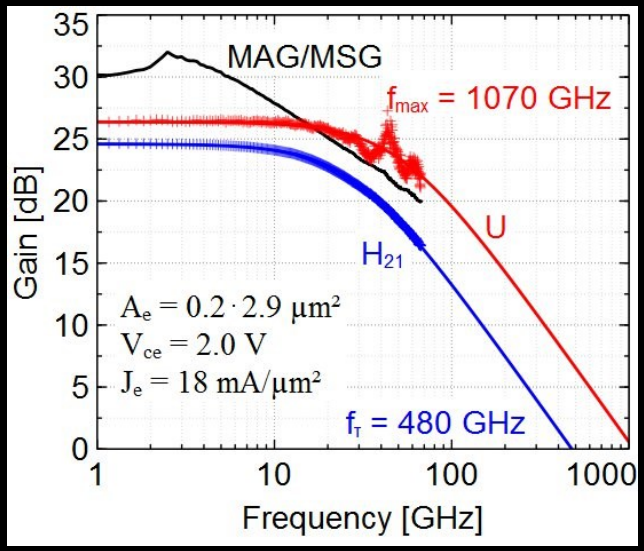


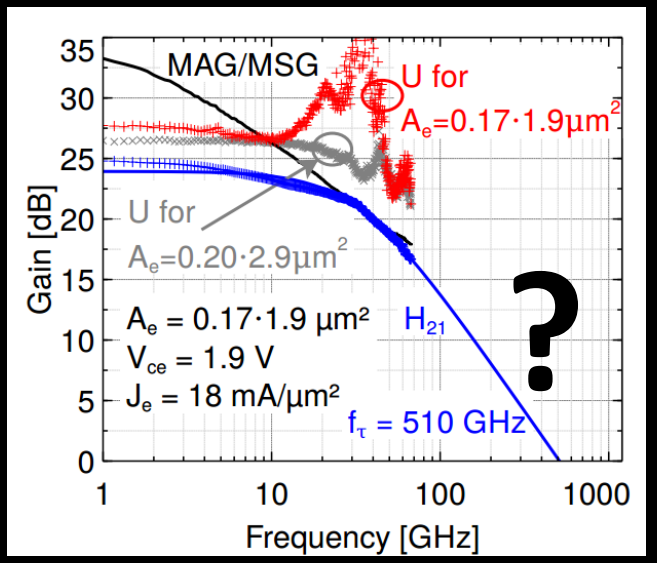
Effect of order of pad stripping



InP HBTs: 1.07 THz @200nm, ?? @ 130nm







Rode et al., IEEE TED, Aug. 2015