

# 185mW InP HBT Power Amplifier with 1 Octave Bandwidth (25-50GHz), 38% peak PAE at 44GHz and Chip Area of 276 x 672 $\mu\text{m}^2$

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**Abstract**— We report a 250nm InP HBT MMIC that demonstrates record output power at 44 GHz for its chip size, having a small signal bandwidth of 25 – 50 GHz, and operating from a 2.5-2.8 V supply. The reported power amplifier delivers up to 185 mW and has a peak PAE of 38% at 44 GHz. The results in this work highlight the relevance of 250nm InP HBT devices for emerging size-constrained platforms including MIMO communication front-ends and radar applications.

**Keywords**— SSPA, broadband PA, 250nm InP HBT, MIMO, high efficiency mm-Wave PA, bipolar MMIC, 5G.

## I. INTRODUCTION

The upcoming 5G standard will likely employ MIMO arrays that will contain several transceiver tiles, thus demanding a reduced component size at the array element due to the high carrier frequencies targeted (i.e., up to 60 GHz). The radiating element size reduction along with the high carrier frequency will also impose the requirement of relatively high efficiency on the power amplifier. Contending 5G technologies have demonstrated high efficiencies at limited bandwidths [1] – [10], or higher fractional bandwidths at the expense of power added efficiency [11] – [12]. While in general, bandwidth and efficiency are commonly accepted trade-offs, we note that the trade-off space arises from the significant transformation ratios that are sometimes required (the Bode-Fano limit quantifies this effect), as well as from the magnitude of the reactive element that must be tuned out when transforming to any real load.

InP HBT devices demonstrate significantly higher RF figures of merit for a given technology node (i.e., for 250nm-node HBTs,  $f_T/f_{MAX} \sim 350/600$  GHz) as well as the possibility of operating using a 2.5-3 V supply, enabling higher output power density as compared to CMOS or SiGe-based power amplifiers [13], higher efficiency with fewer gain stages [14] and an increased bandwidth as a result of the reduced parasitics [15]. In addition, they also offer the possibility of utilizing power cells with optimized fundamental impedance (50  $\Omega$ ) given the power levels required for several mmWave array applications (16-23 dBm).

In this work, we demonstrate a power amplifier chip designed using a very compact matching network approach that is optimized for the InP HBT wiring environment of choice. The amplifier small signal bandwidth is 25-50 GHz. At 44 GHz a saturated power of 185 mW was measured with an associated PAE of 36%, which is the highest reported for an amplifier covering over 1 octave of 3 dB bandwidth at mmWave

frequencies. In addition, the design is extremely compact, occupying a chip area of only 276 x 672  $\mu\text{m}^2$ , including all pads.

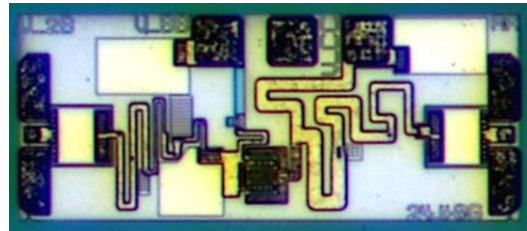


Fig. 1. Micrograph of reported 250nm InP HBT power amplifier. The chip dimensions are only 276 x 672  $\mu\text{m}^2$ .

## II. DESIGN METHODOLOGY

### A. 250nm InP HBT Technology

The HBT device technology used in this work is described in detail in [15]. For the amplifier MMIC design reported here, the HBT total emitter periphery was chosen to deliver up to ~23 dBm from a 2.8 V power supply, at a quiescent bias range of 3.2-5.2 mA/ $\mu\text{m}^2$ .

Owing to its high bandwidth, one key advantage of the 250nm InP HBT is its low effective output capacitance ( $\text{Imag}(Y_{2,2})/2\pi\text{freq}$ ). Fig. 2 illustrates the average HBT output capacitance simulated between 15-55 GHz, for a 30  $\mu\text{m}^2$  power cell, along a target loadline. Since the 250nm HBT technology can deliver around 1.5-2 W/mm of RF output power, and the output capacitance at the frequency band of interest is about 1.87 fF/ $\mu\text{m}$  of emitter periphery, to deliver ~200 mW of power we must tune out ~220 fF across the band.

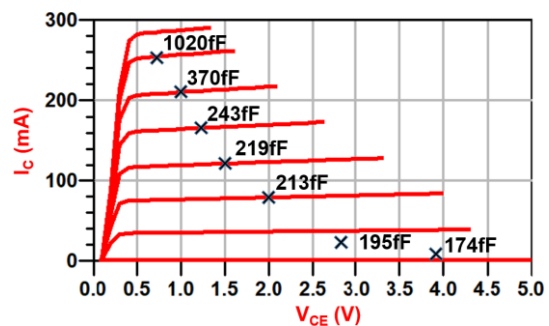


Fig. 2. Effective shunt capacitance modelled looking into the collector in common-emitter configuration, using the technology's Agilent HBT model.

## B. Amplifier Design

The reported amplifier is a one stage single cell in common emitter configuration. To ensure an adequate power match across the frequency band of interest, the optimum load impedance across the band was determined through load-pull simulations using Keysight ADS. Fig. 3 contains the optimum impedance ( $Z_{Opt}$ ) obtained from the simulations across the frequencies of interest, along with the simulated saturated power and associated efficiency.

We note that the optimum input impedance for the selected HBT device is  $\sim 1.8 \Omega$  - transforming such low impedance to the  $50 \Omega$  input requires a very high transformation ratio. We note that a two stage design would require a much lower input matching network transformation, since the input stage can be sized 1:3-1:4 of the second stage, thus greatly simplifying the input matching network design.

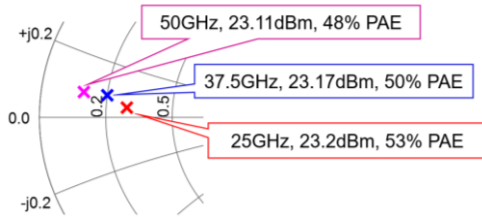


Fig. 3. Simulated optimum load impedances at 25 GHz, 37.5 GHz and 50 GHz, along with associated saturated power and peak PAE from load-pull simulations.

The fundamental load impedance of the device chosen is  $\sim 14 \Omega$ . In order to achieve the required power match to the  $50 \Omega$  load, the device's output impedance was gradually stepped to the load impedance using a hybrid-distributed/lumped multi-section approach. Fig. 4 includes a schematic of the PA reported in this work.

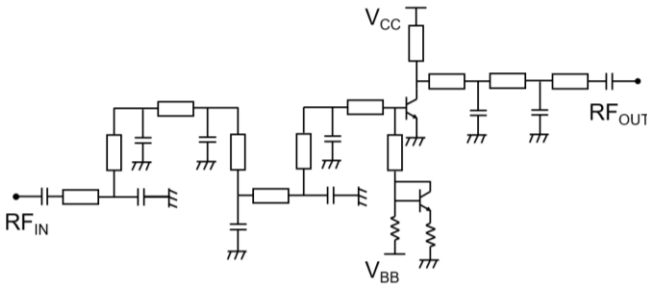


Fig. 4. Schematic of the fabricated power amplifier.

In addition, the HBT wiring environment is ideally suited for common emitter HBT topologies with negligible unwanted emitter degeneration, since it is possible to choose the ground plane on the metal level (M1) that directly connects to the device's emitter along its full length. Using this scheme, it is then possible to design the RF signal routing on a metal layer (M4) that is  $5 \mu\text{m}$  apart from the ground plane, both separated by BCB dielectric. Thus, we note that, since the signal to ground plane distance is  $5 \mu\text{m}$ , it is then feasible to meander transmission lines in a very compact manner, since it can be

verified through E-M simulations that only a spacing of about  $5\text{-}10 \mu\text{m}$  is required to avoid unwanted coupling between adjacent sections of matching network transmission lines.

## III. MEASUREMENT RESULTS

### C. Small Signal Measurements

The amplifier small signal response was measured on wafer, upon performing LRRM calibration to the probe tip using an impedance standard substrate. The two-port measurement was performed using a Keysight PNA-X N5242. The PA small signal response is included in Fig. 5 below, where it can be seen that the PA exhibits a little over an octave of 3 dB bandwidth. Reasonably good agreement between the simulated parameters and the measurement can be seen from Fig. 5.

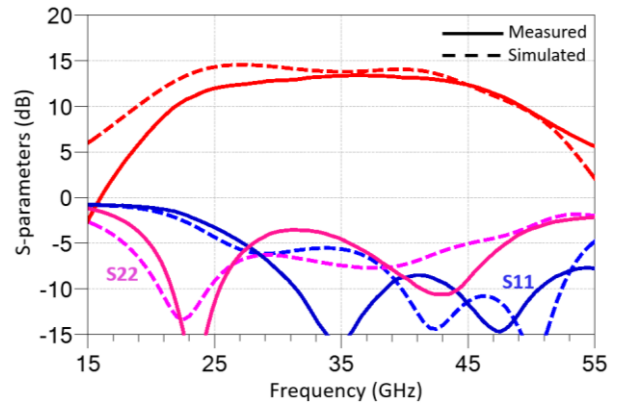


Fig. 5. PA small signal response at  $V_{CC}=2.8 \text{ V}$ ,  $V_{BB}=2.33 \text{ V}$  ( $I_{C,Q} = 142 \text{ mA}$ ).

### D. Power Measurement

The power performance was measured at 44 GHz, also on-wafer. During the power measurement, the MMIC is on a full thickness InP substrate that has a thickness of  $630 \mu\text{m}$ . For the power measurement, a Keysight PNA-X N5242 analyzer was used along with a Quinstar pre-driver in order to saturate the PA. The waves reflected off the DUT input were measured, thus enabling the calculation of the power delivered to the DUT ( $P_{in,del}$  in Fig. 6 below). A saturated power of 185 mW was achieved with an associated PAE of 36%, which compares very favourably to prior art (Table 1).

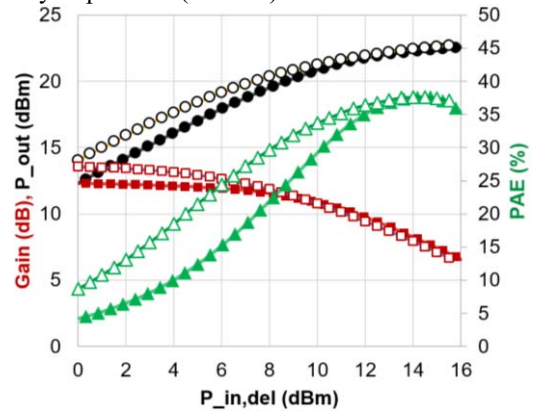


Fig. 6. Measured power sweep at 44 GHz, at  $V_{CC}=2.8 \text{ V}$  and  $V_{BB}=2.33 \text{ V}$  ( $I_{C,Q}=142 \text{ mA}$ ), plotted alongside simulations (traces with empty symbols correspond to simulated performance).

#### IV. CONCLUSION

We have reported a very compact 25 – 50 GHz design using 250nm InP HBT devices. The reported PA delivers record RF power density per unit chip area (1 W/mm<sup>2</sup>) with high efficiency, highlighting the suitability of the InP HBT technology for compact, high efficiency designs for platforms where size is a critical factor.

Table 1. Comparison of the results obtained in this work to prior art.

Ref.	Comparison to Prior Art					
	Freq. (GHz)	Gain (dB)	PSAT (dBm)	PAE (%)	Chip Size (μm <sup>2</sup> )	Power/A <sub>chip</sub> (Watts/mm <sup>2</sup> )
[5]	41	8.9	21.6	25.1	500 x 600	0.48
[6]	42	7	21.8	25	1000 x 2000	0.076
[7]	43	20.8	16.6	24.2	280 x 570**	0.29
[8]	40.5	18	18	43	600 x 950	0.11
[9]	45	10.5	20.2	31.5	740 x 1700	0.083
<b>This Work</b>	<b>44</b>	<b>12.4</b>	<b>22.67</b>	<b>38</b>	<b>276 x 672</b>	<b>1.0</b>

\*\*Does not include all pads

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