# A Broadband Direct Conversion Transmitter/Receiver at D-band Using CMOS 22nm FDSOI

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*Abstract*—**This paper presents a broadband transmitter and receiver at D-band (from 123 to 146GHz) using 22nm FDSOI technology. The direct conversion receiver is implemented with a wideband fully differential LNA at the front end, using a cross coupled pair with capacitive neutralization, followed by a linear double balanced passive mixer and broadband pseudo-differential transimpedance amplifier. The direct conversion transmitter starts with an active double balanced Gilbert cell, followed by a driver amplifier. A 9:1 frequency multiplier circuit realized by two successive tripler stages provides the on-chip 135GHz Local Oscillator (LO) signal for both the Tx and Rx chains. The receiver conversion gain is 27dB with a 20GHz 3-dB bandwidth, and the P1-dB is -30dBm. The transmitter saturated output power is 2.8 dBm. Tx and Rx chains consume 196mW and 198mW respectively from a supply voltage of 0.8V.**

*Keywords*— **Broadband Transceiver, mm-wave integrated circuits, Direct conversion, capacitive neutralization, 22nm FDSOI, transimpedance amplifier, mm-wave transceivers, D-band transceivers.**

## I. INTRODUCTION

The rapidly emerging wave of wireless data services demands high data rate wireless links. The large available spectrum at mm-wave frequencies enables the implementation of high speed and broadband transceivers. The advance in silicon-based radio frequency integrated circuits (RFIC) enable the implementation of low cost, small form factor and low power transceivers at mm-Wave frequencies using low cost CMOS technology. Several designs have been reported at mm-wave frequency band [1][2].

In this paper, a broadband single channel transmitter and receiver at D-band are presented. These designed to serve within 135GHz MIMO transceiver arrays, hence the baseband (I, Q) transmitter input and receiver output signals will be linear superpositions of data streams which must be subsequently separated by a baseband beamformer.

A broadband LNA/PA is designed using cross coupled pairs with capacitive neutralization, and the inter-stage matching networks are stagger-tuned to realize a broadband design. A wideband pseudo-differential transimpedance amplifier (TIA), with a 20GHz 3-dB-bandwidth, is used as a baseband amplifier in the receiver chain. On-wafer characterization for the transmit and receive channels is presented in terms of the conversion gains, 3-dB bandwidth, 1-dB compression points and transmitter saturated output power.

## II. TECHNOLOGY AND TRANSISTOR FOOTPRINT

The single-channel transmitter and receiver are designed using Global Foundries 22nm-FDSOI technology. The reported power gain cut-off frequency ($f_{max}$) and current gain cut-off frequency ($f_t$) for this technology are 230GHz and 240GHz, respectively, both referenced to the top metal layer [3]. The stack used provides 10 metal layers. The footprint of the core device used in this design is based on a super-low threshold voltage ($V_t$) NMOS with 32 fingers. The gate finger pitch is increased 2:1 above minimum to reduce $C_{ds}$ and $C_{gs}$ and to allow the placement of sufficient vias to satisfy electro-migration limits, when operating at 0.3mA/μm at $110^0$ C. Both the drain and gate are routed up to the top metal layer. The source is directly connected to ground through the lower 4 metal layers to reduce the source inductance.

## III. RECEIVER ARCHITECTURE AND BUILDING BLOCK

A direct conversion receiver (Fig. 1) consists of a 4-stage broadband LNA and a double balanced passive mixer, followed by a pseudo differential wideband transimpedance amplifier, for both in-phase (I) and quadrature phases (Q). The mixer is driven by an on-chip LO multiplier (x9), where the LO input signal is driven from external source with -3dBm input power at ~15GHz. The (I, Q) LO signals are generated by adding a (λ/4) delay line in the LO signal path, introducing a $90^0$ phase shift.
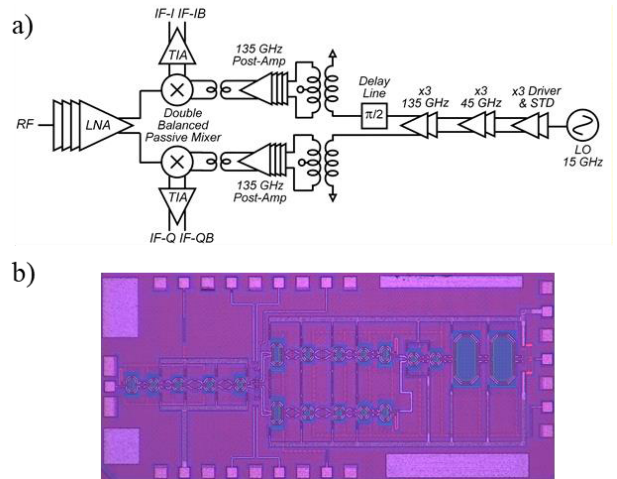


Fig. 1. D-band single-channel direct conversion receiver (a) circuit block diagram and (b) chip micrograph. The die area is 1.9mm x 0.76mm including pads.

### A. D-band LNA/PA

A 4-stage fully differential common source LNA (Fig. 2) is designed using a cross coupled pair with capacitive neutralization to boost the maximum available gain. The neutralization uses alternate polarity metal-oxide-metal
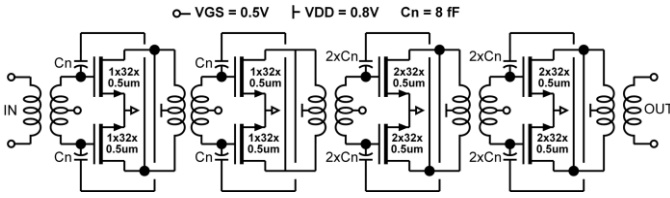
Fig. 2. Circuit diagram of a 4-stage broadband LNA/PA using staggered tuning.

(APMOM) capacitor. A center tapped transformer converts the single-ended input to a differential signal. Transformer center-taps provide DC bias feeds. For broad bandwidth, tuning of the inter-stage matching networks is staggered in frequency. The transformers use the top two wiring layers and were simulated using Keysight Momentum.

We designed this amplifier to be used as an LNA in the Rx chain and as a PA in the Tx chain, so the first stage device sizing was chosen to fulfil minimum noise figure. However, we increased the last two stages device sizing to increase the saturated output power. This LNA/PA draws 55 mA from a 0.8V supply, with a simulated gain of 16-dB and 40GHz 3-dB bandwidth. The simulated noise figure (NF) is 8.5dB.
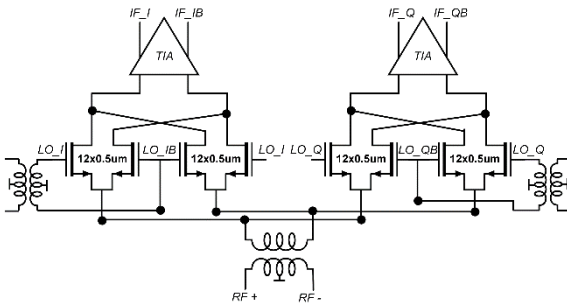
*B. Down Conversion Mixer*



Fig. 3. Circuit diagram of the (I/Q) down conversion mixer, followed by TIA.

A pair of double balanced passive mixers (Fig. 3) down-convert the D-band signal to (I, Q) baseband. The differential output of the LNA ($RF^+$ and $RF^-$) drives both mixer inputs through a transformer, the quadrature (I, Q) LO signals are converted to differential form by transformers before driving the FET mixer gates, and the baseband (I, Q) mixer outputs are DC-coupled to transimpedance amplifiers. To ensure sufficient LO drive power, the outputs of the LO multiplier are passed through a 4-stage post-amplifier before driving the mixer LO ports (Fig. 1a).
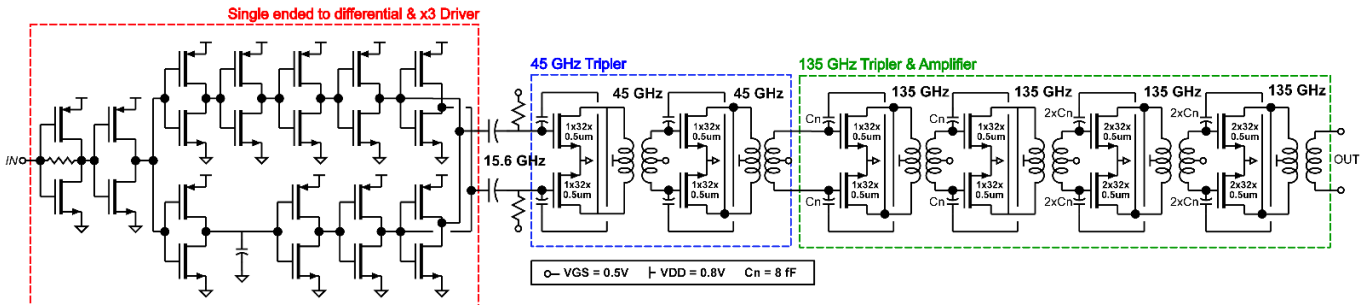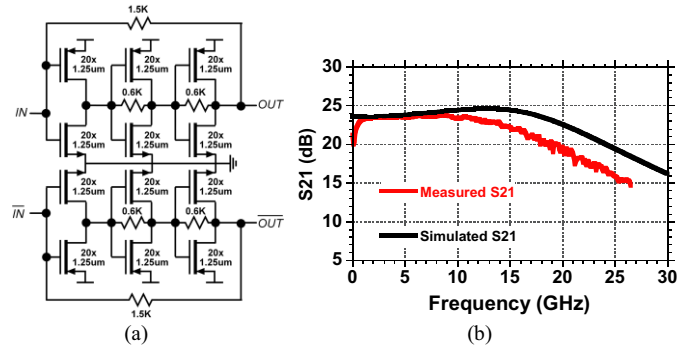


Fig. 4. Broadband TIA (a) circuit diagram of pseudo-differential TIA (b) simulation vs. measurement for single ended TIA test structure.

*C. Broadband Transimpedance Amplifier*

A pseudo-differential transimpedance amplifier provides the receivers' baseband gain. A three-stage voltage amplifier is first formed by an input $g_m$ stage cascaded with two voltage-gain stages formed from $g_m$ cells with local resistive feedback; adding global shunt resistive feedback forms a transimpedance amplifier (Fig. 4a). A test structure for a single ended TIA was measured. Fig. 4b shows the agreement in (S21) gain between simulation and measurement. There is some discrepancy in the 3-dB bandwidth between simulation (22GHz) and measurement (17GHz), which may be due to errors in parasitic extraction. The measured S-parameters shows a notch at DC, this is because the test structure is a single ended, and the supply capacitance in the test structure resonates with the DC supply probe inductance. In the Rx chain, the design is less sensitive to supply inductance, as the design is pseudo-differential.

*D. Frequency Multiplier Circuit and 135 GHz LO Generation*

Both transmitter and receiver employ a 9:1 frequency multiplier to generate a 135GHz LO signal; using an external reference at 15GHz with -3dBm input power. The multiplier design consists of an inverter-based single ended to differential (STD) converter, followed by two cascaded 3:1 frequency multipliers (Fig. 5). A fully differential structure reduces even harmonic generation and reduces supply coupling. The x3 frequency multipliers use a cross coupled pairs with capacitive neutralization, these driven into saturation to generate the third harmonic. The output of the first x3 multiplier is tuned at 45GHz (3rd harmonic of the input signal at 15GHz), while the second x3 multiplier is tuned at 135GHz. The topology and element values within the second 3:1 frequency multiplier are



Fig. 5. Circuit schematic of the 135GHz 9:1 LO frequency multiplier.

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similar to those of the LNA/PA stages. The supply voltage of the entire chain is 0.8V. The simulated saturated output power is 3dBm and the simulated 3-dB bandwidth is 27GHz.

## IV. TRANSMITTER ARCHITECTURE AND BUILDING BLOCK

In the direct conversion transmitter (Fig. 6), a pair of double-balanced Gilbert-cell mixers upconverts the (I, Q) baseband signals to D-band. The (I, Q) signals are then summed and drive a broadband power amplifier. The LO multiplier is the same as that in the receiver.
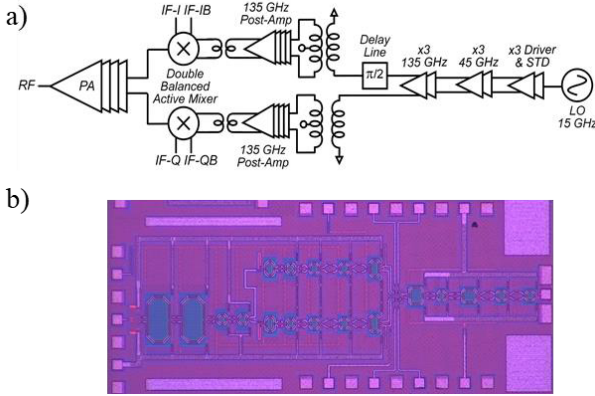


Fig. 6.  D-band single channel direct conversion transmitter (a) circuit block diagram (b) chip micrograph, including pads. The die area is 1.9mm x 0.76mm.

### A.  IQ modulator

A pair of Gilbert cells serve as the IQ modulator (Fig. 7). The baseband inputs are DC coupled, while the LO and RF output ports are transformer-coupled. Tail bias (BIAS) of 0.35V, was chosen to maximize the modulator gain and output power (-10dBm in simulation).
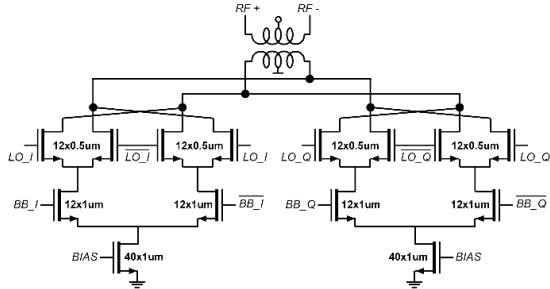


Fig. 7. IQ modulator using Gilbert cells. The (I, Q) LO ports are transformer-coupled.

## V.  MEASUREMENT RESULTS

Transmitter and receiver channels are fully characterized using on wafer probing. The receiver conversion gain is measured using Virginia diodes AMC 333 as the input signal source, followed by GGB (90-140 GHz) probe, to excite receiver input port. The two differential outputs are terminated by 50Ω impedances during measurement.

Fig. 8a shows the measured conversion gain with LO signal fixed at 134GHz and 135GHz, while the input signal is swept from 122GHz to 155GHz. This measures the receiver modulation bandwidth. The measured gain is 27dB, after de-

embedding probe loses and correcting for single ended to differential conversion. The 3-dB bandwidth is 20GHz. There is a good agreement between the measured and simulated gain. However, the simulated 3-dB BW is 1.5:1 larger than the measured, which might be explained as inaccuracy in apmom capacitor modelling in EM simulations. Fig. 8b shows the frequency dependent conversion gain, with a fixed baseband frequency, where the RF and LO signals are swept to keep the baseband frequency fixed at either 1GHz or 100MHz. This measures the receiver RF tuning range. The 3-dB bandwidth here is limited to 10GHz; the smaller bandwidth than in the prior measurement reflects the tuning range of the LO source.

Receiver 1-dB compression point is measured (Fig. 9) at different LO frequencies. The measured input $P_{1dB}$ is -30dBm, which is slightly smaller than the simulated -26dBm. The receiver compression point is limited by the TIA drive capability, as this stage drives 50Ω.
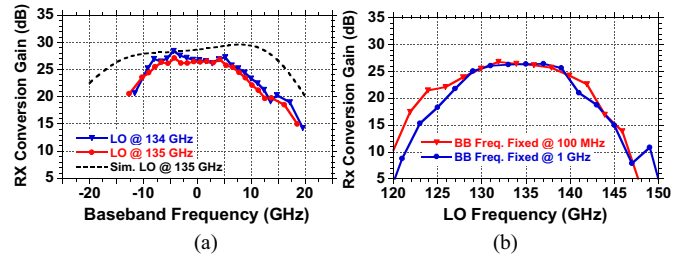


(a)                              (b)

Fig. 8. a) Receiver conversion gain vs. baseband frequency with a fixed LO frequency (b) Receiver conversion gain vs. LO frequency with fixed baseband frequency.
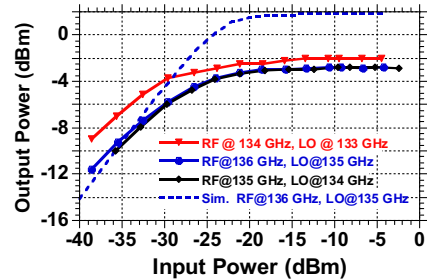


Fig. 9. Receiver normalized output power vs. input power.

Transmitter saturated output power is measured using Erickson PM4 power meter, where external signal generators drive the I and Q mixer inputs.  To determine the transmitter saturated output power as a function of frequency, the transmitter was first driven by -3 dBm signals at 1, 2, or 5GHz at the (I, Q) ports, and the LO was swept from 125GHz to 145GHz (Fig. 10a). The saturated output power is 2.8dBm with a 3-dB bandwidth of 8 GHz. This determines the trasmitter frequency tuning range. Fig. 10b shows the normalized modulation sideband power with the baseband input frequency swept and the LO frequency held fixed. This measures the transmitter modulation response. The output spectrum was measured using an OML M05HWD harmonic mixer and a Rohde & Schwarz spectrum analyzer. There is a good agreement between the simulated and measured 3-dB bandwidth. Fig. 11a shows the gain compression characteristics as a function of carrier frequency. This particular measurement
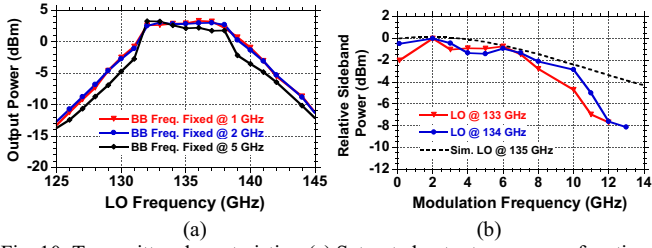
Fig. 10. Transmitter characteristics. (a) Saturated output power as a function of carrier frequency, with a -3 dBm baseband input signal, this showing an 8 GHz RF tuning range. (b) Modulation sideband power as a function of modulation frequency, this showing a ~8GHz (SSB) modulation bandwidth.
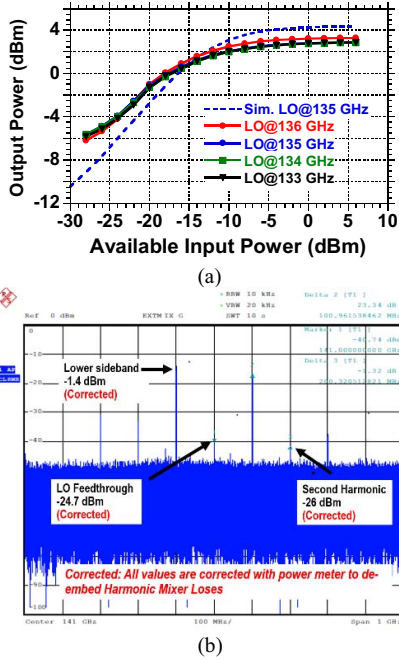


(a)



(b)

Fig. 11 (a) Transmitter output power as a function of input power, showing a typical 18dB gain (b) Transmitter output spectrum with center frequency 141GHz and 100MHz input signal.

shows approximately -7dBm LO leakage, because of incorrectly set DC levels at the transmitter baseband input ports. Fig. 11b shows the transmitter output spectrum with a 141GHz LO, a -6dBm 100 MHz input to the baseband I port, and only DC bias input to the baseband Q port, this producing I-phase but not Q-phase output modulation. With correct input DC levels (Fig. 11b), LO suppression is 23dB. The second harmonic is supressed by 24dB relative to the fundamental output signal.

## VI. CONCLUSION

A broadband single-channel transmitter and receiver at D-band using CMOS 22nm FDSOI are demonstrated. Conversion gain of the entire receive channel is 27dB with a 3-dB bandwidth of 20GHz. The transmitter shows conversion gain of 18dB with a saturated output power of 2.8dBm. The transmitter and receiver consumes 196mW, and 198mW respectively from a 0.8V supply, both dominated by the 137mW LO multiplier DC power consumption. The transmitter and receiver both have bandwidth sufficient for 10 GBaud transmission.

A comparison to the state of the art transceivers at D-band is shown in Table 1. To the best of author's knowledge, this is the first sub-mm-Wave transmit/receive chain using 22nm FDSOI with the lowest supply voltage (0.8V) and highest bandwidth at the D-band.

Table 1. Comparison between state-of-the-art designs for near-140GHz transceivers.

|  | [4] | [5] | [6] | [7] | **This Work** |
|---|---|---|---|---|---|
| **Technology** | 28nm CMOS | 45nm CMOS | 40nm SOI-CMOS | 40nm CMOS | 22nm SOI-CMOS |
| **Frequency (GHz)** | 102-128 | 140 | 155 | 118 | 135 |
| **Conversion Gain (dB)** | 36-38 | 18 Rx - Tx | 23 Rx - Tx | 13 Tx | 27 Rx 18 Tx |
| **3dB Band-width (GHz)** | 18 Rx | 12 Rx 8 Tx$^{\$\$}$ | 9 Rx - Tx | 14 Tx | 20 Rx 8 Tx$^{\$\$}$ |
| **NF (dB)** | 8.4-10.4 | 5.5* | 20* | - | 8.5* |
| **Pdc (mW)** | 51 | 125 Rx 120 Tx | 345 Tx/Rx | 271 | 198 Rx 196 Tx |
| **Tx Psat (dBm)** | NA | -2 | -10 | 4.5 | 2.8 |
| **Integration** | Rx | Tx/Rx | Tx/Rx | Tx | Tx/Rx |

*simulated, $\$\$$single sideband

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