

A W-Band transmitter channel with 16dBm output power and a receiver channel with 58.6mW DC power consumption using heterogeneously integrated InP HBT and Si CMOS technologies

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Abstract—We report a high output power transmitter and a low DC power receiver front-end channels of a phased array transceiver, designed in heterogeneously integrated 250 nm InP HBT and 130 nm Si CMOS technologies. The transmitter channel consists of a variable gain amplifier, an IQ-vector-modulator-based phase shifter, and a power amplifier. External Analog control signals are used to adjust the phase shifter and VGA states. The transmitter has a saturated output power of 16dBm at 90GHz while consuming 885mW DC power. The receiver channel uses a low noise amplifier with a similar phase shifter, and a variable gain amplifier. 4-bit DACs are implemented in the CMOS to control the phase shifter and VGA. The overall the receiver channel has ~26dB small signal gain at 58.6 mW DC power dissipation. The areas of the transmitter and receiver channels are 2.7x0.81mm² and 2.1x0.76mm² respectively.

Keywords—mm-wave, stacked power amplifier, DAHI, high output power, phased array, vector modulation, phase shifter.

I. INTRODUCTION

Integration between advanced CMOS technology nodes with compound semiconductor (CS) technologies attracts many applications [1]. CMOS supports high-density, low-power logic circuits with low cost fabrication. While CS is typically used for high performance circuits at high frequencies due to higher output power capability and better passive components. The integration between heterogenous modules can be done after packaging by 3D technologies, wire bonds or flip chip [2]. However, mm-wave packaging becomes more challenging at higher frequencies which increases the cost and complexity. In the DARPA Diverse Accessible Heterogeneous Integration (DAHI) program, Teledyne 250nm InP HBT process is integrated with GlobalFoundries 130nm CMOS process using 3D wafer stacking process. This way, high-density and low-cost CMOS technology can be used in low-power circuits, and CS can be used to design high performance mm-wave blocks including power amplifiers with high saturated output power.

Here we report a W-band high output power phased array transmit and a low power receive channels. Millimeter wave design challenges and methodologies in the technology are discussed. The transmitter exploits the wiring stack of both InP and CMOS but uses only the active devices in the InP. The transmitter consists of stacked power amplifier, active phase shifters, and a variable gain amplifier (VGA). The VGA and phase shifter control signals are adjusted by external control signals. The transmitter consumes 0.88W DC power and produces 13.3-16dBm saturated output power in the 90-96GHz

frequency band, has an area of 2.7x0.81mm² including the pads. The gain reaches 19dB at the maximum control signals for the phase shifter and mid-gain setting for the VGA.

InP and CMOS wiring stacks are used in the receiver design. Bipolar transistors (InP) are used in the main RF blocks and MOSFET devices (CMOS) are used for the control signals. The receiver uses an inductive degeneration common emitter stage for the LNA followed by gain stages, a phase shifter and a VGA. The architectures for the phase shifter and VGA are identical to the transmitter except that the supply voltage is dropped from 2V to 1.5V to reduce the DC power consumption. The receiver DC power consumption is only 58.6mW and has an area of 2.1x0.76mm². The receiver maximum gain is 26dB with an input referred 1dB compression point of at least -29dBm from 92-96GHz. To verify the heterogenous process, 4-bit DACs are designed in the CMOS to provide the necessary control signals for the VGA and phase shifter designed in the InP.

II. TECHNOLOGY OVERVIEW

The heterogenous integration process and cross section of the wiring stack (Fig. 1) could be found in [3]. The Teledyne InP process offers three Au interconnect layers for routing, 0.3fF/ μm^2 MIM capacitors and 50 Ω /square thin film resistors. The HBT has a maximum power gain cut-off frequency (f_{max}) of 650GHz and the HBTs BV_{CEO} is 4.5V. The 130nm CMOS process has 6 metal layers, and MIM capacitors. The integration between the CMOS and the InP is done using Direct Bond Interfaces (DBIs). Octagonal structures (2.5 μm in the diameter) are necessary for the bonding process and must be added to the whole chip at 5 μm pitch.

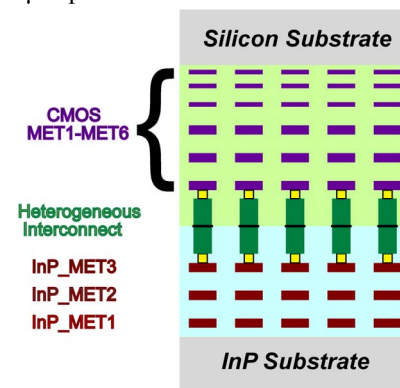


Fig. 1. Simplified cross section of integrated InP/Si CMOS technology

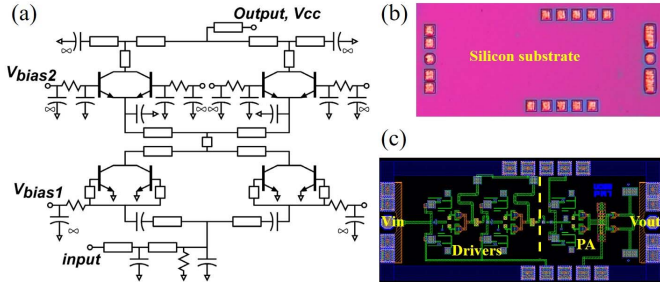


Fig. 2. (a) Schematic diagram of the stacked PA. All transistors are two-finger devices each $5\mu\text{m}$ emitter length. (b) Chip micrograph (only shows the bottom of the silicon substrate and the pads) (c) PA layout ($1.5\text{mm}\times 0.65\text{mm}$ with pads).

III. TX BUILDING BLOCKS AND MEASUREMENT RESULTS

A. Power Amplifier

The wiring stack poses a challenge in the mm-wave design. The signal lines can be routed using the first layer of the InP (InP_MET1) and the third layer (InP_MET3) can serve as a ground plane (inverted microstrip). However, the distance between those layers is only $3\mu\text{m}$. High impedance transmission lines then require very narrow conductors, which results in high skin-effect losses and limits and low maximum current. In our designs, the microstrip ground plane is within the CMOS IC (MET5 and MET6) while the microstrip signal lines are in the InP IC (InP_MET1). This increases the distance between the signal and ground to $\sim 10\mu\text{m}$, thereby reducing transmission-line losses. However, the copper heterogenous interconnects then lie between the microstrip signal line and ground plane. This complex electromagnetic structure must be modeled by electromagnetic simulation; for this, we use Ansoft HFSS. Further, the line losses are increased compared to a microstrip line which does not have the heterogenous interconnects within the field region of the microstrip lines.

Given the high transmission-line losses in this technology, the power amplifiers using series-connected topologies [4] shows high output power with compact matching circuits with minimal transmission-line lengths.

Fig. 2a shows a power amplifier with 2:1 series connection. Each transistor has two cells each has 4 fingers with $5\mu\text{m}$ emitter length per finger. All the matching circuits are designed using the procedures in [4] to guarantee uniform voltages and current distribution across the stack. The transistor capacitance is tuned by short sections of microstrip TL terminated by bypass capacitors. Transmission line network derived from EM simulations combines the output of eight fingers and ensure the proper load lines.

The bases of the input stage are combined and matched to 50Ω . Current mirrors are used to obtain the required DC current. DC feed lines are routed using the CMOS metal stack above the ground plane. This simplifies the routing and reduces the coupling between the DC and RF signal lines. Two driver stages are added to relax the input power requirements. The core of the driver is similar to the input stage of the PA. The output and input are DC decoupled and matched to 50Ω .

S-parameters were measured using HP vector network analyzer with Oleson 75-110GHz frequency extenders and

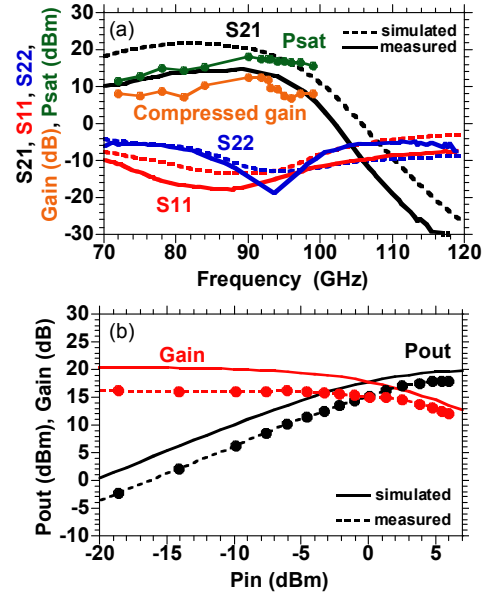


Fig. 3. (a) PA measured and simulated S-parameters, measured output power and compressed gain versus frequency. (b) Measured output power and gain at 90GHz.

GGB probes. Calibration used LRRM standards on an external Cascade substrate to move the reference plane to the probe tips. Large signal characteristics were measured on-wafer using VDI-90GHz driven by microwave synthesizers, GGB 75-110GHz probes and Agilent waveguide power sensor (W8486A). The probe losses were determined by a probe-probe through measurement. Same measurement setups for the S-parameters and power measurement are used to characterize all building blocks in the paper.

Fig. 2b shows the chip micrograph. The photo shows only the silicon substrate and probe pads. The layout (Fig. 2c) shows the details of the circuits. The PA is biased at ($V_{CC}=5\text{V}$, $V_{CB}=3.8\text{V}$, $V_{CE}=1.67$, and $I_{CC}=75\text{mA}$) while the drivers is biased at ($V_{CC}=3\text{V}$, $I_{CC}=77.5\text{mA}$ for each stage). Fig. 3a shows the simulation and measured S-parameters of the PA with two drivers. The amplifier has a peak gain (S21) of 15dB at 90GHz and the 3dB bandwidth extends from 75GHz to 95GHz. There is good agreement between the simulated and measured reflection coefficients. However, the measured gain is lower than the simulation. It has been observed that common emitter transistors show significantly lower gain compared to the simulation. Breakout of the drivers shows that the gain is well below the simulation which limit the gain of the PA. The PA is biased similar to the S-parameter measurements has an 18dBm saturated output power at 12.6dB compressed gain (Fig. 3b) while dissipating 930mW. Fig. 3a shows the output power and the corresponding compressed gain vs frequency. The output power is at least 15dBm from 78GHz up to 99GHz.

B. Variable gain amplifier

Common base topology is used in the VGA (Fig. 4b). The emitters of the two single-finger transistors ($5\mu\text{m}$ emitter length each) are tied together. The total DC current is kept constant by adding a dummy branch. This preserves approximately the

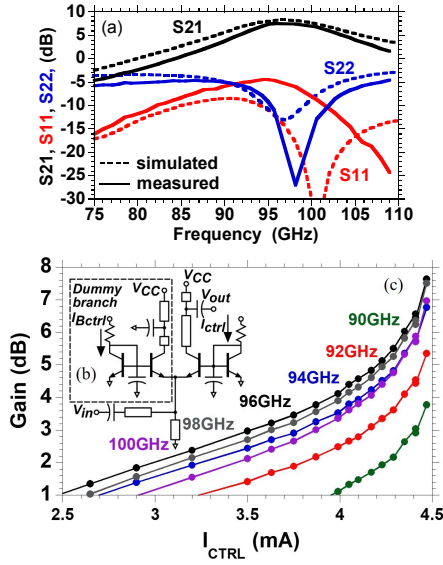


Fig. 4. (a) measured and simulated S-parameters (b) schematic diagram (c) gain versus the control current at different frequencies for the VGA

same input impedance at different control signals. The gain decreases by decreasing the current in the main path while increasing the current in the dummy path. Current mirrors are used to precisely set the required bias current. The collectors are biased at 2V with a constant total current of 8.8mA. There is good agreement in the simulated and measured S- parameters (Fig. 4a). Fig. 4c shows the gain versus the control current at different frequencies. The VGA has an area of 1mm×0.8mm.

C. Phase shifter

An active phase shifter (Fig. 5a) is used to get reasonable insertion loss [5]. A sub-quarter wavelength balun is used to convert a single ended signal to a differential one. A quarter wave length line is added to generate the Q path. The outputs of those baluns go to the Gilbert cell-based vector modulator. Similar baluns are used with the necessary matching circuits to combine the output and convert it to single ended output again. External current sources are used for the control signal in the Tx. To verify the heterogeneous integration, 4-bit binary weighted current DACs (Fig. 5b) are designed in CMOS. pmos3.3V transistor models are used with 0.5μm finger length for the mirroring transistors and 0.3μm for the switches. The reference current is defined by the supply and the reference resistance (R_{ref}) The DACs provide the necessary controls for the phase shifter and VGA in the receiver channel.

D. Transmitter measurement results

The Tx (Fig. 6b) consists of VGA followed by gain stage, phase shifter, gain stages and PA stage. The chip layout is shown in Fig. 6a. The bias conditions for the transmitter blocks are: VGA ($V_{CC}=2V$, $I_{CC}=5mA$), phase shifter ($V_{CC}=2V$, $I_{CC}=12mA$), Drivers ($V_{CC}=3V$, $I_{CC}=152mA$), and PA ($V_{CC}=5V$, $V_{Bias2}=3.8V$, $V_{Bias1}=1.54V$, $I_{CC}=65mA$). Fig. 7c shows the measured S-parameters at 98GHz under different external control signals for the phase shifter with the mid-gain setting of the VGA. Fig. 7b shows the output phase variation from -180°

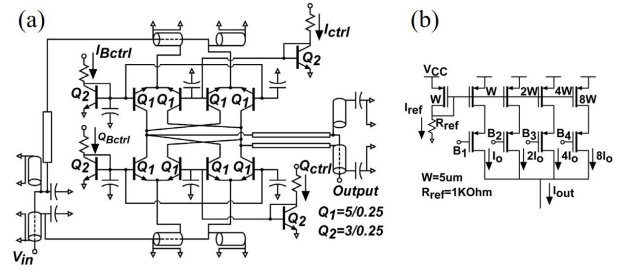


Fig. 5. Schematic diagram of (a) the phase shifter (b) 4-bit DAC

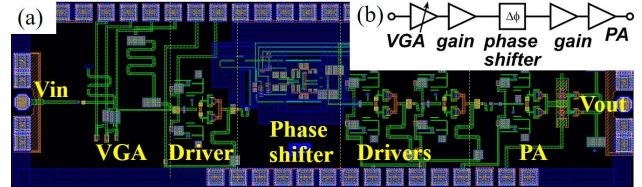


Fig. 6. Transmitter (a) Layout (2.7mm×0.81mm with pads) (b) block diagram

to 180° and the corresponding gain variations are shown in Fig. 7a. Further gain correction could be done using the VGA. The transmitter channel has ~13-16dBm output power from 90 GHz to 97.2GHz (Fig.7d).

IV. RECEIVER DESIGN AND MEASUREMENT RESULTS

The receiver (Fig. 8c) consists of LNA, phase shifter, and VGA. The chip layout is shown in Fig. 8b. The LNA (Fig. 8a) uses a common emitter (CE) with inductor degeneration in the first stage to achieve simultaneous noise and gain matching. Three more CE stages without inductor degeneration are added to further increase the gain. A 5μm emitter finger length is used in the all stages to reduce the DC power consumption. InP_MET1 is used as a signal line where the ground lies in the CMOS top metal layer. The same architectures for the phase shifter and VGA are used in the receiver channel as well. However, the bias condition is changed to reduce the DC power consumption.

Single collector bias (V_{CC}) of 1.5V is used for the receive channel (LNA, phase shifter, VGA). The total collector currents are 16mA, 12mA, and 5mA for the LNA, phase shifter, and VGA respectively. 4-bit DACs designed in the CMOS are used provide the control signals for the phase shifter and VGA. Fig.9c shows the measured receiver S-parameters at 16 DAC states (I_{CTRL} and Q_{CTRL}) for the phase shifter with mid-gain setting for the VGA. The phase varies from -180° to +180° (Fig. 9b) and the corresponding gain variation is shown in (Fig. 9a) which can be corrected using the VGA. The receive channel has an input referred 1dB compression point of ~-28.5dBm from 90-98GHz as shown in Fig. 9d. The noise figure is measured using a Micronetics NSI-9095W noise source and external down conversion mixer connected to N9030B Signal Analyzer (SA) with the system downconverter option. Measured NF is less than 11.6dB from 90-95GHz (Fig. 9d) which is ~3dB higher than the simulation due to the extra losses. The measured gain from the SA matches well to the measured gain from power measurements and small signal measurements.

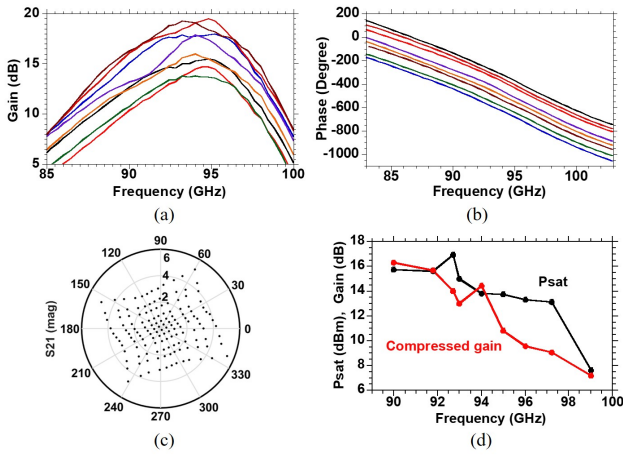


Fig. 7. Transmitter a) measured small signal gain and (b) measured small signal phase at selected control signal vs. frequency (c) measured S-parameters at 98GHz under different control signals ($I_{ctrl}, Q_{ctrl} = [0, 0.2 \dots 1.8 \text{mA}]$) d) Measured output power and compressed gain vs. frequency.

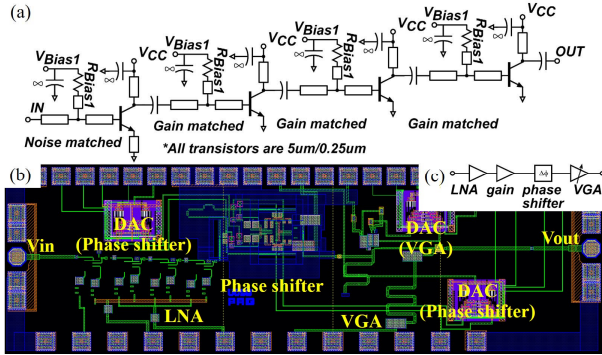


Fig. 8. (a) LNA schematic (b) receiver layout (2.1mm×0.76mm with the pads) (c) receiver block diagram

V. CONCLUSION

Heterogeneous integration of 250 nm InP and 130 nm CMOS technologies combines the advantages of the high-density silicon technology with the high performance HBT devices. This paper presents the mm-wave design challenges and solutions using this technology. A high output power W-band transmitter channel and a low DC power receiver channel for phased array systems have been demonstrated. To the best of author's knowledge, this is the first demonstration of a W-band phased array transmit and receive channels with 16 dBm output power using heterogeneous integration platform. Table 1 summarize the state-of-the art W-band transceiver. This work shows a significant improvement of the saturated output power.

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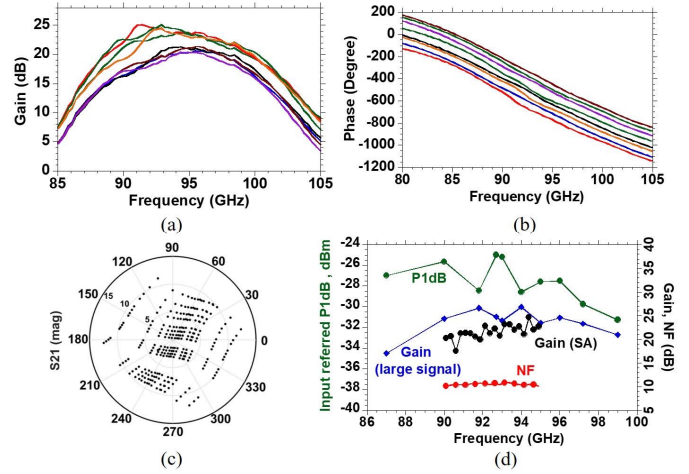


Fig. 9. Receiver a) measured small signal and b) measured small signal phase gain at selected control signal vs. frequency (c) measured S-parameters at 98GHz under different DAC setting for the phase shifter d) measured input referred 1dB compression point and corresponding gain vs. frequency.

Table 1. Comparison of the state of the art W-band transceivers

	[7]	[6]	[5]	This work
Frequency, GHz	84-102 (Tx) 90-102 (Rx)	88-96	92-98	94-98
Tx Psat (dBm)	-5	>2	5	16
Tx Gain (dB)	13	>25	22	19
Tx DC power (mW)	2200*	116	40	885
Rx Gain (dB)	22-25	30	21	26
Rx NF (dB)	10-11	8.5	<9.3	<11.6
Rx DC power (mW)	2200*	160	39	58.6
Technology	SiGe BiCMOS	SiGe BiCMOS	130nm InP HBT	InP/130nm CMOS

* power for the whole chip

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