A High-Efficiency 120-mW InP HBT Power Amplifier with 37% - 46% Peak PAE at Q-band

***Abstract*— A high-efficiency 250-nm InP HBT power amplifier (PA) that demonstrates record collector efficiency (54%) and PAE (46%) at 47 GHz is presented. The reported PA delivers up to ~120 mW at 47 GHz, and it is reactively tuned for high PAE using a multi-section hybrid distributed-lumped matching network. The results in this work constitute the highest PAE reported at 47 GHz for a PA while operating from a 2.75 V power supply.**

***Keywords*— millimeter-wave, power amplifier, SSPA, Q-band PA, InP, HBT, PAE, MMIC**

I. Introduction

III-V semiconductors offer unmatched mm-Wave power amplier performance in terms of power density, efficiency and bandwidth [1-6]. For applications above 60 GHz, InP has demonstrated relatively high output power density and high gain [7-8] as well as high efficiency [9]. However, most prior work uses single characteristic impedance transformation networks and combiners that generally occupy most of the chip area [10-13]. Additionally, the electro-thermal response and associated reliability of multi-finger InP HBT devices is not easily predicted and depends heavily on the fabrication process and epitaxy parameters. We note that prior artwork has generally not included high emitter periphery InP HBT devices for power amplifier designs [14].

In this work, a power amplifier (PA) cell design is presented, demonstrating 57% PAE at 30 GHz from load pull measurements, excellent current handling (0.16 A) and safe operating area (SOA). Utilizing the power cell designed, a high efficiency PA is demonstrated operating at 45-47 GHz. The amplifier exhibits 16 dB of small signal gain and peak PAE of 37% - 46% across 45-47 GHz. The maximum power delivered by the amplifier is 119.7 mW at 47 GHz.

II. Design Methodology

A. 250nm InP HBT Power Cell

The HBT device used to fabricate the amplifier [15] was chosen to have a total emitter periphery of 15 μm^2 in order to deliver ~100 mW. The unit cell design supports excellent SOA a shown in Fig. 1, where the multi-finger device output curves are presented. In order to find the device SOA, the devices were swept to destruction. The I_C vs. V_{CE} curves shown in Fig. 1 correspond to sweeps that were ended prior to destruction. The power cell is configured in common emitter, and the individual HBT emitters are connected using a stack of 3 metal layers (3 μm of total height plus inter layer vias) for thermal management.

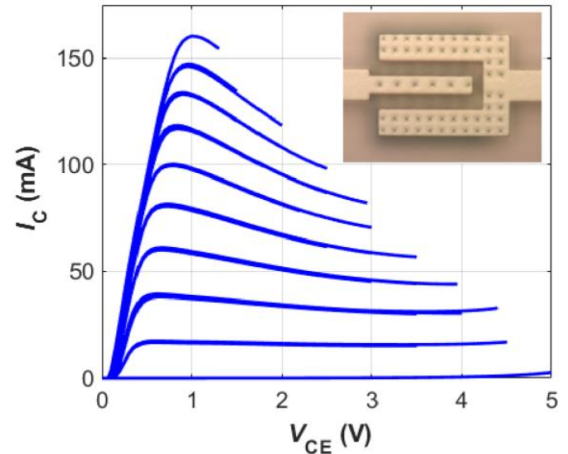

Fig. 1. Output IVs and image of fabricated power cell. The cell is 15 μm^2.

The power cell was load-pulled on-wafer after microstrip device launcher fabrication. The load-pull system utilizes Focus Delta tuners (67200), and it is vector-based, hence both the input power and the reflected power at the DUT input were measured. The power cell was biased at 2.8 V and 58 mA (3.87 mA/ μm^2). Figure 2 shows the power sweep results at optimum gamma where ~57% PAE and ~60mW are demonstrated.

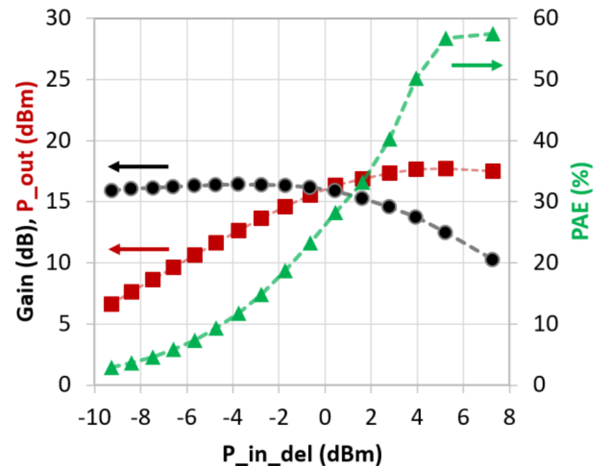

Fig. 2. Load pull measurements of designed power cell, demonstrating >57% PAE at 30GHz while delivering 59mW.

B. Amplifier Design

The device model used for the desigs is Teledyne 250nm InP proprietary's Agilent HBT model. The amplifier (Fig. 3) was designed after determining its optimum load impedance through load-pull simulations at 45-47 GHz using Keysight ADS.

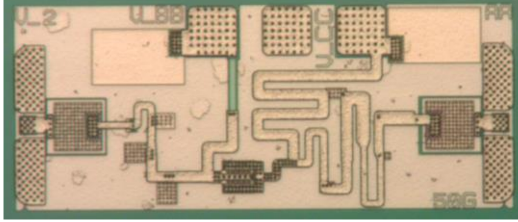

Fig. 3. Micrograph of fabricated InP HBT PA.

The fundamental load impedance of the power cell is ~32-Ω. The optimum load impedance found from the load pull simulations was transformed to the 50-Ω load using 3 transmission line sections. The capacitors were implemented as Metal-Insulator-Metal (MIM) structures, while the inductive lines were implemented as microstrip lines, absorbing some of the capacitance in order to avoid lossy thin lines. Each section transforms the same impedance ratio, at both input and output.

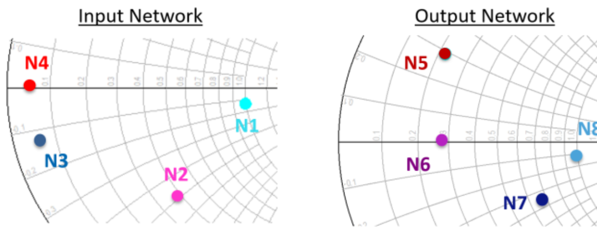

Fig. 4. Simulated optimum input and output impedance transformations, including impedances at intermediate nodes.

Figure 4 shows the optimum and intermediate design impedance at each node. A schematic showing the PA is included in Fig. 5, where the circuit location of the nodes shown in the SC (Fig. 4) is also indicated.

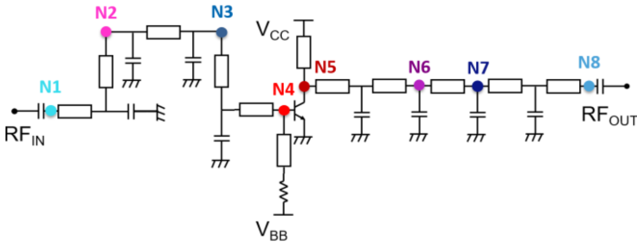

Fig. 5. Schematic of the fabricated power amplifier.

The transmission lines were meandered in the layout [16], since the ground plane is 5 μm below the signal lines, yielding a very compact design having only 276 x 600 μm^2 of inner area (without including RF pads).

III. Measurement Results

C. Small Signal Measurements

Figure 6 shows the amplifier small signal response, measured after performing probe-tip LRRM calibration using an impedance standard substrate. The S-parameter measurement was performed using a Keysight PNA-X N5242. Reasonably good agreement between the simulated parameters and the measurement can be seen from Fig. 6.

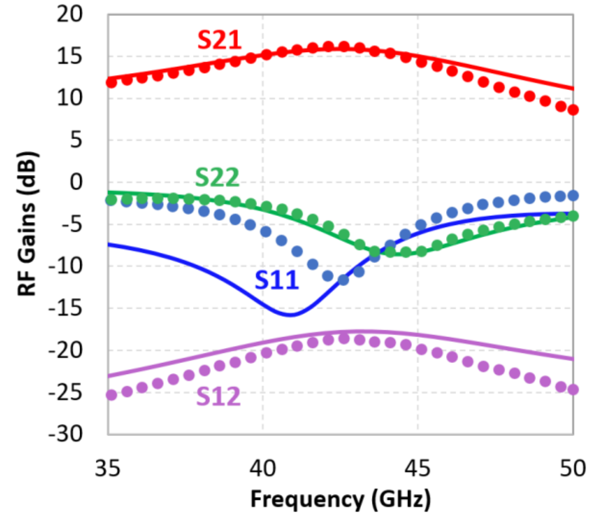

Fig. 6. PA small signal response at V_{CC}= 2.75 V, V_{BB}=2.35 V ($I_{C,Q}$ = 47 mA). The solid lines correspond to simulated performance while the symbols correspond to the measured response.

D. Power Measurement

The power performance was measured at 45, 46 and 47 GHz, after the MMIC wafers were thinned to 3mils and singulated. For the power measurement, a HP 83650A synthesizer sweeper, a Quinstar pre-driver, and a Keysight 8487A power sensor were used. The power reported below corresponds to the results after de-embedding the cable and probe losses. At 47 GHz, an output power of 119.7 mW was achieved at an associated PAE of 46%, which constitutes state-of-the-art (Table 1).

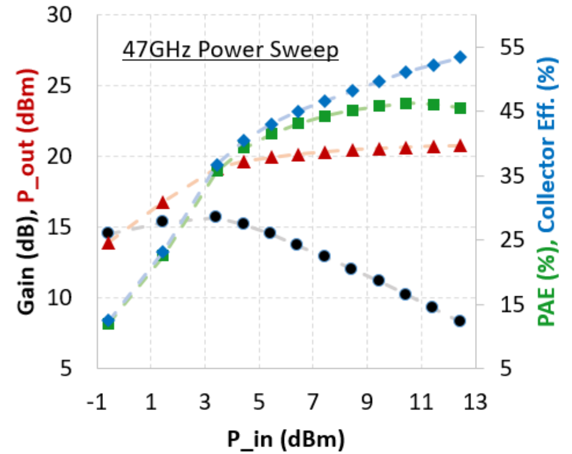

Fig. 7. Measured power sweep at 47 GHz, at V_{CC}= 2.75 V and V_{BB}= 2.35 V ($I_{C,Q}$= 47 mA).

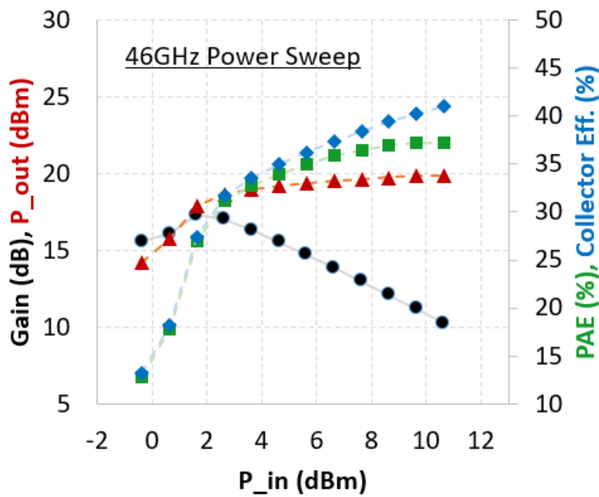

Fig. 8. Measured power sweep at 46 GHz, at V_{CC}= 2.75 V and V_{BB}= 2.35 V ($I_{C,Q}$= 47 mA).

IV. Conclusion

We have reported a high efficiency 250nm InP HBT 45 – 47 GHz power amplifier IC. The PA reported delivers record PAE (46%) and collector efficiency (54%) at 47 GHz, which is state of the art for a moderate power PA from a 2.75 V supply.

Table 1. Comparison of the results obtained in this work to prior art.

Ref.	Comparison with Prior Art				
	Freq. (GHz)	Gain (dB)	P_{SAT} (dBm)	PAE (%)	Process
[17]	47	15.5	22.7	40	GaAs
[18]	45	6	11.4	18	SiGe
[19]	47	13	17.6	34.6	CMOS
[20]	60	10.5	23.5	43	InP HEMT
[21]	59	8	25.5	41	GaN HEMT
This Work	**47**	**16**	**20.78**	**46**	**InP HBT**

References

[1] K. Brown et al., "7kW GaN W-band transmitter," 2016 IEEE MTT-S International Microwave Symposium (IMS), San Francisco, CA, 2016, pp. 1-3.

[2] J. M. Schellenberg, "A 2-W W-Band GaN Traveling-Wave Amplifier With 25-GHz Bandwidth," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 9, pp. 2833-2840, Sept. 2015.

[3] M. Micovic et al., "High frequency GaN HEMTs for RF MMIC applications," 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, 2016, pp. 3.3.1.

[4] H. Park, S. Daneshgar, Z. Griffith, M. Urteaga, B. Kim, and M. Rodwell, “Millimeter-Wave Series Power Combining Using SubQuarter-Wavelength Baluns,” IEEE Journal of Solid-State Circuits, vol. 49, no. 10, pp. 2089-2102, Oct., 2014.

[5] Z. Griffith, M. Urteaga, P. Rowell and R. Pierson, "71–95 GHz (23–40% PAE) and 96–120 GHz (19–22% PAE) high efficiency 100–130 mW power amplifiers in InP HBT," *2016 IEEE MTT-S International Microwave Symposium (IMS)*, San Francisco, CA, 2016, pp. 1-4.

[6] R. Maurer, S. Kim, M. Urteaga and M. J. W. Rodwell, "Ultra-Wideband mm-Wave InP Power Amplifiers in 130 nm InP HBT Technology," *2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Austin, TX, 2016, pp. 1-4.

[7] Z. Griffith, M. Urteaga and P. Rowell, "A 140-GHz 0.25-W PA and a 55-135 GHz 115-135 mW PA, High-Gain, Broadband Power Amplifier MMICs in 250-nm InP HBT," 2019 IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, USA, 2019, pp. 1245-1248.

[8] D. Gritters, K. Brown and E. Ko, "200-260GHz solid state amplifier with 700mW of output power," 2015 IEEE MTT-S International Microwave Symposium, Phoenix, AZ, 2015, pp. 1-3.

[9] T. K. Quach et al., "Ultrahigh-efficiency power amplifier for space radar applications," in IEEE Journal of Solid-State Circuits, vol. 37, no. 9, pp. 1126-1134, Sept. 2002.

[10] V. Radisic, D. W. Scott and C. Monier, "50 mW 220 GHz InP HBT power amplifier MMIC," 2014 IEEE MTT-S International Microwave Symposium (IMS2014), Tampa, FL, 2014, pp. 1-3.

[11] T. B. Reed, Z. Griffith, P. Rowell, M. Field and M. Rodwell, "A 180mW InP HBT Power Amplifier MMIC at 214 GHz," 2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Monterey, CA, 2013, pp. 1-4.

[12] K. W. Kobayashi et al., "A 0.5 watt-40% PAE InP double heterojunction bipolar transistor K-band MMIC power amplifier," Conference Proceedings. 2000 International Conference on Indium Phosphide and Related Materials (Cat. No.00CH37107), Williamsburg, VA, USA, 2000, pp. 250-253.

[13] J. B. Hacker, W. Ha, C. Hillman, M. Urteaga, R. Pierson and B. Brar, "Compact InP HBT Power Amplifiers Using Integrated Thick BCB Dielectrics," 2007 IEEE/MTT-S International Microwave Symposium, Honolulu, HI, 2007, pp. 805-808.

[14] I. Harrison, M. Dahlstrom, S. Krishnan, Z. Griffith, Y. M. Kim and M. J. W. Rodwell, "Thermal limitations of InP HBTs in 80- and 160-gb ICs," in IEEE Transactions on Electron Devices, vol. 51, no. 4, pp. 529-534, April 2004.

[15] M. Urteaga et al., "InP HBT Integrated Circuit Technology for Terahertz Frequencies," 2010 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Monterey, CA, 2010, pp. 1-4.

[16] A. Arias et al., "185mW InP HBT Power Amplifier with 1 Octave Bandwidth (25-50GHz), 38% peak PAE at 44GHz and Chip Area of 276 x 672 µm2," 2019 IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, USA, 2019, pp. 1303-1305.

[17] G. Lv, W. Chen, X. Chen and Z. Feng, "An Energy-Efficient Ka / Q Dual-Band Power Amplifier MMIC in 0.1- μ m GaAs Process," in IEEE Microwave and Wireless Components Letters, vol. 28, no. 6, pp. 530-532, June 2018.

[18] N. Kalantari and J. F. Buckwalter, "A 19.4 dBm, Q-Band Class-E Power Amplifier in a 0.12$\mu {\rm m}$SiGe BiCMOS Process," in IEEE Microwave and Wireless Components Letters, vol. 20, no. 5, pp. 283-285, May 2010.

[19] A. Chakrabarti and H. Krishnaswamy, "High power, high efficiency stacked mmWave Class-E-like power amplifiers in 45nm SOI CMOS," Proceedings of the IEEE 2012 Custom Integrated Circuits Conference, San Jose, CA, 2012, pp. 1-4.

[20] S. M. J. Liu, O. S. A. Tang, W. Kong, K. Nichols, J. Heaton and P. C. Chao, "High efficiency monolithic InP HEMT V-band power amplifier," GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. 21st Annual. Technical Digest 1999 (Cat. No.99CH36369), Monterey, CA, USA, 1999, pp. 145-147.

[21] M. Micovic et al., "GaN DHFETs Having 48% Power Added Efficiency and 57% Drain Efficiency at V -Band," in IEEE Electron Device Letters, vol. 38, no. 12, pp. 1708-1711, Dec. 2017.