A 190-210GHz Power Amplifier with 17.7-18.5dBm Output Power and 6.9-8.5% PAE.

***Abstract*— We report a high-efficiency G-band power amplifier in 250nm InP HBT technology. The amplifier has four capacitively linearized common base stages. Four power cells are combined by a low loss 4:1 corporate combiner. The drivers are scaled to sustain high power-added efficiency (PAE). At 202GHz operation, the amplifier has 18.3dBm saturated output power with 7.9% PAE. Over 190-210GHz, the amplifier's saturated output power is 17.7-18.5dBm with an associated 6.9-8.5%PAE. The peak small signal gain is 23.5dB at 204GHz with more than 20.5GHz 3dB bandwidth. The amplifier has a low DC power consumption of 814mW and a compact area of 1.2mmx0.95mm. To the authors' knowledge, this result is a record PAE.**

Keywords*— G-band, millimeter wave, high-efficiency power amplifier, low DC power consumption, compact combiner, low loss corporate combiner, 250-nm InP, HBT.

I. Introduction

There is an increasing demand for millimeter-wave communication as it provides more available spectrum which supports high data rates [1]. Data rates are further increased by massive MIMO arrays which require high-efficiency amplifiers with moderate output power. This permits long-range communications and relaxes the heatsink complexity. At G-band, recent CMOS work [2] shows 9.4dBm output power with only 1.03% PAE. GaN [3] shows a higher output power of 15.8dBm with 2.4% PAE. InP [4]-[9] shows the highest power and efficiency at mm-wave frequencies.

Here we present a high-efficiency 190-210GHz power amplifier. The four-stage amplifier utilizes capacitively linearized common base topologies for the power and driver cells. The amplifier shows 17.7-18.5dBm saturated output power (P_{sat}) with 13.4-16.8dB associated gain and 6.9-8.5%PAE. The output power at 1dB gain compression (OP_{1dB}) is more relevant in communication systems. The amplifier is optimized for OP_{1dB} and demonstrates a hard compression characteristic where the OP_{1dB} is close to P_{sat}.

II. Power Amplifier Design

IC was fabricated in Teledyne 250nm InP technology (f_{max}=650GHz, 4.5V BV_{CEO}, and 3mA/μm current density). The technology offers four Au interconnect layers, MIM capacitors, and thin film resistors [4].

The amplifier (Fig. 1b) has four cascaded common base stages. Four power cells (stage1) are combined with a low-loss corporate transmission line. Each two power cells are combined and driven by a single driver (stage2). Similarly, two drivers are combined and driven by a single cell (stage3). Finally, another cell (stage4) is added without area scaling to provide the required total gain.

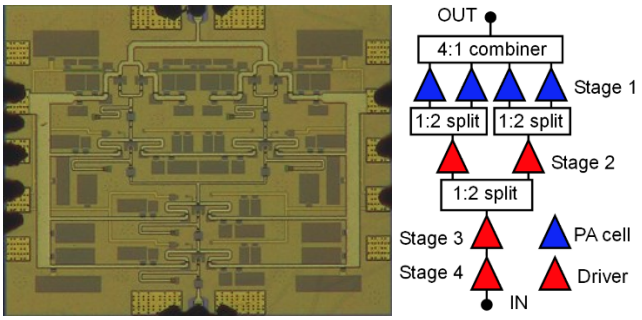

Fig. 1. (a) die photo, the area is 1.2mmx0.95mm. (b) amplifier block diagram.

We recently [5] reported a design study for different unit cells and proposed a low loss 140GHz 4:1 power combiner using 250nm InP HBT technology. Here, we follow the same design procedure. At mm-wave, the capacitively linearized common base shows superior performance compared to the common emitter or grounded common base; the linearized cell has the highest output power and efficiency at 1-dB gain compression. The base bias resistance ensures stable collector current control with minimum efficiency drop [5].

The same transistor size (4·0.25μm·6μm) is used for all cells. Power cells (Fig. 2a) are matched for PAE. A shunt inductive line tunes the transistor output capacitance. A transmission line combiner, similar to [5], uses a single quarter-wave section to transform the 50 Ω load to the necessary impedance per power cell. The output stage has a 96-μm HBT periphery. Drivers are optimized to deliver the necessary input power for the following stages. The drivers scaling (48-μm, 24-μm, 24-μm HBT periphery) is conservative to avoid soft compression characteristics. Only two independent DC supplies are used to reduce the bias complexity; one supply biases all stages' collectors and the second biases the stages' bases. Many bypass capacitors with small series resistance are distributed along the bias lines to avoid out-of-band oscillation. Ansys HFSS, 3-D EM simulation modes all the parasitics and matching circuits

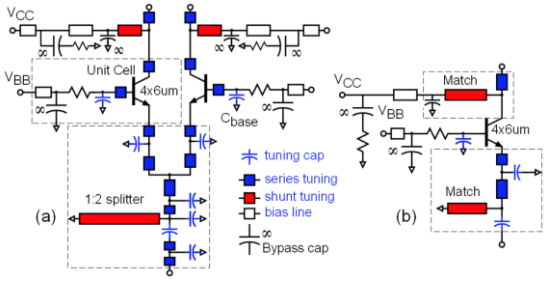

Fig. 2. Schematic diagram of: (a) two combined power amplifier cells; b) driver cell.

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III. Measurement Results

Fig. 1a shows the chip micrograph. The measurement is performed on the 3-mil thinned die mounted on a copper heatsink. S-parameters are measured using Keysight network analyzer with Oleson frequency extender modules and GGB wafer probes. LRRM standard calibration on an external substrate moves the reference plane to the probe tips. Fig. 3a shows a very good agreement between the measured and simulated S-parameters at (V_{CC}=1.9V, V_{BB}=1.6V, I_{CC}=226mA, and I_{BB}=9.9mA). The peak measured small-signal gain, $|S_{21}|$, is 21.8dB at 204GHz. The measured 1dB-BW and 3dB-BW are more than 17.6GHz and 25.6GHz respectively. We could not measure the lower frequency band due to equipment limitations. However, simulations show 34GHz 1-dB BW and 50GHz 3-dB BW. Bias is further increased (Fig. 3b) to (V_{CC}=2.5V, V_{BB}=2.2V, I_{CC}=327.5mA, and I_{BB}=17.7mA). The peak measured gain still matches the simulations. However, a frequency shift or BW shrinkage has been observed. It is believed that this may be due to transistor heating. The measured 3dB-BW is more than 20.5GHz (simulated 50GHz).

Fig. 4 shows the power measurement setup in the calibration and measuring phases. In the calibration phase, a signal generator (N5183B) feeds a x8 VDI frequency multiplier to produce the required output power at~200GHz. Then a 20dB G-band coupler is added after the multiplier

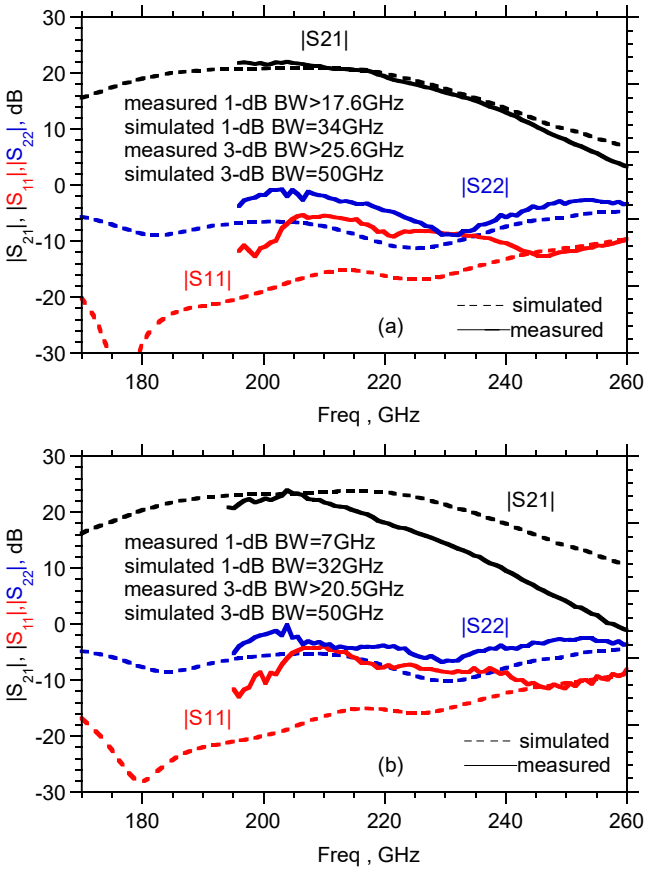

Fig. 3. Measured (solid) and simulated (dashed) S-parameters at different bias conditions: a) DC power (445mW); b) DC power (858mW).

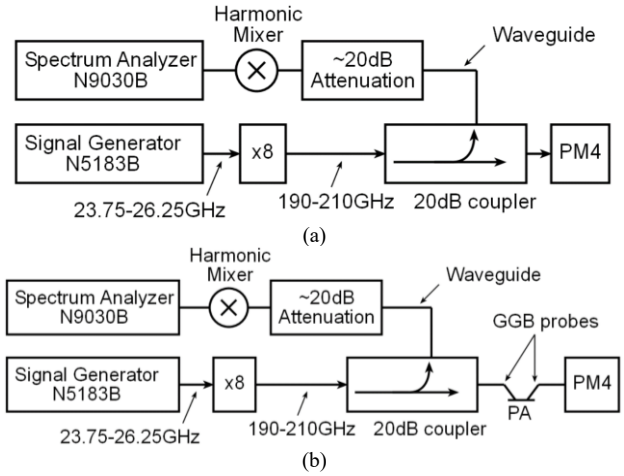

Fig. 4. Power measurement setup: a) calibration phase; b) measuring phase.

chain. The thru port goes to the power sensor and Erickson power meter (PM4) while the coupled port goes to a ~20dB fixed attenuation followed by a G-band harmonic mixer and spectrum analyzer (N9030B). The power difference, in dB scale, between the power meter and spectrum analyzer readings is recorded at different frequencies. This power difference is called the correction factor and it depends on the frequency, yet it is independent of the multipliers' output power as long as the harmonic mixer is operating in the linear region.

In the measuring phase, the setup is similar (Fig. 4b) except that the coupler thru port goes to the G-band GGB probes, amplifier, and power meter. The amplifier's input power is swept by controlling the signal generator power which feeds the VDI multiplier. The amplifier's input power is monitored by measuring the spectrum analyzer power reading and apply the appropriate correction factor, based on the frequency, from the calibration phase. This allows measuring the amplifier's input power with reasonable accuracy even at lower power levels which is necessary to measure accurate gain. The accuracy of the minimum input power is limited by the spectrum analyzer noise level while the sweeping step is limited by the signal generator resolution. Additionally, all the power data points could be measured without lifting the probes or turn off the amplifier's DC power supplies which makes the measurement more accurate and more convenient.

The measurement is performed on the 3-mil thinned part mounted on a copper heatsink. At zero RF input signal, the DC biases are (V_{CC}=2.4V, V_{BB}=2.2V, I_{CC}=323mA or 1.7mA/um, and I_{BB}=17.7mA) and V_{CC} is monitored by the RF probe at the output to get the on-wafer voltage. The DC power (P_{DC}) increases at high RF input power and reaches its maximum at ~OP_{1dB} (Fig.5 and 6), then it begins to drop again. This is a conservative bias condition and could be increased further to get higher output power. The probe losses are determined by a probe-probe through measurement. The output power, P_{DC}, gain, and PAE are recorded at many points at different power

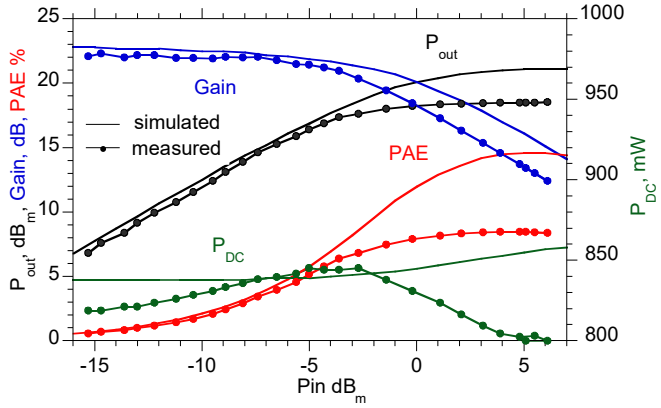

Fig. 5. Measured and simulated output power, PAE, and gain versus the input power at 194GHz.

levels and frequencies to verify the functionality. No indications for oscillations have been observed. At 194GHz operation (Fig. 5), the amplifier has a measured 17.4dBm OP_{1dB} with 6.4%PAE and 21dB associated gain. The measured saturated power is 18.5dBm with 8.5%PAE and 14.6dB associated gain. At 202GHz frequency (Fig. 6), the amplifier shows a measured 16.6dB OP_{1dB} with 21.5dB gain and 5.3%PAE. Measured P_{sat} is 18.3dB with 15.2dB gain and 7.9%PAE. The amplifier demonstrates a wide-band large-signal operation. Over 190-210GHz (Fig. 7), P_{sat} varies between 17.7-18.5dBm with more than 6.9% PAE. The amplifier demonstrates hard compression characteristics where the OP_{1dB} is very close to P_{sat}. The OP_{1dB} (Fig. 7) is 16-17.4dBm with more than 4.8% PAE across a 190-210GHz frequency range. These results demonstrate record efficiency.

IV. Conclusion

This paper demonstrated a high-efficiency G-band power amplifier. The design key features are; capacitively linearized common base, low-loss combiner, and driver scaling. The four-stage amplifier shows 17.7-18.5dBm saturated output power with a 6.9-8.5%PAE over a 190-210GHz frequency band. Table 1 shows the state-of-the-art high-efficiency G-band amplifiers. This work demonstrates record PAE.

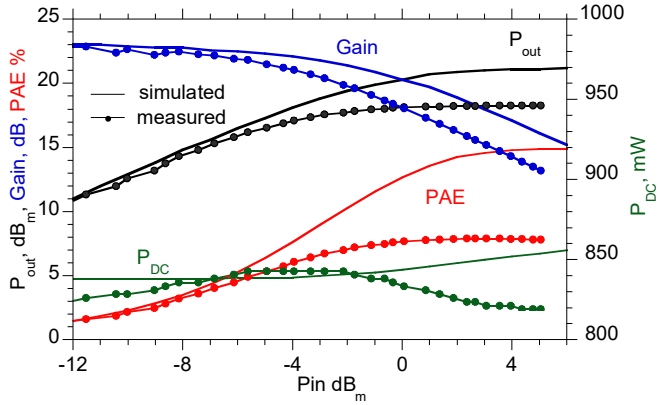

Fig. 6. Measured and simulated output power, PAE, and gain versus the input power at 202GHz.

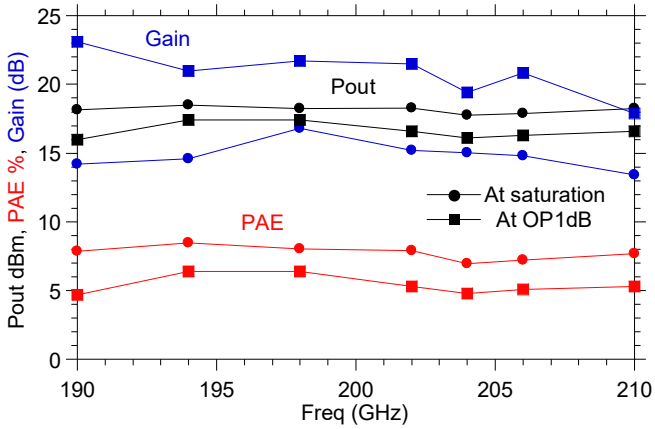

Fig. 7. Measured output power with the associated PAE and compressed gain vs. frequency reported at the saturated output power and OP_{1dB}.

Table 2. State-of-the-art high-efficiency G-band amplifiers.

Ref	[6]	[7]	[8]	[9]	**Here**
Freq, GHz	190	190-260	190.8-244	205-235	**190-210**
P_{sat}, dBm	11	17.5-21.5	16.2-18.9[a]	17.8-20.4[a,b]	**17.7-18.5**
Gain at P_{sat} (dB)	19.2	13-17.5	19-22 a	4-6	**13.4-16.8**
PAE at P_{sat}%	9.6	5.1	3.3-6.1	2-5.1[b]	**6.9-8.5%**
OP_{1dB}, dBm	3	-	-	-	**16-17.4**
PAE at OP_{1dB}%	2	-	-	-	**4.7-6.4**
Gain at OP_{1dB}	-	-	-	-	**17.9-23.1**
BW_{3dB}, GHz	26	18a	53	-	**>20.5**
Size (mm^2)	0.45	1.8	1.54	1.38	**1.14**
P_{DC} (mW)	970	2.62	1270	-	**814**
P_{sat}/Area mW/mm^2	28.2	77.9	50.6	79	**62.1**
Technology	250-nm InP HBT				

[a]Graphically estimated. [b]Loss due to the RF pads and TL feeds de-embedded for the reported values

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