A Packaged 135GHz 22nm FD-SOI Transmitter on an LTCC Carrier

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***Abstract*—We present a packaged 135GHz broadband direct conversion transmitter IC integrated with a series-fed patch antenna on a high-performance Kyocera ceramic interposer GL771 ($\varepsilon_r = 5.2, \delta = 0.003$) . The IC, designed in GlobalFoundries (GF) 22nm SOI CMOS, is flip-chip bonded to the interposer using 50 µm diameter copper pillars. The IC-package interface has ~0.9 dB measured loss. The measured antenna has 11dB gain, 12° E-plane 3-dB beam-width, and 6-GHz 3-dB bandwidth. The integrated transmitter module has measured 13dBm EIRP and 6GHz 3-dB modulation bandwidth, the latter limited by the antenna. Measurements of the transmitter's modulation constellations shows that it can support 16Gbps using 16QAM and 15Gbps using 64-QAM.**

***Keywords*— D-band transmitter, millimeter wave packaging, Ceramic interposers, LTCC carrier, Flip chip technology, D-band antenna, series-fed patch antenna, millimeter wave integrated circuits.**

I. Introduction

The future demand for high data rate wireless communications can be fulfilled using the large available spectrum between 100-300GHz. Recent advances in silicon and III-V technologies have enabled broadband, compact transceivers above 100GHz [1,2]. To serve mass markets, low-cost, high-performance 100-300GHz packaging technologies are required. Recent work on >100GHz IC packaging includes wire-bonded interfaces between ICs and PCB antennas [3] with 2.5dB transition losses at 140GHz, 130GHz ICs with a Cu pillar flip-chip bond but unstated loss for the flip-chip transition [4], and 1dB transition loss at 115-155GHz between a flip-chip transceiver and a glass interposer [5].

Here we present a low cost, high performance packaging solution at D-band, where a direct conversion CMOS transmitter is flip-chip bonded on a low-temperature-cofired ceramic (LTCC) interposer using 50 µm diameter copper pillars, thereby connecting to an 8-element series-fed patch antenna on the carrier (Fig. 1a). The transmitter module has 13dBm saturated EIRP, and 6-GHz 3-dB modulation bandwidth. Measurements of the transmitter's modulation constellations shows that it can support 16Gbps using 16QAM and 15Gbps using 64-QAM.

II. Transmitter IC

The broadband direct conversion transmitter IC was designed in GlobalFoundries 22nm SOI CMOS (22FDX), with an I/Q double balanced up-conversion mixer connected to a four-stage differential power amplifier; the LO signal is generated on wafer by a 9:1 frequency multiplier (Fig. 1b). The Tx is identical to that reported in [1], except that probe pads were replaced with Cu pillars to permit flip-chip bonding to an

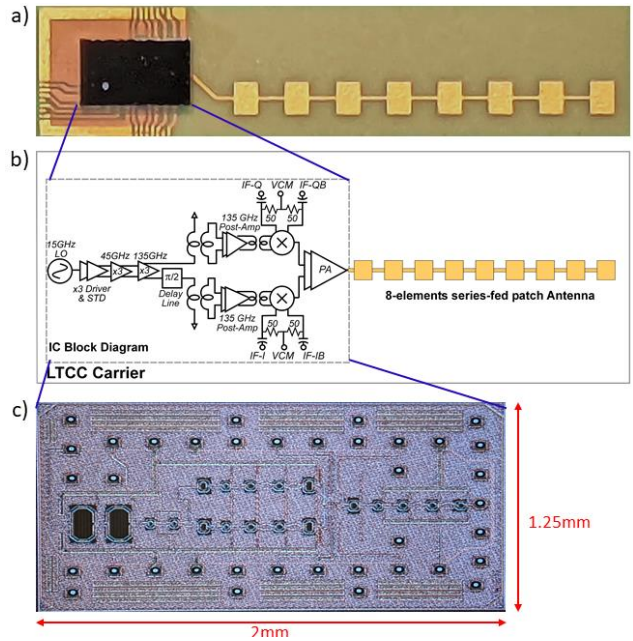


Fig. 1. (a) D-band integrated transmitter module (b) transmitter architecture, and (c) micrograph of the IC with copper pillars with a die area of 1.25mm× 2mm.

LTCC interposer. The transmitter die is 1.25mm×2mm (Fig. 1c), while the copper pillars have 30µm height and are placed at 175µm pitch.

III. Ceramic carrier design

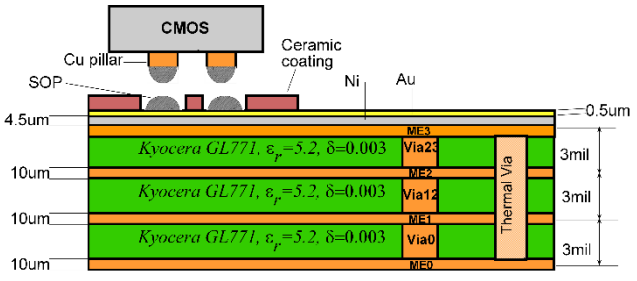
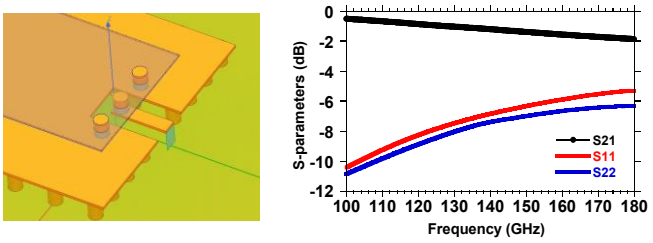


Fig. 2. Ceramic interposer layer stack.

The ceramic carrier (Fig. 2) has 3 dielectric layers of Kyocera GL771 ($\varepsilon_r = 5.2$, loss tangent $\delta = 0.003$) and has 4 metal layers. The top metal layer (ME3) routes the transmitter I/Q and LO signals and forms the series-fed patch antenna. The 2nd lowest metal layer (ME1) routes the supply and bias voltages. ME2 and ME0 are used as ground planes. A ceramic coat, with 75µm openings at the copper pillar locations, was

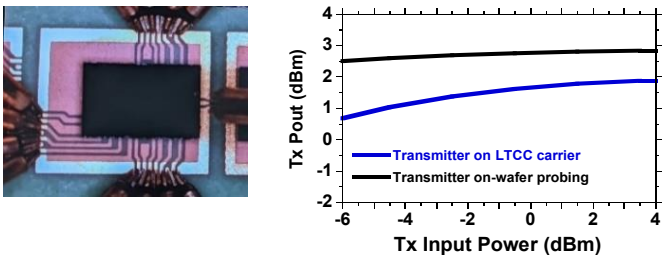
added to prevent the solder dome on the copper pillar from excessively wicking away during solder bonding. Nevertheless, given the minimum 75µm ceramic coat openings, for reliable bonding it was necessary to add additional solder on pad (SOP) to the ceramic carrier.



(a) (b)

Fig. 3. (a) Cu stud flip-chip transition, (b) Simulated performance of the chip transition (copper pillar plus CPW transition)

Fig. 3a shows the copper stud flip-chip transition. The CPW center conductor on the LTCC carrier is 50µm width, while the ground-ground separation is 150µm. The CPW line section is 220µm length. Fig. 3b shows the simulated performance of the chip transition in Ansys HFSS, which shows a simulated 1.15dB insertion loss and -7.1dB return loss at 135 GHz.



(a) (b)

Fig. 4. (a) Flip-chip transmitter mounted on carrier with wafer probe connection (b), and measured Pin-Pout characteristics of the mounted transmitter compared to that of an otherwise identical transmitter tested by on-wafer probing.

To characterize the transition loss of the flip-chip interface, a CMOS transmitter was flip chip bonded to an LTCC carrier (Fig. 4a), with the transmitter saturated output power (1.95dBm) measured with a probe contacting the LTCC carrier. This measurement was then compared to the transmitter saturated output power (2.8dBm) measured by directly probing an IC [1] of identical design, operating at the same bias condition. The measured 0.85dB difference is close to the simulated 1.15dB simulated transition loss, shown in Fig. 3b, for the combined attenuation of the copper pillar interface and 220µm of the CPW on the LTCC carrier.

IV. Series-Fed Patch Antenna

An 8-elements series-fed microstrip patch antenna [6] was designed on the LTCC carrier and simulated using Ansys HFSS, with antenna dimensions shown in Fig 5.a. A quarter-wave transformer matches the antenna to the transmitter output 50Ω, where the matching network includes the 30µm height, 50µm diameter copper pillar on the CMOS side.

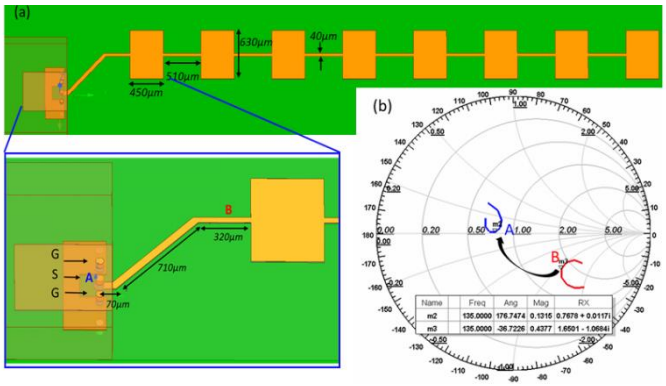
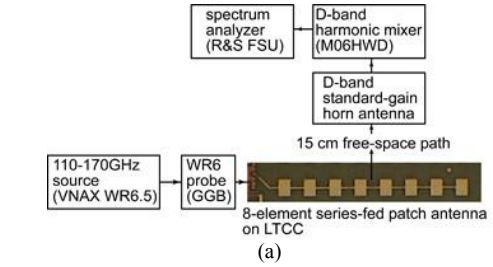
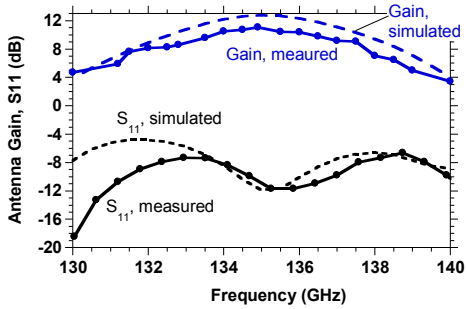


Fig. 5. Series-fed patch antenna (a) simulated antenna structure (b)smith chart of antenna matching network

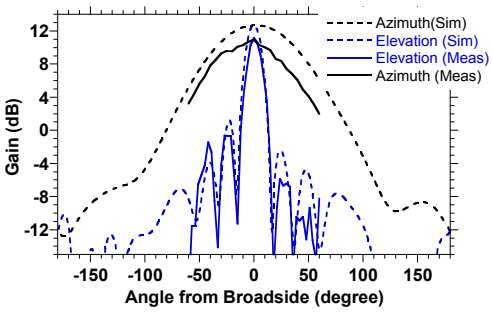
A test structure of this 8-elemetns series fed-patch antenna was tested using the setup shown in Fig. 6a



(a)



(b)



(c)

Fig. 6. (a) Series-fed patch antenna measurement setup, (b) Antenna measured gain and return loss vs. frequency, (c) measured antenna radiation pattern

Fig. 6b shows the measured antenna gain (11dB) and 3-dB bandwidth (6-GHz). The measured antenna gain is 1dB below simulation, while the measured return loss (S_{11}) is -12dB. Fig. 6c shows the measured antenna far field radiation pattern at 135GHz. The antenna has 12° E-plane 3-dB beam width, while the sidelobes are suppressed by 12-dB.

V. INTEGRATED TRANSMITTER MODULE

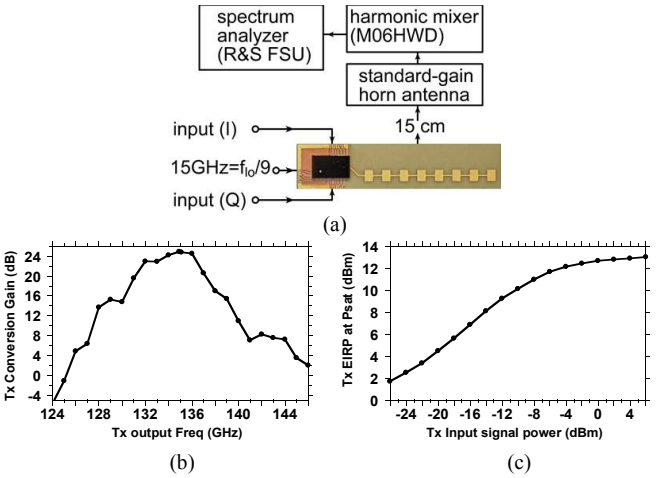


Fig. 7. (a) Swept-frequency measurement setup (b) measured transmitter frequency response, (c) and input-output power characteristics.

The transmitter module was first characterized (Fig. 7a) with swept-frequency and swept-power measurements. The LO is 135GHz, the Tx input signal was swept from 0.1 to 10GHz, and the transmitter upper and lower sideband powers were captured using a spectrum analyser and D-band harmonic mixer. The module has 6GHz modulation bandwidth (Fig. 7b) at the 3dB points (131-137GHz). The measured saturated EIRP (Fig. 7c) is 13dBm, with 8.4dBm EIRP at the output 1-dB compression point

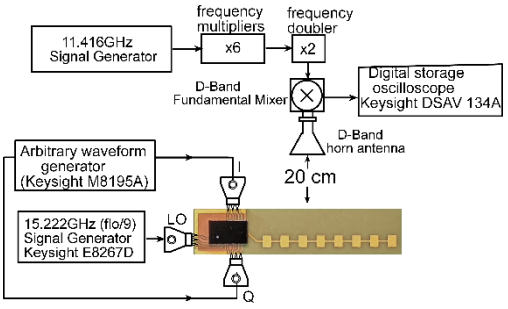


Fig. 8. Transmitter module modulation characterization.

Modulation performance of the transmitter module was then characterized (Fig. 8) using an arbitrary waveform generator (AWG) for the transmitter input signals, and monitoring the module output at 20cm propagation distance using a horn antenna, a D-band fundamental mixer for frequency down conversion, and a digital storage oscilloscope (DSO) for signal acquisition. The AWG was set to generate different signal constellations modulating a 2GHz IF, as the transmitter is planned to be used in low IF mode for future beamforming arrays, with the transmitter module then upconverting this modulated signal to a 137GHz carrier. The DSO demodulates the received signal, and, after adaptive equalization displays (Table 1) the modulation constellation and computes the error vector magnitude (EVM). The stated EVM magnitudes are referenced to the constellation's RMS amplitude.

Table. 1. Transmitter module measured modulation constellations and computed error vector magnitudes. Power levels are quoted relative to the saturated output power.

rate	4 GBaud	4 GBaud	2.5 GBaud
power	3dB backoff	6dB backoff	8dB backoff
EVM (RMS)	7.9%	9.2%	7.4%

Table 2. Comparison between state-of-the-art transmitter module at D-frequency band (110-170GHz)

	[4]	**[5]**	**[7]**	This Work
Package	RO4350	Radio on Glass	Astra MT77	LTCC GL771
IC Tech	55nm SiGe HBT	0.13um SiGe-BICMOS	45nm CMOS SOI	22nm FDSOI
Antenna Integration	No	No	Yes	Yes
Frequency (GHz)	110-150	115-155 135-170	142-147	131-137
EIRP at Psat	-	-	14dBm/ channel	13dBm
Tx-Psat	-0.5dBm	13dBm	2dBm	1.95dBm
Tx Pdc (mW)	220	1350 2100	-	210
Package Loss	3dB	1dB	2.5dB	0.85~1.1 dB
Supported Modulation	QPSK	256QAM	BPSK	64QAM

Table 2 compares the transmitter module with recent published packaged modules at the same frequency band (D-band)

V. CONCLUSION

A high-performance packaging for D band transmitter is presented, with a low transition loss of 0.9dB. The transmitter module has 6GHz 3-dB modulation bandwidth, limited by the antenna BW. The peak measured EIRP of this module is 13dBm. In [8] the packaged CMOS transmitter, presented here, drives a high-efficiency InP power amplifier resulting in a peak measured EIRP of 27.5dBm.

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