A 200 GHz InP HBT Direct-Conversion LO-Phase-Shifted Transmitter/Receiver with 15 dBm Output Power

Munkyo Seo[#1], Ahmed S. H. Ahmed[$*], Utku Soylu[*], Ali Farid[*], Yunsik Na[#], Mark Rodwell[*]
[#]Department of Electrical and Computer Engineering, Sungkyunkwan University, South Korea
[$]Marki Microwave Inc., USA
[*]Department of Electrical and Computer Engineering, University of California, Santa Barbara, USA
[1]mkseo@skku.edu

***Abstract*—Fully-integrated 200 GHz direct-conversion transmitter and receiver ICs in InP-HBT process are presented. The transmitter exhibits > 20 dB conversion gain for 190-217 GHz, with 16.5 dBm / 15.3 dBm saturated output power at 195 GHz / 200 GHz, consuming 1,250 mW. The receiver has >15dB conversion gain over 190-213 GHz, 825 mW dissipation, and 7.7-9.3 dB noise figure over 200-212 GHz. An LO phase shifter enables sets of these ICs to form phased-array transceivers.**

***Keywords*—millimeter wave integrated circuits, THz integrated circuits, direct conversion, InP HBT.**

I. Introduction

The 100-300GHz spectrum has been drawing significant interest due to its potential for beyond-5G high-speed communication [1]. Recently, integrated transmitters and receivers in various technologies, operating at around 200 GHz or beyond, have been reported [2]-[13]. Challenges in wireless communication at such high frequencies include relatively high path loss and low active device gain. To secure link margin overcoming the path loss, the output power from a single transmitter must be increased. Multiple transmitters can form a phased array, further extending the communication range, with built-in beamforming capability. Low available transistor gain translates into a low power efficiency, e.g. ~1%, typical for 100-200 GHz transmitters. To extend the battery life without excessive heating, the transmitter efficiency must be increased. In this paper, we report the design and measured results of 200 GHz QPSK/QAM-compatible transmitter (Fig. 1) and receiver IC (Fig. 2) with high output power and integrated LO phase shifter, fabricated in Teledyne 250nm InP HBT Technology.

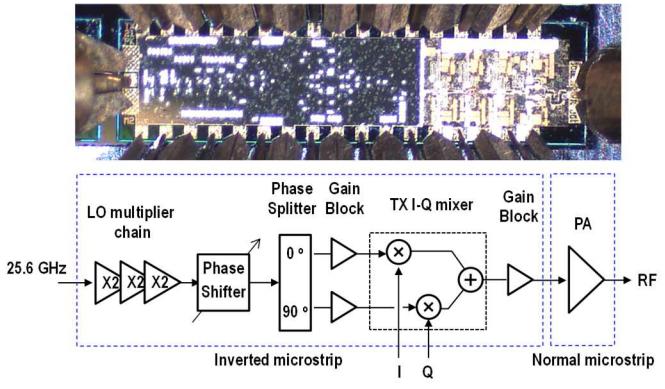


Fig. 1. A 200 GHz direct-conversion transmitter: chip photo (top) and block diagram (bottom). Chip size: 2.9×0.75mm^2

II. Transmitter Design

The 200 GHz transmitter consists of a LO multiplier (×8), phase shifter, phase splitter, I-Q mixer and power amplifier, as shown in Fig. 1. Two types of lines are used: inverted microstrip (IMSL) and normal microstrip lines (MSL). IMSLs are used for LO circuits, mixer and gain block, where the device density is relatively high. The top-metal (M4) provides a continuous ground plane regardless of device contacts at M1, eliminating performance degradation (reduced bandwidth and gain, cross-talk) from impedances due to ground plane holes. Uncertainty in layout EM modelling is thus reduced at the cost of extra line loss: 2.5 dB/mm and 1.1 dB/mm at 200 GHz, for IMSL and MSL, respectively. The PA and LNA are implemented in MSL for best PAE and lowest noise figure. Simulated loss of an IMSL-MSL transition is < 0.1dB.

A. LO Multiplier (×8)

The 8:1 LO multiplier is implemented by cascading three stages of frequency-doublers in push-push configuration. In simulation, the minimum required power at the multiplier input is -15 dBm, and the output power remains > 0 dBm for 180-230 GHz, while consuming 250 mW.

B. LO Phase shifter

A 200 GHz phase shifter is implemented in the LO path to enable multiple ICs to form LO-beamforming phased-arrays. The benefit of LO-beamforming, compared to the RF-beamforming counterpart, is that the system performance is

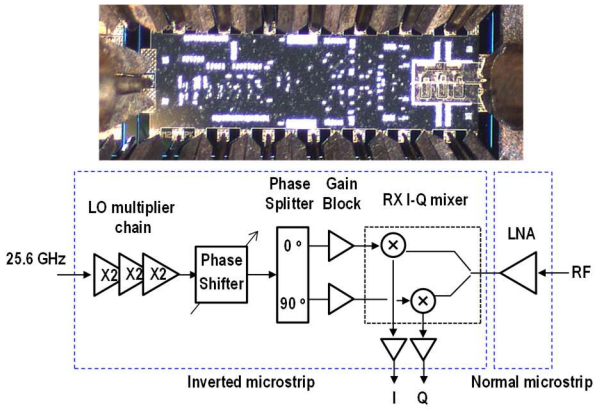
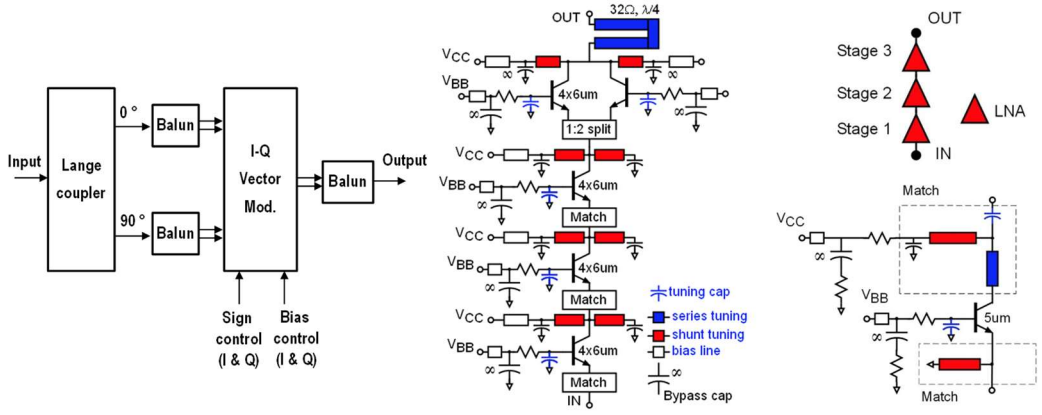


Fig. 2. A 200 GHz direct-conversion receiver: chip photo (top) and block diagram (bottom). Chip size: 2.3×0.85mm^2



(a) (b) (c)

Fig. 3. Circuit schematics: (a) phase shifter, (b) power amplifier, (c) LNA

less sensitive to the bandwidth and linearity of the phase shifter, at the cost of multiple up-conversion mixers. The phase shifter is based on I-Q vector-modulator (Fig. 3 (a)), to avoid insertion loss and amplitude variations of passive phase shifters. A Lange coupler generates I and Q-path with 90° relative phase shift. The magnitude and polarity of each LO path is controlled by a double-balanced mixer, followed by a balun for a single-ended output. The designed phase shifter has -5 dB insertion loss at 200 GHz, consuming 160 mW. In simulation, the magnitude and phase error of the Lange coupler is < 0.3 dB and < 2°, respectively, with < 1.5 dB insertion loss, for 170-250 GHz.

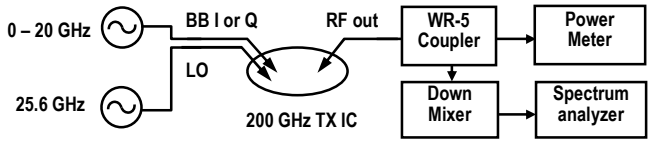
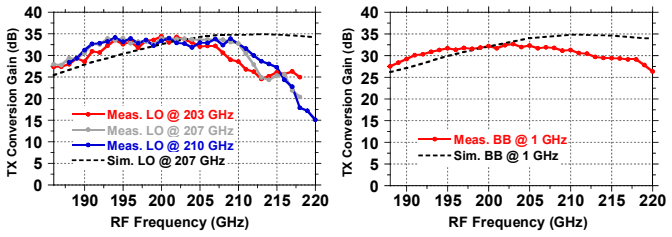
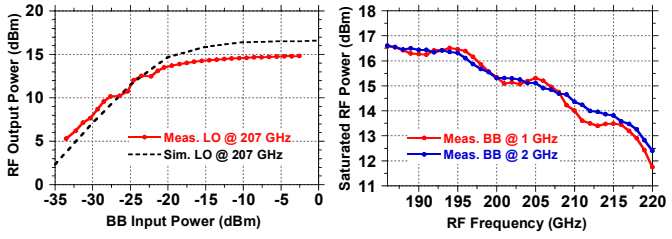


Fig. 4. On-wafer transmitter IC testing setup.



(a) (b)

Fig. 5. TX measured results: (a) conversion gain vs. baseband frequency at a fixed LO, (b) conversion gain vs. LO frequency at a fixed baseband frequency.



(a) (b)

Fig. 6. TX measured results: (a) RF output power vs. baseband input power at 1 GHz baseband frequency, (b) saturated RF power vs. RF frequency.

C. *TX I-Q mixer*

The phase shifter output is split into I and Q-paths by another Lange coupler. The I-Q mixer consists of two double-balanced mixers with a common inductor load. A 5-10μm wire will introduce 3-4° phase delay at 200 GHz, and such delays, especially if accumulated, tend to reduce the bandwidth. Layout asymmetries in I and Q-path will create amplitude and phase imbalance, degrading the error-vector magnitude (EVM) performance. Therefore, minimum design rules were used in the mixer layout, while minimizing I-Q asymmetry. Simulated I-Q imbalance is < 0.7 dB and < 3° up to 20 GHz baseband input, including layout parasitics.

D. *Power Amplifier*

The PA uses four capacitively linearized common-base (CB) stages, designed for high efficiency and compact layout (Fig. 3(b)). This design shows superior efficiency compared to common-emitter or grounded common-base at 1dB gain compression [14]. Two power cells (48-μm HBT periphery) are combined by a 2:1 combiner based on a single $\lambda/4$ line [14]-[16]. Shunt inductors tune the transistor parasitics. One level driver scaling is used for a reasonable efficiency while reusing the same transistor footprint. The drivers have a separate bias which can be separately tuned for high efficiency. Simulated saturated power of the PA is 17 dBm at 200 GHz with > 20 dB gain, while dissipating 450 mW.

III. Receiver Design

The 200 GHz receiver shares the same LO building blocks in the transmitter. The LNA is implemented in MSL to keep its noise figure low, while other circuits use IMSL.

A. *LNA*

The LNA uses common-base stages with the base capacitance adjusted so that the source impedance for minimum noise measure is equal to the stage input impedance, this allowing simultaneous input matching for reflection coefficient and for noise (Fig. 3(c)). The HBT junction area of each stage is scaled so that the source conductance for minimum noise measure is 20mS; this permits the input stage to be noise-

Table I. Comparison of recently published >200 GHz integrated transmitters

Ref.	Technology	Integrated TX circuit blocks	Modulation	Freq. (GHz)	P_{sat} (dBm)	P_{DC} (mW)	Efficiency (%)
[2]	0.1μm GaAs mHEMT	IF-mixer, LO multiplier (×2), PA, antenna	External mod.	220	-6	110	0.23
[3]	50nm GaAs mHEMT	IF-mixer, PA	External mod.	240	1	N/A	N/A
[4]	32nm SOI CMOS	LO VCO, OOK mod, PA, antenna	OOK	210	4.6	240	1.20
[5]	65nm CMOS	IQ-mixer, tripler	QPSK	240	-0.5	220	0.41
[6]	250nm InP-HBT	IF-mixer, LO driver, LO oscillator	External mod.	298.1	-2.3	452	0.13
[7]	130nm SiGe	IQ-mixer, LO multiplier (×16), PA	16-QAM/64-QAM	240	-4.4	1,033	0.04
[8]	130nm SiGe	Mixer, LO driver, antenna	BPSK	190	-6	32[1]	0.78
[9]	40nm CMOS	IQ-mixer, LO multiplier (×3)	16-QAM	265.68	-1.6	890	0.08
[10]	130nm SiGe	IQ-mixer, LO multiplier (×16), PA	16-QAM	220-255	5	960	0.33
[11]	130nm SiGe	IQ-mixer, LO multiplier (×16), PA	QPSK	225-255	7.5	960[2]	0.59
[12]	130nm SiGe	IQ-mixer, LO multiplier (×8), PA	16-QAM	240	12[4]	1,237	1.28
[13]	80nm InP-HEMT	IF-mixer, LO driver, PA[3]	External mod.	290	12	6,600	0.24
This work	**250nm InP-HBT**	**IQ-mixer, LO multiplier (×8), phase shifter, PA**	**QPSK / QAM**	**195**	**16.5**	**1,250**	**3.57**
				200	**15.3**	**1,250**	**2.71**

[1]P_{DC} not including LO generator at 190 GHz [2]P_{DC} for 1-channel I-Q TX+LO [3]Individually packaged, not integrated [4]Measured from PA breakout

matched to 50Ohms with a single inductive shunt element, avoiding the added attenuation, hence the added noise, of a series matching element. Center frequencies of the three stages are staggered to provide wider bandwidth.

B. RX I-Q Mixer and 50-ohm Driver

The receiver I-Q mixer consists of two double-balanced cores, and minimum design rules were used in layout, similarly to the TX mixer. The mixer is followed by an emitter-degenerated differential pair to drive 50-ohm load.

IV. Measured Results

The fabricated transmitter IC was measured using on-wafer test setup in Fig. 4. A WR-5 directional coupler was used for simultaneous spectrum and power measurement. First, the baseband frequency f_{BB} was varied with fixed LO frequency f_{LO}. In Fig. 5(a), the peak measured conversion gain was 34 dB with ~20 GHz of 3-dB bandwidth (only I-channel was driven). Second, f_{LO} was swept with f_{BB} = 1 GHz. The measured conversion gain was > 25 dB for 190-220 GHz in Fig. 5(b), implying the LO multiplier bandwidth is > 30 GHz. The measured saturated output power was 16.5 dBm and 15.3 dBm, at f_{RF} = 195 GHz and 200 GHz, respectively, in Fig. 6. The transmitter IC consumes 1,250 mW.

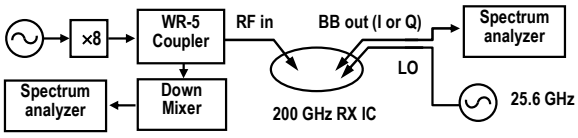
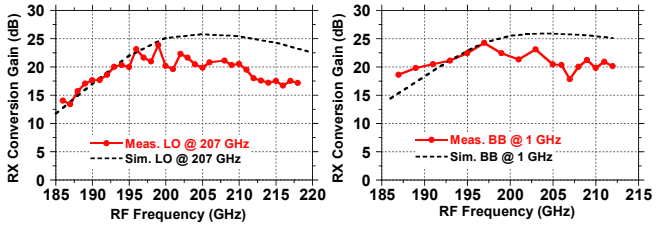
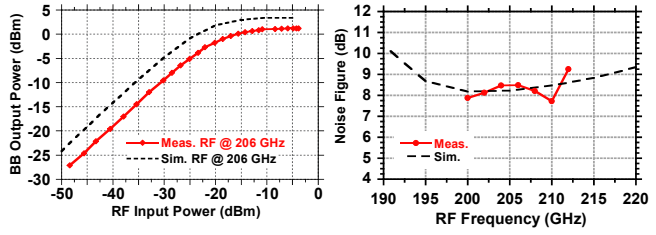


Fig. 7. On-wafer receiver IC testing setup.



(a) (b)

Fig. 8. RX measured results: (a) conversion gain vs. RF frequency at a fixed LO, (b) conversion gain vs. RF frequency at a fixed BB frequency.



(a) (b)

Fig. 9. RX measured results: (a) baseband output power vs. RF input power at f_{LO} = 207 GHz and f_{RF} = 206 GHz, (c) measured vs. simulated noise figure.

The receiver was tested using on-wafer setup in Fig. 7. The peak measured conversion gain was 25 dB and remains > 15 dB for 190-213 GHz (Fig. 8). The measured input P_{1dB} of the receiver was -24 dBm in Fig. 9(a), with 825 mW dissipation. The receiver noise figure (Fig. 9(b)), measured with a VDI-WR5.1NS hot/cold noise source connected to the receiver input, was 7.7-9.3 dB over 200-212 GHz. The receiver output noise power spectral density was measured at 100MHz using a ~20dB low-noise post-amplifier and a spectrum analyser.

Testing of a breakout circuit shows that the 200 GHz phase shifter is fully functional. For all measurement, the reference plane was at the probe tip, with losses of 140-220 GHz GGB probes, coupler, waveguides, cables, etc, all de-embedded. Table I compares this work with prior publications. To the best of authors' knowledge, the presented transmitter exhibits the highest output power and efficiency, among all integrated up-converting transmitters beyond 200 GHz.

V. Conclusion

A 200 GHz transmitter and receiver IC were presented with record output power (15.3-16.5 dBm) and efficiency (2.71-3.57%) over 195-200 GHz. Further testing is under way, including modulated testing (e.g. QPSK or QAM).

Acknowledgment

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