Lg = 40nm Composite Channel MOS-HEMT Exhibiting f_τ = 420 GHz, f_{max} = 562 GHz

Brian Markman, Simone Tommaso Šuran Brunelli, Matthew Guidry, Logan Whitaker, and Mark J.W. Rodwell
ECE, University of California Santa Barbara, Santa Barbara, CA, 93106, USA
Email: brian.markman@keysight.com Phone: (215) 264-9890

Overview: An L_g = 40 nm, t_{ch} = 7.0 nm $In_{0.53}Ga_{0.47}As$ / InAs MOS-HEMT exhibiting f_t = 420 GHz and f_{max} = 562 GHz at V_{DS} = 0.70 V, V_{GS} = 0.30 V, and I_{DS} = 0.793 mA/µm is reported. A 0.83 nm / 1.71 nm $Al_xO_yN_z$ / ZrO_2 high-k gate dielectric is used with a 3.0 / 4.0 nm $In_{0.53}Ga_{0.47}As$ / InAs composite channel. At 40 nm L_g, high peak $g_{m,e}$ = 2.9 mS/µm and record low $g_{ds,e}$ = 0.18 mS/µm at V_{DS} = 0.70 V was achieved. Long gate length SS_{min} = 69 mV/dec is observed. Bandwidth of the present devices is limited by parasitic $C_{GS,p}$, $C_{GD,p}$.

Fabrication: Device fabrication closely follows [3]. The starting epitaxial structure was purchased from Intelligent Epitaxy. From substrate to air the grown layers are: 100 nm UID-$In_{0.52}Al_{0.48}As$ buffer, 3 nm modulation doped Si:$In_{0.52}Al_{0.48}As$ (1.2 x 10^{19} cm^{-3}), 3 nm UID-$In_{0.52}Al_{0.48}As$ spacer, 3 / 4 / 6 nm UID-$In_{0.53}Ga_{0.47}As$ / strained UID-InAs / UID-$In_{0.53}Ga_{0.47}As$ composite channel. After thinning the channel to 7 nm the link region was grown. From channel to air the grown layers are: 3.0 nm UID-InP spacer, 3.5 nm Si:InP (1.0 x 10^{19} cm^{-3}) modulation doping, 10 nm UID-InP cap. Cross-sectional TEM images of the device are shown in Fig. 1; wet etching through the link region prior to re-growing the S/D yields isotropic undercutting, bringing the link surface closer to the plane of modulation doping, resulting in a local reduction of n_{QW}, resulting in large end resistances R_{end} and no improvement to R_A compared to [3]. Recessing into the link reduces the barrier height and tunneling distance beneath the S/D while maintaining topology. Finally, 30 cycles of ZrO_2 was used giving 0.83 nm $Al_xO_yN_z$ / 1.71 nm ZrO_2.

DC results: DC characteristics were measured on large gate-footprint devices (L_{GM} = 1.2 µm). Measurements were made from V_{DS} = 0.1 V to 1.0 V. Fig. 2 shows the transfer and output characteristics of a L_g = 40 nm, $(0\bar{1}1)$ device. Peak g_m = 2.4 mS/µm, I_{on} > 1.4 mA/µm. I_{off} = 6 nA/µm and 2 µA/µm while minimum subthreshold slope SS_{min} is 122 mV dec and 252 mV/dec for V_{DS} = 0.1 V and 0.5 V respectively. Long gate length (1 µm) SS_{min} = 69 mV/dec at V_{DS} = 0.1 V and I_G < 4 nA/µm^2 at V_{DS} = 0.5 V for all devices. Two sets of TLMs are used to measure R_S. One measures the N+ film resistance R_N and ohmic contact resistance R_C while the other measures R_L and R_A. The measured values are R_C = 6.5 Ω•µm, R_N = 7.5 Ω•µm, R_A = 49.4-54.5 Ω•µm (orientation dependent), R_L = 11.4 Ω•µm, for total R_S = 75-80 Ω•µm. Extrapolating R_{on} to zero-L_g for V_{GS} = 0.4-0.7 V gives $R_{on}(0)$ = 226-261 Ω•µm. Lin *et al.* showed that extrapolated R_{on} in scaled III-V FETs contain a significant ballistic resistance $R_{ballistic}$ component, which can explain the discrepancy in $R_{S,TLM}$ and $R_{on}(0)$ [4].

RF results: S-parameters were measured from 250 MHz to 67 GHz using on-wafer probing and -27 dBm port power. Prior to measurement off-wafer load-reflect-reflect-match calibration was done. On-wafer open and short-circuit pad parasitics were de-embedded where the order of pad extraction only minimally changes the transistors 2-port parameters. This paper quotes the more conservative extraction. Devices are two finger, W_g = 10 µm for total gate periphery of 20 µm. f_τ, f_{max} are determined by fitting the -20 dB/dec roll off of current gain H_{21} and unilateral power gain U from 10-50 GHz and 30-45 GHz respectively. Contour plots of f_τ, f_{max}, H_{21} fit, and U fit for a L_g = 40 nm $(0\bar{1}1)$ device are shown in Fig. 3. The small signal equivalent circuit (SSEC) used to fit the measured S-parameters of a L_g = 40 nm $(0\bar{1}1)$ device is illustrated in Fig. 4 as well as measured and modeled U, H21, and maximum stable and available gain (MSG/MAG). Like [2] and [3], a series L-R network is used to describe the parasitic bipolar current gain observed at low frequencies due to breakdown at the drain-edge. The fitted L/R time constant (τ_p) is 33 ps, consistent with [2].

An L_g series of SSEC parameters, determined by automatic fitting based on [5], is shown in Fig. 5. Balanced f_τ, f_{max} at short L_g was realized by reducing $R_G \leq 10$ Ω by overdeveloping the T-Gate foot at the expense of large C_{GS} and C_{GD}. $C_{GS} \geq 0.75$ fF/µm and $C_{GD} \geq 0.25$ fF/µm severely limit f_τ, f_{max}. High peak $g_{m,e} \geq 2.70$ mS/µm and extremely low $g_{ds,e} \leq 0.20$ mS/µm are observed for most measured devices. Extracted R_S = 95-110 Ω•µm, corresponding to peak $g_{m,i}$ = 4.28 mS/µm and $g_{ds,i}$ = 0.27 mS/µm [6] or $g_{m,i}$ = 4.2 mS/µm and $g_{ds,i}$ = 0.26 mS/µm, by SSEC modeling, for L_g = 40 nm at V_{DS} = 0.7 V, V_{GS} = 0.3 V. The extremely high g_m and low g_{ds} suggest that MOS-HEMTs can achieve f_τ, f_{max} in excess of 700 GHz, similar to [1] and [7] if $C_{GS,p}$ and $C_{GD,p}$ can be reduced. Most state-of-art HEMTs use self-aligned processes that limit $C_{GS,p}$ and $C_{GD,p}$ by eliminating gate overlap. Egard *et al.* demonstrated a self-aligned, regrown MOSFET process that can be adapted to the double regrowth MOS-HEMT process used here, providing a possible pathway forward [8].

Conclusions: Improved R_S was accomplished by thinning t_{Link} and increasing N_δ while g_m was increased by reducing t_{ins} and increasing t_{ch}. Balanced f_τ and f_{max} were realized by reducing R_G. Exceptionally high $g_{m,e}$ = 2.90 mS/µm was demonstrated while simultaneously demonstrating extremely low $g_{ds,e}$ = 0.18 mS/µm. C_{GS} and C_{GD} in excess of 0.75 fF/µm and 0.25 fF/µm limit high-frequency performance. A self-aligned process is needed to address parasitic capacitances and misalignment concerns.

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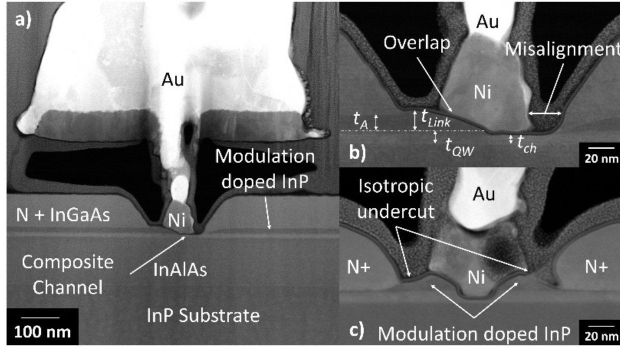

Fig. 1. Cross-sectional TEM of (a) recessed source-drain device (b) intrinsic region of recessed source-drain device (c) intrinsic region of removed link device

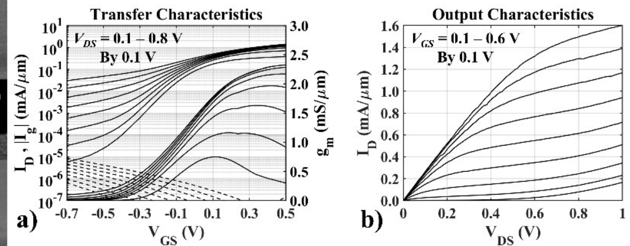

Fig. 2. (a) Transfer and (b) output characteristics of large gate footprint L_g = 40 nm $(0\bar{1}1)$ conduction device

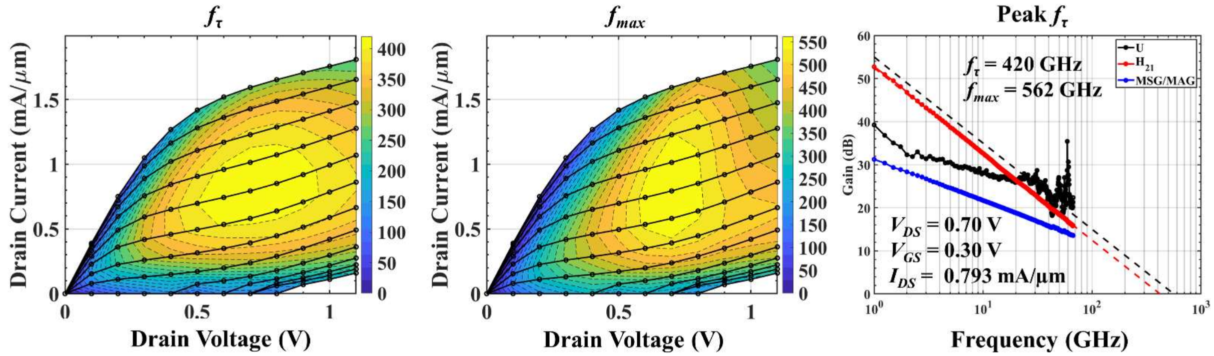

Fig. 3. High frequency FOM contours and extrapolated FOMs at peak $f\tau$ bias

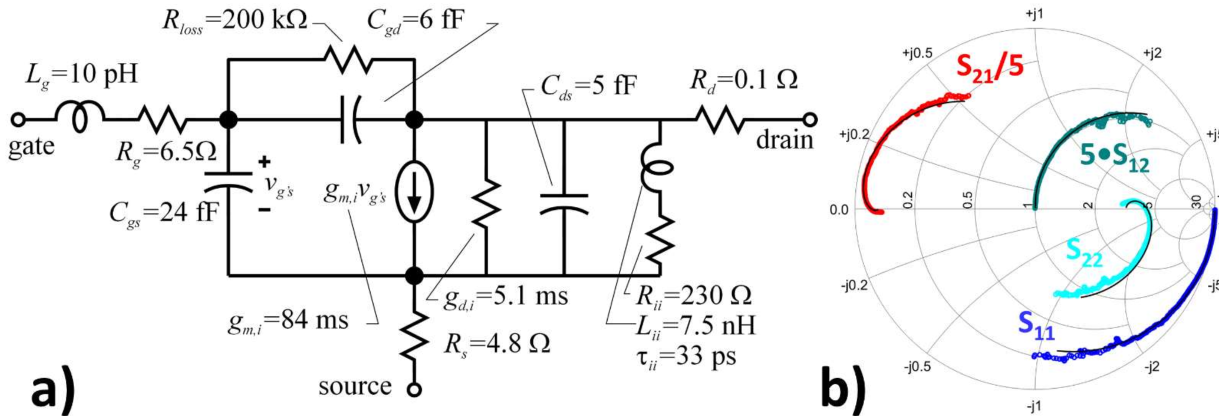

Fig. 4. (a) common-source SSEC of L_g = 40 nm $(0\bar{1}1)$ conduction device and (b) measured/modeled S-parameters

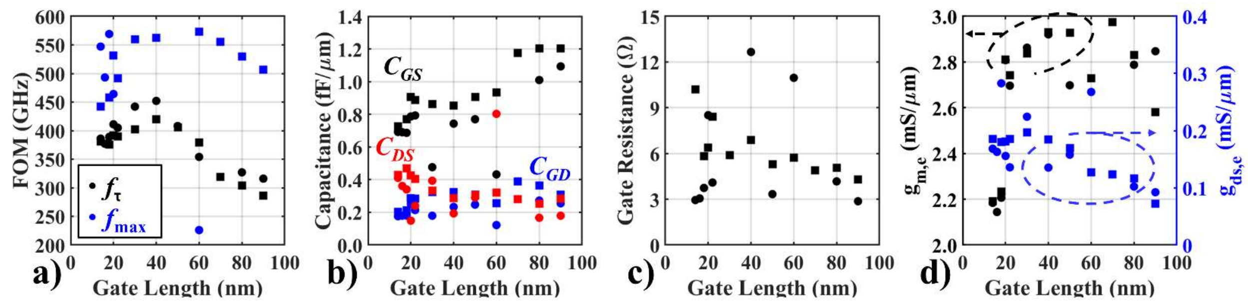

Fig. 5. Gate length series of extracted common-source SSEC elements where circles are (011) and squares are $(0\bar{1}1)$ conduction (a) $f\tau$, f_{max} determined by extrapolation (b) C_{GS}, C_{GD} (c) R_G (d) $g_{m,e}$, $g_{ds,e}$