$L_g = 40$nm Composite Channel MOS-HEMT
Exhibiting $f_\tau = 420$ GHz, $f_{\text{max}} = 562$ GHz

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UCSB Department of Electrical and Computer Engineering

Funding: SRC & DARPA
1. High $f_t, f_{max}$ HEMT Motivation
2. MOS-HEMT Advantage
3. Device 1 – Link Wet Etched
   • Fabrication
   • DC Characteristics
   • RF Characteristics
4. Device 2 – Link “Recessed”
   • Fabrication
   • DC Characteristics
   • RF Characteristics
High $f_T, f_{\text{max}}$ HEMT Motivation

- Current electromagnetic bands are crowded
- Need to move into currently unallocated bands at higher frequencies
- Higher frequency = higher data rate = faster upload/download speeds
- For circuits to be efficient (high PAE) need $f_{\text{op}} \approx 0.1-0.2 \cdot f_{\text{max}}$
- Atmospheric attenuation means many base stations and spatial multiplexing
HEMT Motivation – Reduce Noise Figure

- 2:1 to 4:1 increase in $f_t$:
  - Improved noise
  - Less required transmit power
  - Smaller PAs, less DC power
- Or higher-frequency systems

\[
F_{\text{min}} \approx 1 + 2 \sqrt{g_m (R_s + R_g + R_t) \Gamma} \cdot \left(\frac{f}{f_t}\right)
+ 2 g_m (R_s + R_g + R_t) \Gamma \cdot \left(\frac{f}{f_t}\right)^2
\]

\[
\Gamma \approx 1
\]
Noise Figure / Measure Considerations

PA = Power Amplifier
LNA = Low Noise Amplifier

\[ F_{\infty} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots \]

\[ M = F_{\infty} - 1 \]

• Noise of cascaded amplifiers is more important than noise of one
• \( F_{\infty} \) can be big even if \( F_1 \) is small \( \rightarrow \) cannot forget \( G_1 \)
• Cannot forget about \( f_{\text{max}} \) \( \rightarrow \) Need balanced \( f_{\tau}, f_{\text{max}} \)
Reduce Noise Figure – What Device?

**MOSFETs**
- Gate dielectric and $L_g$ can’t be much further scaled (CMOS and mm-wave)
- $g_m/W_g$ (mS/μm) hard to increase → $C_{end}/g_m$ prevents $f_t$ scaling
- Move source-drain further away → HEMTs
Reduce Noise Figure – What Device?

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HEMTs
- Gate leakage current density → small CBO of InAlAs to InGaAs
- $R_s$ associated with getting electrons through widegap modulation doped link
Reduce Noise Figure – What Device?

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**HEMTs**
- Gate leakage current density → small CBO of InAlAs to InGaAs
- $R_S$ associated with getting electrons through widegap modulation doped link

**MOS-HEMTs**
- Replace InAlAs gate dielectric with high-$k$
  - Reduces gate leakage, increases $C_{g-ch}$, increases $g_m$, increases $f_t$
  - Better electrostatics, increases $g_m/G_{DS}$, increases $f_{max}$
- Regrowth process rather than recess etch process
  - Place N+ source-drain directly on channel, reduces $R_S$, increase $g_m$
Device 1 – Link Wet Etched
Device 1 – Device Structure

<table>
<thead>
<tr>
<th>$t_{ch}$</th>
<th>Channel Material</th>
<th>ZrO$_2$ Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 nm</td>
<td>InGaAs</td>
<td>30</td>
</tr>
</tbody>
</table>
Device 1 – DC Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak $g_m$</td>
<td>1.6 mS/µm</td>
</tr>
<tr>
<td>$R_A$</td>
<td>69 Ω•µm</td>
</tr>
<tr>
<td>$I_{on}$</td>
<td>&gt; 0.75 mA/µm</td>
</tr>
<tr>
<td>$I_{off}$</td>
<td>&gt; 1.0 µA/µm</td>
</tr>
<tr>
<td>$I_g$</td>
<td>&lt; 10 nA/µm</td>
</tr>
<tr>
<td>Long $L_g SS_{min}$</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Same as [1]  →  likely large $R_{end}$ due to isotropic undercut, $R_{vert}$ likely lower
**Device 1 – Peak Performance**

- Peak $f_T = 356$ GHz and $f_{\text{max}} = 403$ GHz on the same device ($L_g = 12$ nm (011) conduction)
- Shift to larger $V_{GS}$ due to thin channel and higher $V_{DS}$
- Why aren’t $g_m$ and $f_t$ larger? Channel is thin, have high-k, both should be high!
Thin Channels are not the Whole Picture

• Thin channel gives large $C_{QW}$ and $C_{DOS}$
  • $C_{QW}$: Wave-function moves towards oxide
  • $C_{DOS}$: in-plane effective mass increases

Wave function has “thickness”

\[ C = \frac{\varepsilon_{ch}}{t_{ch}/2} \]

Fermi Level moves to populate low DOS

\[ C = \frac{g_v m^* q^2}{2\pi\hbar^2} \]

\[ g_m \equiv \frac{\partial I_D}{\partial V_{GS}} \propto \sqrt{(C_{GS}[V_G - V_T])} \]
Thin Channels are not the Whole Picture

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**Wave function has “thickness”**

- Oxide
- Channel
- Back Barrier

**Fermi Level moves to populate low DOS**

- Oxide
- Channel
- Back Barrier

\[
g_m \equiv \frac{\partial I_D}{\partial V_{GS}} \propto \sqrt{(C_{GS}[V_G - V_T])}
\]
Ultra-thin Body Quantum Wells

- Maximum $(V_{gs} - V_{th}) \propto (E_F - E_1)$, depends on band offset of channel | back barrier

- Thin Channel Take-Aways:
  - Larger $E_1 \propto \frac{1}{m^* t^2}$ → less available $(E_F - E_1)$, small $m^*$ channels $\rightarrow E_1$ move faster
  - Channel needs to be thick enough for small $E_1 = \text{high } g_{m,i}, I_{DS}$
  - Channel needs to be thin enough for high $C_{gs,i}$ and high aspect ratio $(g_m / G_{DS})$
  - Sweet spot ~6-10nm, unsurprisingly consistent with SOA MOSFETs and HEMTs
Device 1 – Take Away

1. Wet etching gives unpredictable link region profile
2. $R_S$ moderately reduced but isotropic profile not worth reduction
   • Results in larger $R_L$ due to resistive ends
3. Thin channels limit maximum $g_m$
4. Low $I_g \rightarrow$ room to thin high-k
5. Optimize channel thickness $\rightarrow$ thicker **NOT** thinner
Device 2 - Fabrication

Composite Channel

InP → HSQ

InGaAs

Fe:InP → Fe:InP → Fe:InP

InAlAs → InAlAs → InAlAs

T-Gate

N+ → N+ → N+

Fe:InP → Fe:InP → Fe:InP

InAlAs → InAlAs → InAlAs
Device 2 – Device Structure

<table>
<thead>
<tr>
<th>$t_{ch}$</th>
<th>Channel Material</th>
<th>ZrO$_2$ Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.0 nm</td>
<td>InAs / InGaAs</td>
<td>30</td>
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</tbody>
</table>
Device 2 – DC Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak $g_m$</td>
<td>2.4 mS/µm</td>
</tr>
<tr>
<td>$R_A$</td>
<td>49 – 55 Ω•µm</td>
</tr>
<tr>
<td>$I_{on}$</td>
<td>&gt; 1.45 mA/µm</td>
</tr>
<tr>
<td>$I_{off}$</td>
<td>&lt; 10 nA/µm</td>
</tr>
<tr>
<td>$I_g$</td>
<td>&lt; 10 nA/µm</td>
</tr>
<tr>
<td>Long $L_g SS_{min}$</td>
<td>76 mV/dec</td>
</tr>
</tbody>
</table>
Device 2 – Peak Performance – $L_g = 40 \text{ nm}$, $W_{\text{mesa}} = 10\mu\text{m}$

- Peak $f_\tau = 420 \text{ GHz}$ on $L_g = 40 \text{ nm}$ (011) conduction device, peak $f_{\text{max}}$ at $L_g = 50 \text{ nm}$
- Extrapolation of $f_{\text{max}}$ difficult because of noisy U $\rightarrow$ occasionally see “spiking”
Deice 2 – Take Away

1. Link thinning gives excellent $R_S$ and predictable profile
2. Peak $g_m$ likely limited source-starvation $\rightarrow$ need more $n_{Link}$
3. Low $I_g$ $\rightarrow$ room to thin high-k
4. Need to improve T-Gate process to reduce $C_{GS,p}$ and $C_{GD,p}$
Conclusions

1. Extremely high $g_m = 2.9 \text{ mS/µm}$ $\rightarrow$ competitive with SOA HEMTs
2. Extremely low $R_s < 100 \, \Omega \cdot \mu\text{m}$ $\rightarrow$ will increase with InAlAs link
3. Extremely low $g_{ds} = 0.2 \, \text{mS/µm}$ $\rightarrow$ significantly better than SOA HEMTs
4. Improving high frequency FOMs $\rightarrow f_T, f_{\text{max}} > 400 \, \text{GHz}$
5. Need to improve T-Gate process to reduce parasitics!
MOS-HEMT Future Work

Problems:
• Peak $f_T$ severely limited by large $C_{GS,p} \rightarrow$ need a self-aligned process
• Peak $f_{max}$ limited by large $R_G$ (poor yield & reproducibility) $\rightarrow$ improve T-Gate process
• Low breakdown voltage and therefore low power-handling $\rightarrow$ wide $E_g$ channel

Solutions:
• Self-Aligned "Regrowth Reversal" Process $\rightarrow$ reduces $C_{GS,p}$ and improves T-Gate process
• Wide-bandgap back-barriers (AlAsSb) for improved $G_{DS}$
• InP channel / AlAsSb back-barrier MOS-HEMT for high-power
Acknowledgements

**Funding:** DARPA ComSenTer
QUESTIONS
FET Scaling Laws (Now Broken)

<table>
<thead>
<tr>
<th>FET parameter</th>
<th>change</th>
</tr>
</thead>
<tbody>
<tr>
<td>gate length</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>current density (mA/mm)</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>specific transconductance (mS/mm)</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>transport mass</td>
<td>constant</td>
</tr>
<tr>
<td>2DEG electron density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>gate-channel capacitance density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>dielectric equivalent thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>channel thickness</td>
<td>decrease 2:1</td>
</tr>
<tr>
<td>channel state density</td>
<td>increase 2:1</td>
</tr>
<tr>
<td>contact resistivities</td>
<td>decrease 4:1</td>
</tr>
</tbody>
</table>

Wave function has “thickness”

Fermi Level moves to populate low DOS
\[ V_{DS} = 0.70 \text{ V} \]
\[ V_{GS} = 0.30 \text{ V} \]
\[ I_{DS} = 0.852 \text{ mA/\mu m} \]

Device 0 SSEC: \( L_g = 8 \text{ nm} \)

\[ f_t = 533 \text{ GHz} \]
\[ f_{max} = 204 \text{ GHz} \]
Device 1 SSEC: $L_g = 12 \text{ nm}$

- $R_{loss} = 200 \text{ k}\Omega$
- $C_{gd} = 4.4 \text{ fF}$
- $C_{ds} = 32 \text{ fF}$
- $R_{Leak} = 65 \text{ }$
- $V_{DS} = 1.00 \text{ V}$
- $V_{GS} = 0.50 \text{ V}$
- $I_{DS} = 0.664 \text{ mA/\mu m}$
- $f_T = 375 \text{ GHz}$
- $f_{max} = 326 \text{ GHz}$

SSEC very difficult to fit... do not trust this model
Device 2 SSEC: \( L_g = 40 \text{ nm} \)

- Significantly improved fit, trustable

- \( f_\tau = 454 \text{ GHz} \)
- \( f_{\text{max}} = 567 \text{ GHz} \)

- \( V_{DS} = 0.70 \text{ V} \)
- \( V_{GS} = 0.30 \text{ V} \)
- \( I_{DS} = 0.852 \text{ mA/\mu m} \)
# Model vs. Extrapolation

<table>
<thead>
<tr>
<th>Device</th>
<th>Extraction</th>
<th>$L_g$ (nm)</th>
<th>$f_T$ (GHz)</th>
<th>$f_{max}$ (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Extrapolation</td>
<td>8</td>
<td>511</td>
<td>256</td>
</tr>
<tr>
<td>0</td>
<td>Modeled</td>
<td>8</td>
<td>533</td>
<td>204</td>
</tr>
<tr>
<td>1</td>
<td>Extrapolation</td>
<td>12</td>
<td>356</td>
<td>398</td>
</tr>
<tr>
<td>1</td>
<td>Modeled</td>
<td>12</td>
<td>375</td>
<td>326</td>
</tr>
<tr>
<td>2</td>
<td>Extrapolation</td>
<td>40</td>
<td>402</td>
<td>560</td>
</tr>
<tr>
<td>2</td>
<td>Modeled</td>
<td>40</td>
<td>454</td>
<td>567</td>
</tr>
</tbody>
</table>
[1] Device 0 - Fabrication

Composite Channel

InAlAs

Fe:InP

InP

HSQ

InGaAs

T-Gate

N+

Fe:InP

InAlAs

Fe:InP

InAlAs

Fe:InP

N+

Fe:InP

InAlAs

Fe:InP
[1] Device 0 – Device Structure

<table>
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<tr>
<td>6.5 nm</td>
<td>InAs / InGaAs</td>
<td>40</td>
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</table>
[1] Device 0 – DC Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Peak $g_m$</td>
<td>2.2 mS/µm</td>
</tr>
<tr>
<td>$R_A$</td>
<td>68 – 85 Ω•µm</td>
</tr>
<tr>
<td>$I_{on}$</td>
<td>&gt; 0.90 mA/µm</td>
</tr>
<tr>
<td>$I_{off}$</td>
<td>&gt; 1.0 µA/µm</td>
</tr>
<tr>
<td>$I_g$</td>
<td>&lt; 10 pA/µm</td>
</tr>
<tr>
<td>Long $L_g SS_{min}$</td>
<td>N/A</td>
</tr>
</tbody>
</table>
[1] Device 0 – Peak Performance

$V_{GS} = -0.5V$ to $0.5V$ by $0.1V$

Drain Current (mA/μm) vs Drain Voltage (V)

Peak $f_t$
- MSG/MAG
- $H_{21}$
- Unilateral Gain

$f_t = 511$ GHz
$f_{max} = 256$ GHz

$V_{DS} = 0.70$ V
$V_{GS} = 0.20$ V
$I_{DS} = 0.778$ mA/μm

Gain (dB) vs Frequency (GHz)
Device 1 – RF Characteristics

- **Balanced** \( f_{\tau}, f_{\text{max}} \)
  - Rapid drop in FOMs due to thin channel

- **Extremely high** \( C_{GS} \approx 0.9 \text{ fF/\mu m} \)
  - \( C_{GD} \approx 0.3 \text{ fF/\mu m} \)
  - \( C_{DS} \approx 0.9 \text{ fF/\mu m} \)

- **Low peak** \( g_{m,e} \approx 2.0 \text{ mS/\mu m} \)
  - \( g_{ds,e} \approx 0.3 \text{ mS/\mu m} \)

- **Improved** \( R_G \leq 10 \Omega \)

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**Graphs:**

- **Graph a)**: Variation of FOMs with gate length.
- **Graph b)**: Capacitance variation with gate length.
- **Graph c)**: Gate resistance variation with gate length.
- **Graph d)**: Conductance variation with gate length.
Device 2 – RF Characteristics

**Balanced** $f_r$, $f_{max}$
- Gradually decreasing $f_r$
- Constant / increasing $f_{max}$

**Capacitance (fF/µm)**
- Extremely high $C_{GS} \approx 0.9$ fF/µm
- High $C_{GD} \approx 0.4$ fF/µm

**Gate Resistance (Ω)**
- Maintained $R_G \leq 10$ Ω

**Conductance (mS/µm)**
- High peak $g_{m,e} \approx 2.9$ mS/µm
- Excellent $g_{ds,e} \approx 0.2$ mS/µm
# HEMT / MOS-HEMT State-of-the-Art

<table>
<thead>
<tr>
<th>Institution</th>
<th>Device</th>
<th>Year</th>
<th>$g_m$ (mS/µm)</th>
<th>$f_t$ (GHz)</th>
<th>$f_{\text{max}}$ (GHz)</th>
<th>$\sqrt{f_t \cdot f_{\text{max}}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Teledyne</td>
<td>HEMT</td>
<td>2011</td>
<td>2.75</td>
<td>688</td>
<td>800</td>
<td>742</td>
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<tr>
<td>Tokyo Tech</td>
<td>HEMT</td>
<td>2013</td>
<td>2.1</td>
<td>710</td>
<td>478</td>
<td>583</td>
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<tr>
<td>NGC</td>
<td>HEMT</td>
<td>2015</td>
<td>3.1</td>
<td>610</td>
<td>1500</td>
<td>957</td>
</tr>
<tr>
<td>NTT</td>
<td>HEMT</td>
<td>2019</td>
<td>2.8</td>
<td>703</td>
<td>820</td>
<td>759</td>
</tr>
<tr>
<td>Fraunhaufer</td>
<td>MOS-HEMT</td>
<td>2019</td>
<td>2.4</td>
<td>275</td>
<td>640</td>
<td>420</td>
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<tr>
<td>UCSB Gen. 0</td>
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<td>357</td>
<td>410</td>
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<tr>
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<td>511</td>
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<td>361</td>
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<td>UCSB Gen. 2</td>
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<td>379</td>
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<td>UCSB Gen. 3</td>
<td>MOS-HEMT</td>
<td>2020</td>
<td>2.9</td>
<td>406</td>
<td>562</td>
<td>477</td>
</tr>
</tbody>
</table>
MOS-HEMT Future Work

- Peak $f_T$ severely limited by large $C_{GS,p} \rightarrow$ need a self-aligned process
- Peak $f_{max}$ limited by large $R_G$ (poor yield & reproducibility) $\rightarrow$ improve T-Gate process
- Develop $> 1 \times 10^{19}$ cm$^{-3}$ In$_{0.52}$Al$_{0.48}$As for link region top barrier
- Elegantly *hopefully* solved in one simple process
MOS-HEMT Future Work
MOS-HEMT Future Work

Advantages
- Larger T-Gate aperture
- Improved RG
- Self-aligned Gate-Recess and T-Gate foot
- Self-aligned ohmics possible

Disadvantages
- Etching (dry & wet) in critical regions
- Topography on wafer before critical dimension definition
- Regrowth dynamics