L_g = 40nm Composite Channel MOS-HEMT Exhibiting f_τ = 420 GHz, f_{max} = 562 GHz

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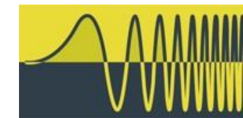
UCSB Department of Electrical and Computer Engineering

Funding: SRC & DARPA

JUMP
Joint University Microelectronics Program

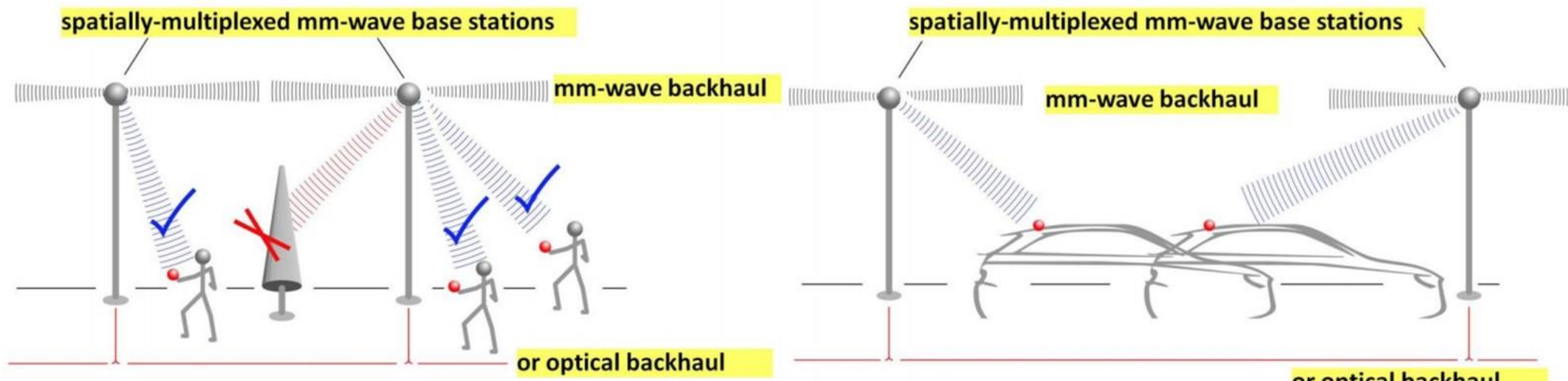


ComSenTer
COMMUNICATIONS SENSING TERAHERTZ

1. High f_{τ} , f_{max} HEMT Motivation
2. MOS-HEMT Advantage
3. Device 1 – Link Wet Etched
   - Fabrication
   - DC Characteristics
   - RF Characteristics
4. Device 2 – Link “Recessed”
   - Fabrication
   - DC Characteristics
   - RF Characteristics

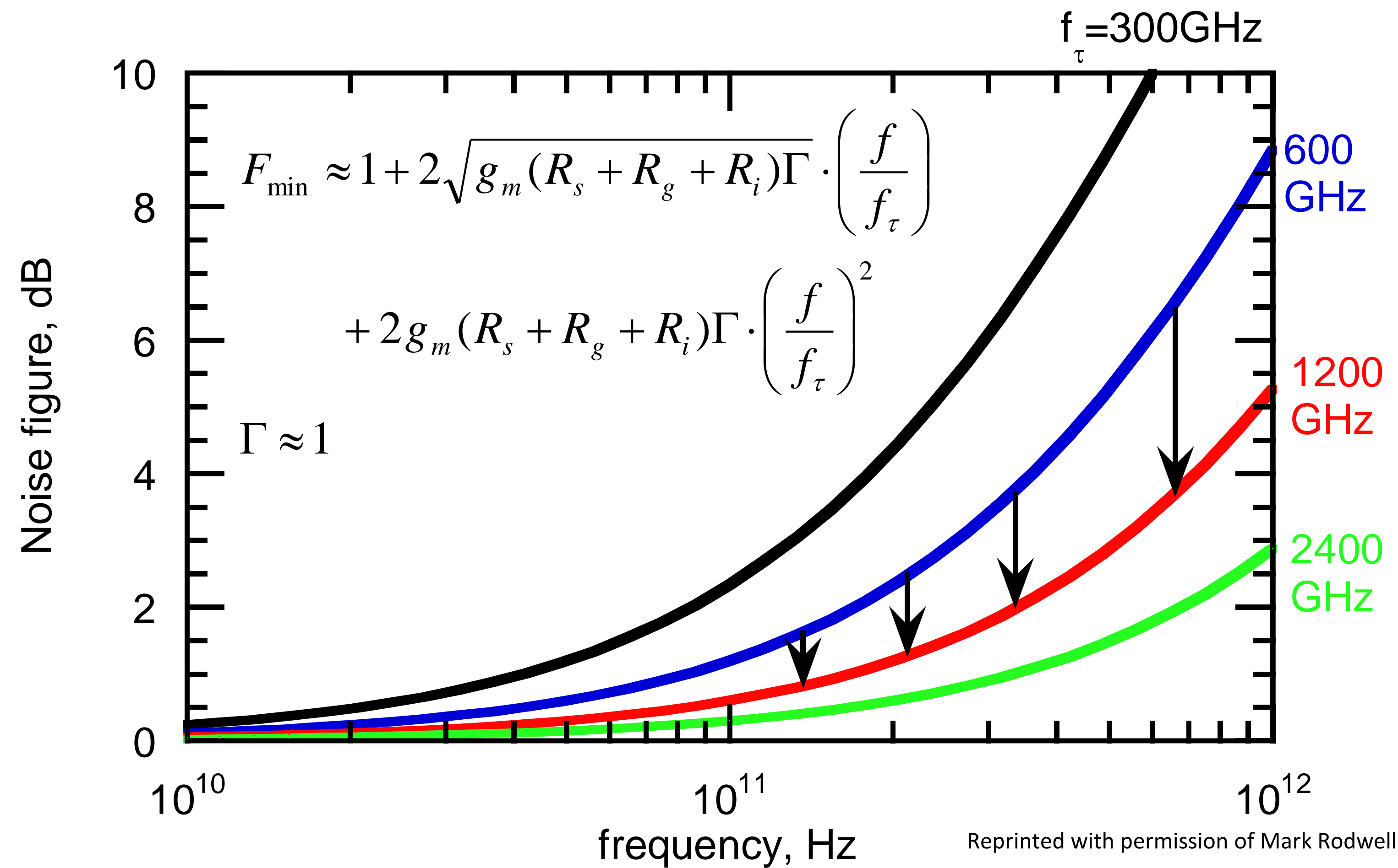
High f_τ , f_{max} HEMT Motivation

- Current electromagnetic bands are crowded
- Need to move into currently unallocated bands at higher frequencies
- Higher frequency = higher data rate = faster upload/download speeds
- For circuits to be efficient (high PAE) need $f_{op} \approx 0.1\text{-}0.2 \bullet f_{max}$
- Atmospheric attenuation means many base stations and spatial multiplexing



HEMT Motivation – Reduce Noise Figure

- *2:1 to 4:1 increase in f_τ:*
  - *Improved noise*
  - *Less required transmit power*
  - *Smaller PAs, less DC power*
- *Or higher-frequency systems*



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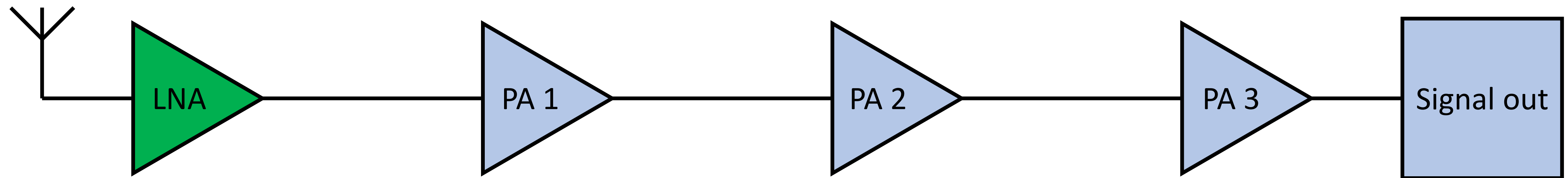
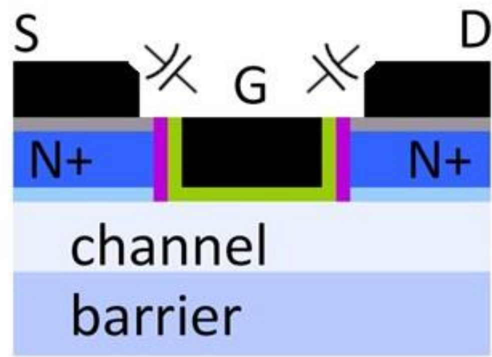
Noise Figure / Measure Considerations



$$F_\infty = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} \ldots \longrightarrow \mathrm{M} = F_\infty - 1$$

- Noise of cascaded amplifiers is more important than noise of one
- F_∞ can be big even if F_1 is small → cannot forget G_1
- Cannot forget about f_{max} → Need balanced f_τ , f_{max}

Reduce Noise Figure – What Device?



MOSFETs

- *Gate dielectric and L_g can't be much further scaled (CMOS and mm-wave)*
- *g_m/W_g (mS/μm) hard to increase → C_{end}/g_m prevents f_τ scaling*
- *Move source-drain further away → HEMTs*

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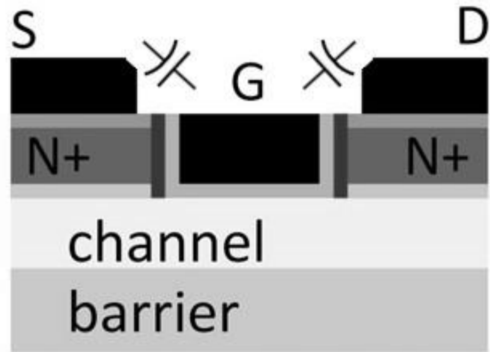

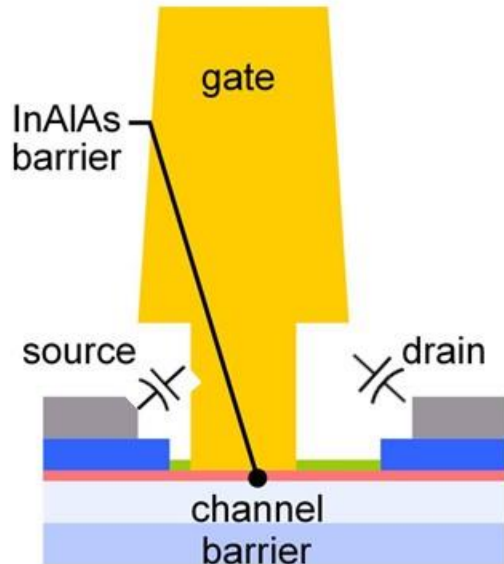

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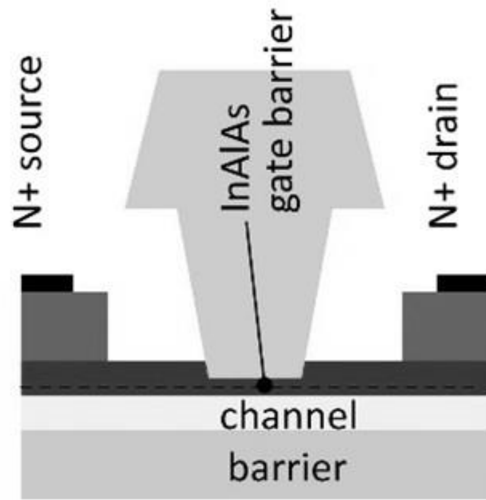
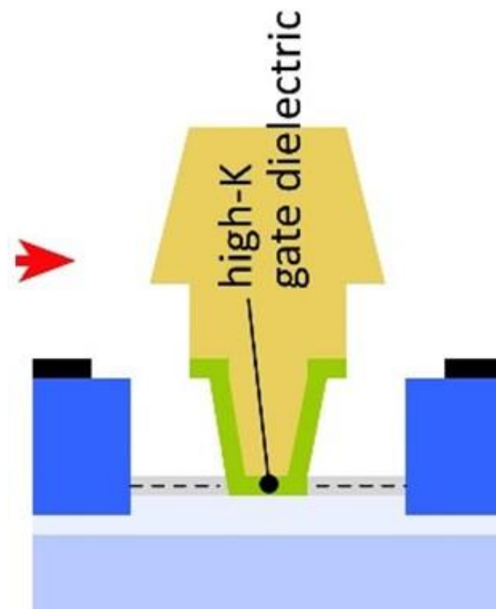
HEMTs

- *Gate leakage current density → small CBO of InAlAs to InGaAs*
- *R_S associated with getting electrons through widegap modulation doped link*

Reduce Noise Figure – What Device?





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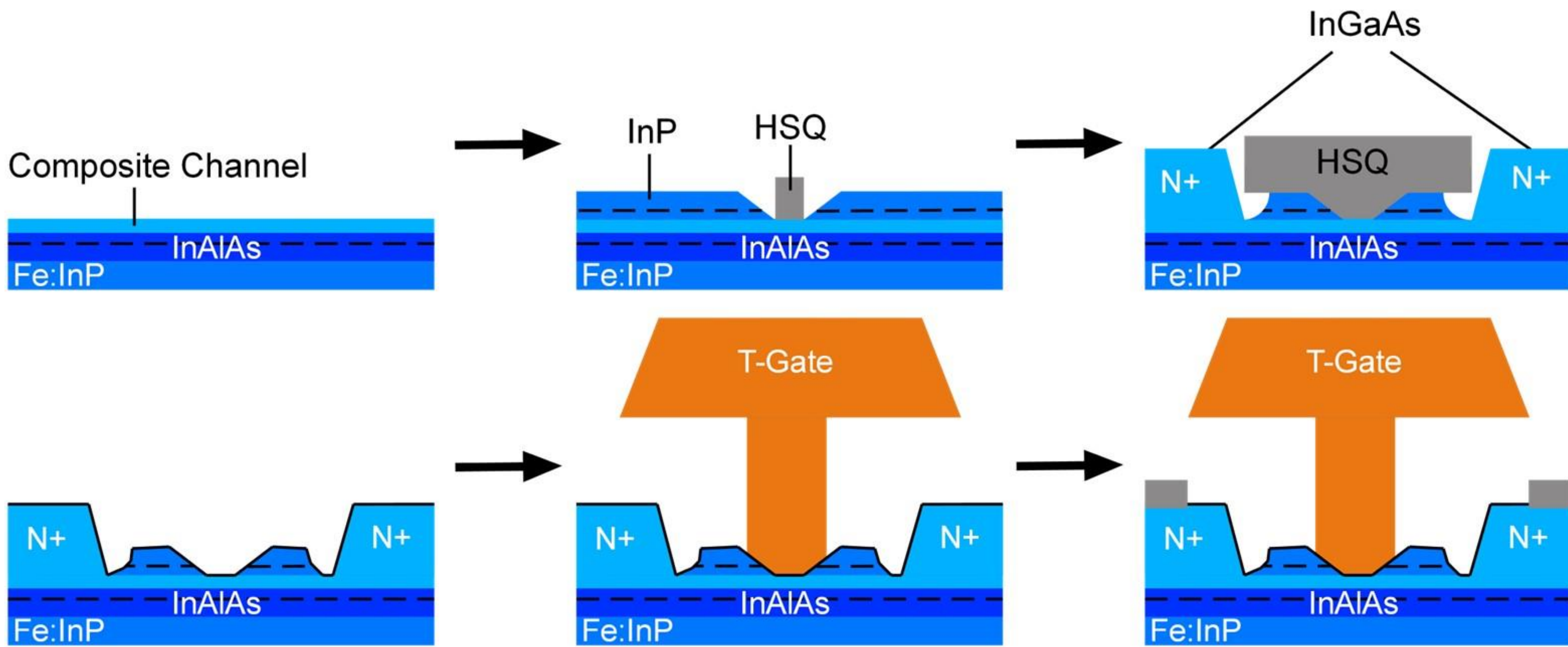
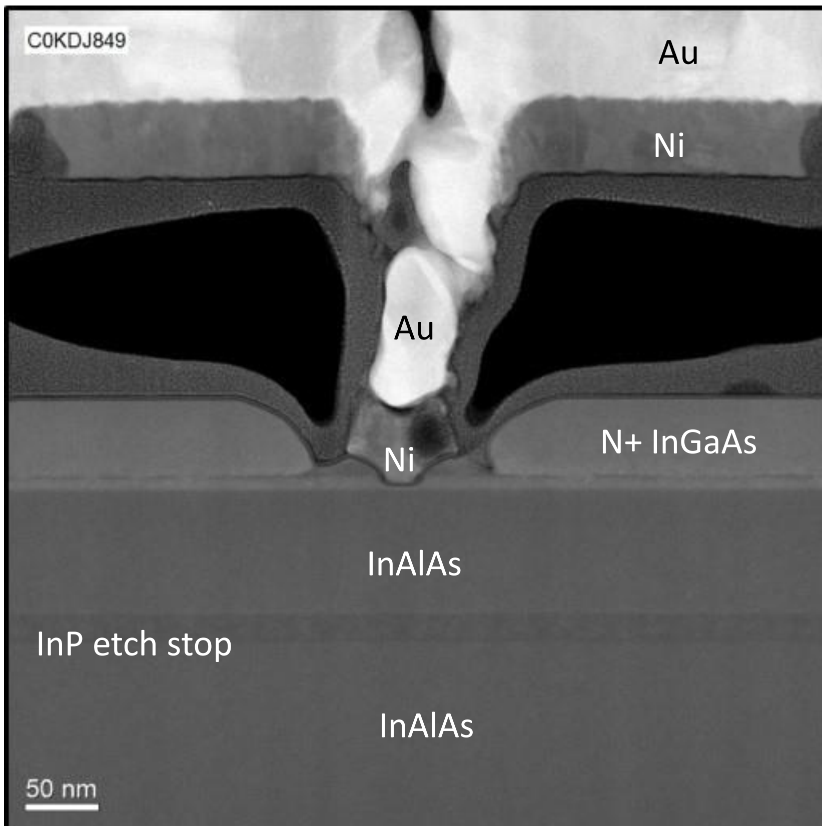
MOS-HEMTs

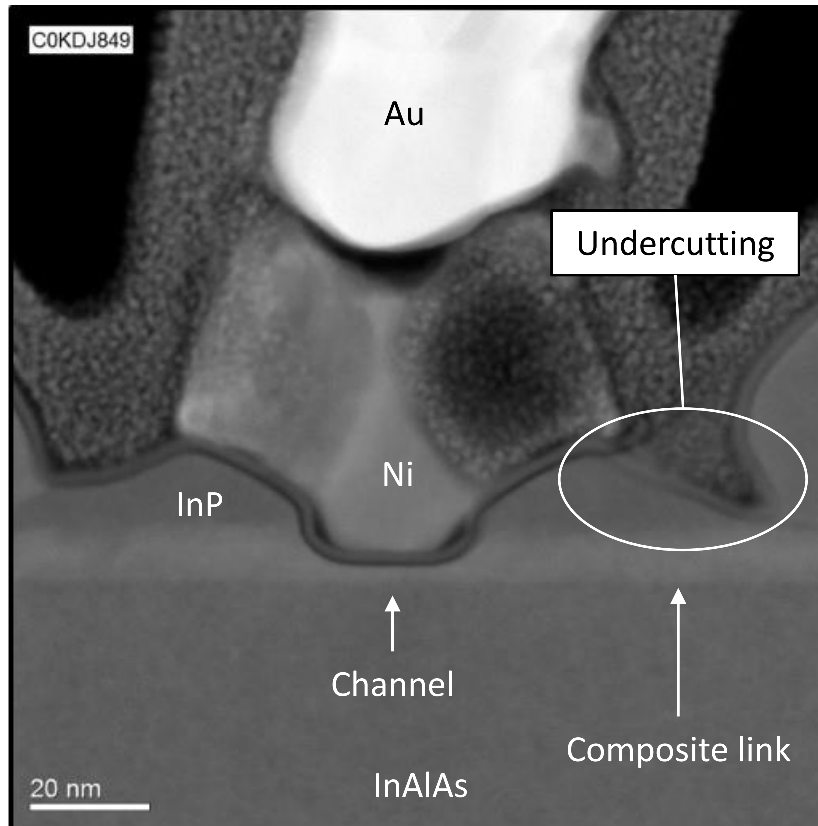
- *Replace InAlAs gate dielectric with high-k*
  - *Reduces gate leakage, increases C_{g-ch}, increases g_m, increases f_τ*
  - *Better electrostatics, increases g_m / G_{DS}, increases f_{max}*
- *Regrowth process rather than recess etch process*
  - *Place N+ source-drain directly on channel, reduces R_S, increase g_m*

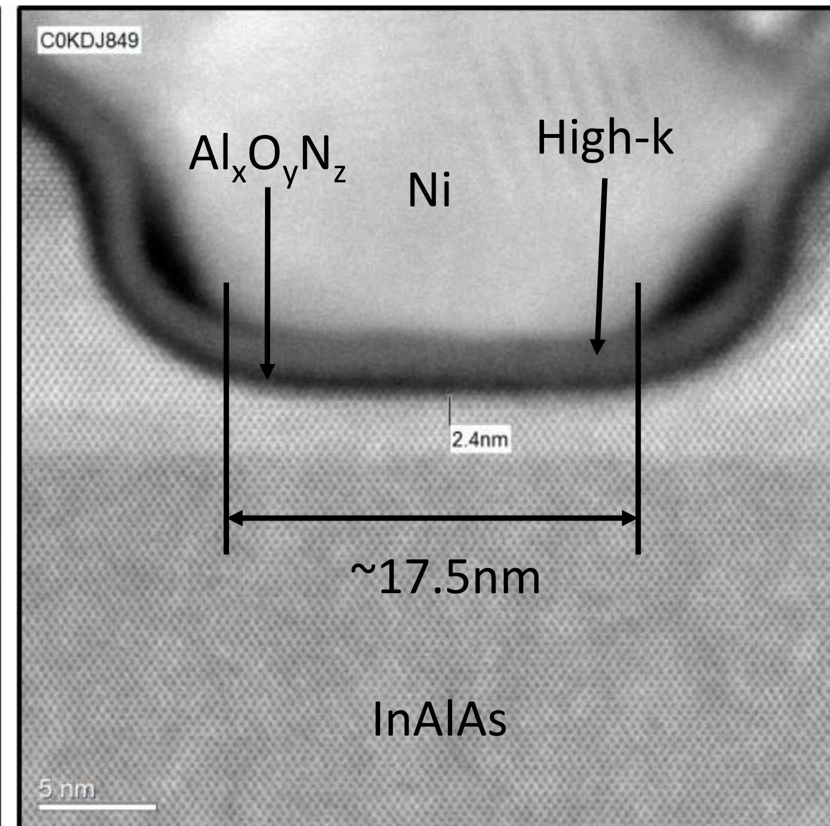
Device 1 – Link Wet Etched



Device 1 – Device Structure

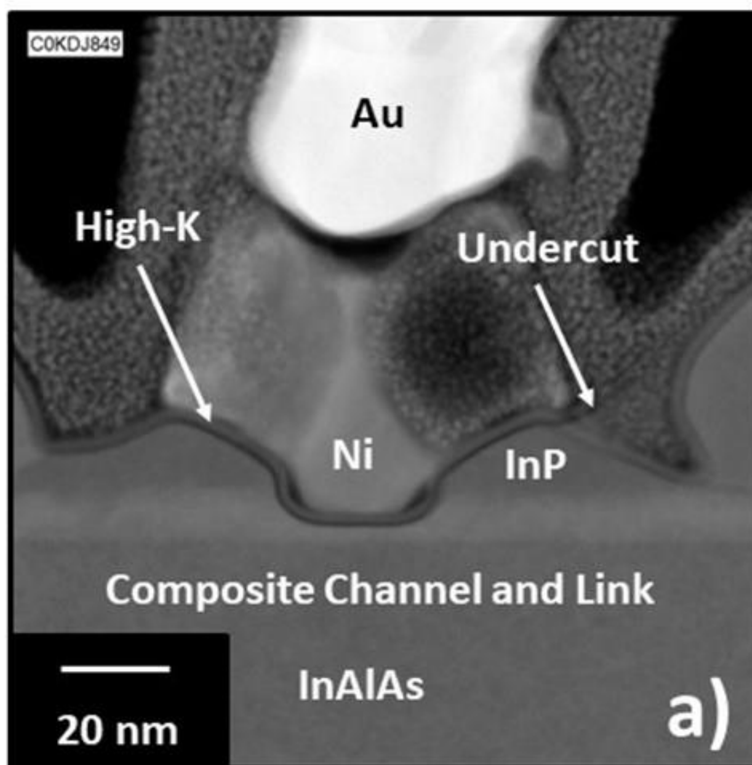


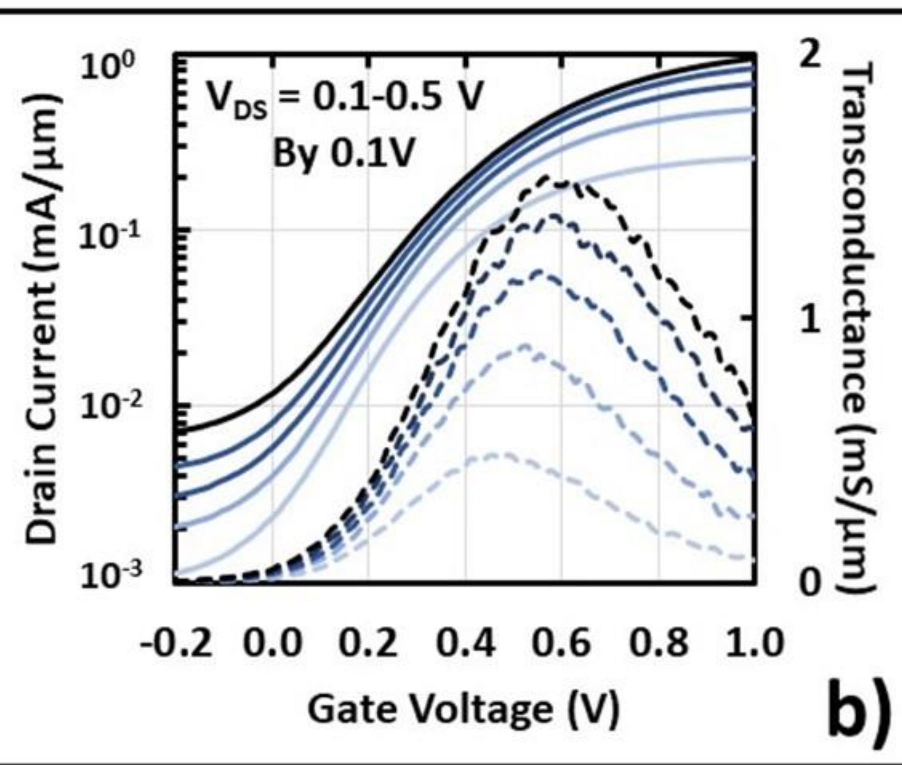


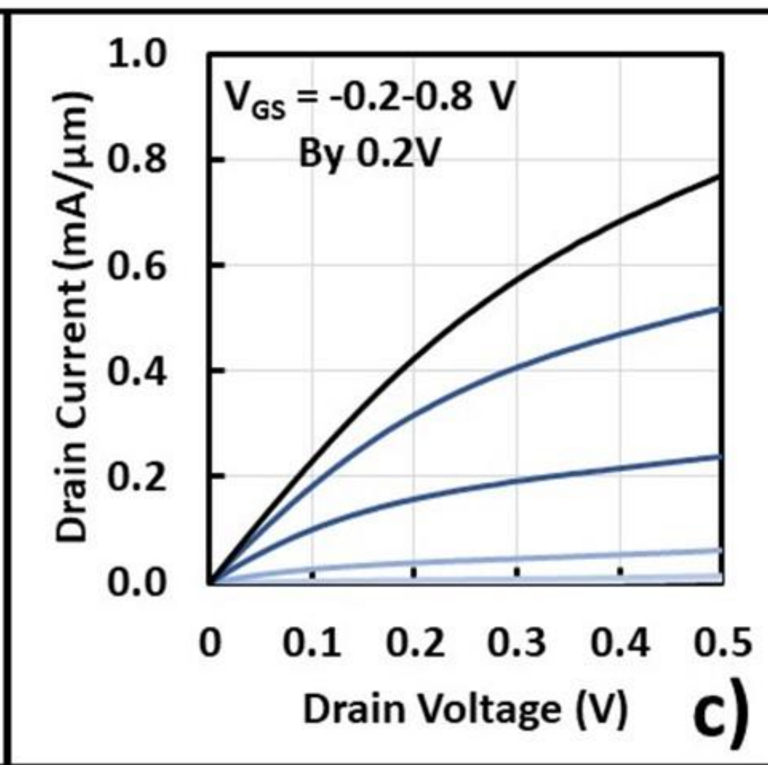


t_{ch}	Channel Material	ZrO_2 Cycles
2.5 nm	InGaAs	30

Device 1 – DC Characteristics



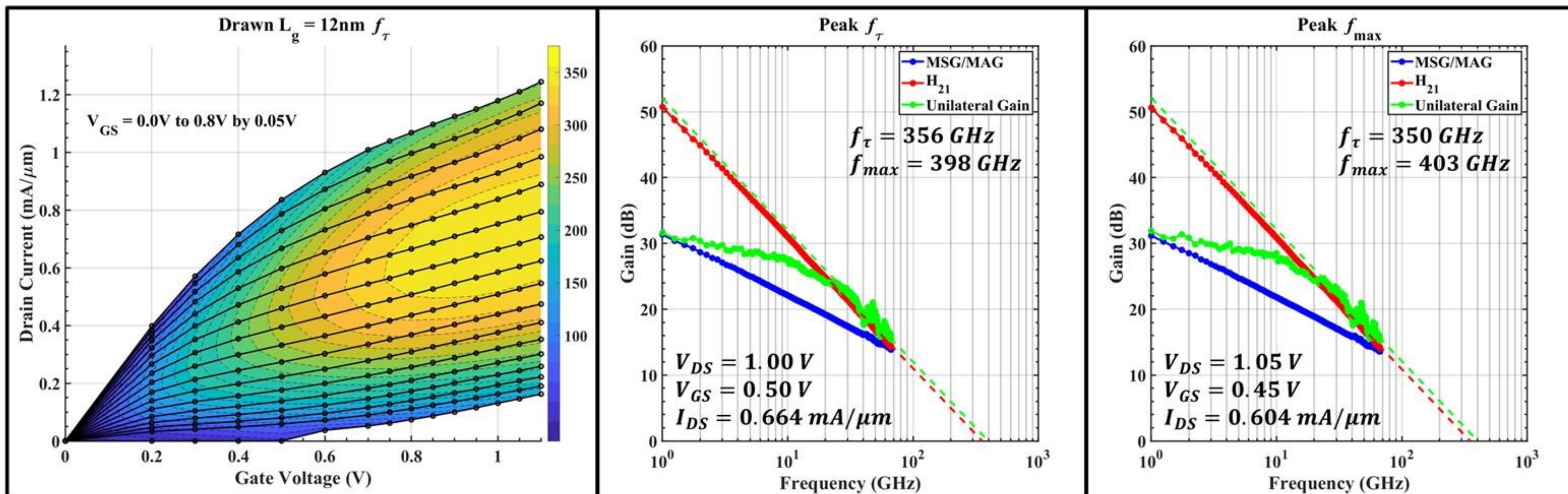




Same as [1] → likely large R_{end} due to isotropic undercut, R_{vert} likely lower

Peak g_m	R_A	I_{on}	I_{off}	I_g	Long L_g SS_{min}
1.6 mS/µm	69 Ω•µm	> 0.75 mA/µm	> 1.0 µA/µm	< 10 nA/µm	N/A

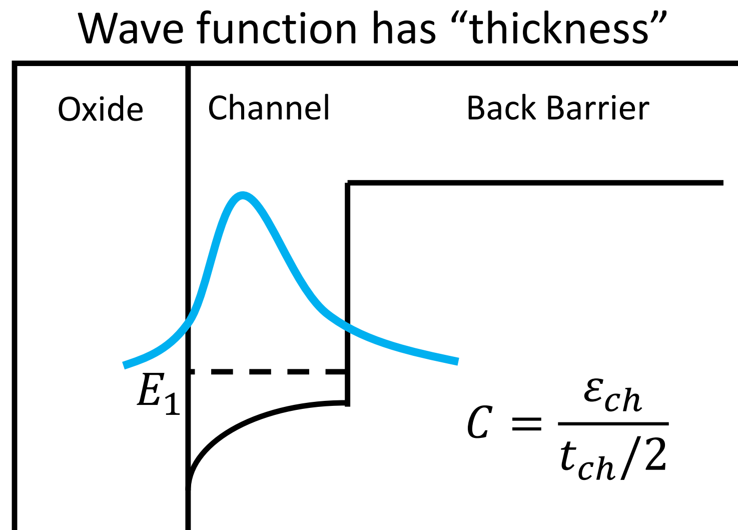
Device 1 – Peak Performance

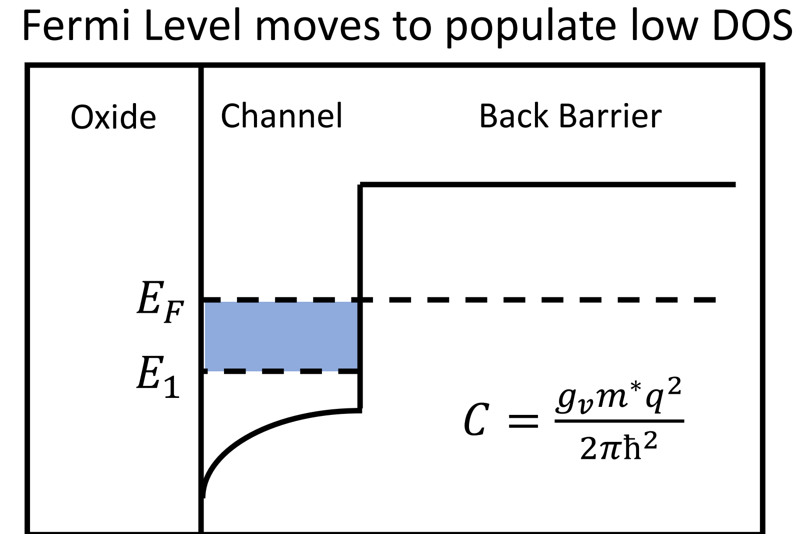


- Peak f_τ = 356 GHz and f_{max} = 403 GHz on the same device (L_g = 12 nm (011) conduction)
- Shift to larger V_{GS} due to thin channel and higher V_{DS}
- Why aren't g_m and f_t larger? Channel is thin, have high-k, both should be high!

Thin Channels are not the Whole Picture

- Thin channel gives large C_{QW} and C_{DOS}
  - C_{QW}: Wave-function moves towards oxide
  - C_{DOS}: in-plane effective mass increases





$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} \propto \sqrt{(C_{GS}[V_G - V_T])}$$

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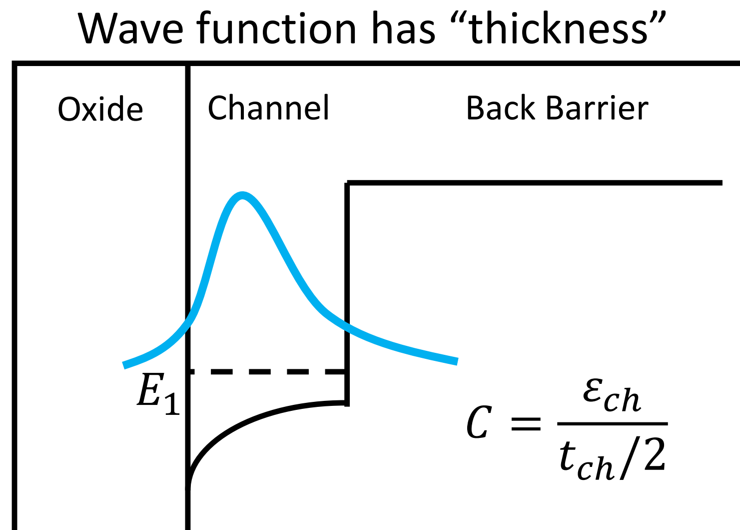
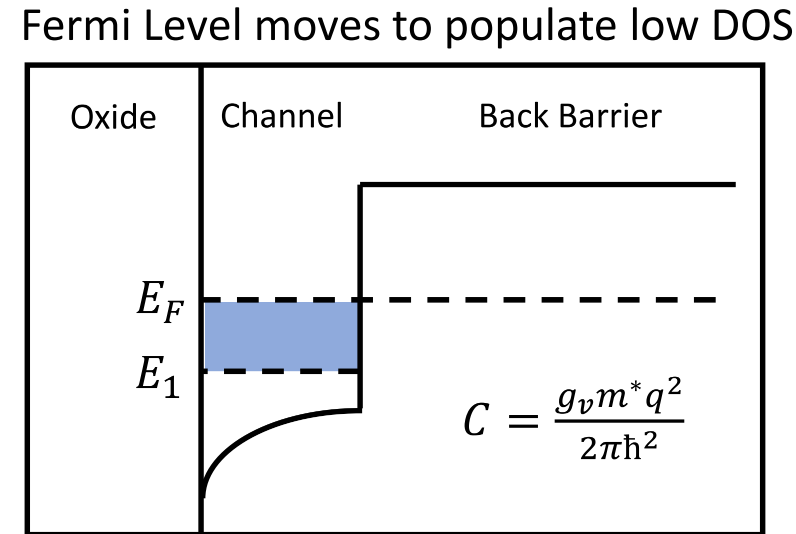
Wave function has "thickness"



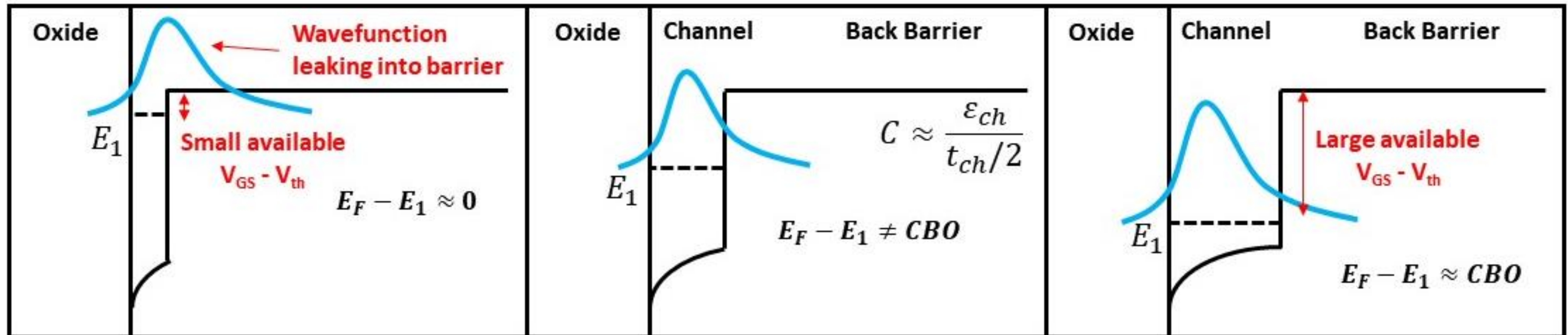
Fermi Level moves to populate low DOS



$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} \propto \sqrt{(C_{GS}[V_G - V_T])}$$

Ultra-thin Body Quantum Wells

- Maximum $(V_{gs} - V_{th}) \propto (E_F - E_1)$, depends on band offset of channel | back barrier

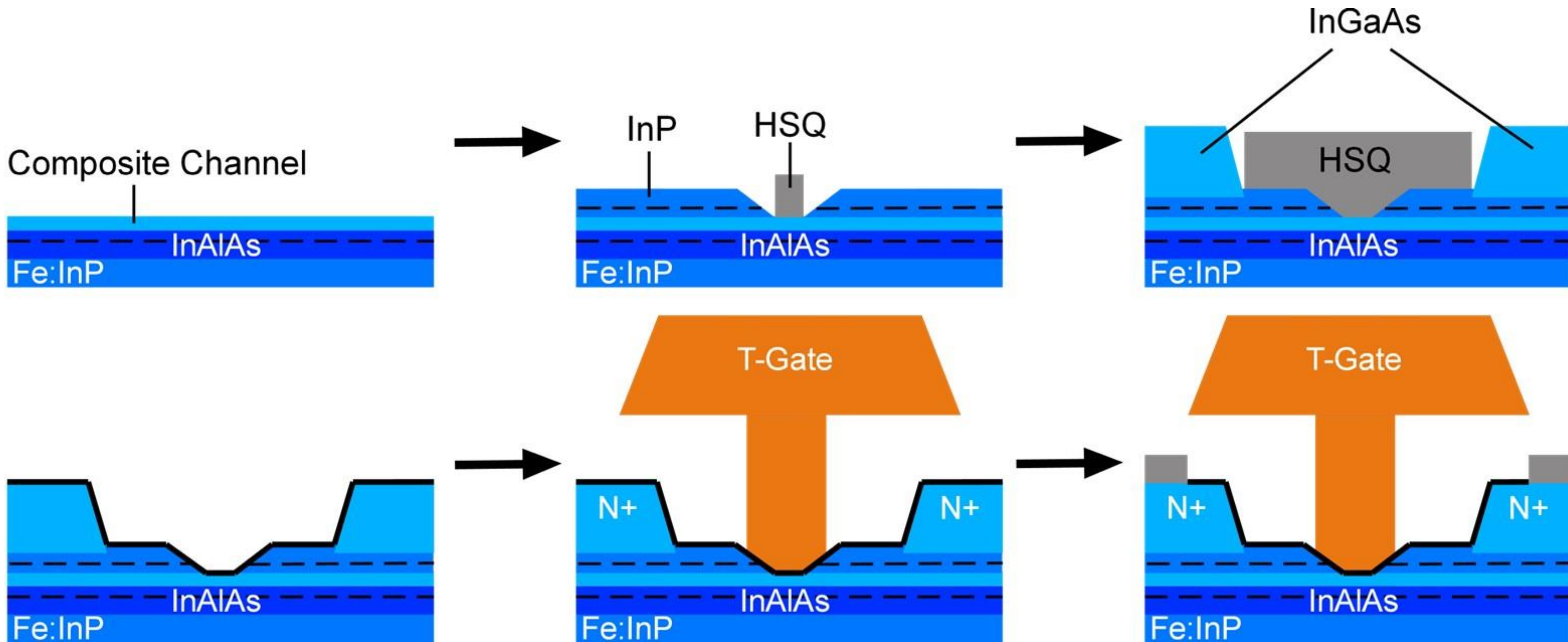


- Thin Channel Take-Aways:
  - Larger $E_1 \propto \frac{1}{m^* t^2}$ → less available $(E_F - E_1)$, small m^* channels → E_1 move faster
  - Channel needs to be thick enough for small E_1 = high $g_{m,i}$, I_{DS}
  - Channel needs to be thin enough for high $C_{gs,i}$ and high aspect ratio (g_m / G_{DS})
  - Sweet spot ~6-10nm, unsurprisingly consistent with SOA MOSFETs and HEMTs

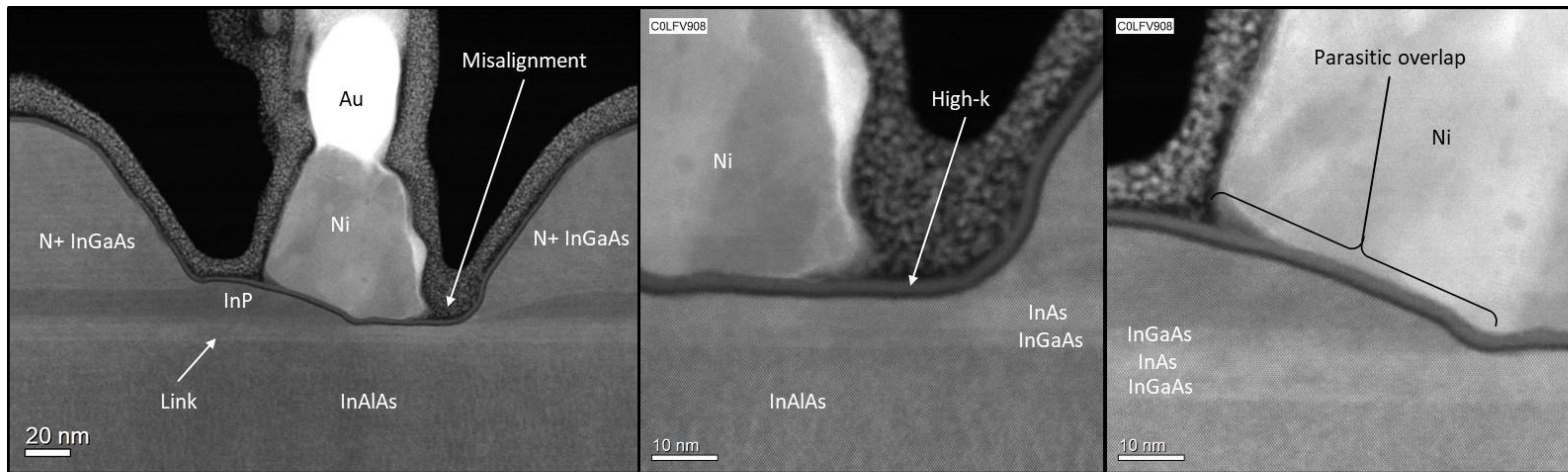
Device 1 – Take Away

1. Wet etching gives unpredictable link region profile
2. R_S moderately reduced but isotropic profile not worth reduction
   - Results in larger R_L due to resistive ends
3. Thin channels limit maximum g_m
4. Low I_g → room to thin high-k
5. Optimize channel thickness → thicker **NOT** thinner

Device 2 - Fabrication

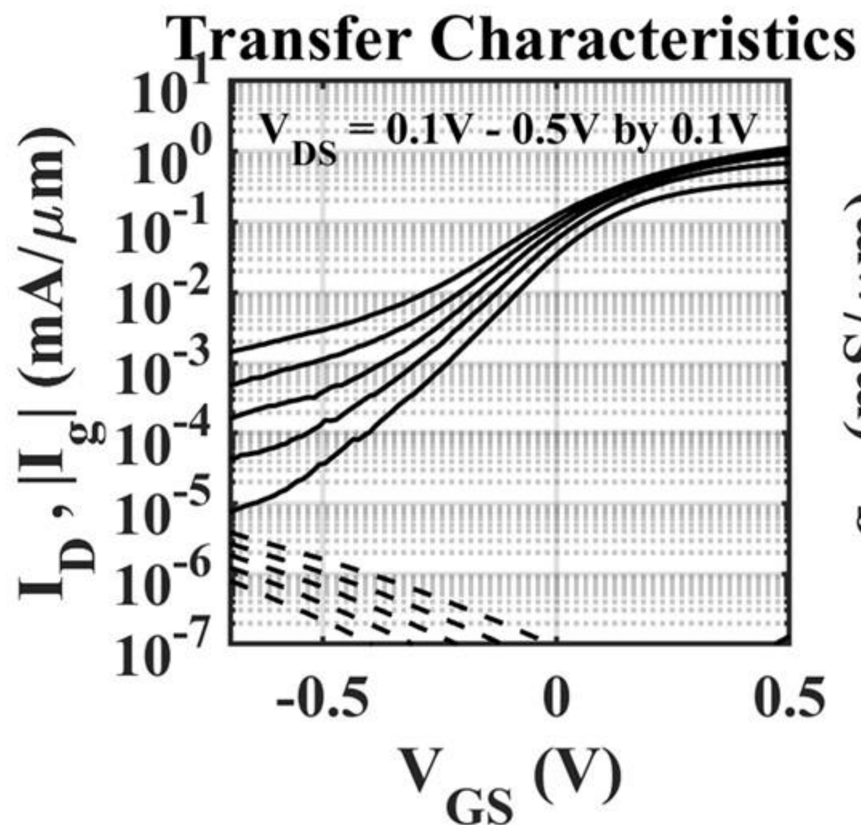


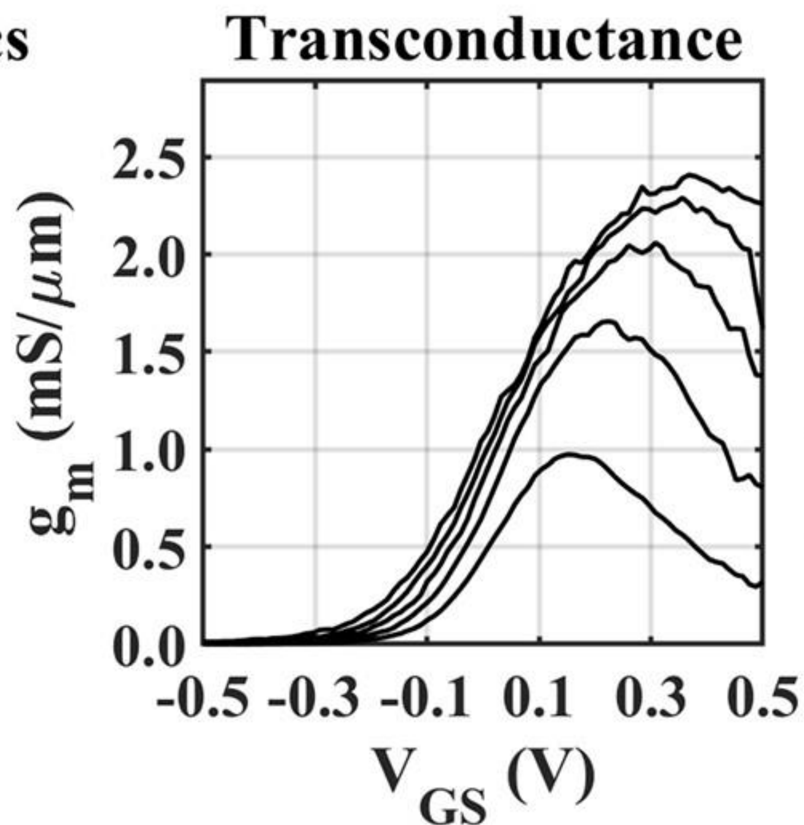
Device 2 – Device Structure

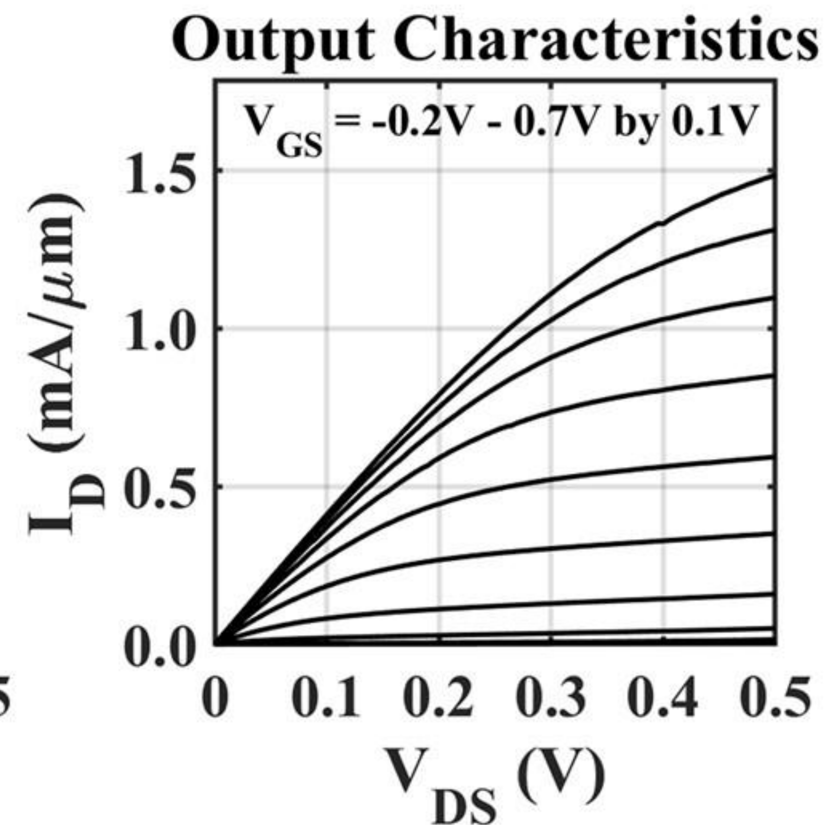


t_{ch}	Channel Material	ZrO_2 Cycles
7.0 nm	InAs / InGaAs	30

Device 2 – DC Characteristics

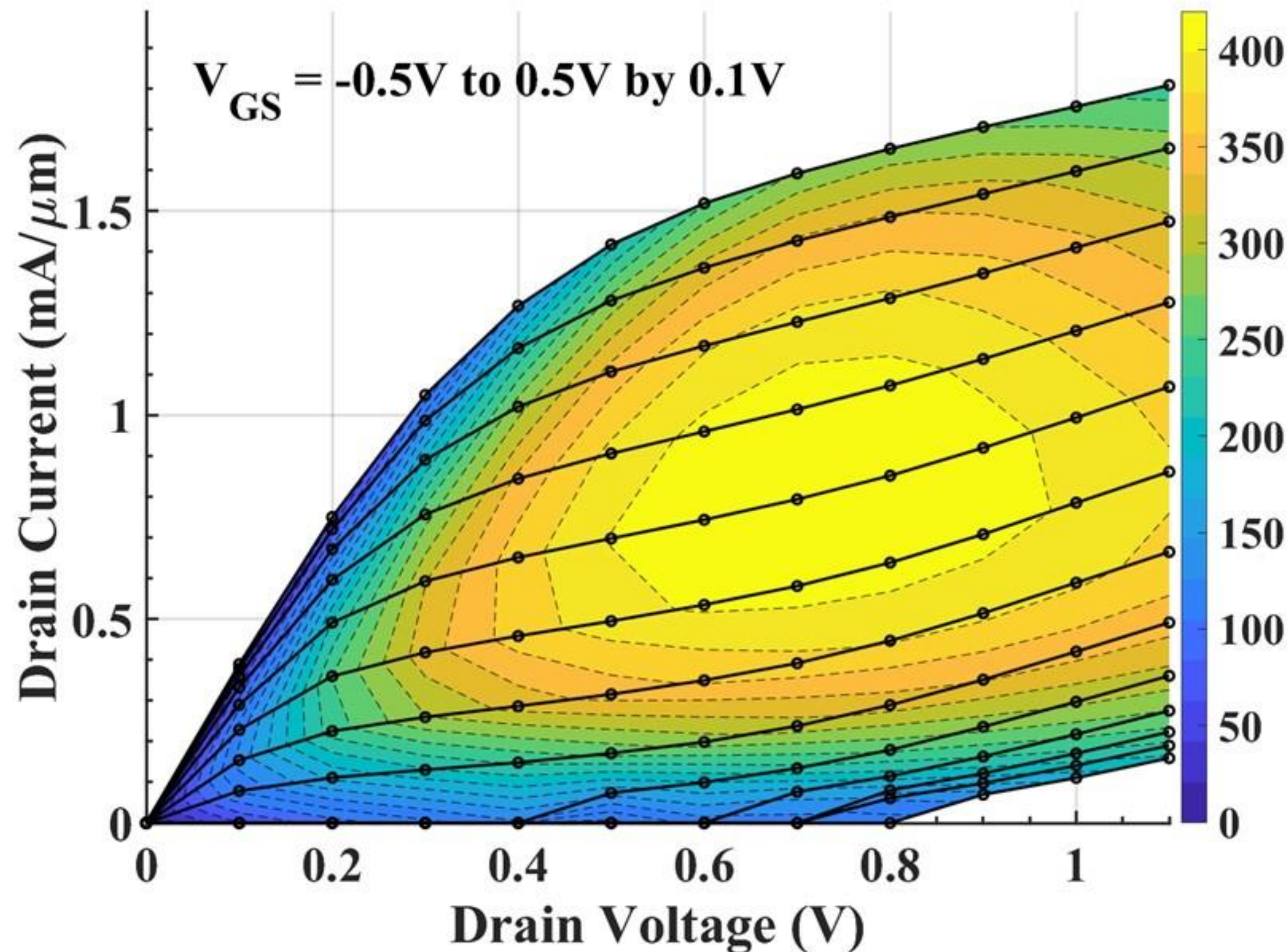


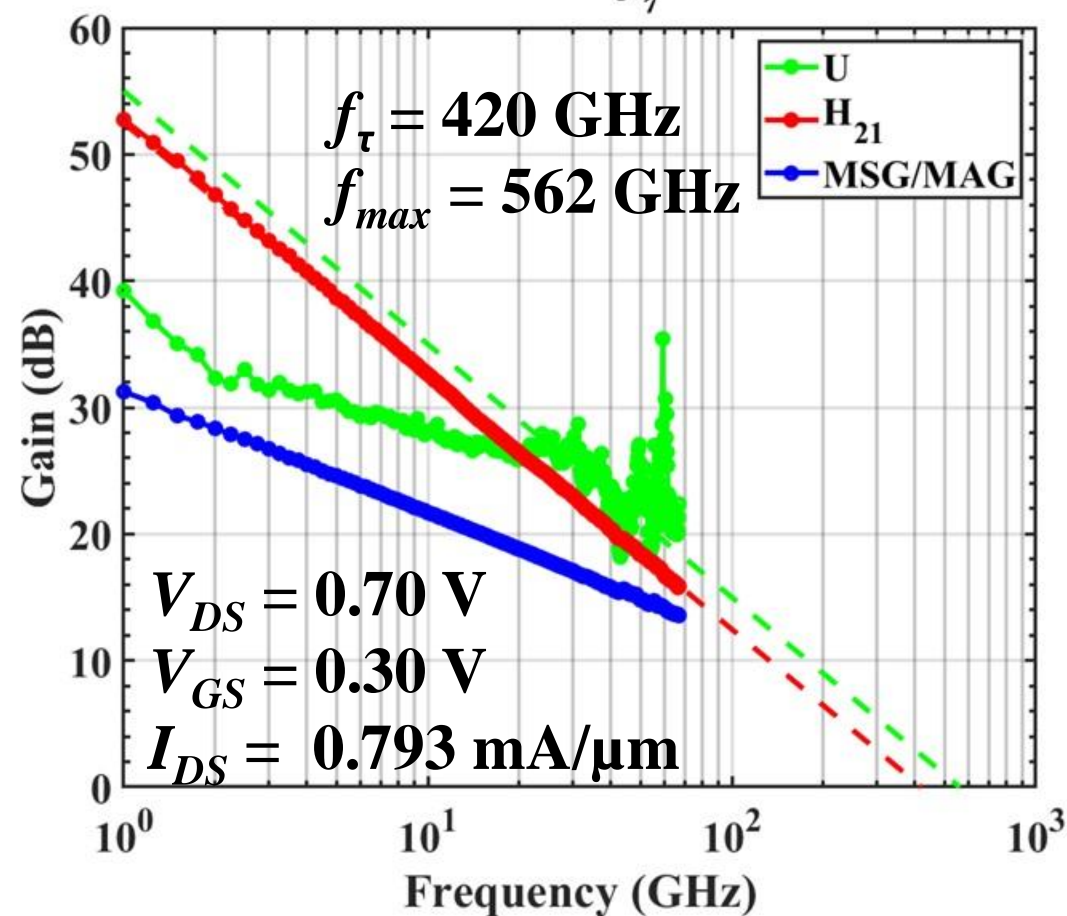




Peak g_m	R_A	I_{on}	I_{off}	I_g	Long L_g SS_{min}
2.4 mS/μm	49 – 55 Ω•μm	> 1.45 mA/μm	< 10 nA/μm	< 10 nA/μm	76 mV/dec

Device 2 – Peak Performance – L_g = 40 nm, W_{mesa} = 10µm



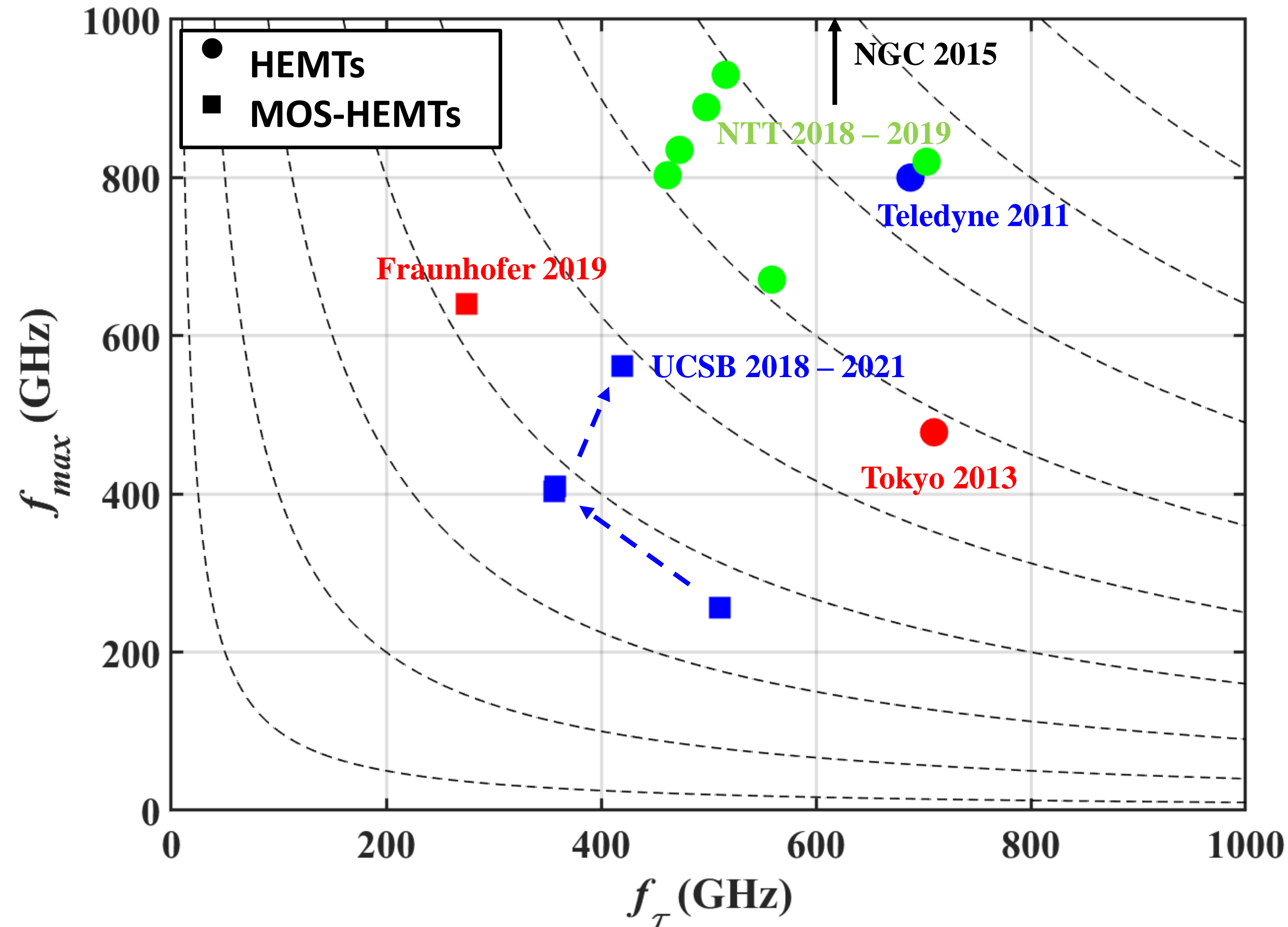


- Peak f_τ = 420 GHz on L_g = 40 nm $(0\bar{1}1)$ conduction device, peak f_{max} at L_g = 50 nm
- Extrapolation of f_{max} difficult because of noisy U → occasionally see “spiking”

Deice 2 – Take Away

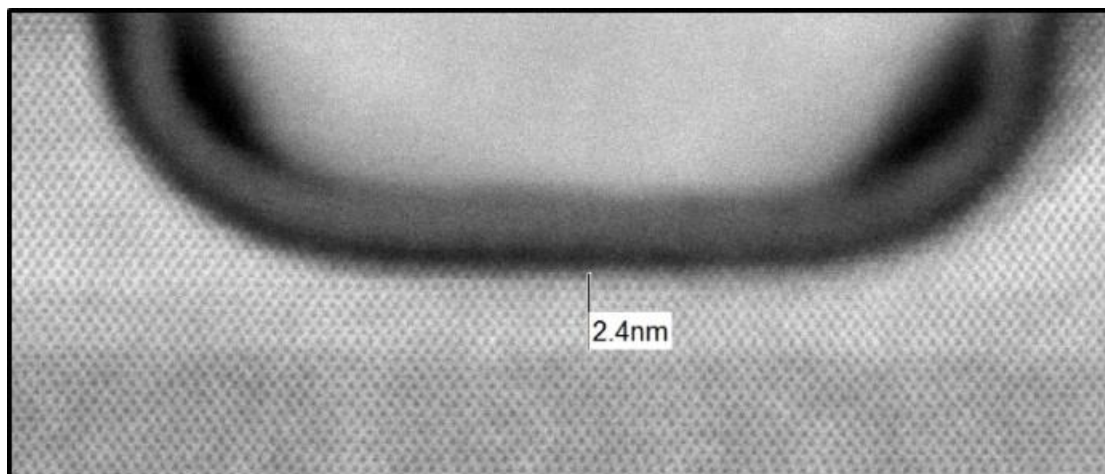
1. Link thinning gives excellent R_S and predictable profile
2. Peak g_m likely limited source-starvation → need more n_{Link}
3. Low I_g → room to thin high-k
4. Need to improve T-Gate process to reduce $C_{GS,p}$ and $C_{GD,p}$

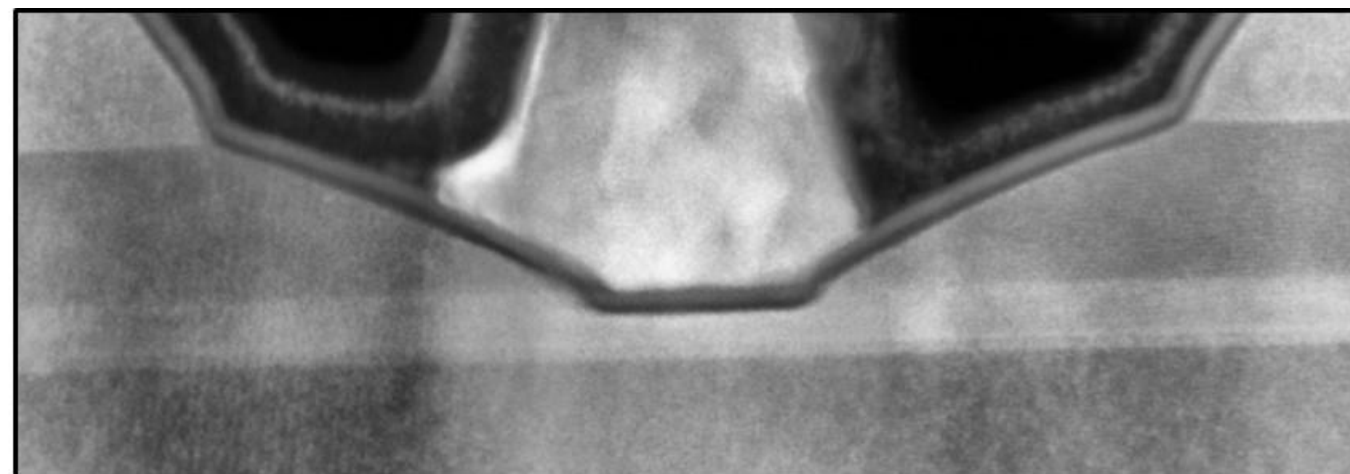
HEMT / MOS-HEMT State-of-the-Art



Conclusions

1. Extremely high g_m = 2.9 mS/μm → competitive with SOA HEMTs
2. Extremely low R_S < 100 Ω•μm → will increase with InAlAs link
3. Extremely low g_{ds} = 0.2 mS/μm → significantly better than SOA HEMTs
4. Improving high frequency FOMs → f_τ , f_{max} > 400 GHz
5. Need to improve T-Gate process to reduce parasitics!





MOS-HEMT Future Work

Problems:

- Peak f_τ severely limited by large $C_{GS,p}$ → need a self-aligned process
- Peak f_{max} limited by large R_G (poor yield & reproducibility) → improve T-Gate process
- Low breakdown voltage and therefore low power-handling → wide E_g channel

Solutions:

- Self-Aligned "Regrowth Reversal" Process → reduces $C_{GS,p}$ and improves T-Gate process
- Wide-bandgap back-barriers (AlAsSb) for improved G_{DS}
- InP channel / AlAsSb back-barrier MOS-HEMT for high-power

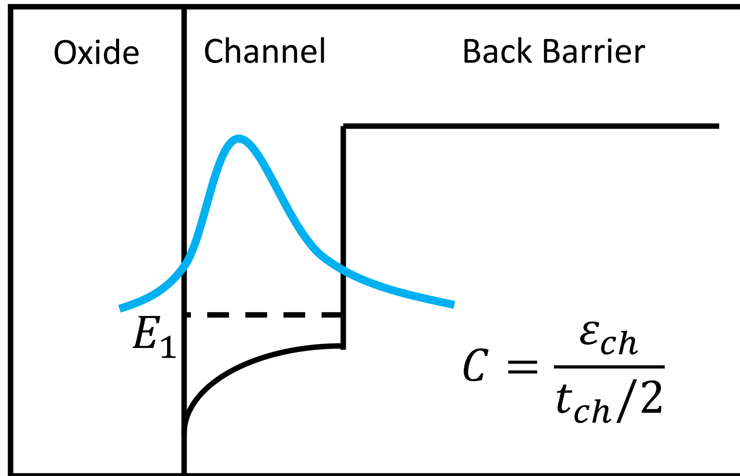
Acknowledgements

Funding: DARPA ComSenTer

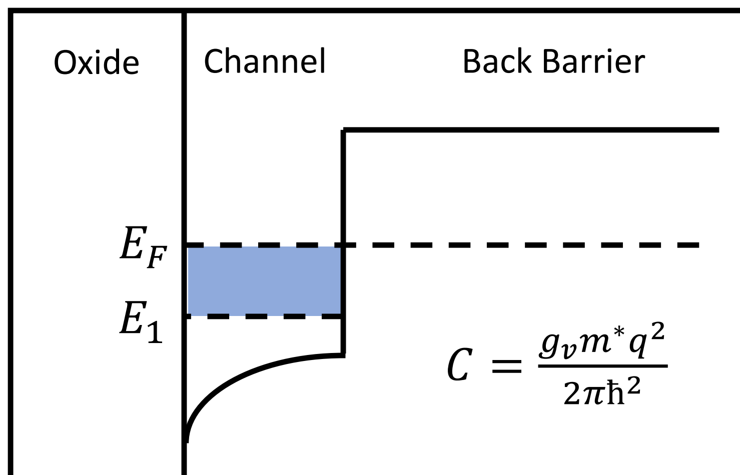
QUESTIONS

FET Scaling Laws (Now Broken)

Wave function has "thickness"

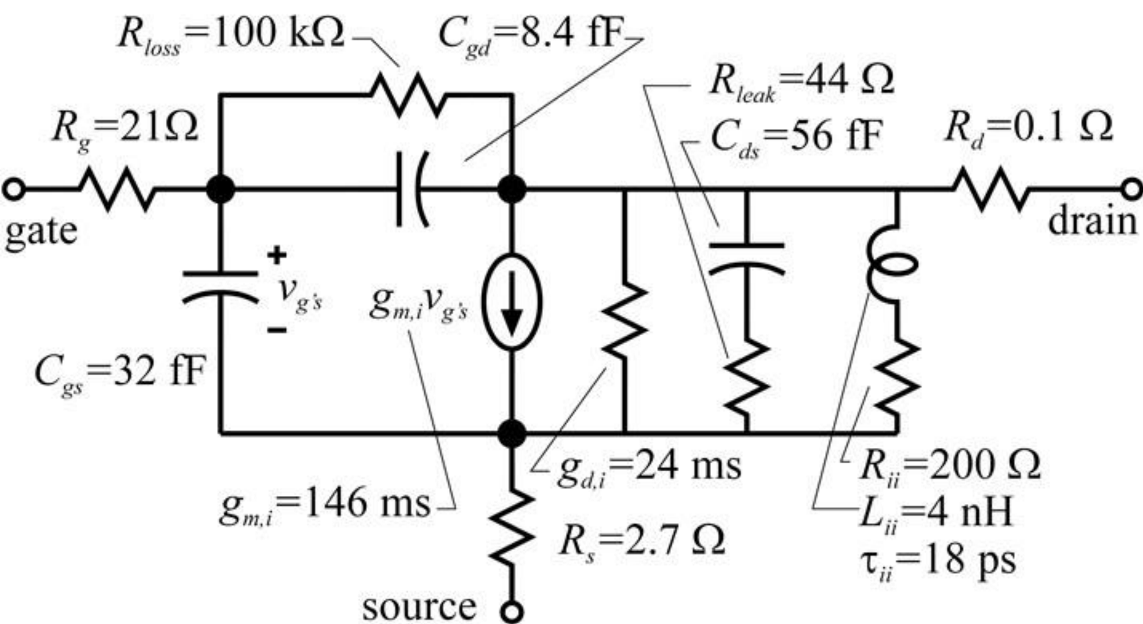


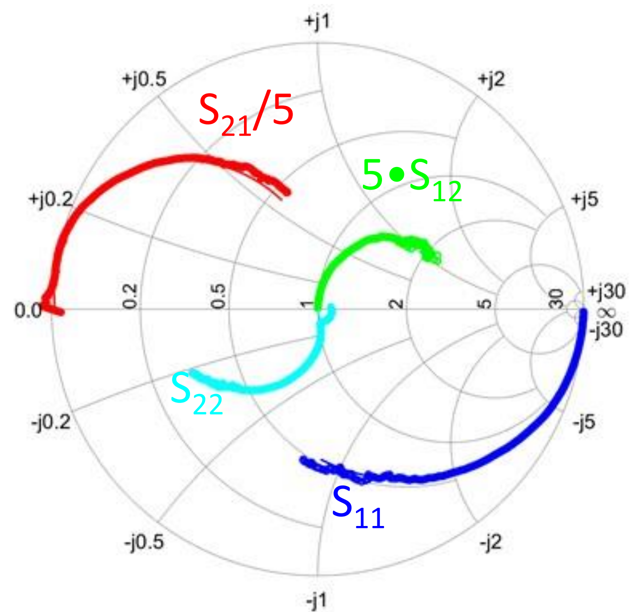
Fermi Level moves to populate low DOS



FET parameter	change
gate length	decrease 2:1
current density (mA/mm)	increase 2:1
specific transconductance (mS/mm)	increase 2:1
transport mass	constant
2DEG electron density	increase 2:1
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel state density	increase 2:1
contact resistivities	decrease 4:1

[1] Device 0 SSEC: L_g = 8 nm





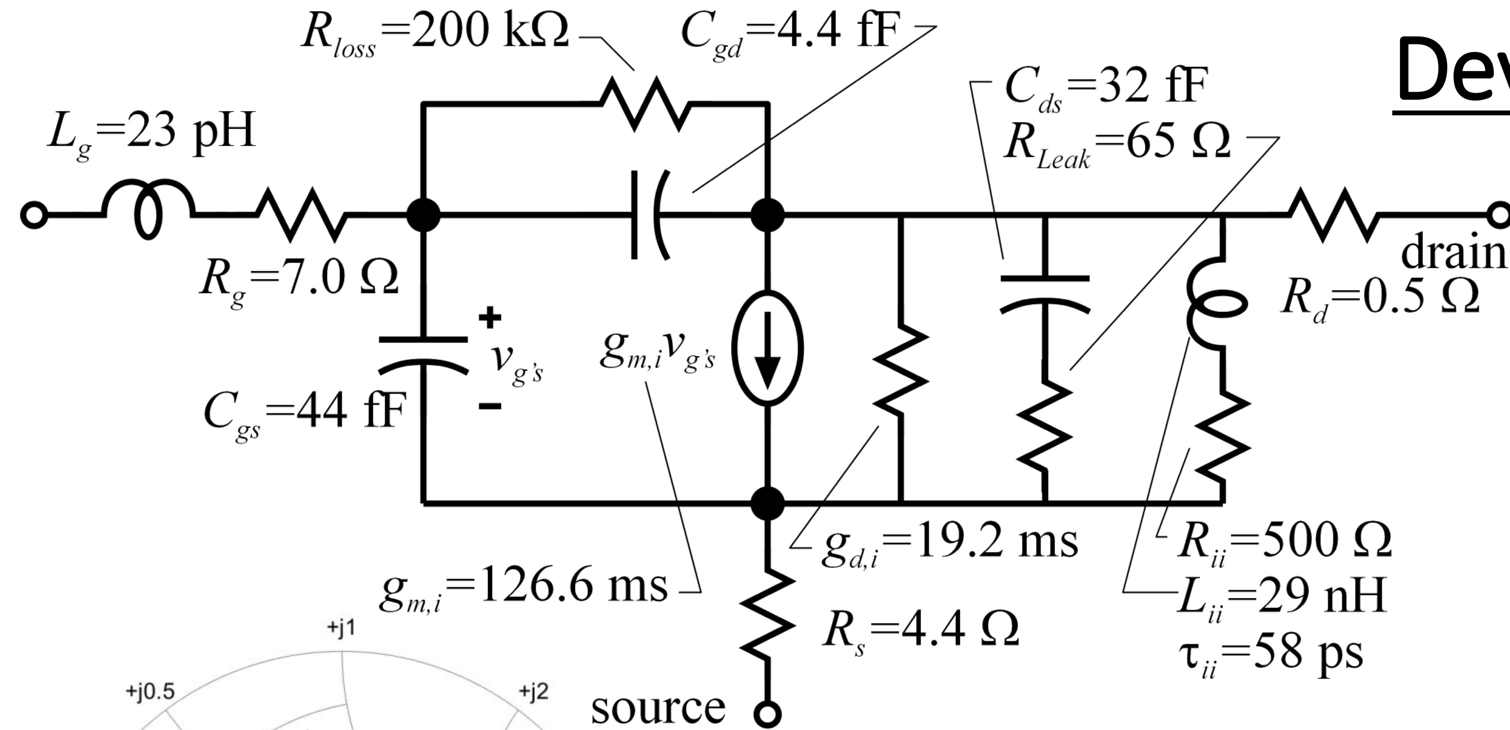
Gain (dB) vs. Frequency (GHz)

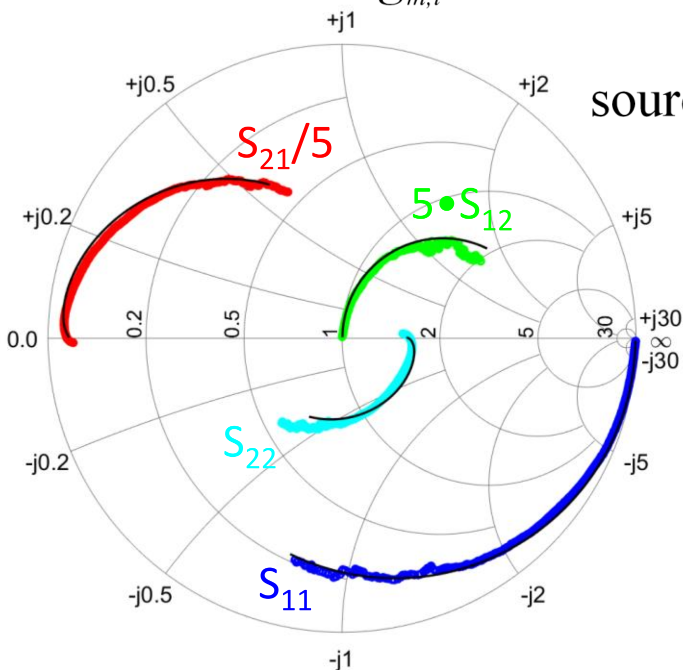
U
H_{21}
MSG/MAG

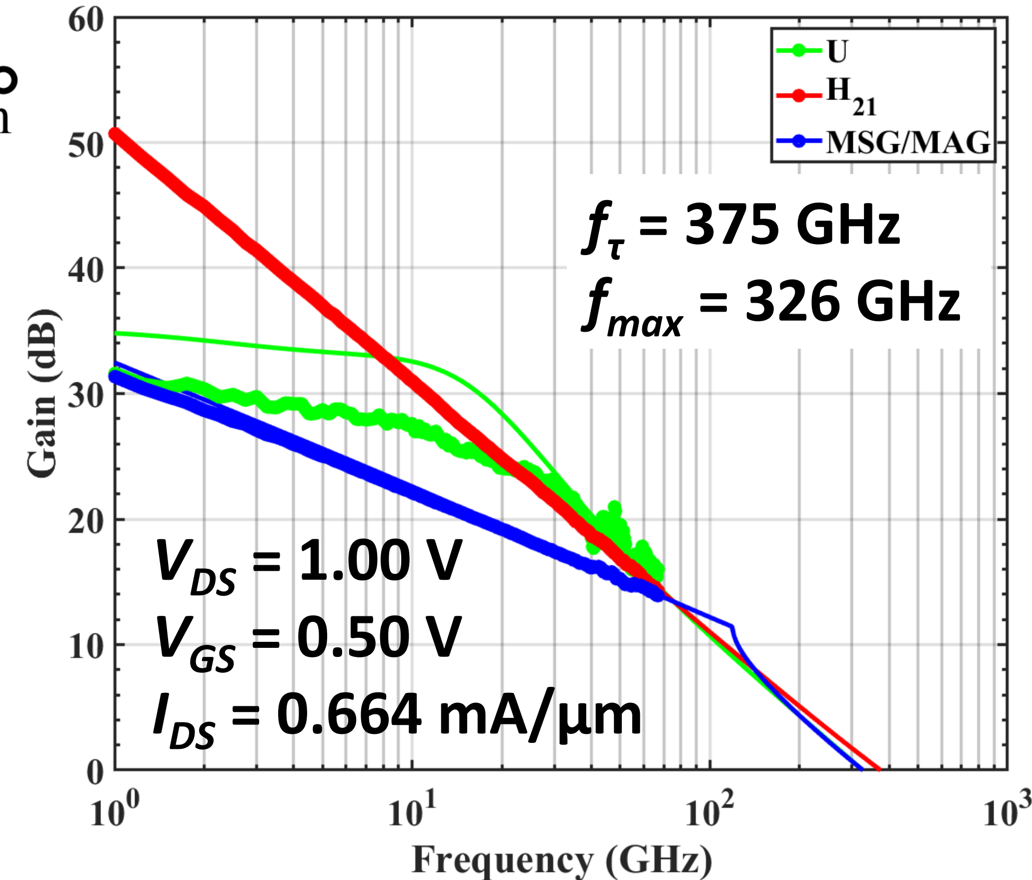
f_τ = 533 GHz
f_{max} = 204 GHz

V_{DS} = 0.70 V
V_{GS} = 0.30 V
I_{DS} = 0.852 mA/μm

Device 1 SSEC: L_g = 12 nm

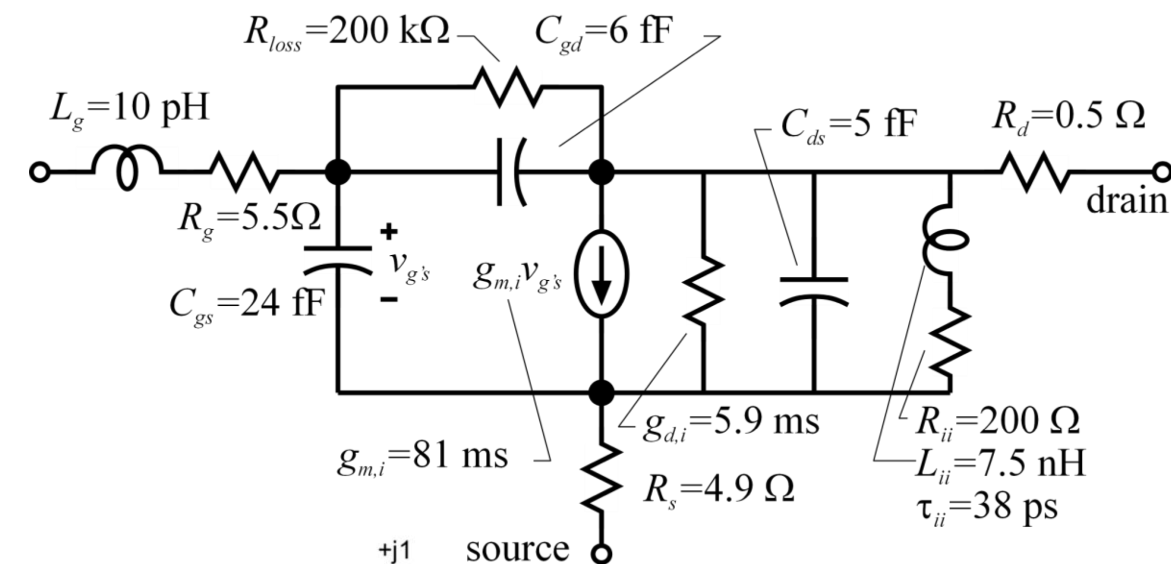


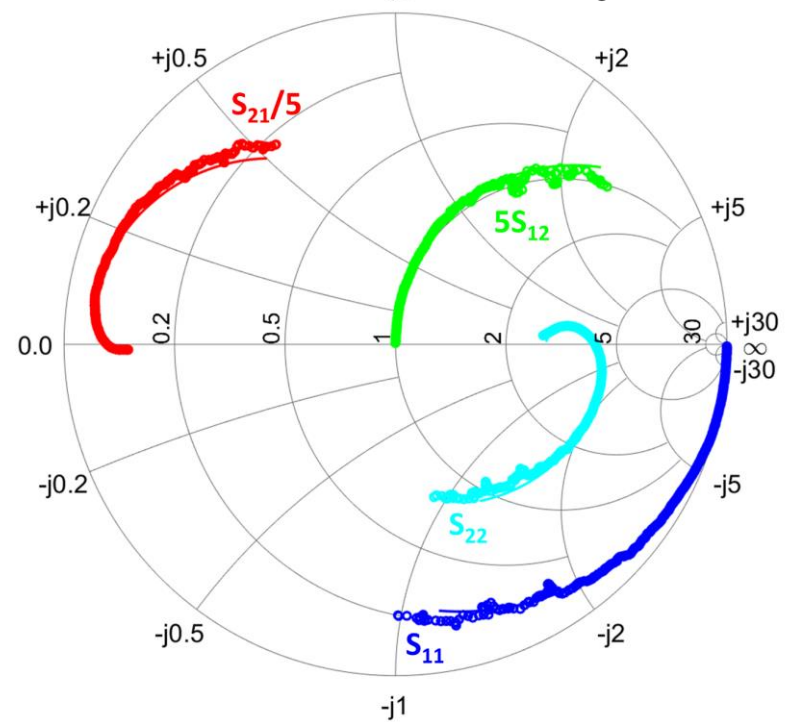




SSEC very difficult to fit… do not trust this model

Device 2 SSEC: L_g = 40 nm





Significantly improved fit, trustable

U
H_{21}
MSG/MAG

f_τ = 454 GHz
f_{max} = 567 GHz

V_{DS} = 0.70 V
V_{GS} = 0.30 V
I_{DS} = 0.852 mA/µm

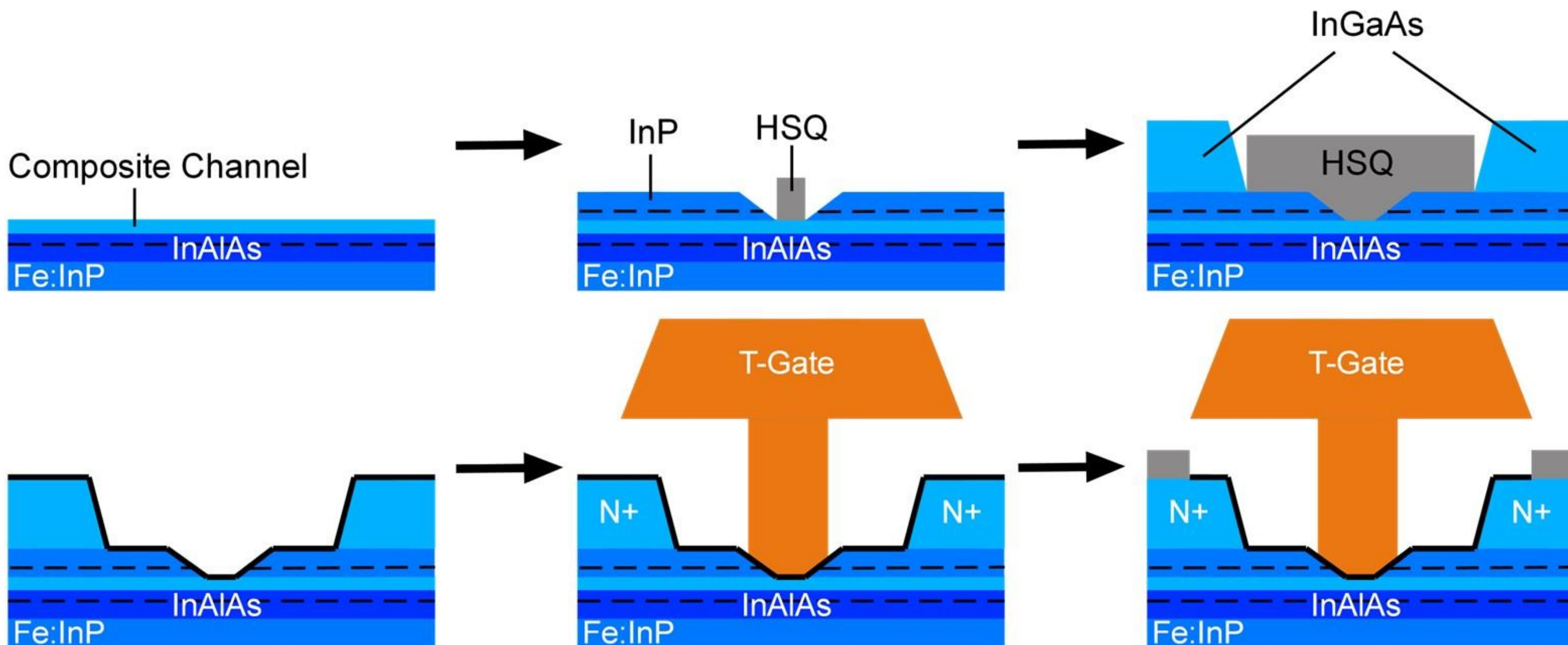
Gain (dB): 0, 10, 20, 30, 40, 50, 60

Frequency (GHz): 10^0, 10^1, 10^2, 10^3

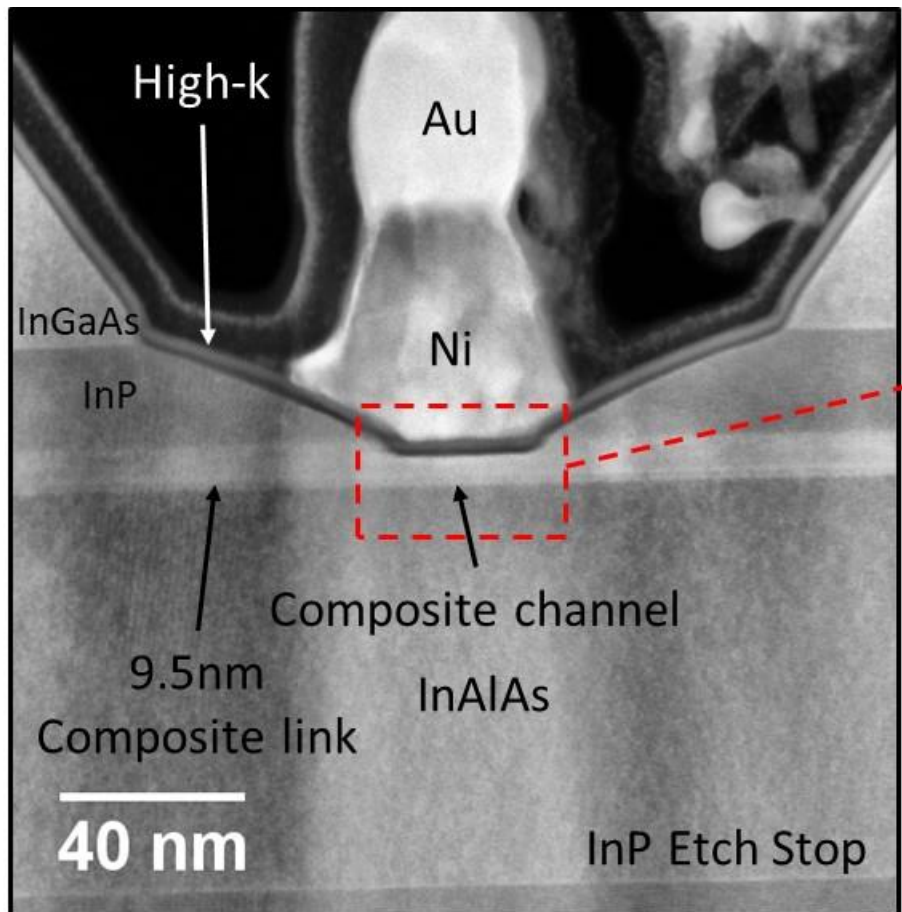
Model vs. Extrapolation

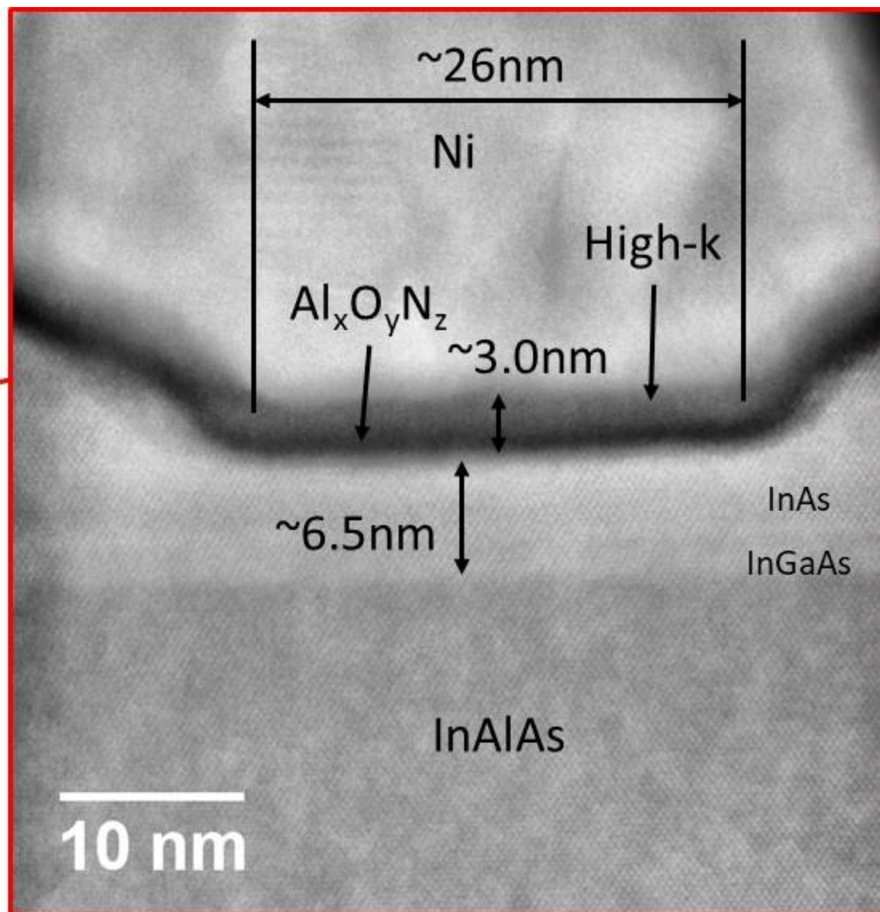
Device	Extraction	L_g (nm)	f_τ (GHz)	f_{max} (GHz)
0	Extrapolation	8	511	256
0	Modeled	8	533	204
1	Extrapolation	12	356	398
1	Modeled	12	375	326
2	Extrapolation	40	402	560
2	Modeled	40	454	567

[1] Device 0 - Fabrication



[1] Device 0 – Device Structure





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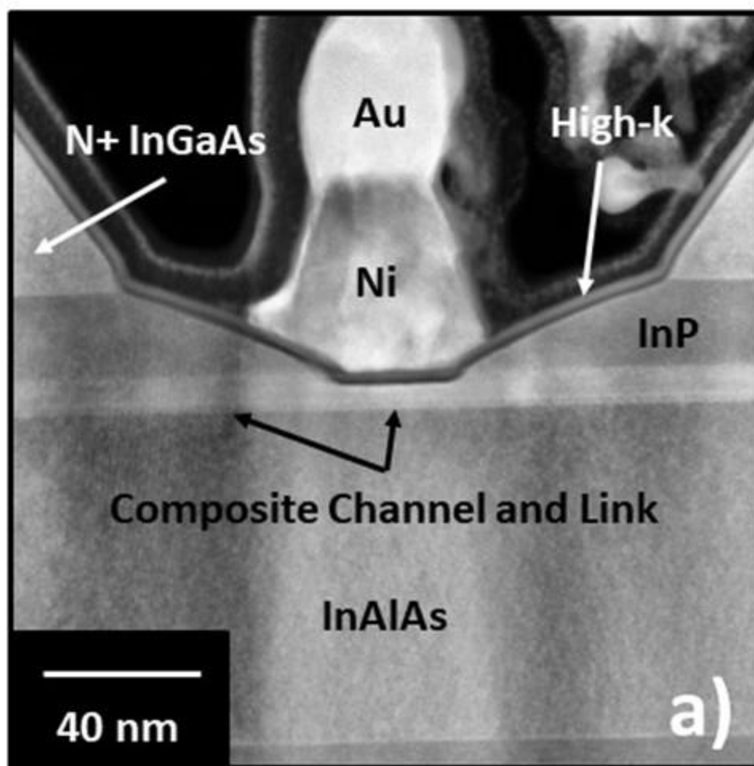
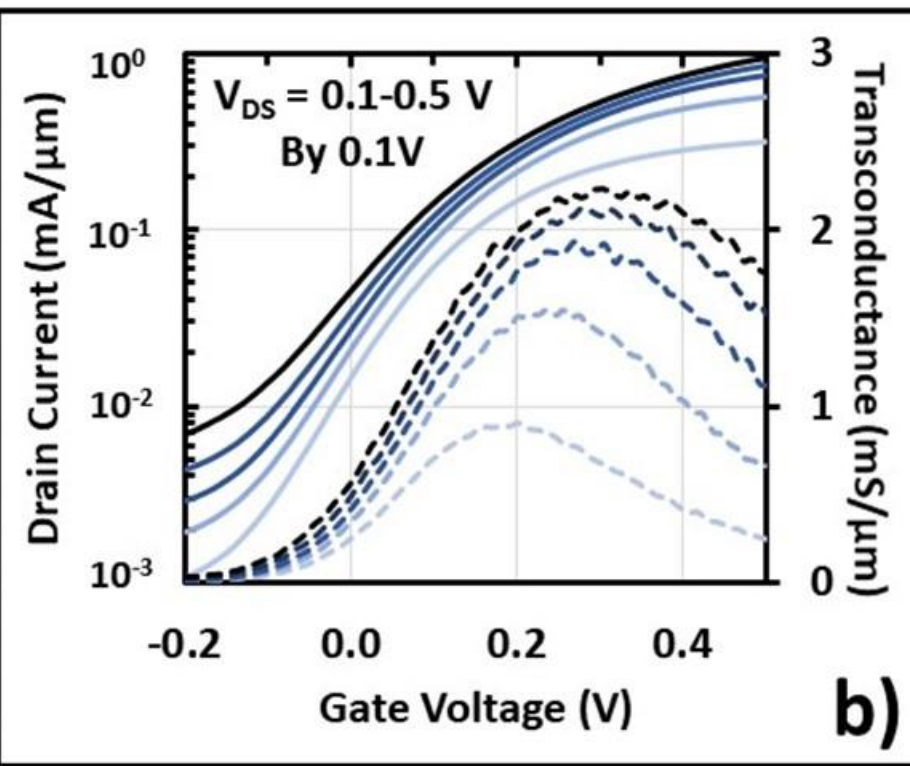
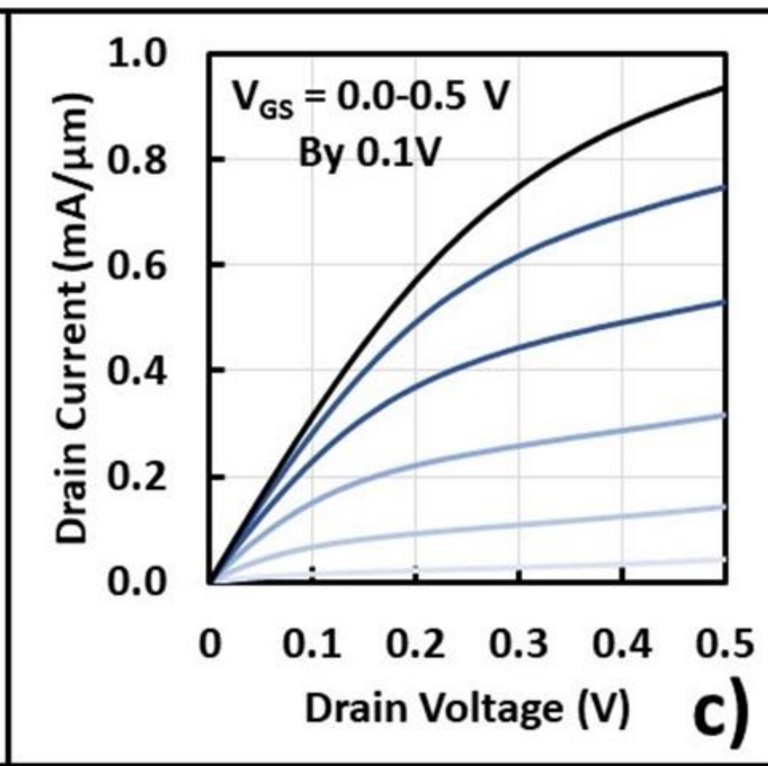
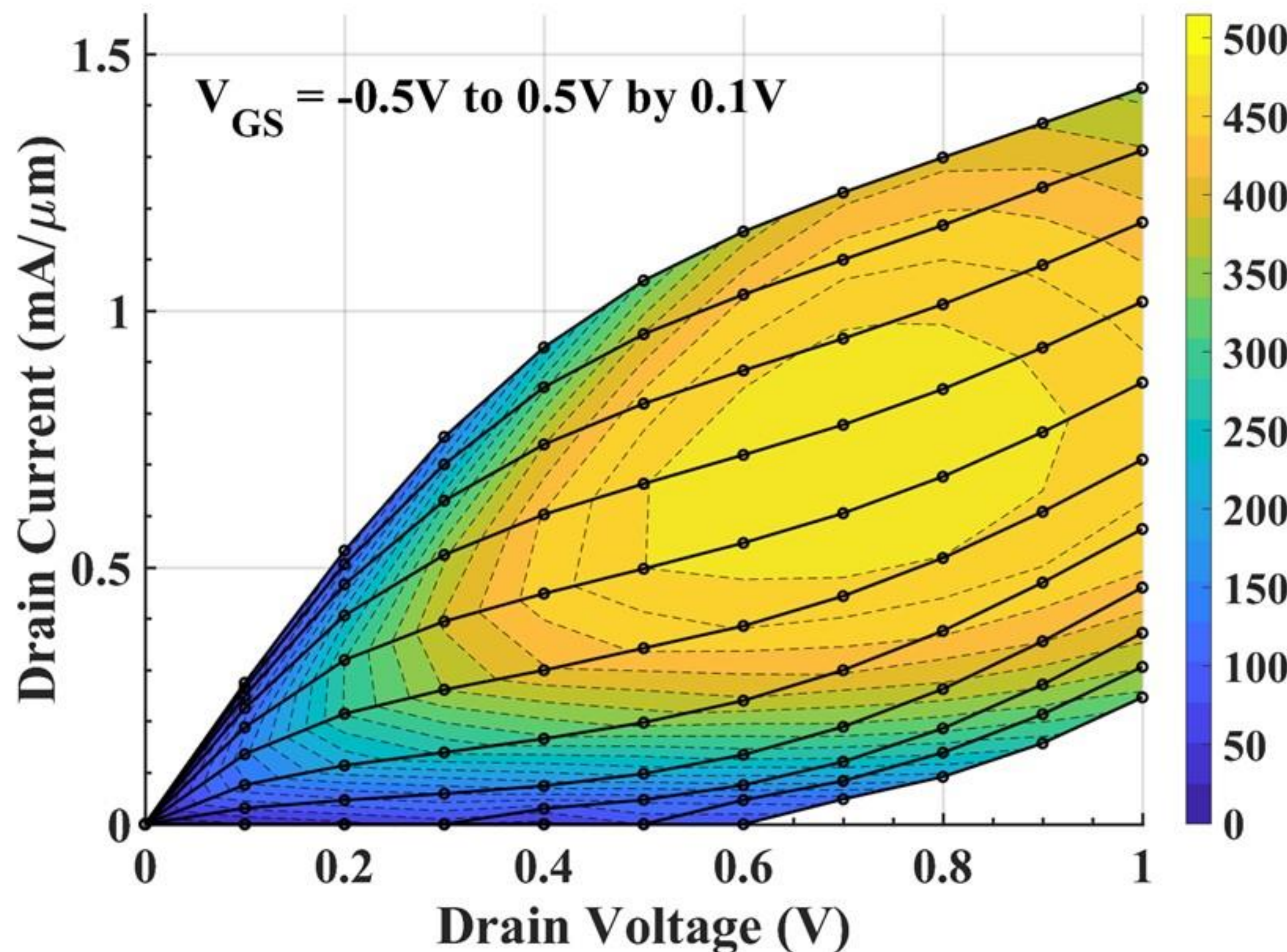


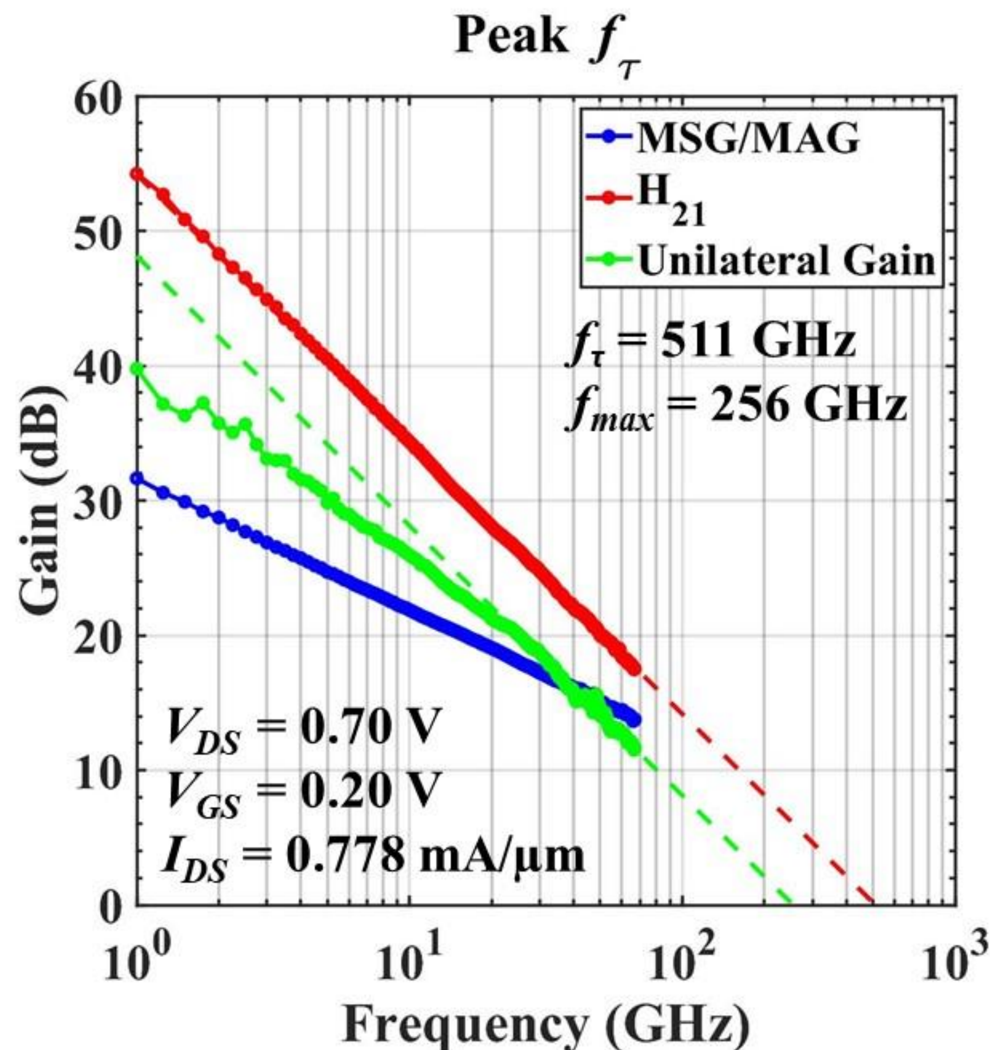




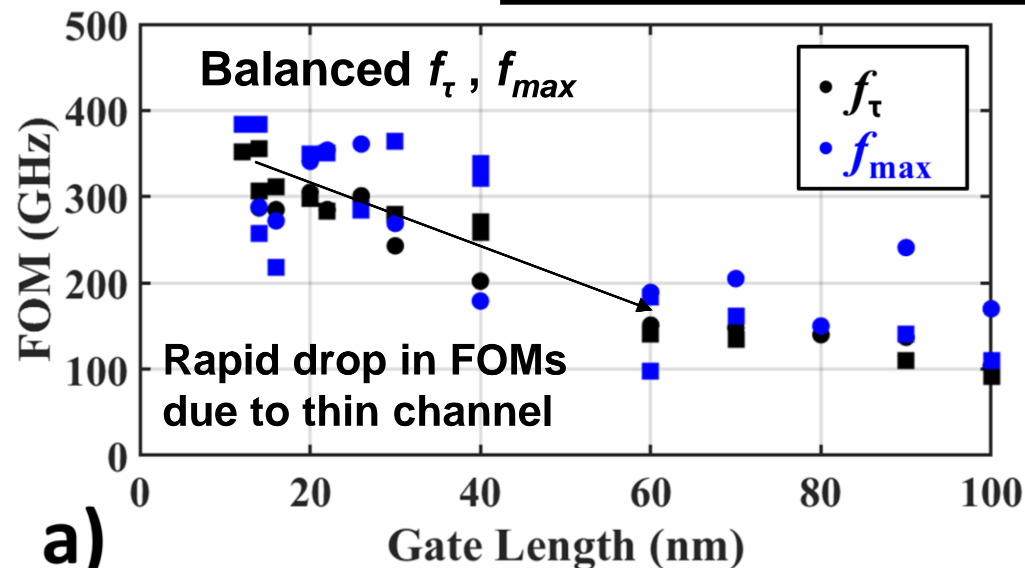
Peak g_m	R_A	I_{on}	I_{off}	I_g	Long L_g SS_{min}
2.2 mS/μm	68 – 85 Ω•μm	> 0.90 mA/μm	> 1.0 μA/μm	< 10 pA/μm	N/A

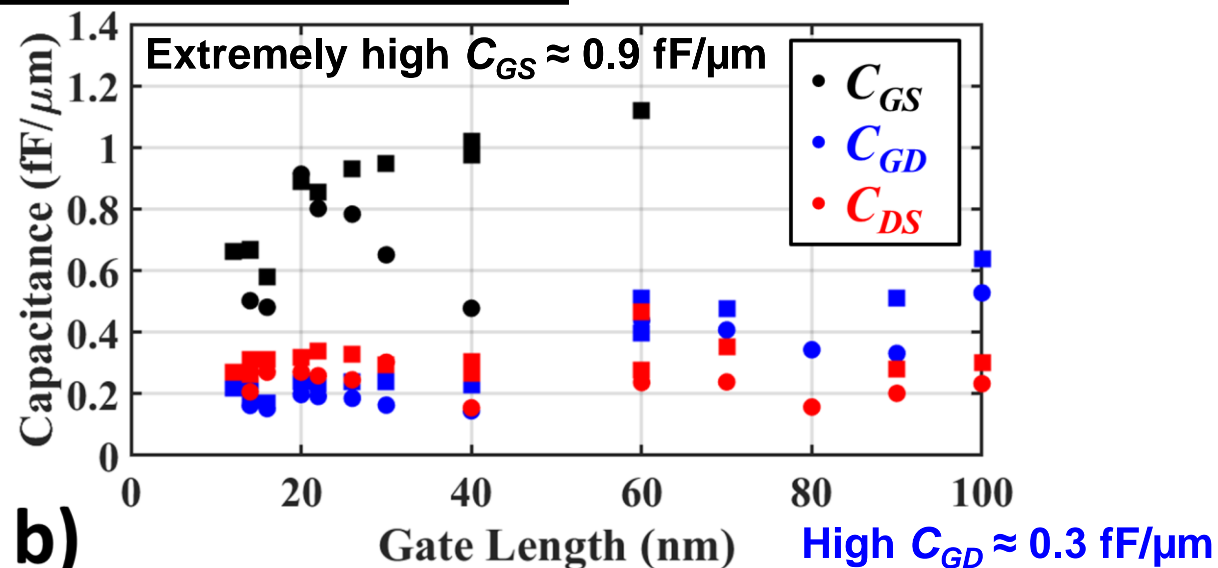
[1] Device 0 – Peak Performance

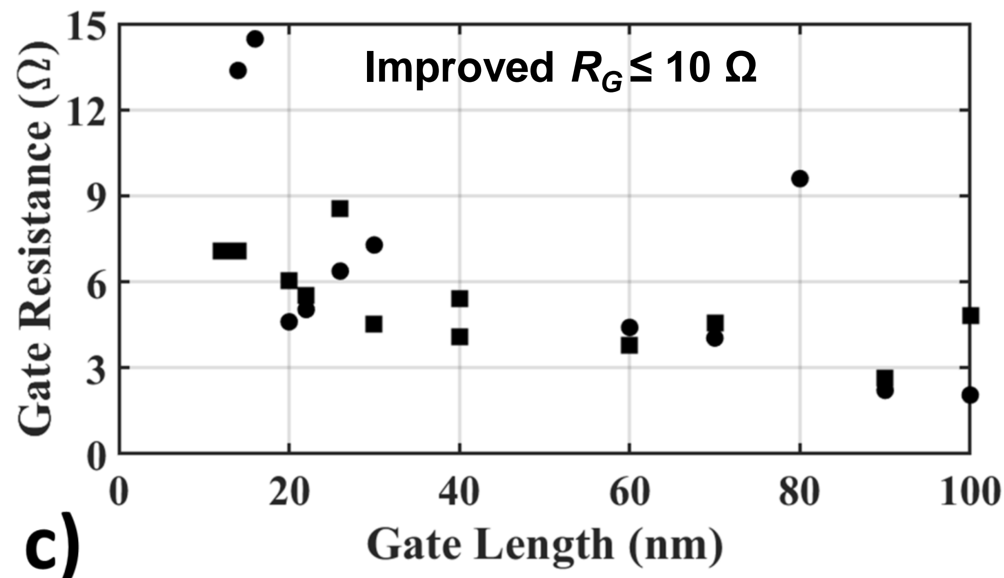


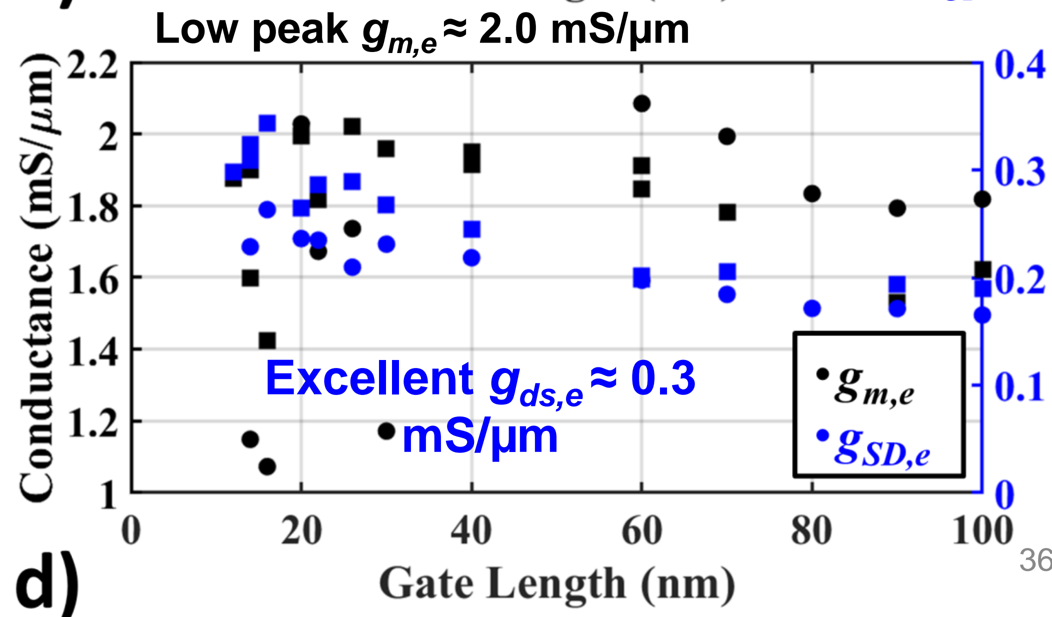


Device 1 – RF Characteristics

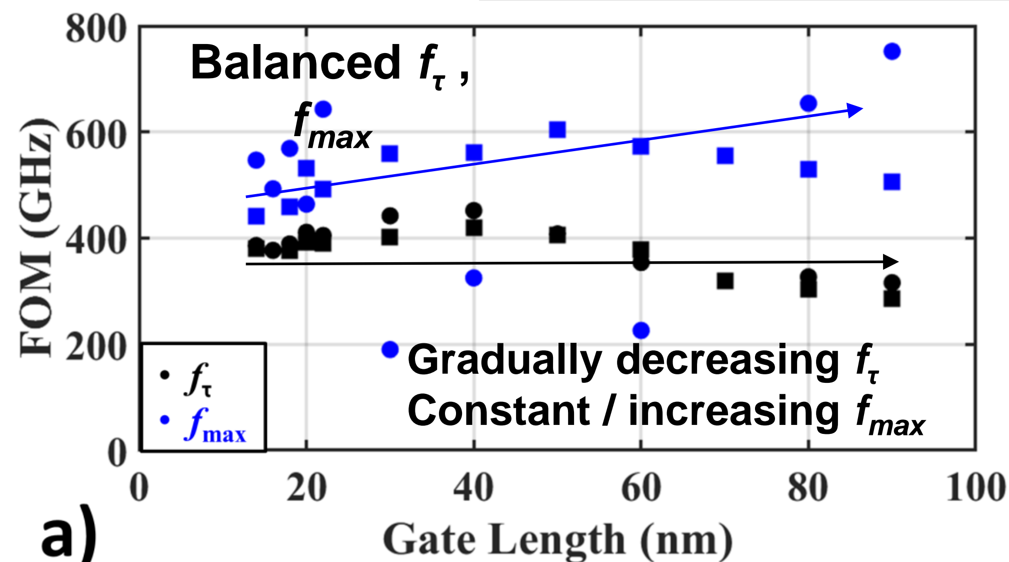


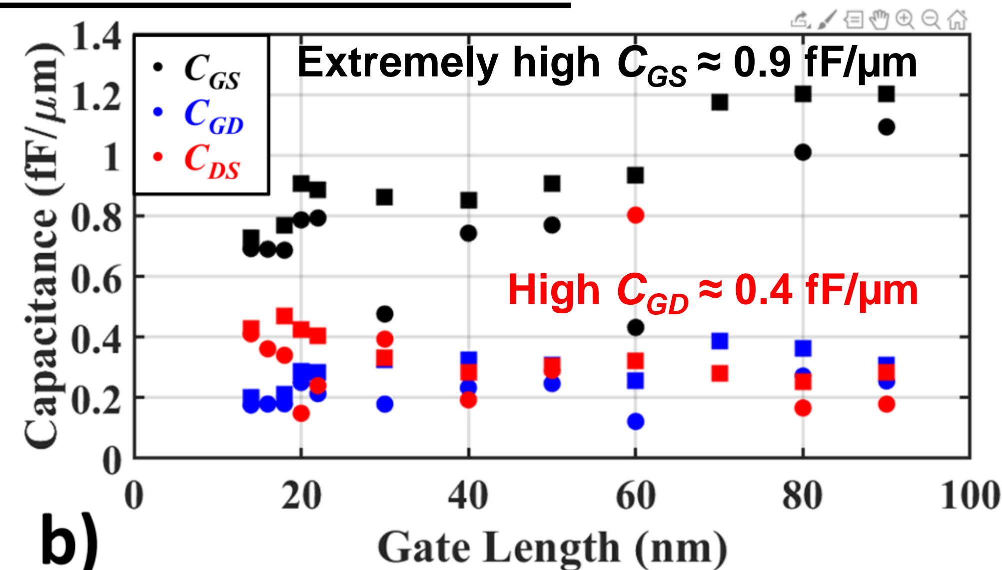


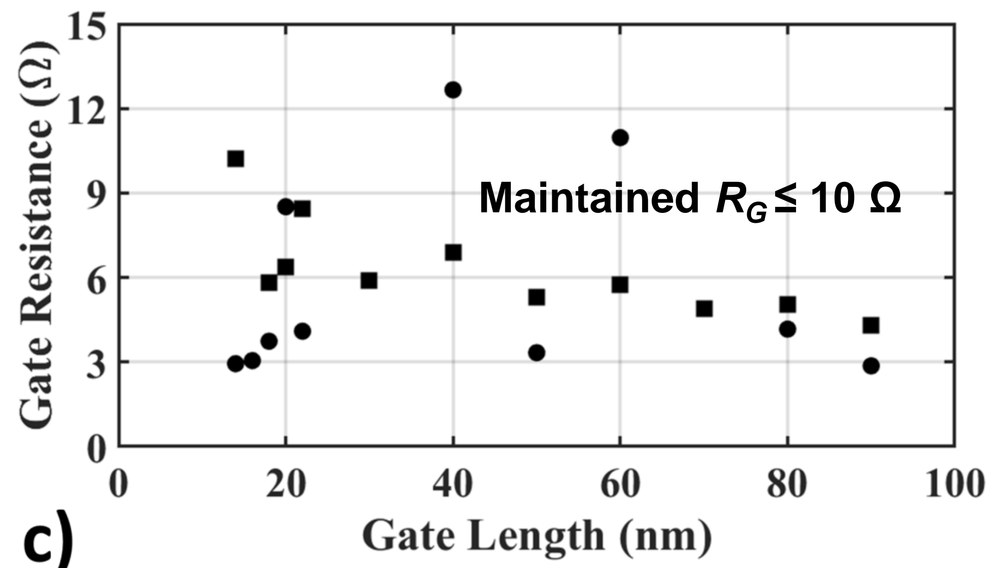


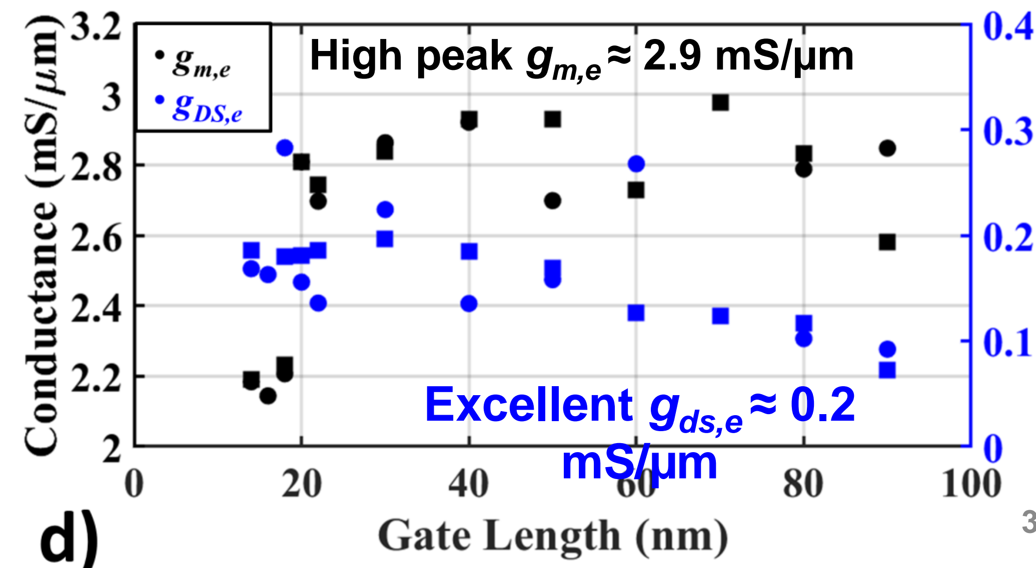


Device 2 – RF Characteristics







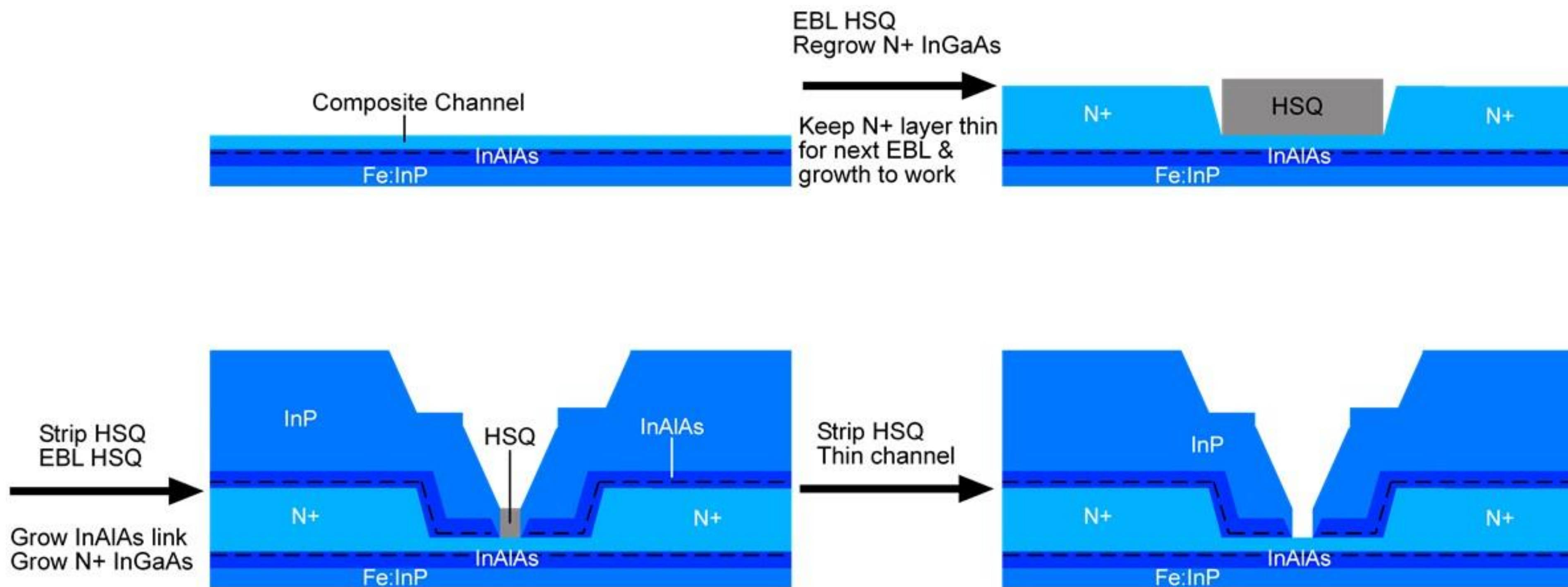


HEMT / MOS-HEMT State-of-the-Art

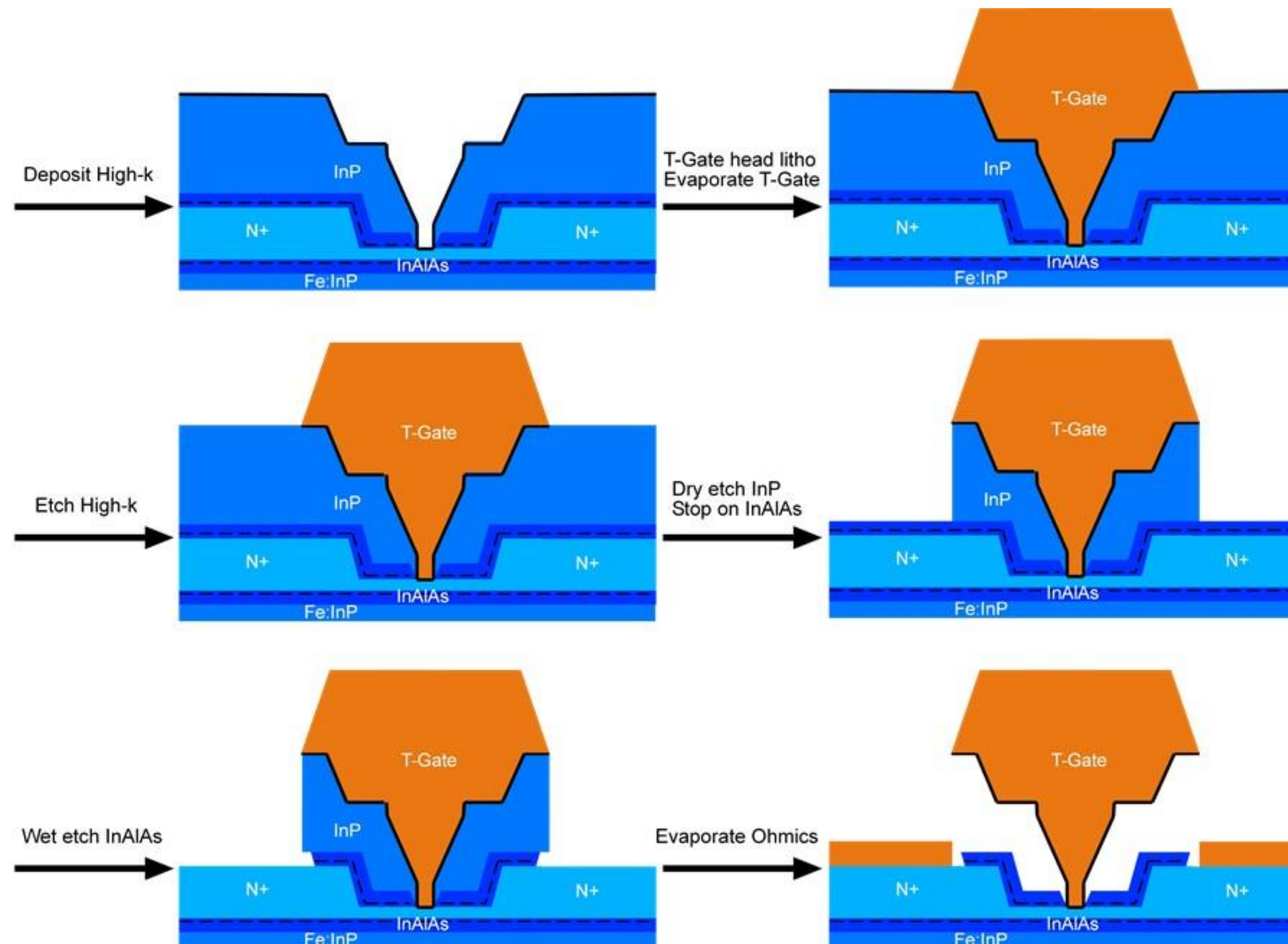
Institution	Device	Year	g_m (mS/µm)	f_t (GHz)	f_{max} (GHz)	$\sqrt{f_t \bullet f_{max}}$
Teledyne	HEMT	2011	2.75	688	800	742
Tokyo Tech	HEMT	2013	2.1	710	478	583
NGC	HEMT	2015	3.1	610	1500	957
NTT	HEMT	2019	2.8	703	820	759
Fraunhaufer	MOS-HEMT	2019	2.4	275	640	420
UCSB Gen. 0	MOS-HEMT	2018	1.5	357	410	383
UCSB Gen. 1	MOS-HEMT	2019	2.3	511	256	361
UCSB Gen. 2	MOS-HEMT	2019	1.6	356	403	379
UCSB Gen. 3	MOS-HEMT	2020	2.9	406	562	477

MOS-HEMT Future Work

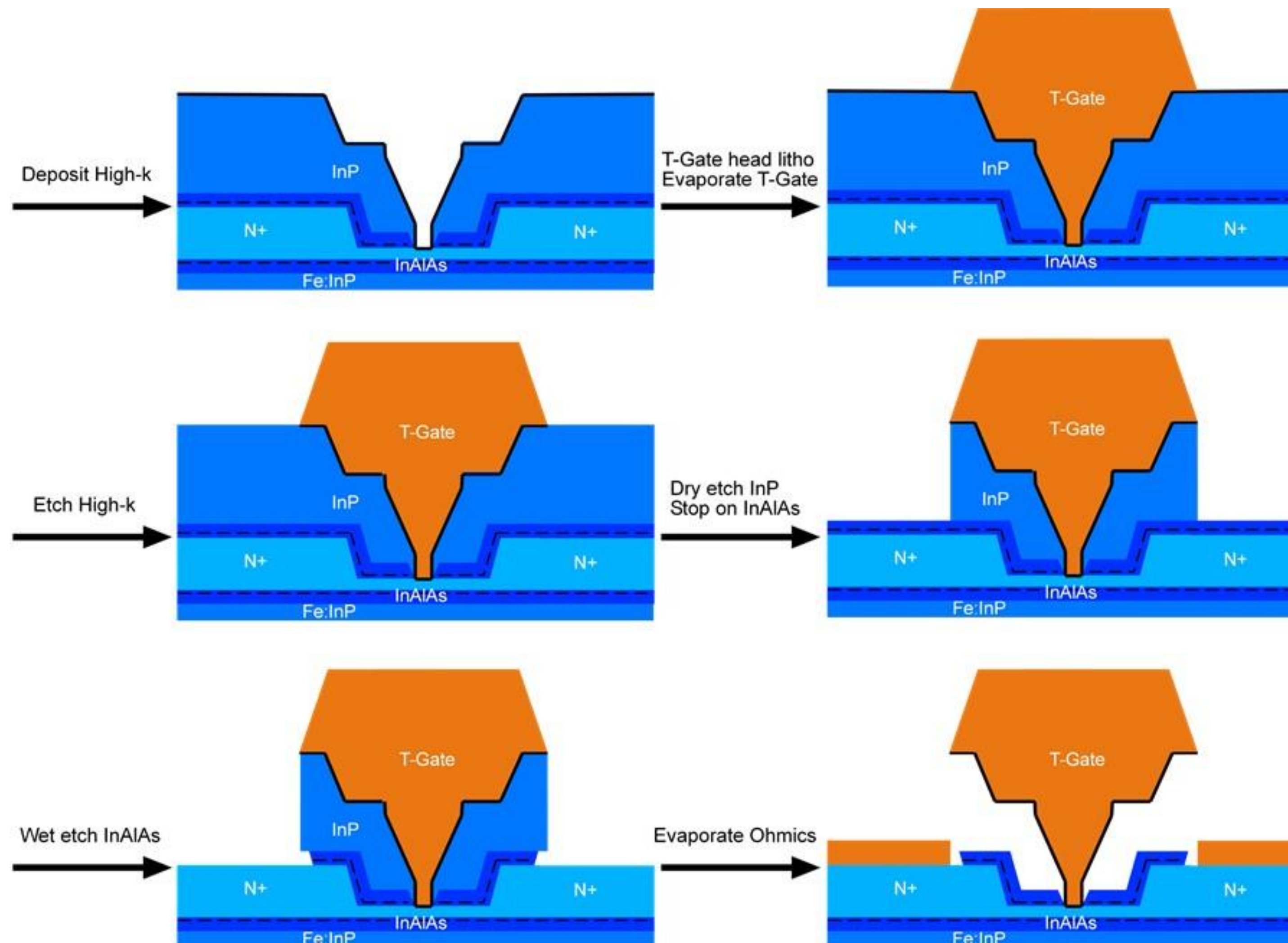
- Peak f_τ severely limited by large $C_{GS,p}$ → need a self-aligned process
- Peak f_{max} limited by large R_G (poor yield & reproducibility) → improve T-Gate process
- Develop > 1 x 10^{19} cm^{-3} $In_{0.52}Al_{0.48}As$ for link region top barrier
- Elegantly *hopefully* solved in one simple process



MOS-HEMT Future Work



MOS-HEMT Future Work



Advantages

- Larger T-Gate aperture
- Improved RG
- Self-aligned Gate-Recess and T-Gate foot
- Self-aligned ohmics possible

Disadvantages

- Etching (dry & wet) in critical regions
- Topography on wafer before critical dimension definition
- Regrowth dynamics