

IC and Array Technologies for 100-300GHz Wireless

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Abstract: 100-300 GHz wireless systems can provide very high data rates per signal beam, and, given the short wavelengths, even compact arrays can contain many elements, and hence can simultaneously transmit, in the same frequency band, many simultaneous independent signal beams to further greatly increase capacity. We will describe representative system designs, including wireless hubs and backhaul links using massive spatial multiplexing, plus imaging radar systems, evaluate their feasible performance, and identify the key challenges in implementation, including transistor and IC performance, array physical design, digital beam former complexity, and systems cost.

Introduction: Rapidly increasing use of wireless communications is exhausting the presently allocated spectrum, hence the wireless industry is moving to 5G wireless systems, with carrier frequencies from below 6 GHz to 86 GHz. Research now considers next-generation systems with carrier frequencies between 100-300 GHz. Capacity can be further increased over 5G, both because of the wide potentially available spectrum and because the short wavelengths permit even compact arrays to have many elements which can then support many simultaneous independent signal beams, this being known as massive spatial multiplexing or massive MIMO. With present state-of-the-art power- and low-noise amplifiers, aggregate capacities can approach or exceed 1 Tb/s in short-range (few hundred meter) backhaul and endpoint links. The challenges in realizing such systems are in efficient digital beamforming, in the array physical design, and in realizing the front-end ICs and modules at low power consumption and low cost, particularly given the large number of required RF channels.

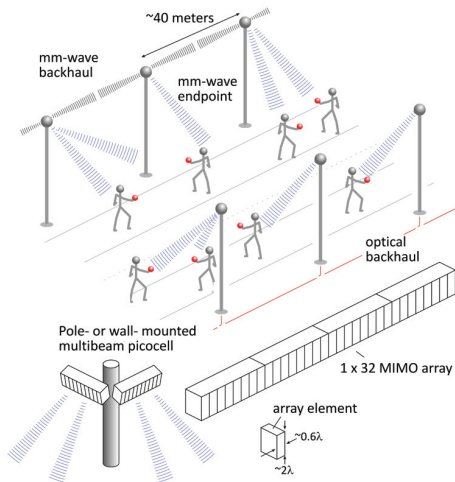


Figure 1: Spatially multiplexed network 140 GHz picocell hub. The hub has 2 faces, each a 32-element MIMO array, each providing up to 16 independent signal beams. At 40 m range, 10 Gb/s transmission per beam is feasible with large operating margins

100-300 GHz Wireless Systems: Consider first a 140 GHz wireless communications hub [1, 2, 3, 4] (base station) serving many mobile users (Figure 1). Each array face has 32 elements and supports 16 users but is only 41 mm long. If we assume that the hub's power amplifiers each provide 120 mW at the 1 dB gain compression point, that the handset has a 1 cm² array (8×8 at $\lambda/2$ spacing) and has 8 dB noise figure, that it is raining 50 mm/hr., and that the signaling is QPSK at 10⁻³ uncoded error rate, then the hub can provide each user with 1 Gb/s (10 Gb/s) data rate at 70 m (40 m) range, even with 17 dB total safety margins for partial beam blockage, equipment aging, and manufacturing variations. The net transmission capacity is 160 Gb/s per array face. If we assume the

same link parameters at 75 GHz, keep the base station at 32 elements, but constrain the handset array to the same 1 cm² area (4×4 elements at $\lambda/2$ spacing) as at 140 GHz, then the same range is obtained at the same data rate; at 140 GHz, it is more likely that the needed spectrum can be allocated

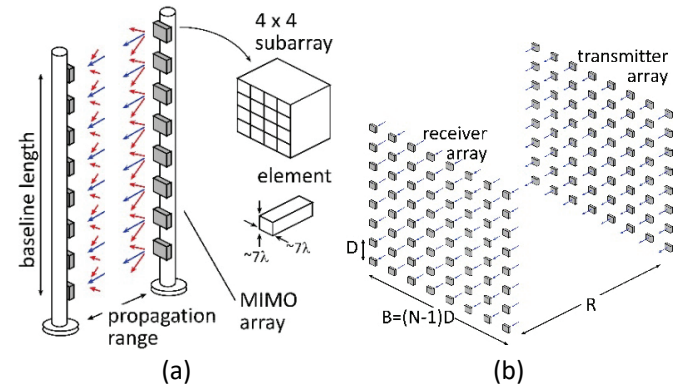


Figure 2: Spatially multiplexed wireless backhaul link, using (a) linear transmitter and receiver arrays, with each element being a 4×4 subarray. With a fixed range and baseline length, the maximum number of channels scales in proportion to the carrier frequency. Spatially multiplexed link using (b) a square array, with the number of channels scaling in proportion to the square of the carrier frequency.

Figure 2a shows a spatially multiplexed backhaul link. N transmitters, carrying independent data, form an array of length L . The receiver, at distance R , has a similar array but uses MIMO [5] beamforming. If the array angular resolution λ/L is smaller than the element apparent angular separation L/NR , then the signals can be recovered without channel-channel crosstalk degrading the SNR. Link capacity is increased $N:1$. In a square array (Figure 2b), the capacity is increased $N^2:1$.

Short wavelengths are of great advantage, as a short array can then carry many channels; at 500 m range, an 8-element linear array must be 2.1 m long at 210 GHz, but 3.5 m at 75 GHz. At 210 GHz, if each array element is an 8×8 subarray of 7λ by 7λ elements (for small beam angle adjustment) then, with 20 dB total margins, QPSK at 10⁻³ uncoded error rate, and 6 dB receiver noise figure, transmitting 640 Gb/s over 500 m range in 50 mm/hr. rain requires only 63 mW/element output power at the 1 dB gain compression point. Given the same system parameters, the square array would transmit 5.1 Tb/s but would require only 8 mW/element output power (P_{1dB}).

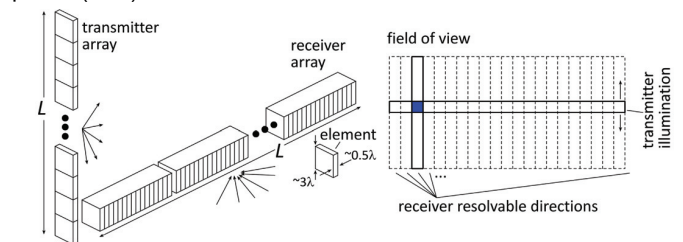


Figure 3: Automotive imaging radar system using a $N \times 1$ vertical linear phased-array transmitter and a $1 \times N$ horizontal linear MIMO array receiver to produce an $N \times N$ image.

A third example system (Figure 3) is a 210 GHz FMCW imaging radar, for driving in e.g. heavy fog or rain. Crossed linear 36×1 transmit and 1×216 receive arrays form a 36 (vertical) × 216 (horizontal) pixel image. If the elements are 3λ (v) × 0.5λ (h), then the array length L is only 15.3 cm, yet the 3 dB beamwidth is 0.27°, while the field of view is 10° (v) × 90° (h). Given a 40 Hz image scan rate, a 22 cm diameter target (a soccer ball) of -10 dB reflectivity at 200 m range, a minimum 10 dB SNR for target detection, 22 dB/km atmospheric attenuation (heavy fog or 50 mm/hr. rain), and 4 dB operating margins, then with 2 dB transmit and 2 dB receive packaging losses and a 6 dB receiver noise figure, the required transmitter output power per element is 50 mW.

Signal Processing Requirements: The MIMO systems considered above collectively carry many high-rate signal streams, hence signal-signal crosstalk from RF/IF/baseband signal chain (Figure 4) nonlinearities (P_{1dB} , IP3), ADC/DAC resolution, and local oscillator phase noise are of potential concern. Yet, detailed systems simulations of the MIMO hub of 1 indicate that, if received power leveling is employed, RF component 1 dB gain compression points need only be 4 dB above average power levels [6], that 3-4 bit ADC/DAC resolution is sufficient for QPSK transmission [6], and that the phase noise need be no smaller than that required of a single-channel system of the same symbol rate and constellation [7]. These findings suggest that the design requirements of the RF, IF, and baseband analog ICs are not particularly stringent. Given that ~16 high-rate (1-10 Gb/s) user data streams must be recovered from ~32 wideband (I,Q) signals, the digital beam former might potentially be very computationally complex. Yet, with the development of computationally efficient beam space beamforming algorithms [8] and efficient VLSI digital implementations [9], high-rate all-digital MIMO beamforming appears to be feasible.

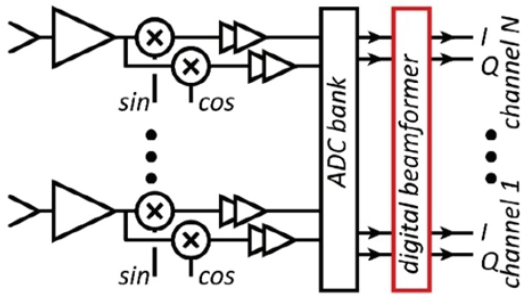


Figure 4: Sketch of the RF through baseband signal chain, with digital beamforming, for the massive MIMO receiver of Figure 1. The transmitter is similar, with digital beam former, DAC bank, (I,Q) baseband to RF up conversion, power amplifiers, and antennas..

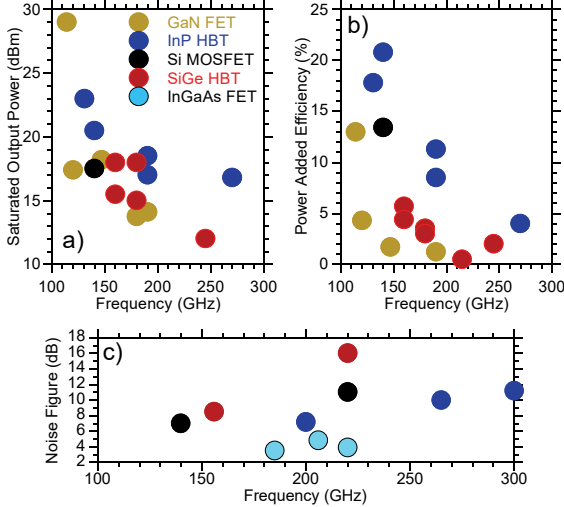


Figure 5: Representative state-of-the-art results at 100-300 GHz for power amplifier saturated output power (a) and power-added-efficiency (b) and receiver or LNA noise figure (c). Because it is difficult to simultaneously present power amplifier operating frequency, output power, and efficiency, results with very low efficiency but high output power, or low output power but high efficiency are not shown.

IC Technologies for 100-300 GHz Wireless: Even today's IC technologies (Figure 5) can provide the frequency range, transmitter power and receiver noise required for the systems of figures 1-3; the challenge is in either realizing the ICs in lower-cost CMOS and SiGe technologies, or, if higher-performance InP or GaN [10, 11, 12] technologies are to be used, in bringing these to low cost and high production volumes. CMOS works well at 140-150 GHz, [13,14] providing low receiver noise and moderate output power [15,16]; 140 GHz arrays have been reported [15,17], but receiver noise and power amplifier output power and efficiency

degrade markedly at higher frequencies [18]. Best CMOS performance at 100-200 GHz is for the 65 nm through 22 nm nodes, not more highly scaled technologies. Longer-range ~150 GHz wireless links can use CMOS with external InP HBT [19,20, 21, 22] or SiGe HBT power amplifiers [23,24,25] for increased output power; InP, in particular, provides record power and efficiency at these frequencies. InP HEMT or GaAs PHEMT or MHEMT low-noise amplifiers can be used for better receiver sensitivity [26,27,28]. For systems having >200 GHz carrier frequencies, though CMOS can still be used for frequency conversion [29,30], for best IC performance, and to reduce the number of high-frequency IC-IC connections, it may be attractive to build the entire RF front end from III-V or SiGe technologies.

Given signal frequencies approaching the transistor f_{max} , transistor noise figure, RF output power density, power-added efficiency, and gain are all compromised. Low-noise and power amplifiers should therefore be designed so that their performance is close to the limits imposed by the transistors.

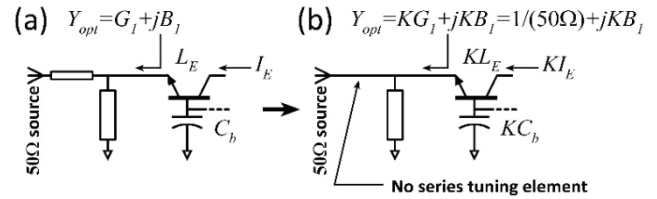


Figure 6: (a) LNA input matching network with an emitter junction area, and (b) with the junction area scaled to eliminate the series tuning element.

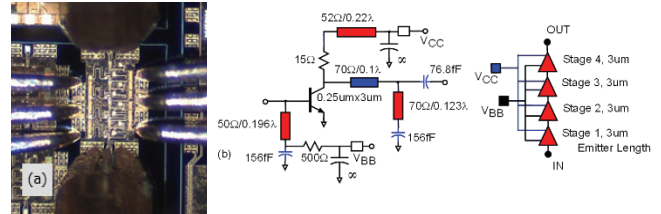


Figure 7: Common-emitter LNA: die photo (a) and amplifier circuit diagram (b). The amplifier obtains 13 dB gain and 7.2 ± 0.4 dB noise figure over 196-216 GHz.

In designing a multi-stage LNA for low total (cascaded) noise figure, the individual stages should be designed for lowest noise measure (M_a), not lowest noise figure (F_a), as this minimizes the total noise contribution of input and subsequent LNA gain stages. Regardless of circuit configuration, the amplifier cascaded noise figure cannot be less [31] than $(M_i + 1)$, where M_i is the transistor minimum noise measure. To obtain LNA performance close to this limit, the transistor bias voltage and current density for minimum M_i is first determined. In common-emitter LNAs, an appropriate nonzero common-lead inductive reactance $j\omega L_E$ allows input tuning for zero input reflection coefficient simultaneously with tuning for minimum M_a , doing so without increasing the minimum M_a . In common-base, a nonzero common-lead capacitive reactance $1/j\omega C_{base}$ plays exactly the same role. Subsequently, the transistor emitter length or gate width is scaled, together with the DC current and the common-lead reactance, so that the source conductance for minimum M_a is 20 mS; this permits the input stage to be noise-matched to 50 Ohms with a single inductive shunt element (Figure 6), avoiding the added attenuation, hence the added noise, of a series matching element. A 200 GHz InP HBT LNA [32] designed by this technique (Figure 7) had 13 dB gain and 7.2 ± 0.4 dB measured noise figure; only 0.5 dB above the transistor minimum cascaded noise figure ($M_i + 1$).

Power-combining losses in 100-300 GHz power amplifiers must also be minimized. Reported combining techniques include corporate combiners (Figure 8a), direct series connection (Figure 8b) [33], and series connection using baluns (Figure 8c) [34, 35] or segmented transformers (Figure 8d) [36]. Noting first the transistor terminal RF voltages and currents measured or simulated under optimum load-pull conditions (Figure 8e), these terminal voltages and currents can be duplicated in a set of cascaded transistors

stages by using appropriate inter-stage matching networks and common-lead reactances. The RF output powers of a series of cascaded transistor stages then sum at the output of the cascade. This technique, cascade combining [37, 22], is an extension of direct series combining. For lower-frequency power amplifiers series techniques are popular because they avoid the high losses of corporate combiners. However, because IC corporate combiner losses, in dB, vary in proportion to $f^{-1/2}$, the advantage of series techniques over corporate combiners diminishes at higher frequencies. The designs of Figure 9 [19,20,21,22] use a combination of corporate and cascade combining.

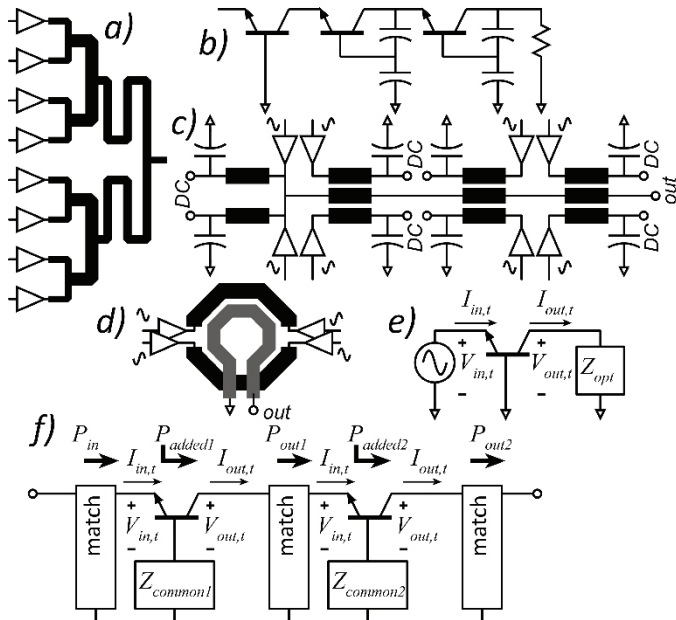


Figure 8: Millimeter-wave power-combining techniques include (a) corporate combiners, (b) direct series connection, and series connection using sub- $\lambda/4$ baluns (c) or segmented transformers (d). By duplicating the transistor RF voltages and currents arising (e) under optimum load-pull conditions, cascade power-combining (f) uses inter-stage matching networks and common-lead impedances to sum the output powers of transistors in a cascade of gain stages.

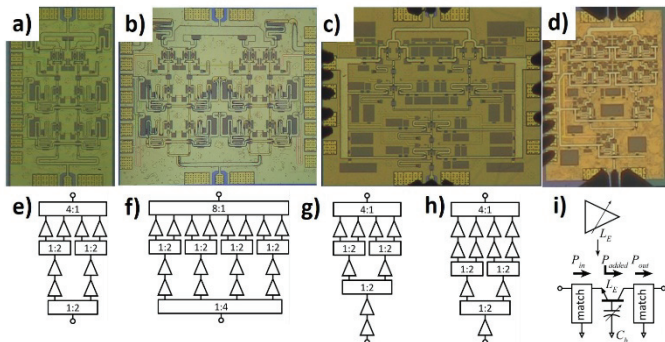


Figure 9: InP HBT power amplifiers at (a) 140 GHz with 109 mW power and 20.8% PAE, (b) 131 GHz with 200 mW power and 17.8% PAE, (c) 194 GHz with 55 mW power and 8.5% PAE, and (d) 266 GHz with 48 mW power and 4% PAE. (e-h) show the corresponding amplifier block diagrams. The amplifiers use capacitively degenerated common-base gain stages (i); the 266 GHz design has significant cascade power-combining.

Figure 10 shows RF front-end transmitter and receiver ICs at 140 GHz in GlobalFoundries 22 nm SOI CMOS [14], and at 200 GHz in Teledyne 250 nm InP HBT [38]. In these, mixers convert signals between RF and (I,Q) baseband, with the mixer local oscillators generated by frequency multipliers to provide low phase noise.

Array Module Design: 100-300 GHz array transceivers present significant packaging challenges. To steer over 180° both in azimuth and elevation, the array must be 2-dimensional and must have $\sim \lambda/2$ element spacing, ~ 1 mm at 140 GHz and 0.5 mm at 300

GHz. It is difficult to fit the necessary RF electronics in a small available area, and it can be difficult to remove the heat, particularly if inefficient or high-power power amplifiers are used.

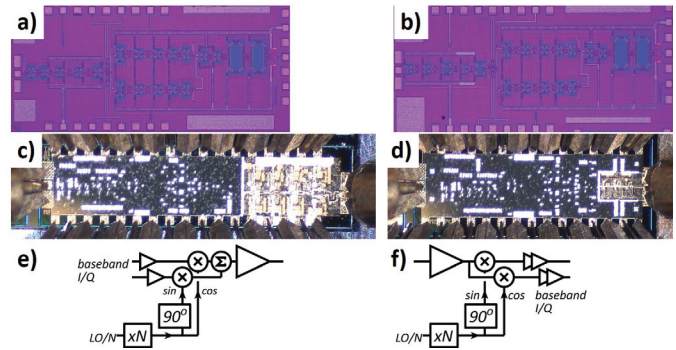


Figure 10: Representative 100-300 GHz transceiver ICs, including a 140 GHz receiver (a) and transmitter (b) in 22 nm SOI CMOS, a (c) 200 GHz transmitter with 34 mW output power, and (d) a 200 GHz receiver with 7.7-9.3 dB noise figure, both in 250 nm InP HBT; (e,f) show transmitter and receiver block diagrams

If the users are mostly distributed over the ground, then the array is best designed to steer only in azimuth, and is then 1-dimensional (Figure 1). There is then sufficient space along the edges of the array both to fit the mm-wave front-end ICs and to remove the heat. Figure 11 shows an 8-channel receiver array tile module designed for 140 GHz MIMO hubs (Figure 1). With these, we have demonstrated [39] MIMO digital beamforming (Figure 12) and data transmission (Figure 13). 8-channel transmitter MIMO hub array modules are also in development, and will be subsequently reported.

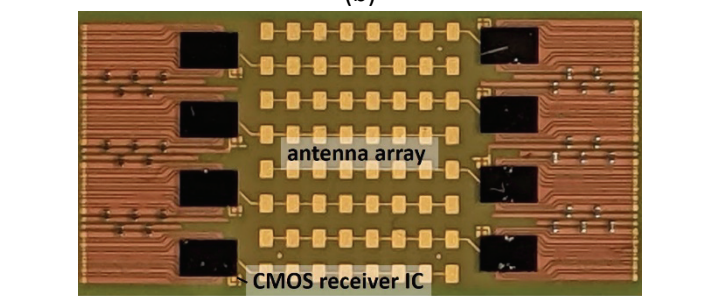
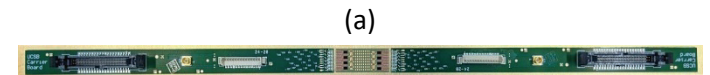
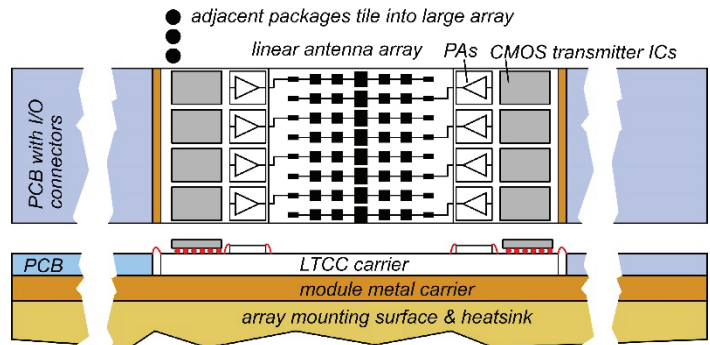


Figure 11: Eight-channel 140 GHz MIMO hub receiver array tile module: (a) schematic cross-section diagram showing the interface printed circuit boards, the LTCC carrier, connectors, and ICs, (b) photograph of the overall module, and (c) photograph of the LTCC carrier showing the antennas and CMOS ICs. The overall module is 450 mm \times 15 mm, while the LTCC carrier is approximately 12 mm \times 25 mm. A similar 8-channel transmitter module, with InP power amplifiers and CMOS ICs, is in development.

In MIMO backhaul links (Figure 2), phased-array beam steering in two planes over a small angular range can correct for small angular

aiming errors from installation. For 10° beam steering range, the elements can be spaced at $\sim 7\lambda$. Figure 14 shows an array tile design for this application, with linear arrays of antennas and ICs mounted on a metal tray, with trays then stacked to form a 2D array. We are presently developing versions of these modules both at 200 GHz using previously-designed ICs [38] and at 280 GHz using ICs now in development.

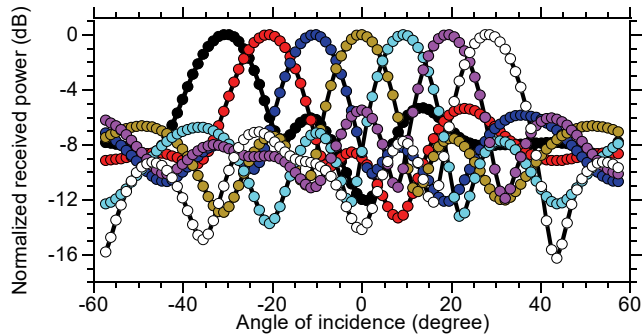


Figure 12: Measured patterns for the 8-channel receiver array, taken with the test transmitter located at varying angular positions

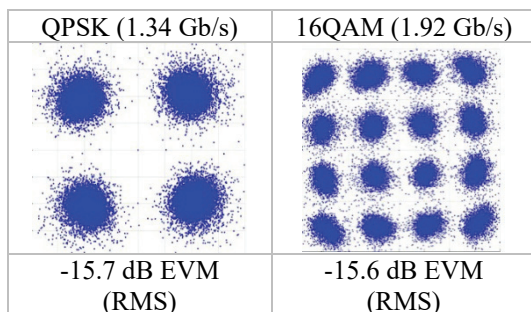


Figure 13: Receiver tile module measured modulation constellations and computed error vector magnitudes. The data is transmitted using OFDM, with 960 kHz subcarrier spacing.

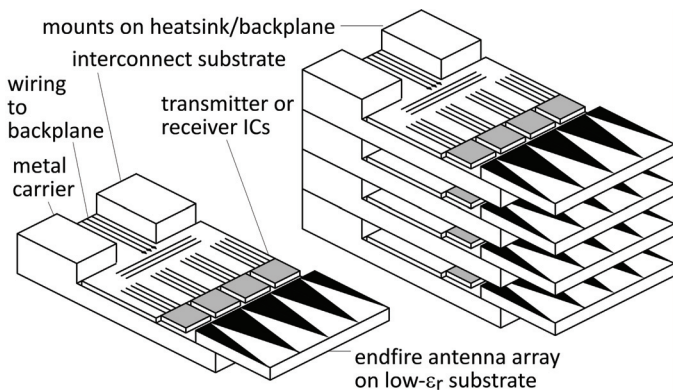


Figure 14: Array tile design with $\sim 7\lambda$ spacing for small-angular-deviation 2D beam steering in fix-aimed point-point links.

Conclusions: A wide radio spectrum is available between 100 GHz and 300 GHz; further, because the wavelengths are short, massive spatial multiplexing is feasible even from compact arrays. Aggregate capacities in endpoint and backhaul links can approach or even exceed 1 Tb/s, but high atmospheric losses limit range to 100-500 m. Challenges include digital beamforming, array module packaging, and the cost and power consumption of the mm-wave arrays, these containing many elements..

Acknowledgments: This work was supported in part by the Semiconductor Research Corporation and DARPA under the JUMP program. The authors thank Kyocera for fabrication of the LTCC carriers and module assembly and GlobalFoundries for 22 nm FDSOI IC fabrication and for free access to advanced copper pillars. Thanks to Gary Xu and Navneet Sharma of Samsung Research America for guidance and encouragement.

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