D-band CMOS+InP and CMOS-only MIMO communication transceiver technologies

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Acknowledgments

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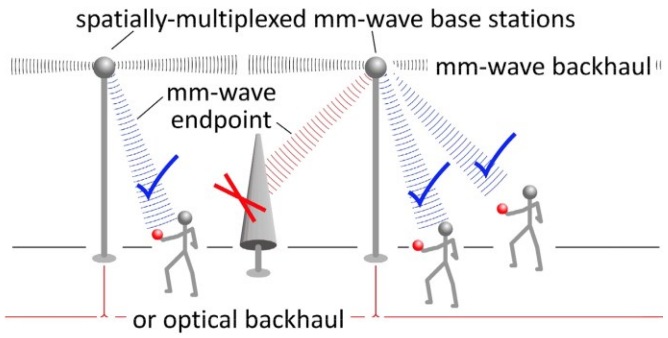
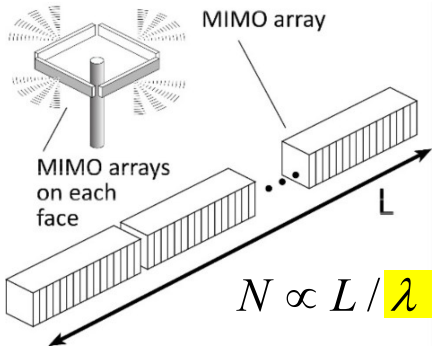
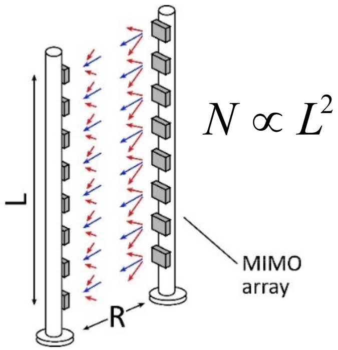
Benefits of Short Wavelengths

Communications: Massive spatial multiplexing, massive # of parallel channels. Also, more spectrum.



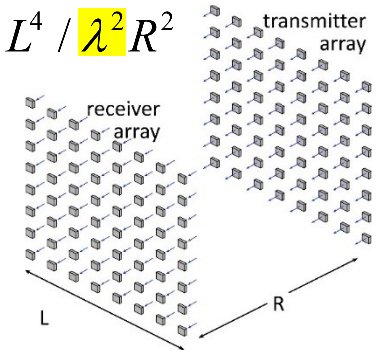


$N \propto L / \lambda$

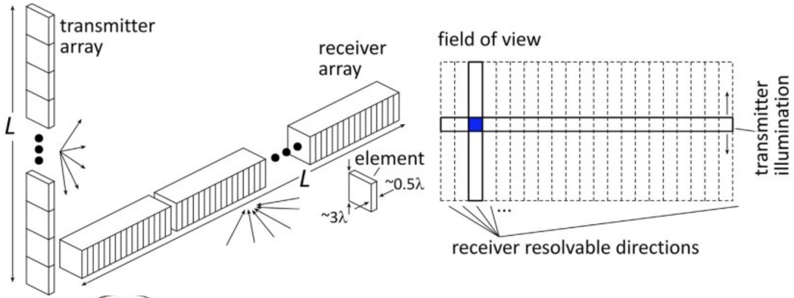


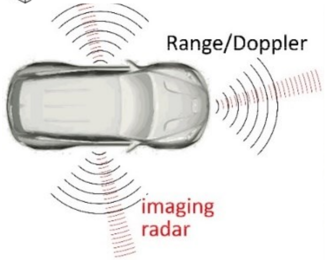
$N \propto L^2 / \lambda R$

$N \propto L^4 / \lambda^2 R^2$



Imaging: very fine angular resolution





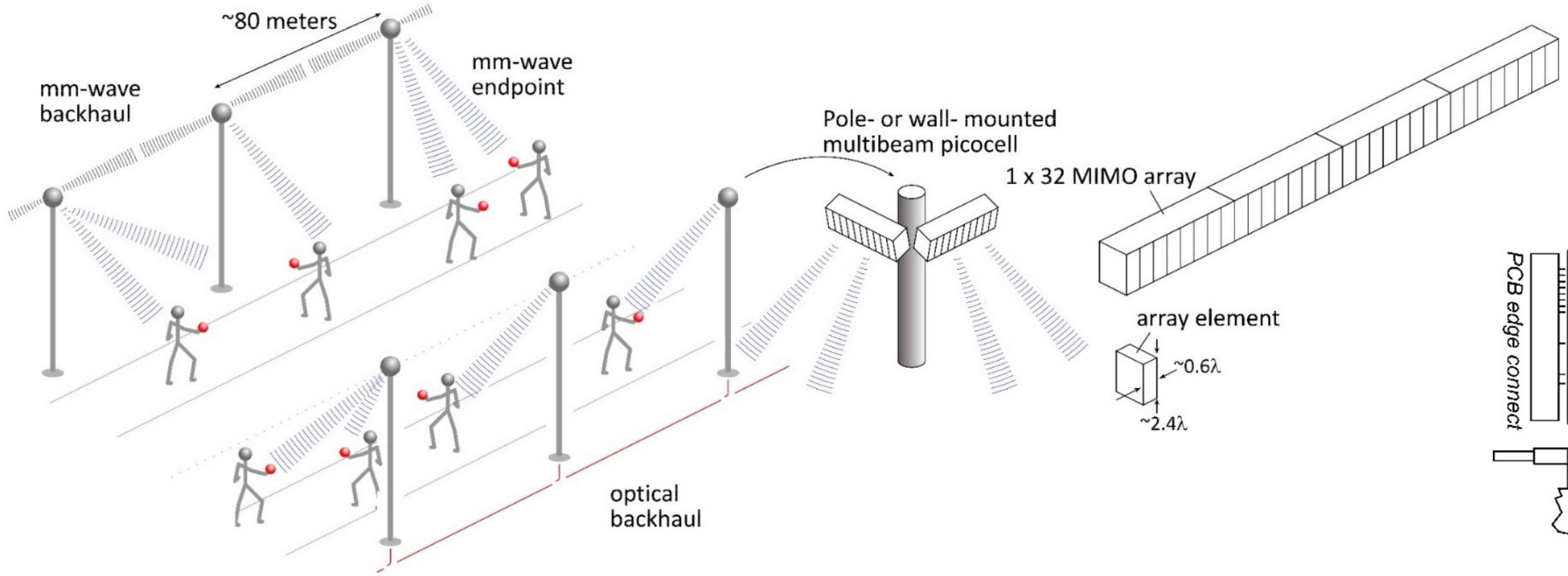
$\Delta\theta \propto \lambda / L$

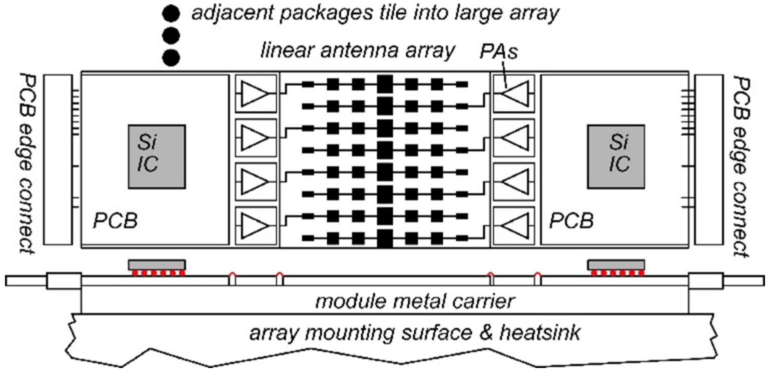
But:

High losses in foul or humid weather.
High λ^2/R^2 path losses.
ICs: poorer PAs & LNAs.
Beams easily blocked.

100-300GHz wireless:
terabit capacity,
short range,
highly intermittent

140GHz moderate-MIMO hub



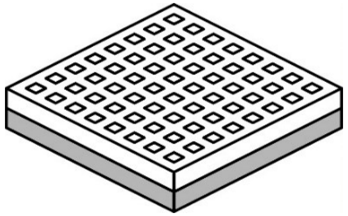


If hub uses 32-element array (four 1×8 modules):

16 users/array. P_{1dB}=21 dB_m PAs, F=8dB LNAs

1,10 Gb/s/beam→ **16**, 160 Gb/s total capacity

70, 40 m range in 50mm/hr rain with **17**dB total margins



Handset:
8 × 8 array
(9×9mm)

70 GHz spatially multiplexed base station

If we use instead a 70GHz carrier,
the range increases to **70 meters** (vs. **40 meters**)
but the handset becomes 16mm×16mm (vs. 8mm×8mm),
and the hub array becomes 19mm×612mm (vs. 10mm×328mm)

Or, use a 4×4 (8mm×8mm) handset array,
and the range becomes ..**about 40 meters**.

Same handset area (more handset elements)→ same link budget
Easier to obtain license for 140±2.5GHz than 70±2.5GHz

210 GHz, 640 Gb/s MIMO Backhaul

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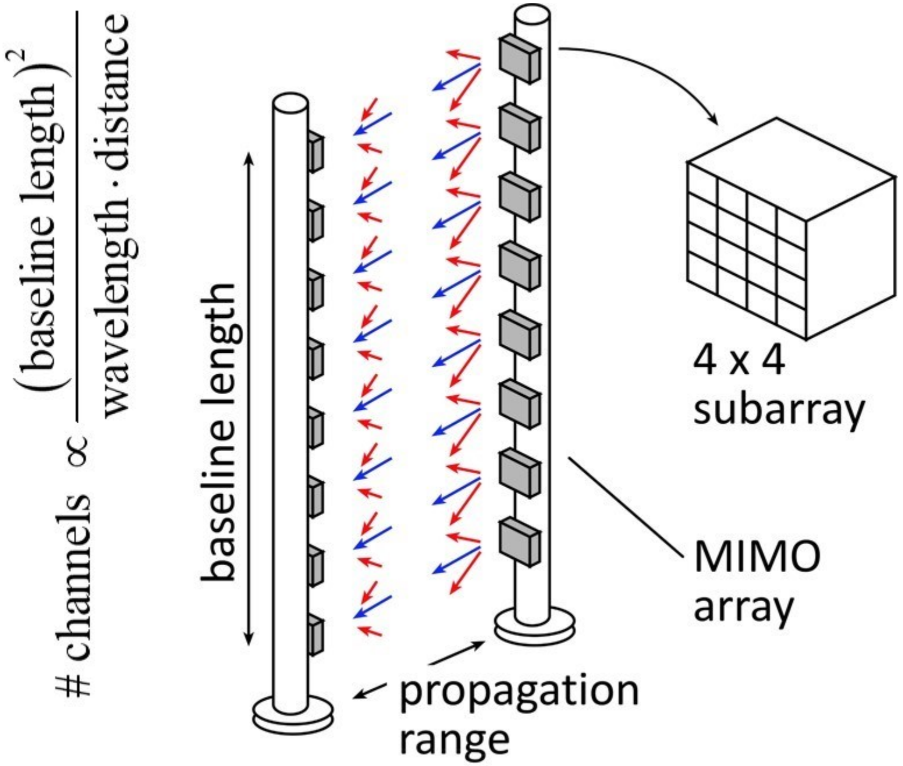
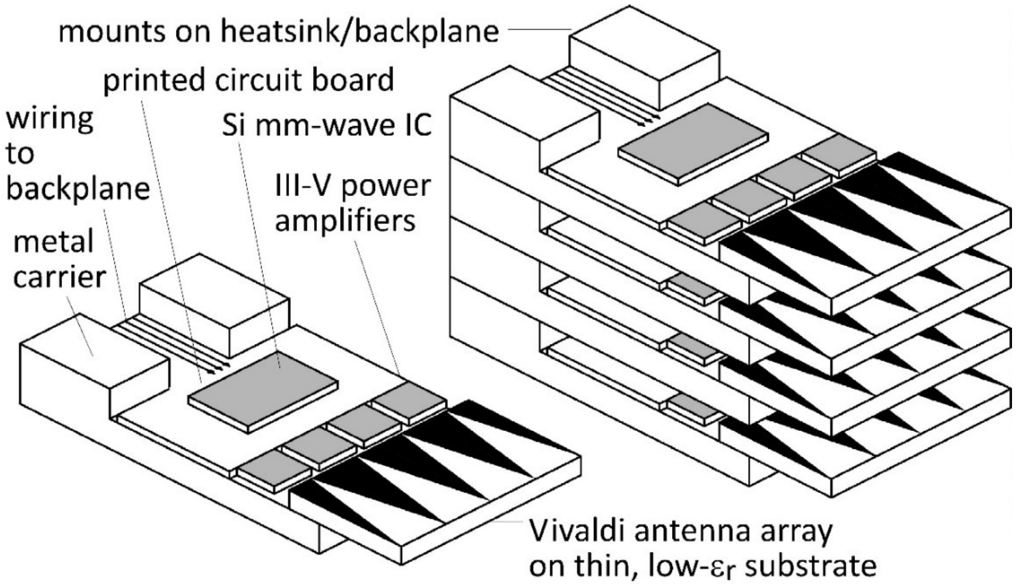


8-element MIMO array
2.1 m baseline.
80Gb/s/subarray→ 640Gb/s total
4 × 4 sub-arrays → 8 degree beamsteering

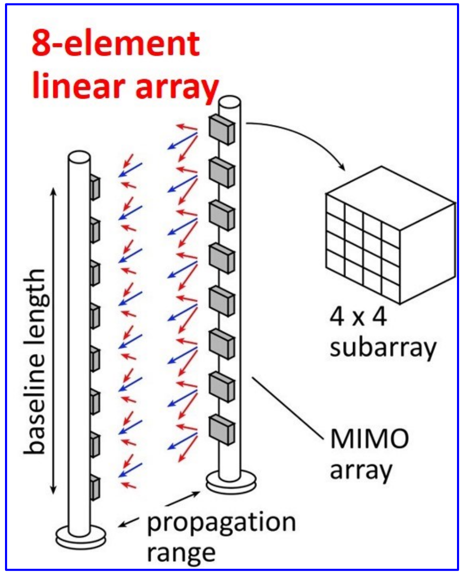


Key link parameters
500 meters range in 50 mm/hr rain; 23 dB/km
20 dB total margins:
packaging loss, obstruction, operating, design, aging
PAs: 18dBm $=P_{1dB}$ (per element)
LNAs: 6dB noise figure

75 GHz, 640 Gb/s MIMO backhaul (16QAM)

Why not use a lower-frequency carrier, e.g. 75 GHz ?

Must use at least 16QAM, given 80Gb/s/channel…



8-element 640Gb/s linear array:

requires 16dB$_m$ transmit power/element (P_{out})

requires 3.5m linear array

Similar RF power output, physically larger

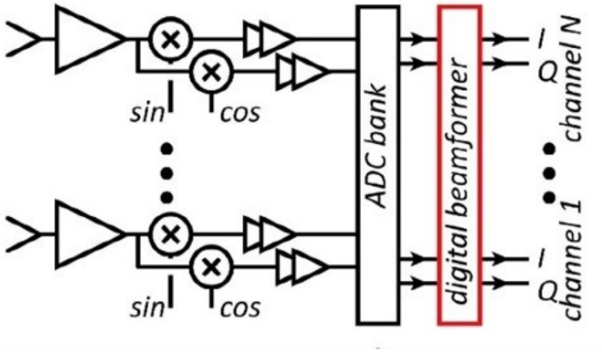
Systems Design

MIMO System Design

ADCs/DACs[1]: QPSK needs only 3-4 bit ADC/DACs

N ADC bits, *M* antennas, *K* signals: $SNR=6N+1.76+10\cdot\log_{10}(M/K)$

3 bits, $(M/K)=2 \rightarrow$ SNR=23 dB. QPSK needs 9.8 dB.



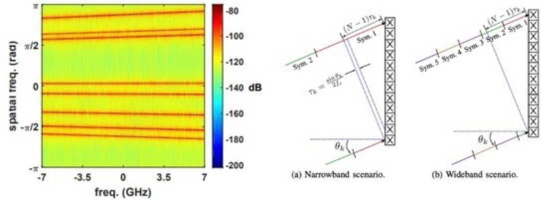
Linearity[1]: Amplifier P_{1dB} need be only 4 dB above average power

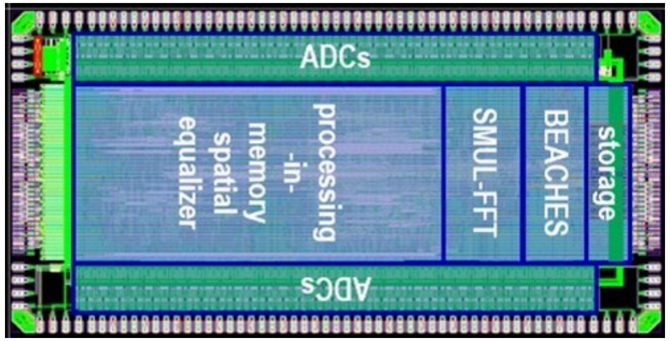
Phase noise[2,3]: Requirements same as for SISO

Efficient digital beamforming[4,5]: beamspace algorithm=complexity ~N× log(N)

Efficient VLSI digital beamformer implementation[6]: low-resolution matrix

Efficient beamforming in broadband arrays[7]: combined spatial & temporal FFTs.





1) M. Abdelghany et al, IEEE Trans. Wireless Comm, Sept. 2021
2) M. E. Rasekh et al, IEEE Trans. Wireless Comm, Oct. 2021
3) A. Puglielli et al, 2016 IEEE ICC
4) M. Abdelghany, et. al, , 2019 IEEE SPAWC
5) S. H. Mirfarshbafan et al, IEEE Trans CAS 1, 2020
6) O Castañeda Fernández et. al, 2021 ESSCIRC
7) M. Abdelghany et al 2019 IEEE GLOBECOM

100-300 GHz IC design: Transistors

Transistors for 100-300GHz

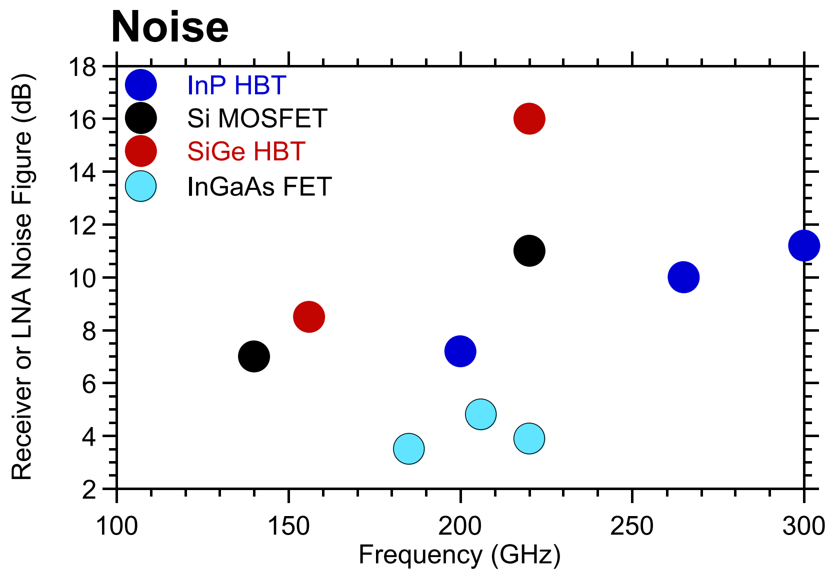
CMOS: good power & noise up to ~150GHz. Not much beyond. 65-32nm nodes are best.

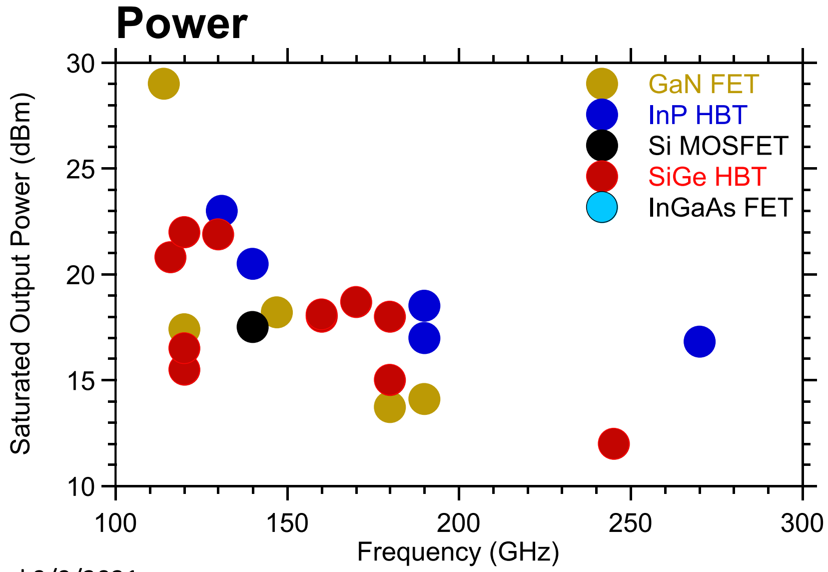
InP HBT: record 100-300GHz PAs

SiGe HBT: out-performs CMOS above 200GHz

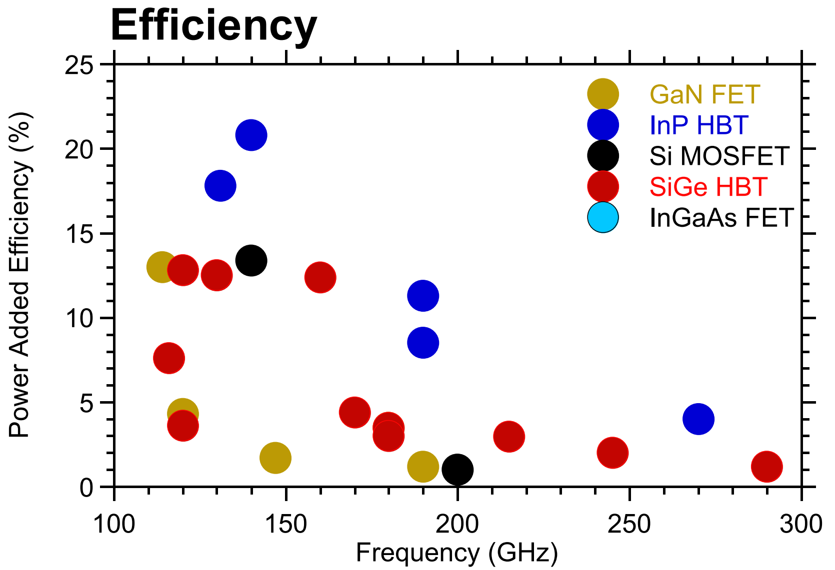
GaN HEMT: record power below 100GHz. Bandwidth improving

InGaAs-channel HEMT: world's best low-noise amplifiers





Results with low power but high PAE, or low PAE but high power, are not shown

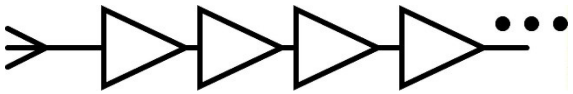


Results compiled 9/9/2021

100-300 GHz IC design: Low-noise amplifiers

LNA design: noise close to transistor limits

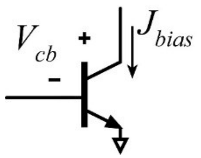
1) Goal: low noise measure, not noise figure

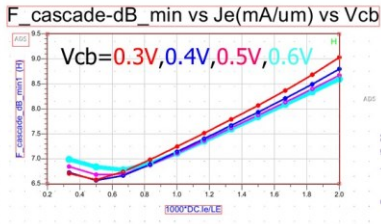


$$F_{\text{cascade}} = M + 1 = F + \frac{F-1}{G} + \frac{F-1}{G^2} + \ldots = \frac{F - 1/G}{1 - 1/G}$$

F = noise figure, M = noise measure

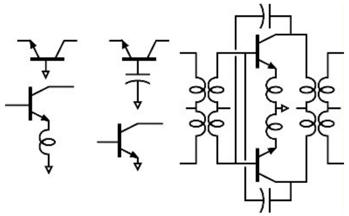
2) Find bias current density for lowest noise measure





@210GHz,
$F_{cascade,min}$= 6.57 dB
given:
J_e=0.5 mA/um,
V_{cb}=0.3V

3) Minimum M is independent of circuit configuration*; pick for high bandwidth or high gain/stage (= low P_{DC})

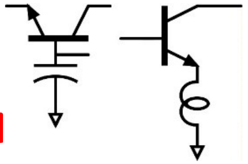


<-- all give the same minimum M…

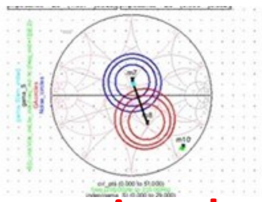
…but common-base gives highest gain (InP HBT @210GHz).

*HA Haus, RB Adler, Proceedings of the IRE, 1958

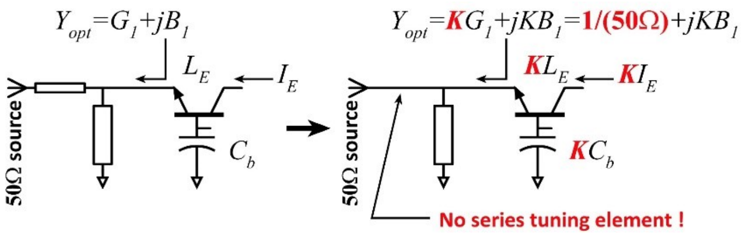
4) Capacitance in common-base; just like inductance in common-emitter, allows simultaneous tuning for zero reflection coefficient and minimum M



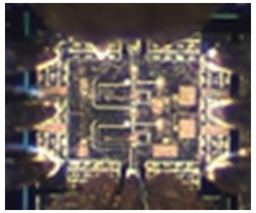
5) Write ADS Python code to display source impedance for minimum M.

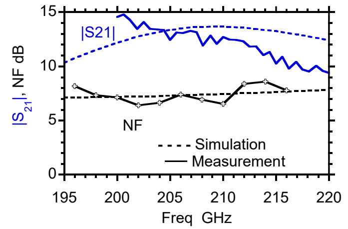


6) Scale transistor size to eliminate series tuning element.
Less input tuning→ less noise from passive element loss.



Result: 7.2-7.4dB LNA noise given 6.6dB transistor $F_{cascade}$.



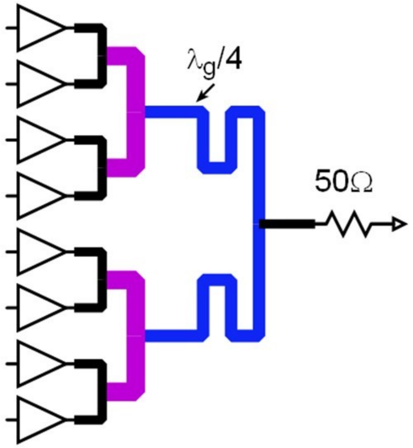


U. Solyu et. al, to be presented, 2021 EuMIC Conference

100-300 GHz IC design: Power amplifiers

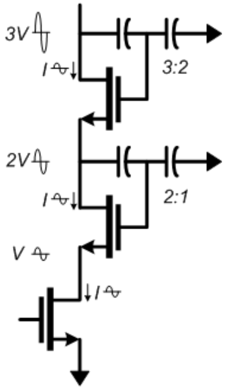
100-300GHz Power combining: what is best ?

Corporate T-line



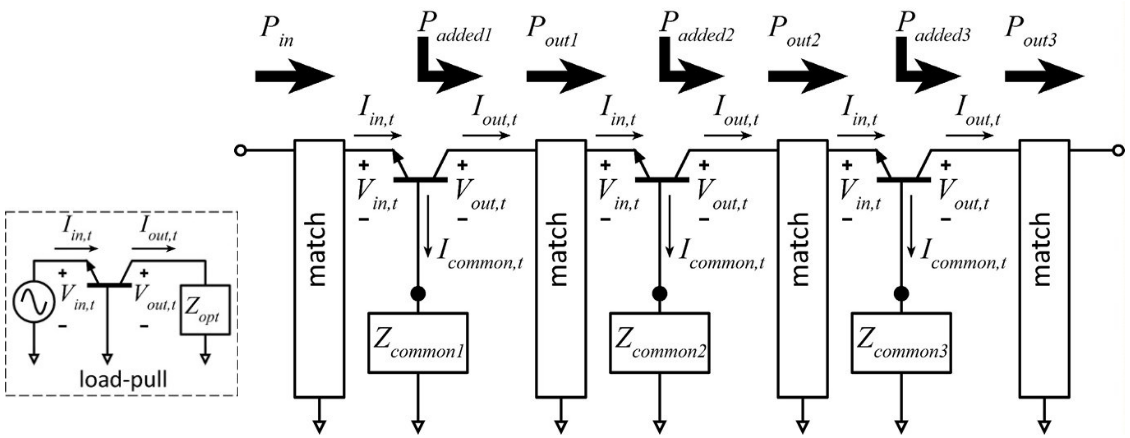
Direct series-connected

M. Shifrin: 1992 IEEE μWave/mmWave Monolithic Circuits Symp. **(Raytheon)**



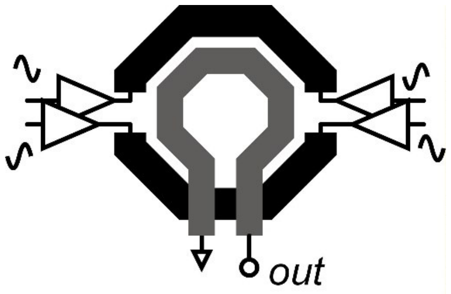
Cascaded combining

A. Ahmed 2018 EuMIC, 2021 RFIC **(UCSB)**



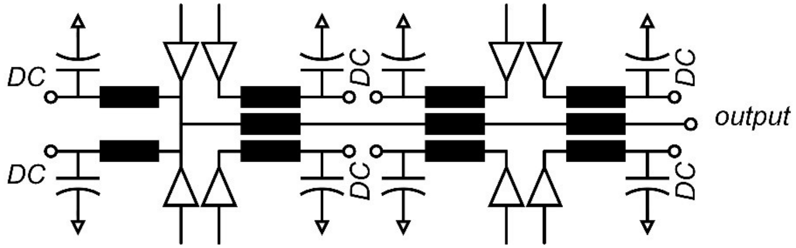
Distributed Active Transformer

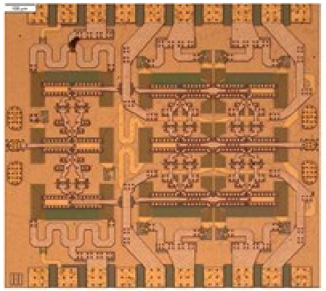
I. Aoki, IEEE Trans MTT, Jan. 2002 **(CalTech)**



Balun series-connected

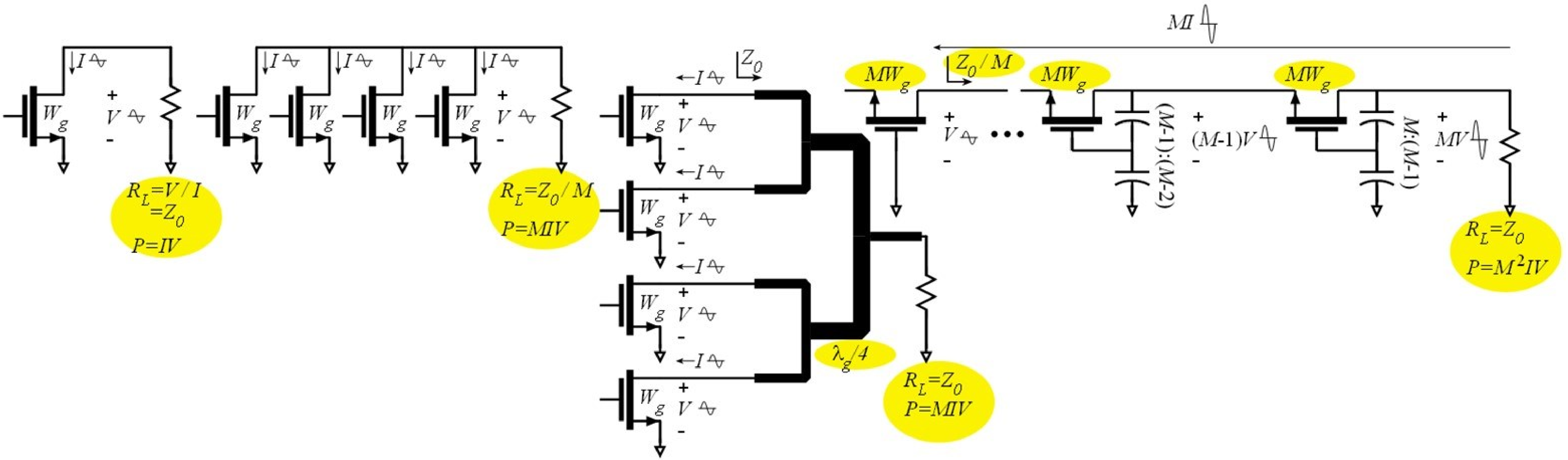
λ/4 baluns: Y. Yoshihara, 2008 IEEE Asian Solid-State Circuits Conference **(Toshiba)**
sub-λ/4 baluns: H. Park, et al, IEEE JSSC, Oct. 2014 **(UCSB)**





470mW, 81GHz, 23.4% PAE

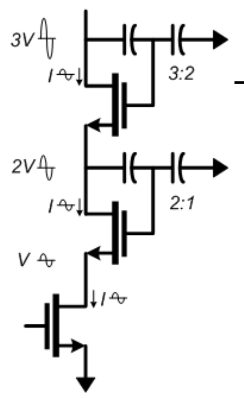
Transistor stacking. Why ? Why not ?

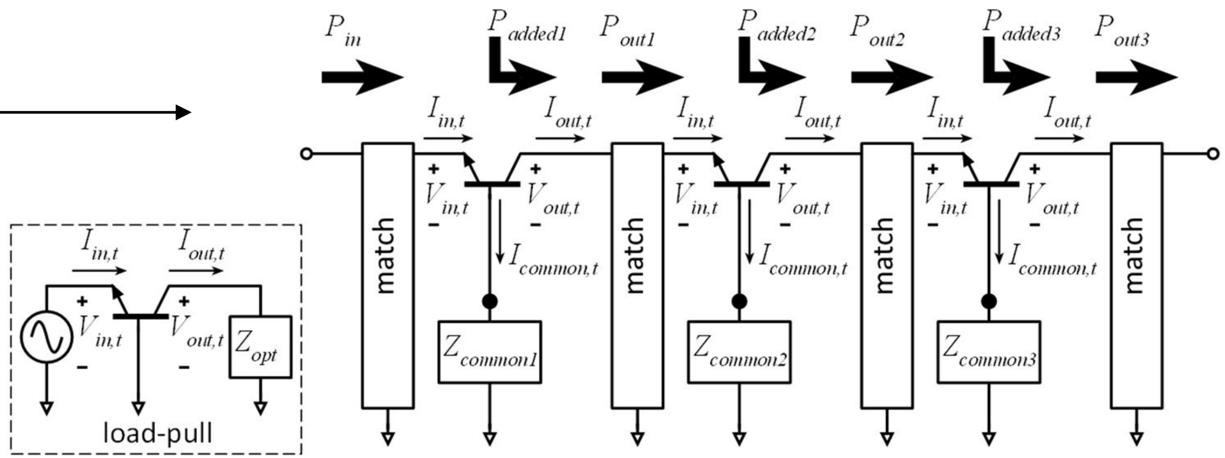


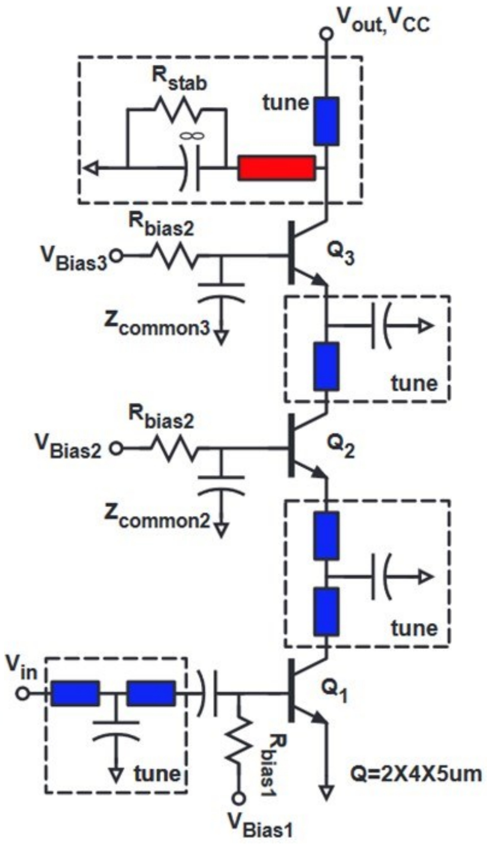
	Lower frequencies	Higher frequencies
Corporate combining	length ∝ $1/f$ → large die area ✗ dB loss ∝ $1/\sqrt{f}$ → high loss ✗	length ∝ $1/f$ → small die area ✓ dB loss ∝ $1/\sqrt{f}$ → low loss ✓
Series-connected	more transistor fingers per cell → ok ✓	more transistor fingers per cell → parasitics ✗

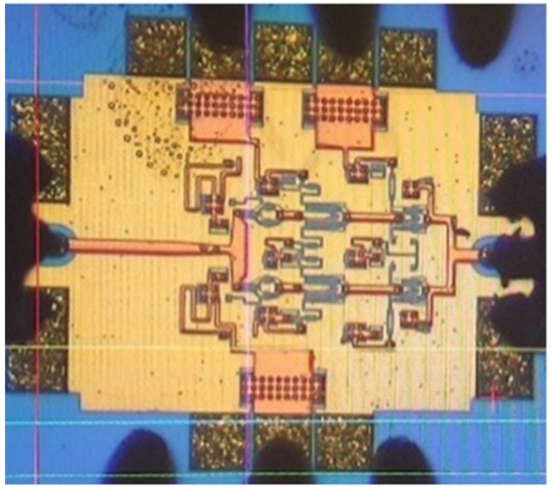
Cascade combining as stacking plus matching

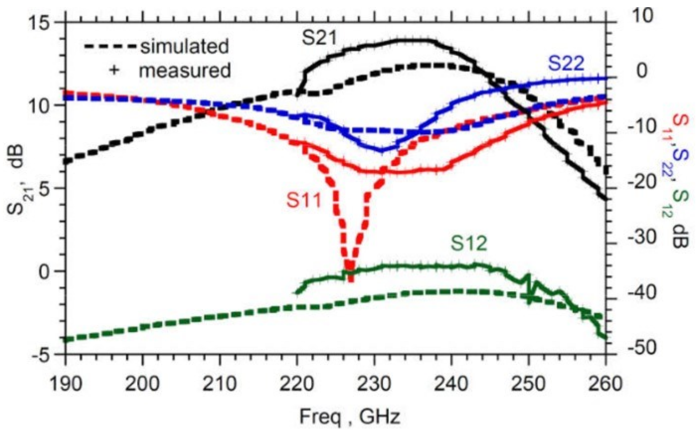
A. S. H. Ahmed et al, 2018 EuMIC (UCSB)

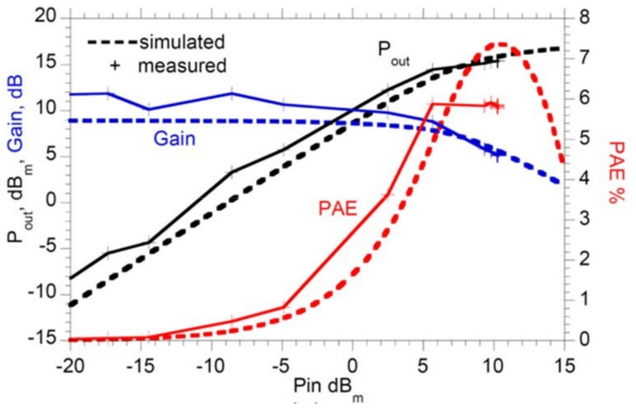








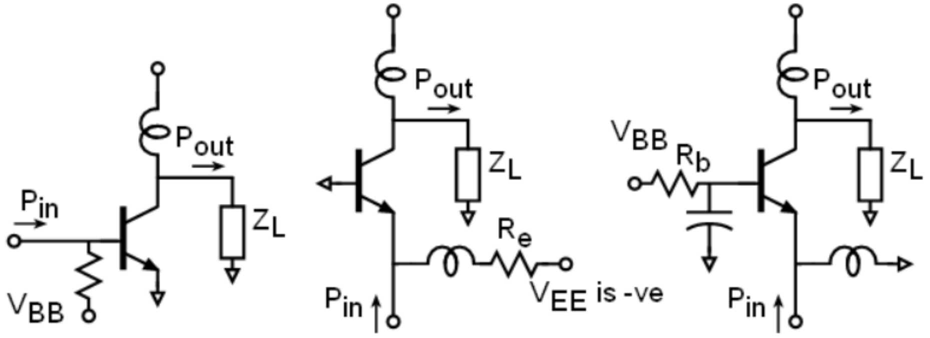




Capacitively degenerated common-base

Lower gain, same peak PAE, higher PAE at P_{1dB}.

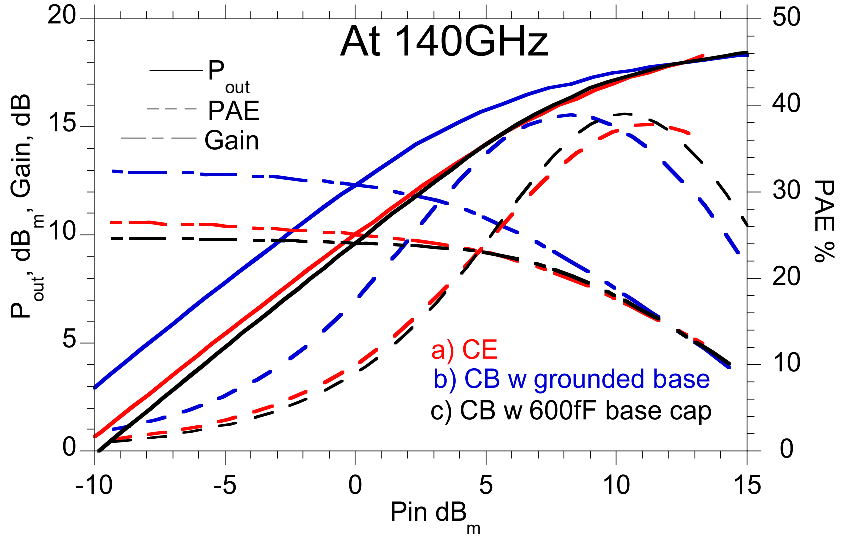
How does this differ from stacking ?

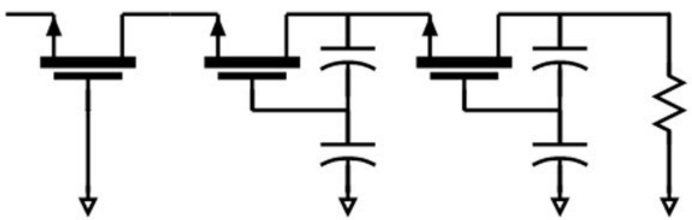


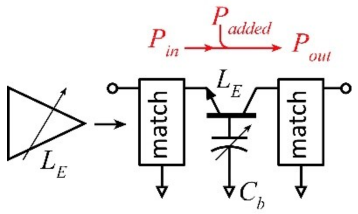
(a) CE

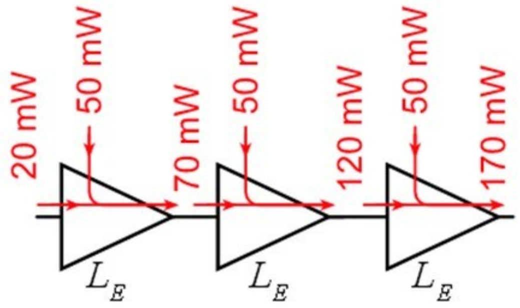
(b) CB with grounded base

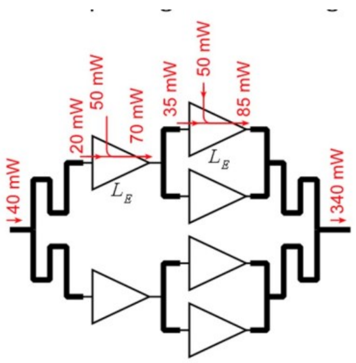
(c) CB with base capacitor





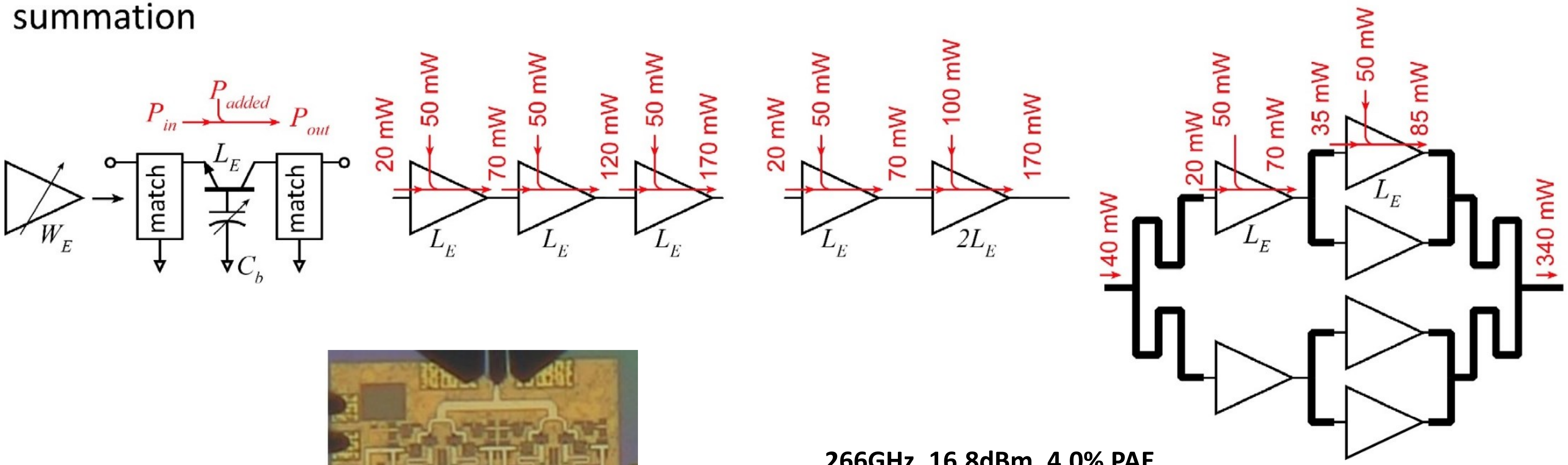




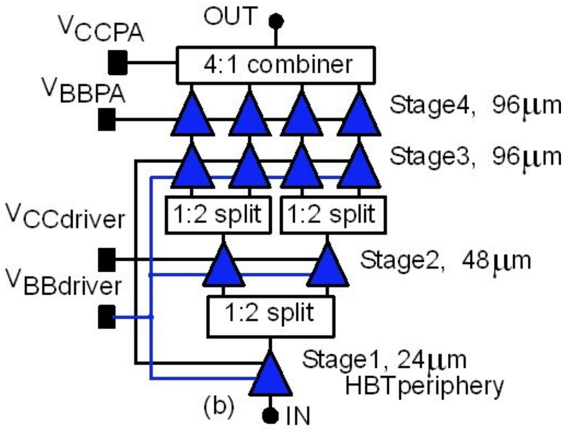


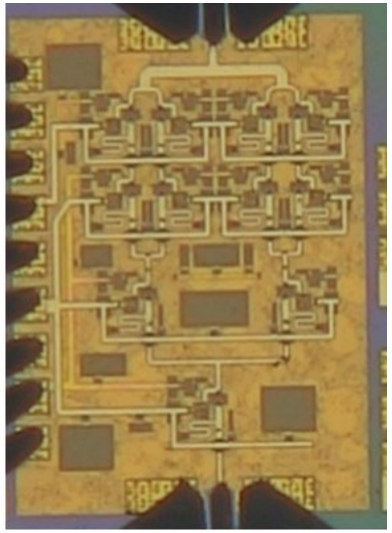
Generalized cascade combining

adjustable power summation =stacking + matching nonuniform with spittling or combining

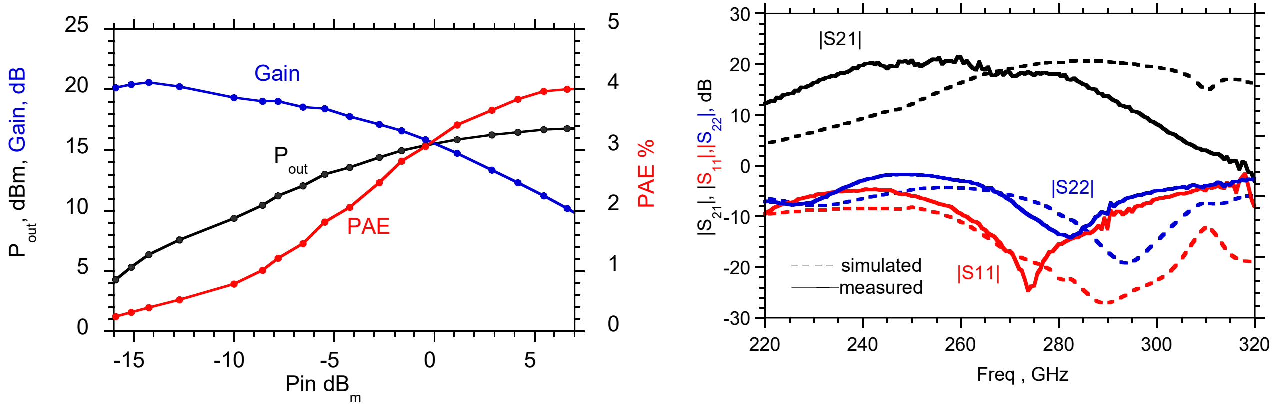


A. S. H. Ahmed et al, 2018 EuMIC (UCSB)
A. S. H. Ahmed, et al, 2021 RFIC Symposium

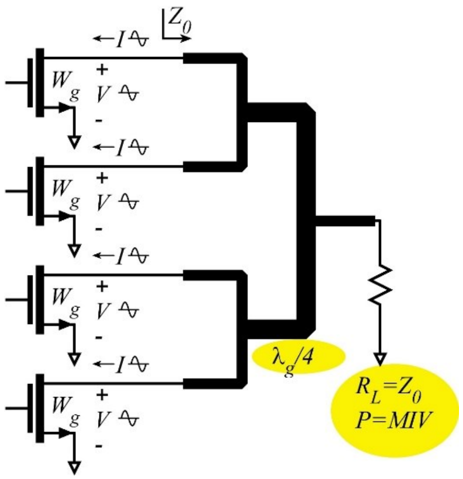


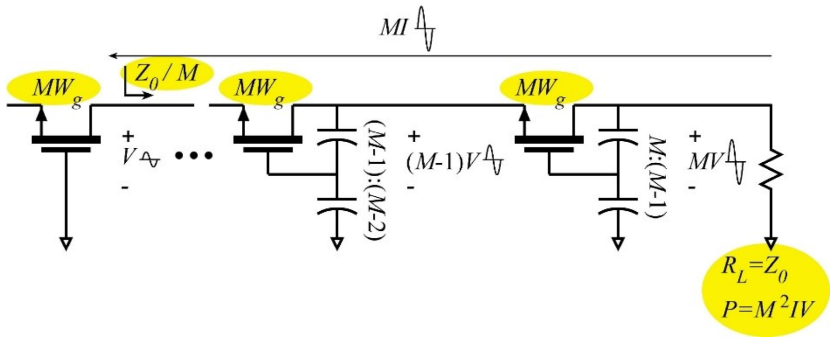


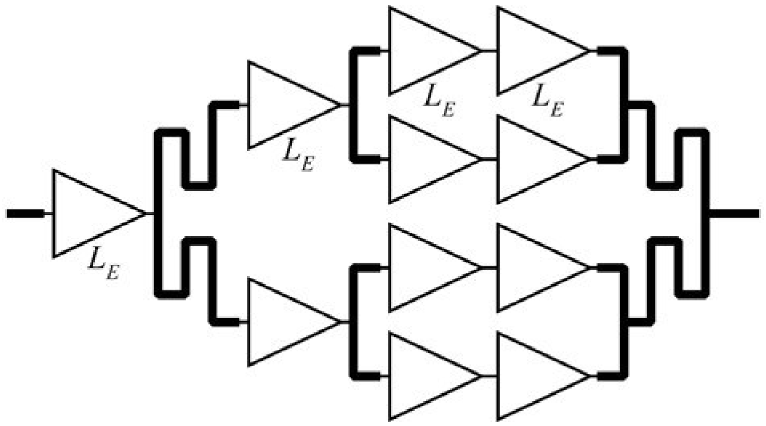
266GHz, 16.8dBm, 4.0% PAE



Cascade Combining: Why ? Why not ?







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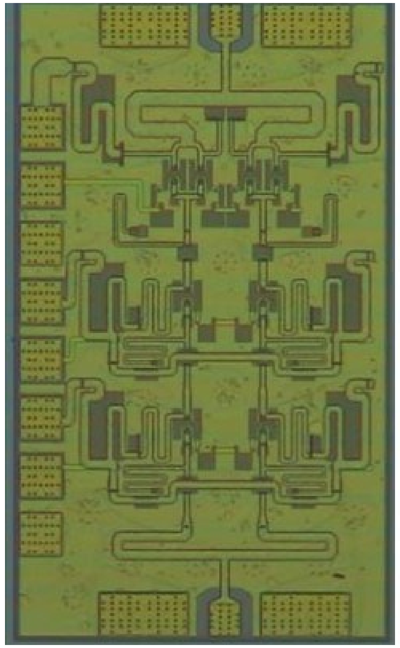
Corporate combining	length $\propto 1/f \rightarrow$ large die area ✗ dB loss $\propto 1/\sqrt{f} \rightarrow$ high loss ✗	length $\propto 1/f \rightarrow$ small die area ✓ dB loss $\propto 1/\sqrt{f} \rightarrow$ low loss ✓
Series-connected	more transistor fingers per cell → ok ✓	more transistor fingers per cell→ parasitics ✗
Cascade combining	large interstage matching networks ✗	small interstage matching networks ✓ small # transistor fingers per cell → ok ✓ cascade cell pass-though losses ✗

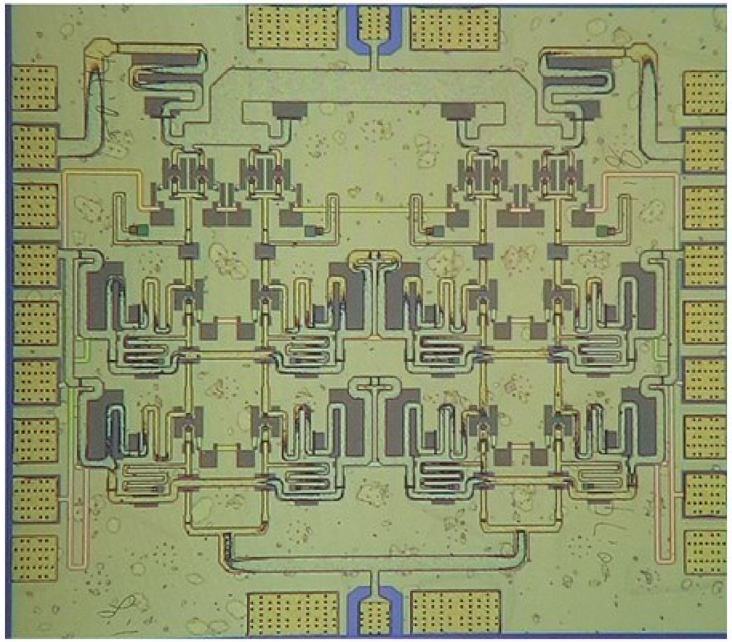
Recent high-efficiency 100-300GHz PAs

Teledyne 250nm InP HBT technology

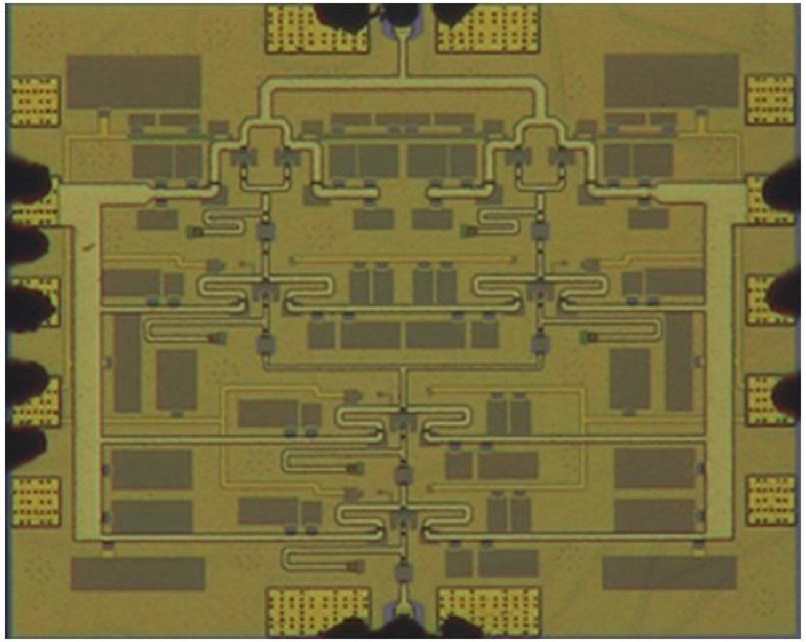
Ahmed et al, 2020 IMS, 2020 EuMIC, 2021 IMS, 2021 RFIC



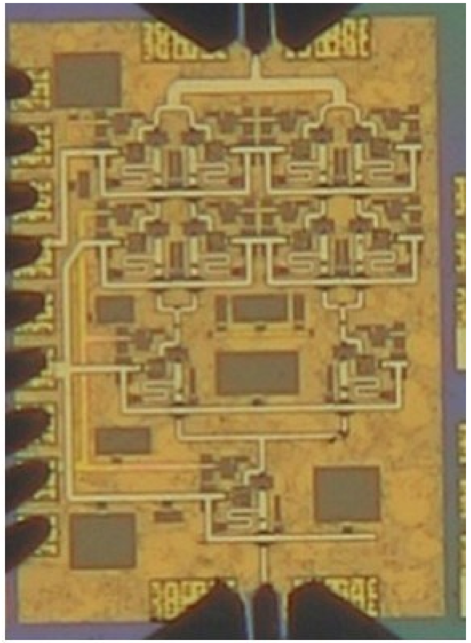
140GHz, 20.5dBm, 20.8% PAE



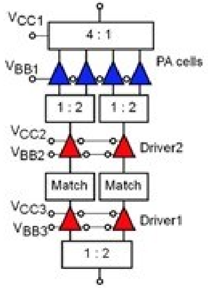
130GHz, 200mW, 17.8% PAE

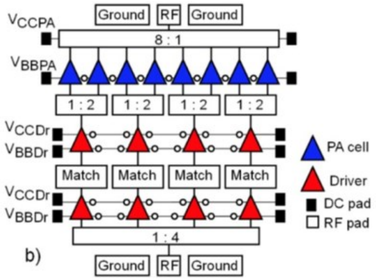


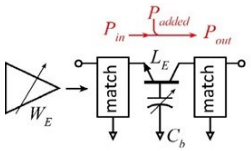
194GHz, 17.4dBm, 8.5% PAE

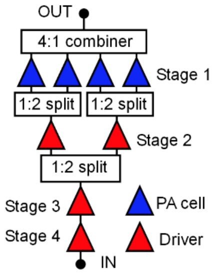


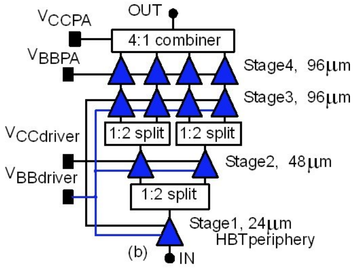
266GHz, 16.8dBm, 4.0% PAE







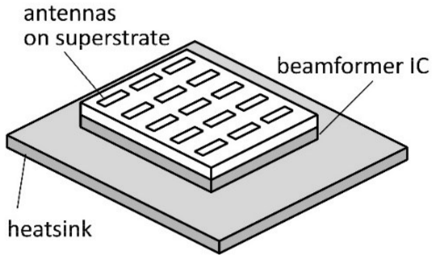


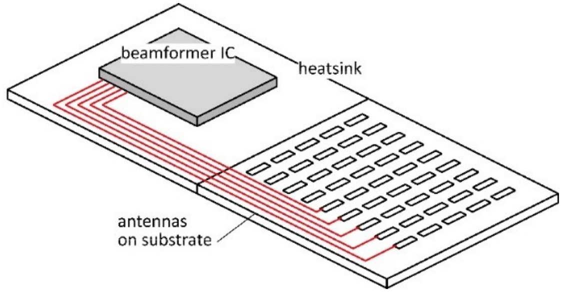


ICs and Modules: 140 GHz

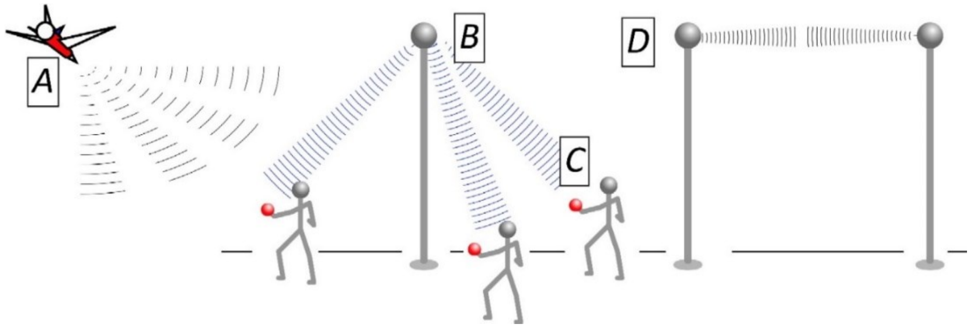
The mm-wave module design problem

How to make the IC electronics fit ?
How to avoid catastrophic signal losses ?
How to remove the heat ?

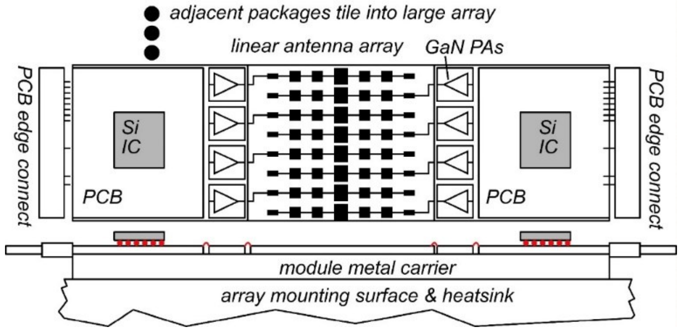


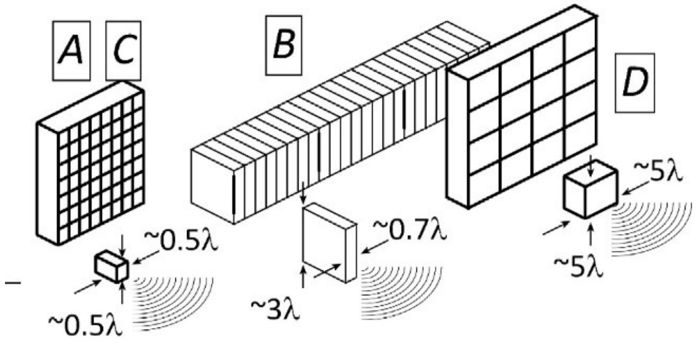


Not all systems steer in two planes...
...some steer in only one.



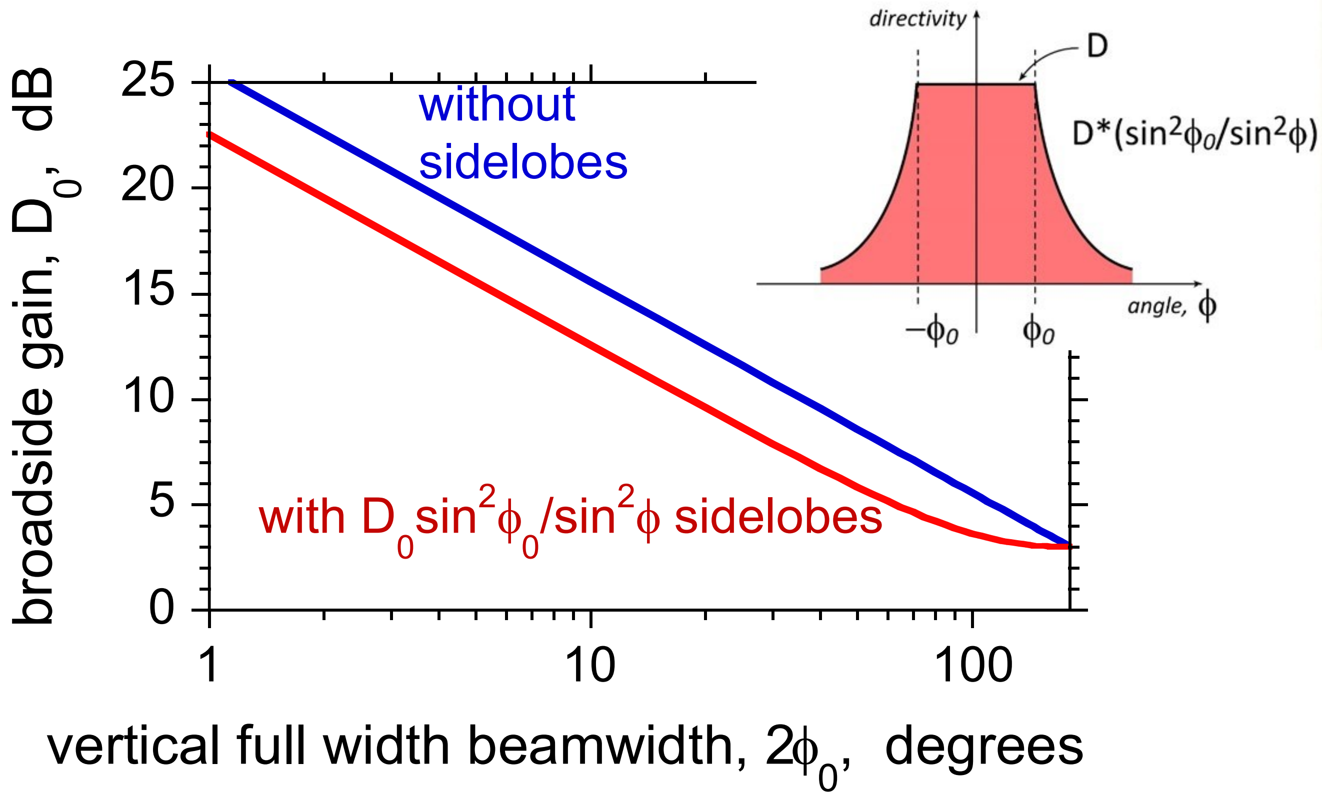
Not all systems steer over 180 degrees...
...some steer a smaller angular range

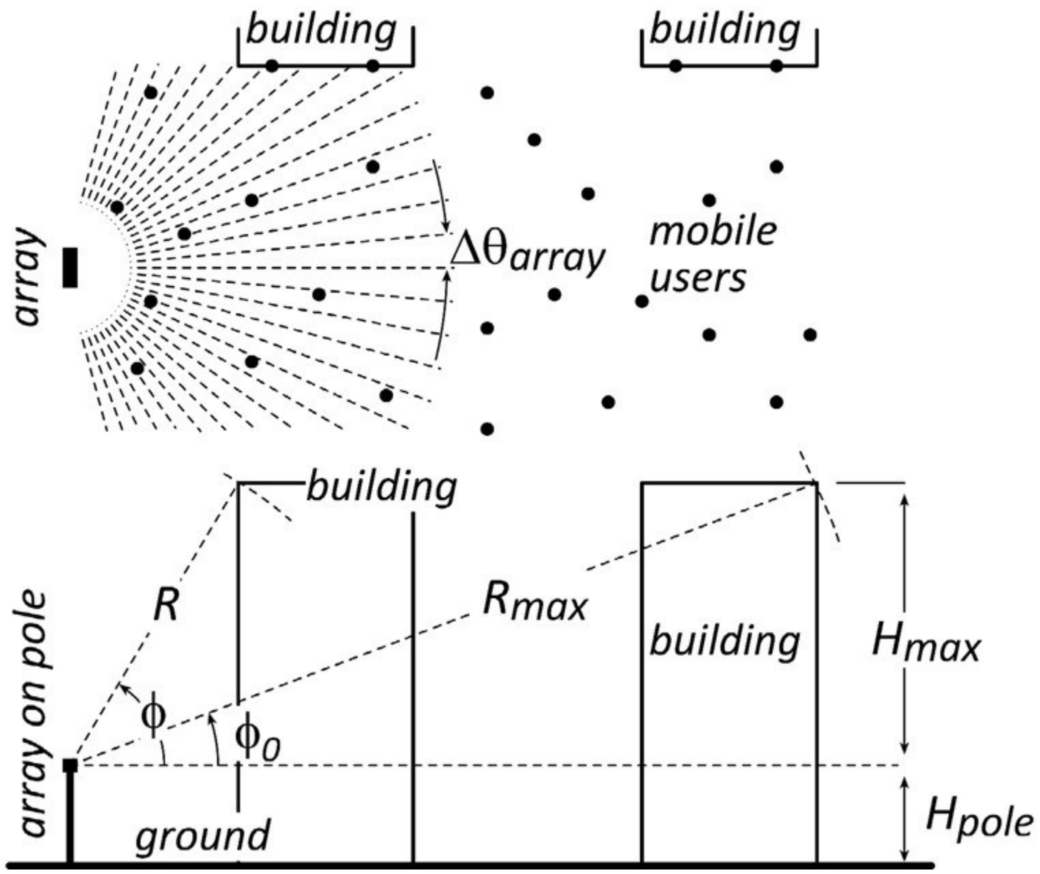




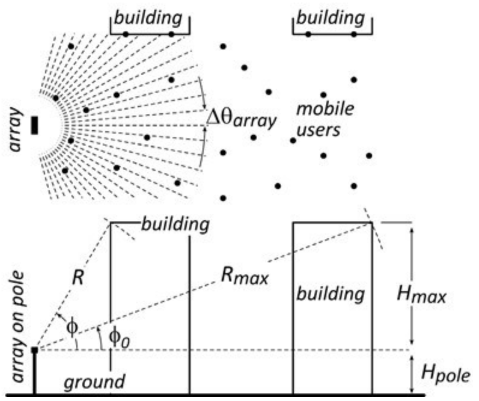
Do we need 2D arrays ? 1D might be fine.

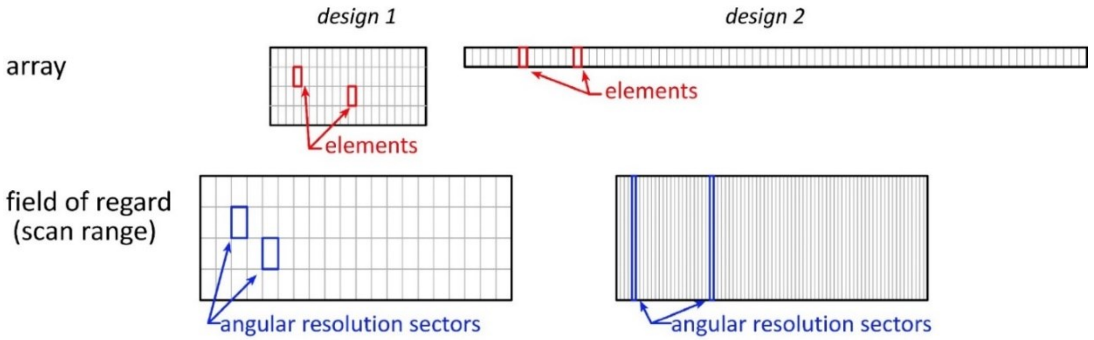
$1/\sin^2\phi$ sidelobes provide strong signals to tall buildings.
Providing sidelobes reduces broadside gain by less than 3dB.
→ Don't need 2D arrays to serve tall buildings





2D vs. 1D: user spatial distribution



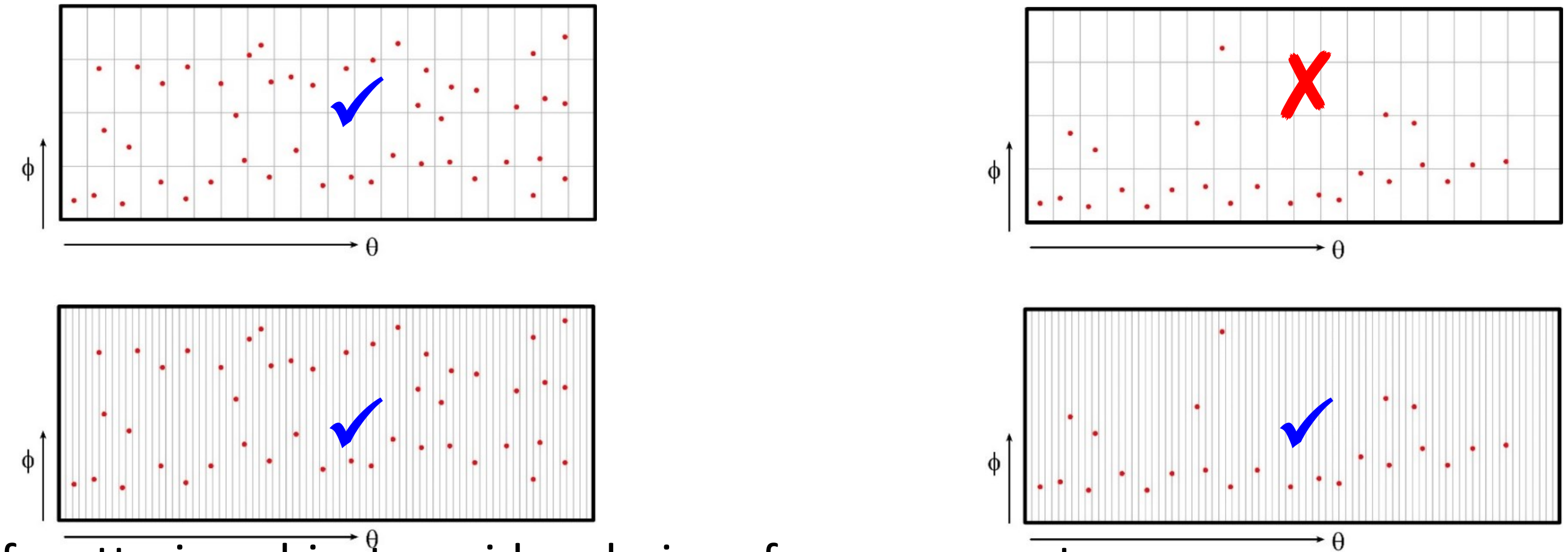


uniform horizontal & vertical user distributions

uniform horizontal, nonuniform vertical

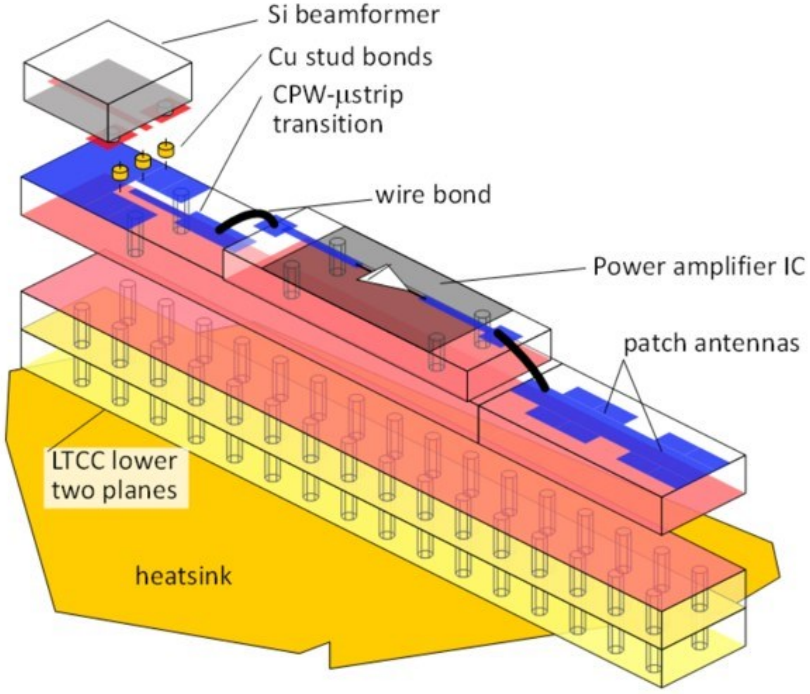
design 1: 2D array

design 2: 1D array

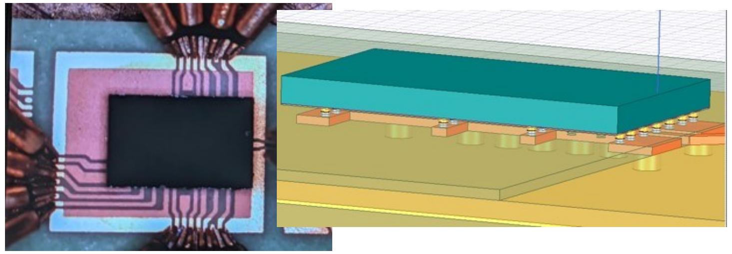


Spatial distribution of users, and of scattering objects, guides choice of array geometry.

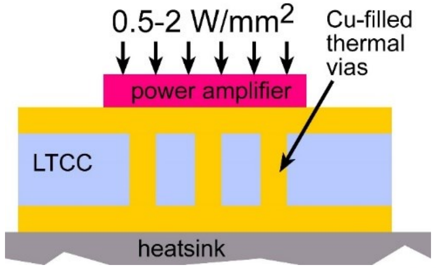
140GHz hub: packaging challenges



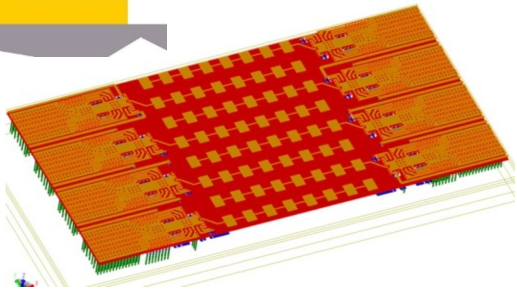
IC-package interconnects
Difficult at > 100 GHz



Removing heat
Thermal vias are marginal



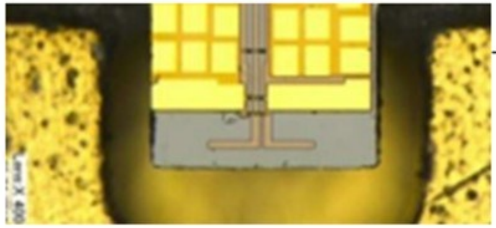
Interconnect density
Dense wiring for DC, LO, IF, control.
Hard to fit these all in.



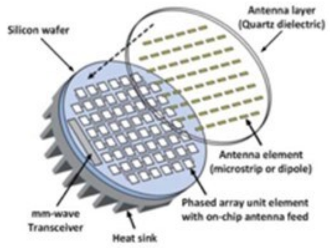
Economies of scale
Advanced packaging standards require sophisticated tools
High-volume orders only
Hard for small-volume orders (research, universities)
Packaging industry is moving offshore

100-300GHz IC-package connections

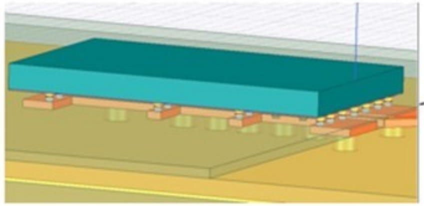
type	Frequency	technology	cost	heatsinking
micromachined waveguide interface	1000 GHz	Research. Cheap one day ?	high ✗	good
ribbon, mesh bond	200 GHz	Handcrafted.	high ✗	good
patch antennas on superstrate	1000 GHz	Straightforward	low	good
Cu stud flip-chip	>200 GHz	Industry standard	low	ok, marginal for PA ✗
hot vias	200 GHz	Development	low ?	good
(ball) wirebonds	100 GHz ✗	Industry standard	low	good

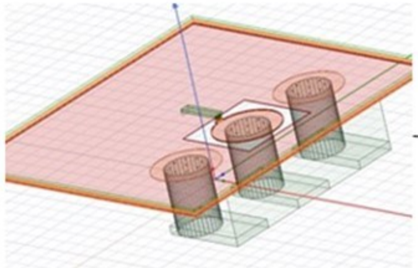


Deal, IEEE Trans THz, Sept 2011



G. Rebeiz

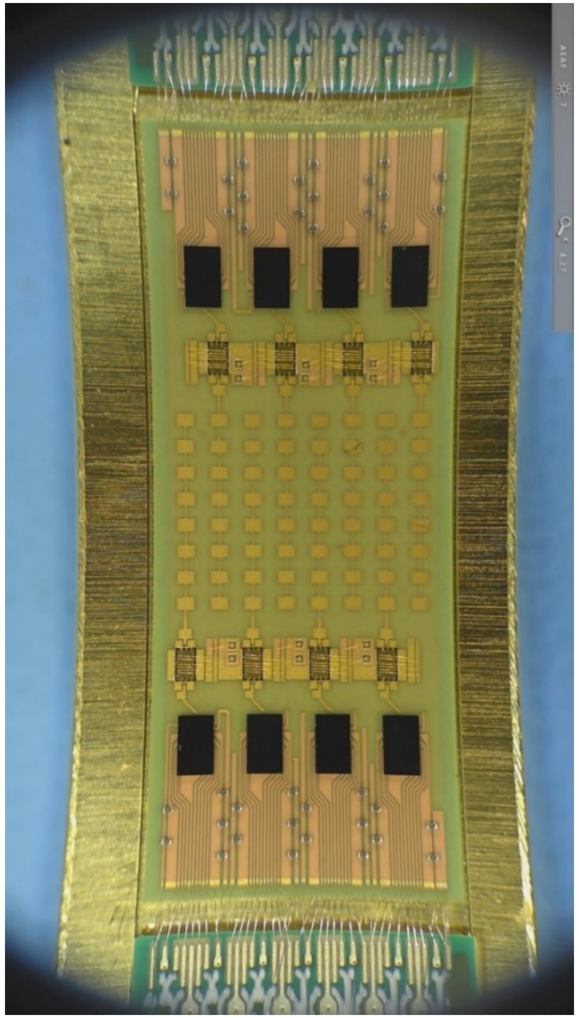




135GHz 8-channel MIMO hub array tile modules

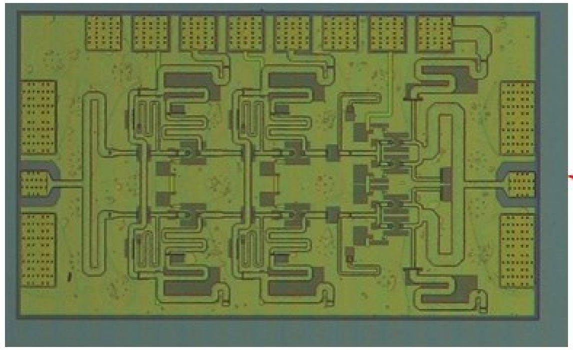
EUROPEAN MICROWAVE WEEK
EuMW 2021
United in Microwaves
EXCEL, LONDON
13-18 FEBRUARY 2022
www.eumw2021.com

Receiver: A. Farid et. al, 2021 IEEE BCICTS; Transmitter in review

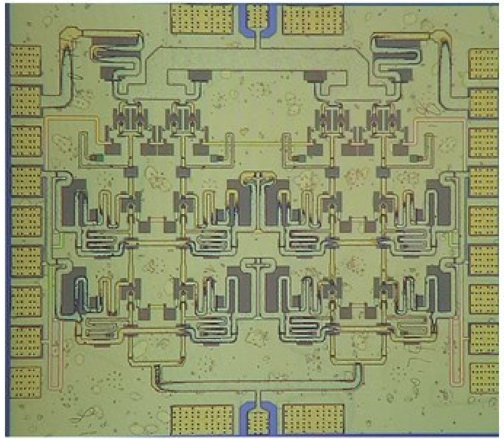


140GHz hub: ICs & Antennas

110mW InP Power Amplifier
20.8% PAE

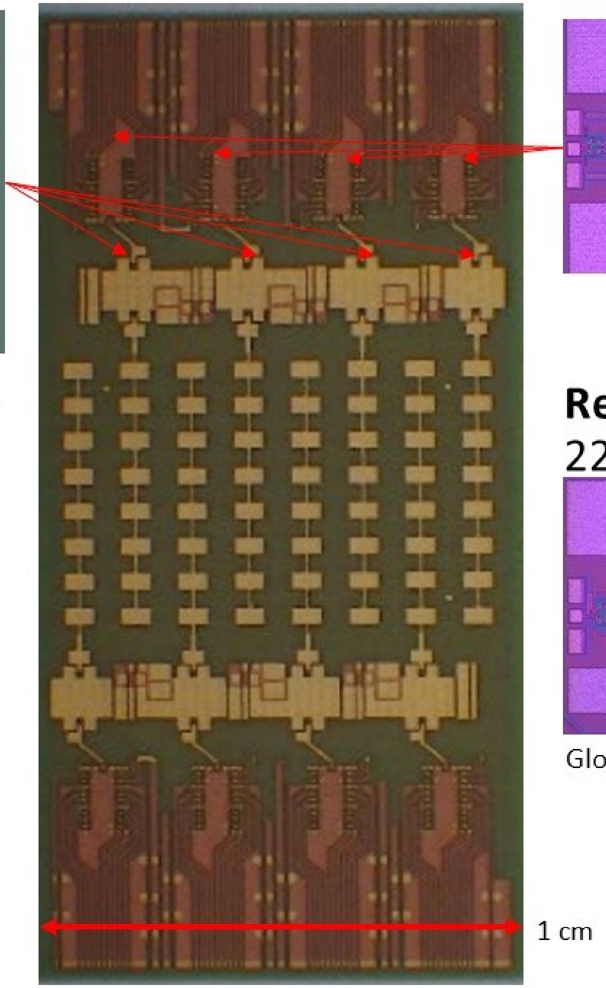


190mW InP Power Amplifier
16.7% PAE



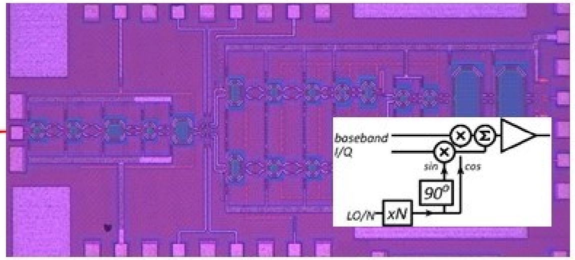
Teledyne InP HBT

LTCC Array module

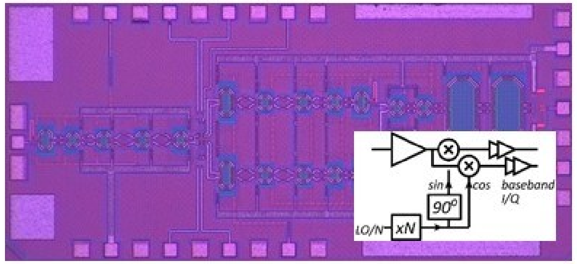


Kyocera

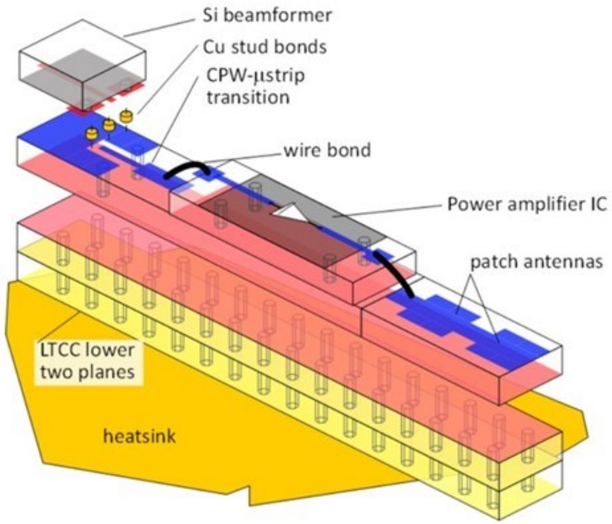
CMOS Transmitter IC
22nm SOI CMOS.



Receiver IC
22nm SOI CMOS.



GlobalFoundries 22nm SOI CMOS



135 GHz Cu stud CMOS / LTCC transition

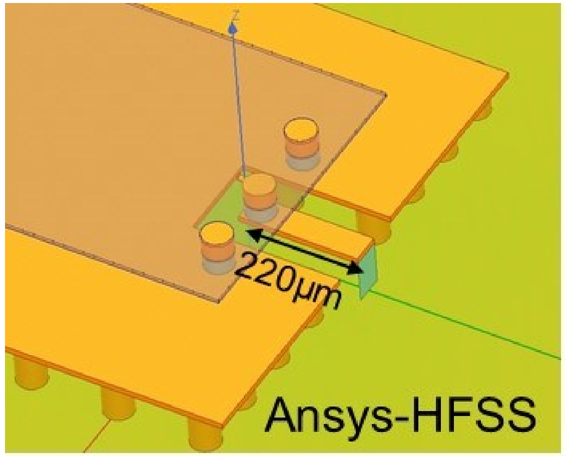
50 µm diameter Cu studs

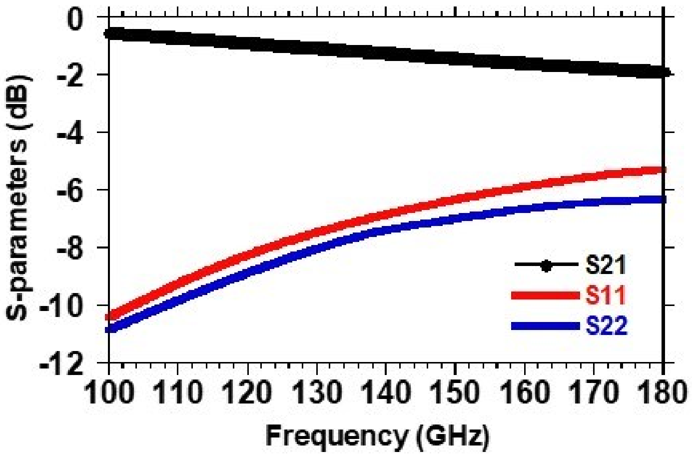
1.15 dB simulated loss

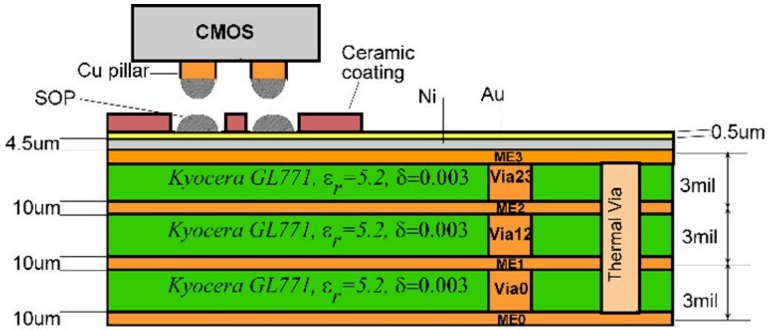
Includes Cu pillar, 220 µm CPW section

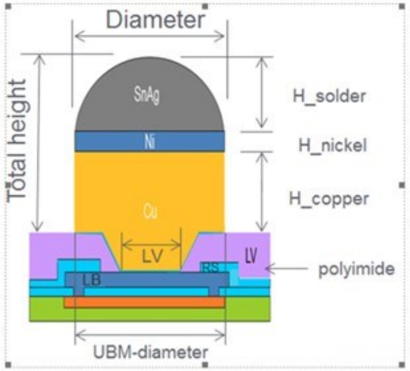
~0.85 dB measured loss.

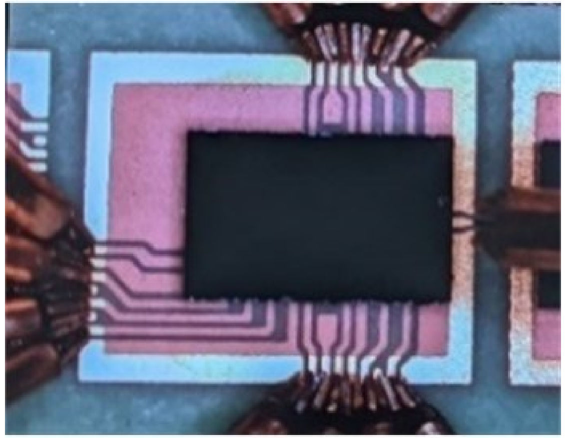
Low assembly yield with LTCC; too small

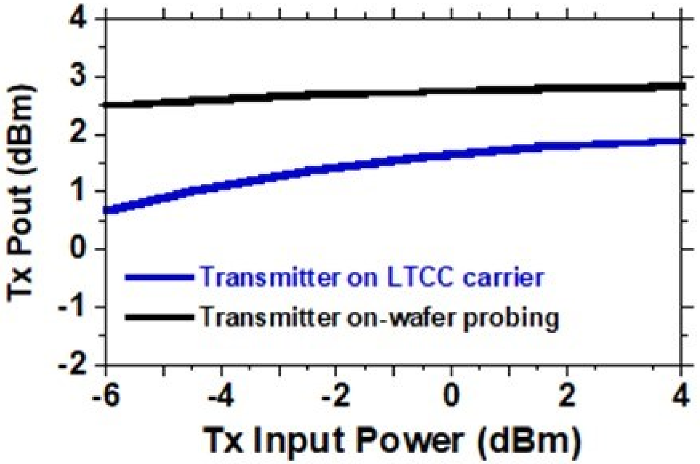




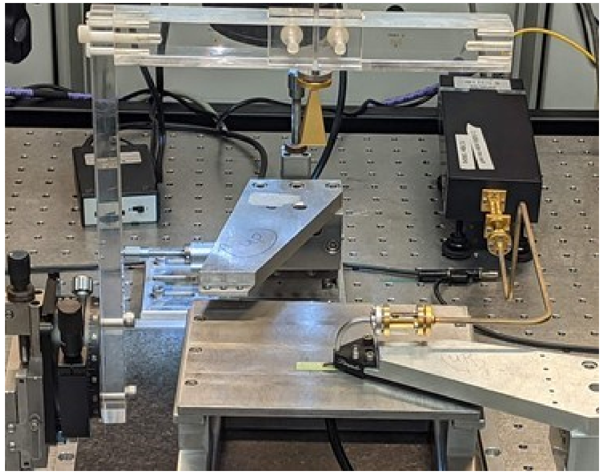


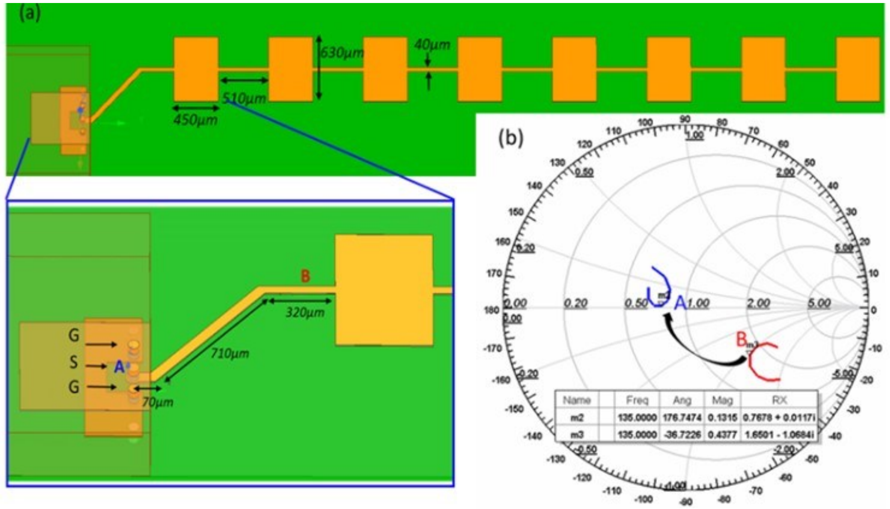


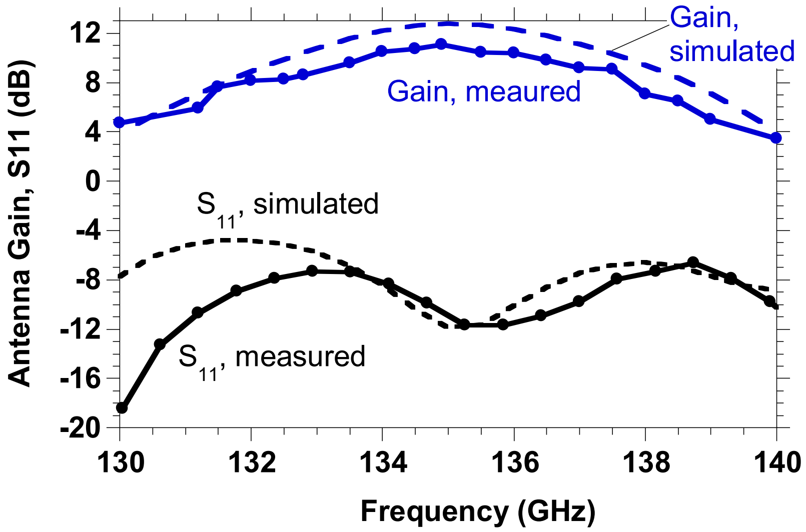


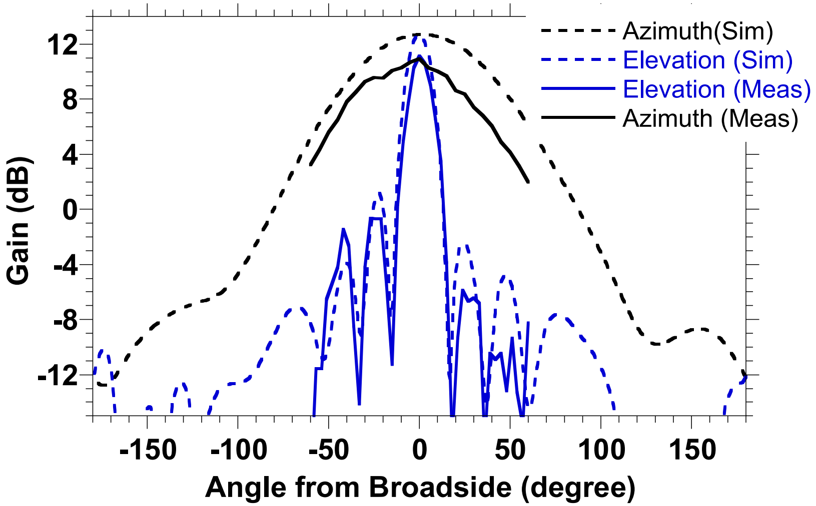


Series-fed patch antenna on LTCC









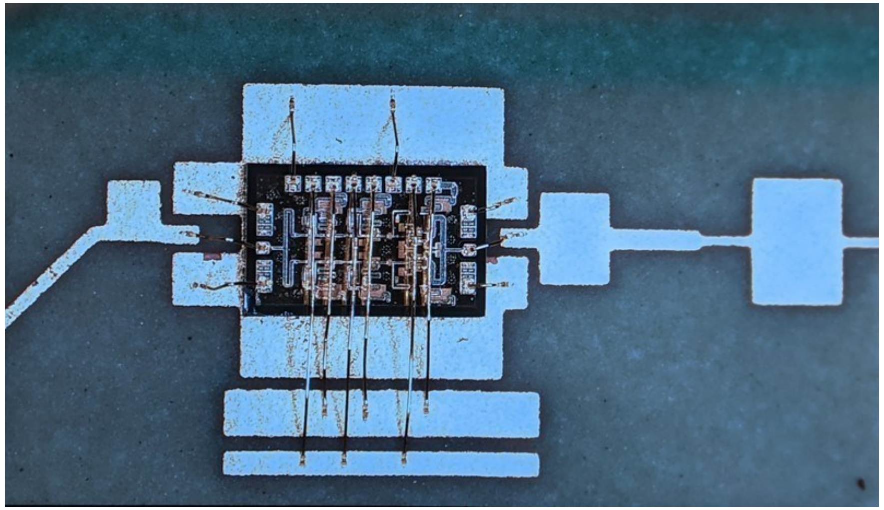
CMOS/InP PA transition design

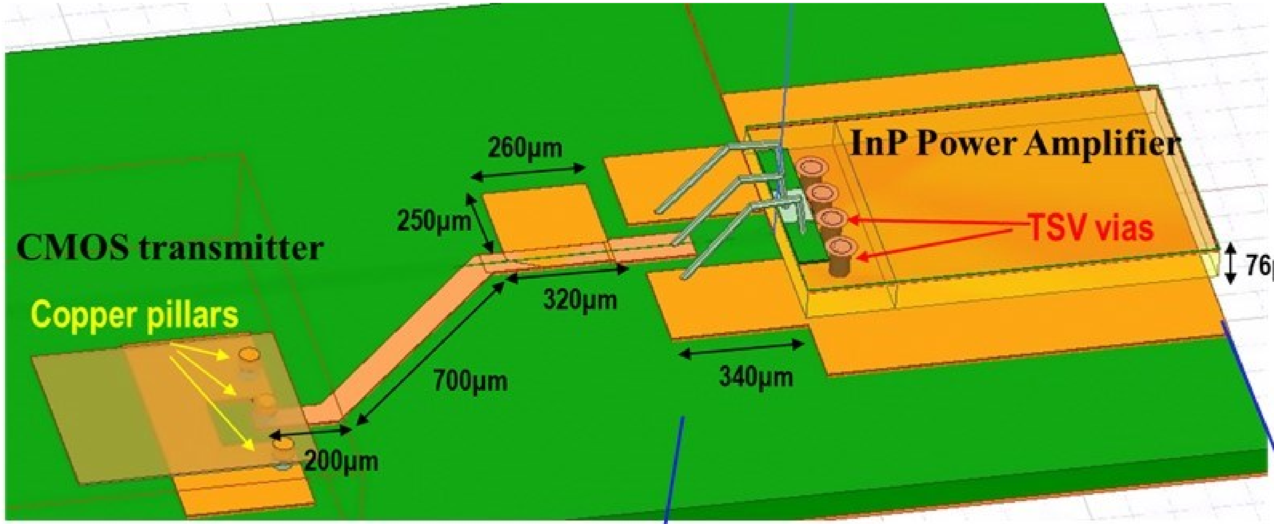
Au wirebonds: poor but easily obtained

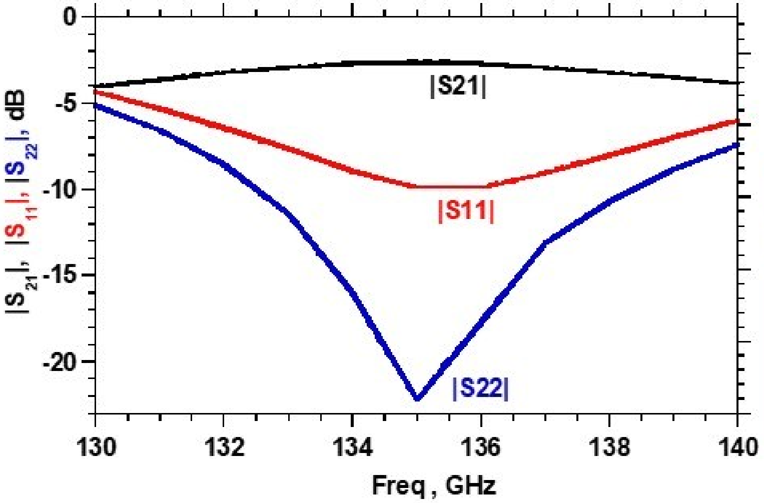
- 150 µm long, 25 µm diameter
- Ground return: through IC TSV's
- 2.6dB simulated insertion loss

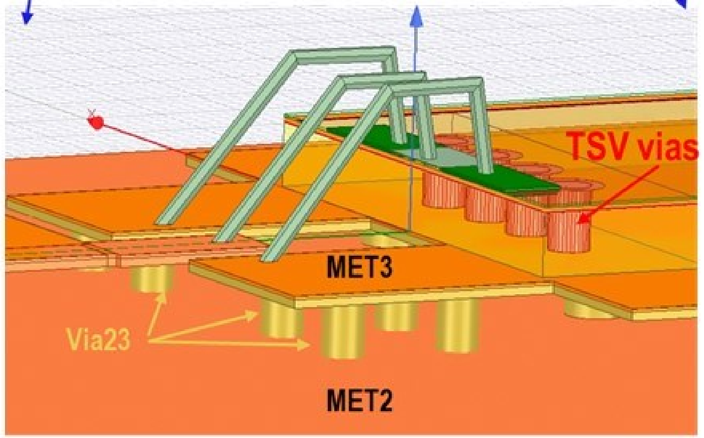
Ribbon bonds, flip-chip bonds: harder to get.

- both much better at 140 GHz
- InP flip-chip bonds: ~$80k per MPW run
- investigating firms for ribbon-bonding







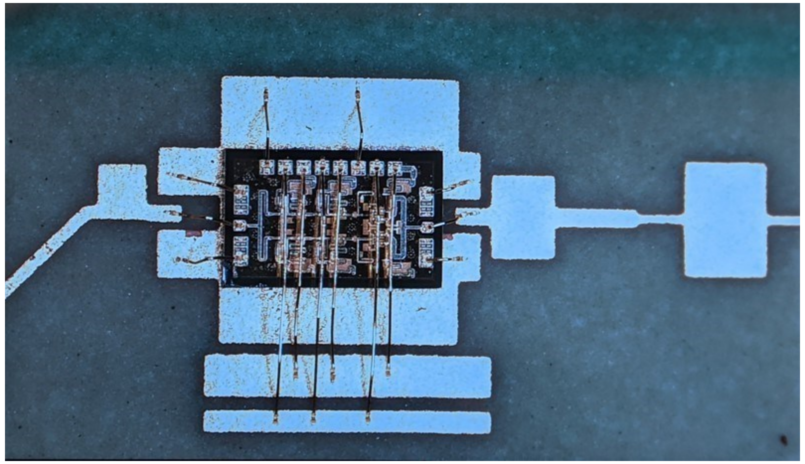


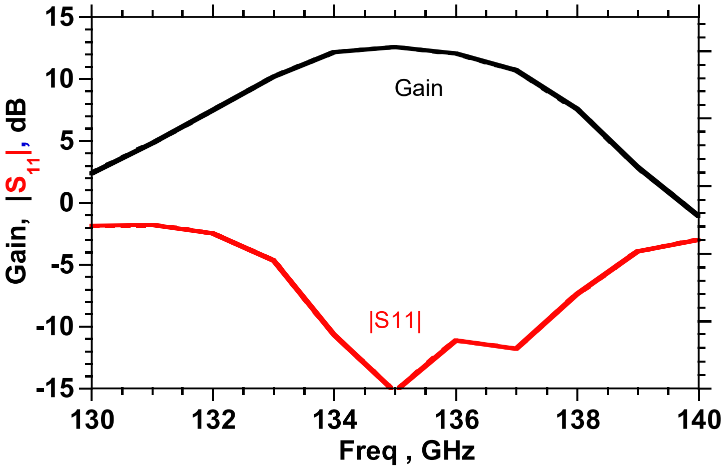
InP PA/antenna transition design

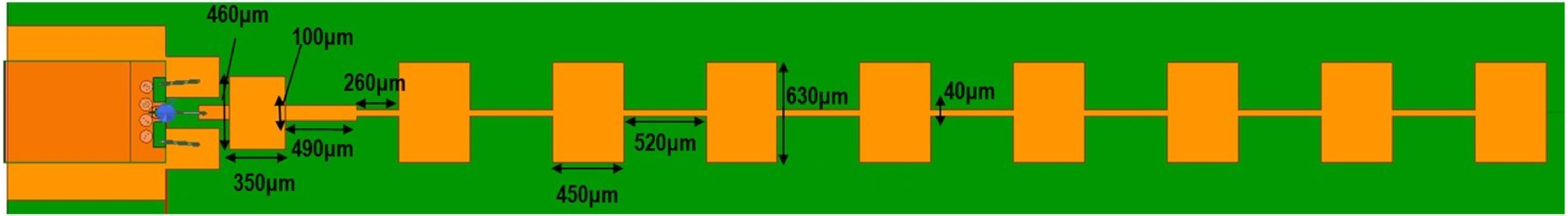
8-element series-fed patch antenna

Antenna-PA match:
stepped-impedance line

Simulations:
12dB antenna gain,
6GHz 3-dB bandwidth







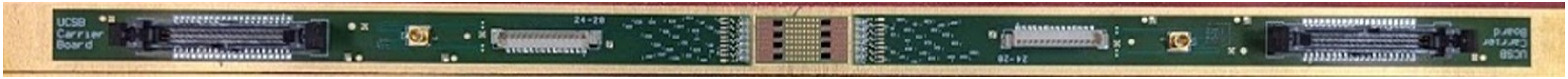
8-element 135 GHz MIMO receiver array

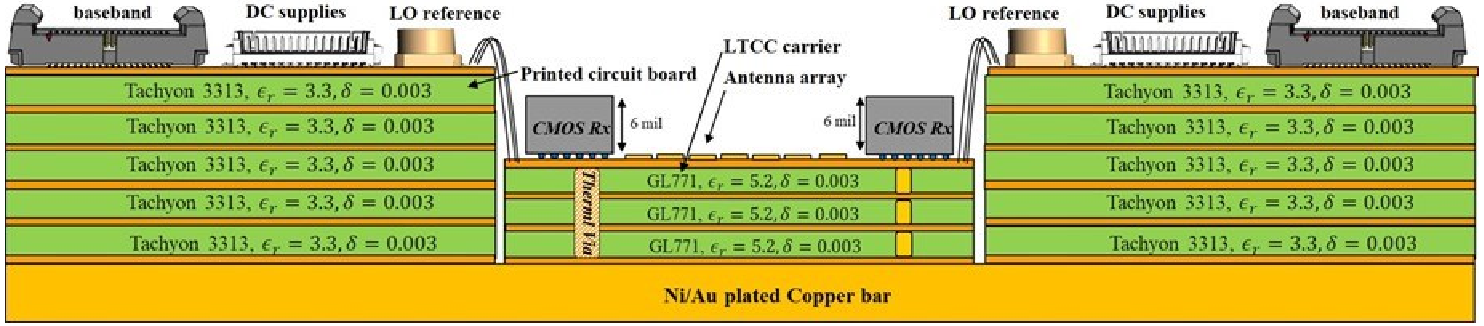
4 channels/side

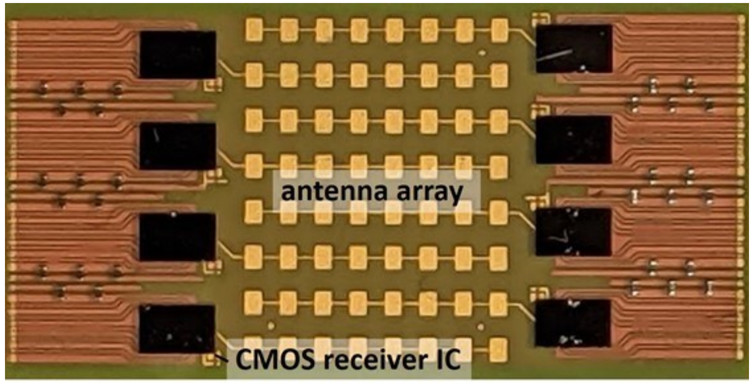
8-elements series fed-patch antenna/channel

0.65 λ antenna spacing

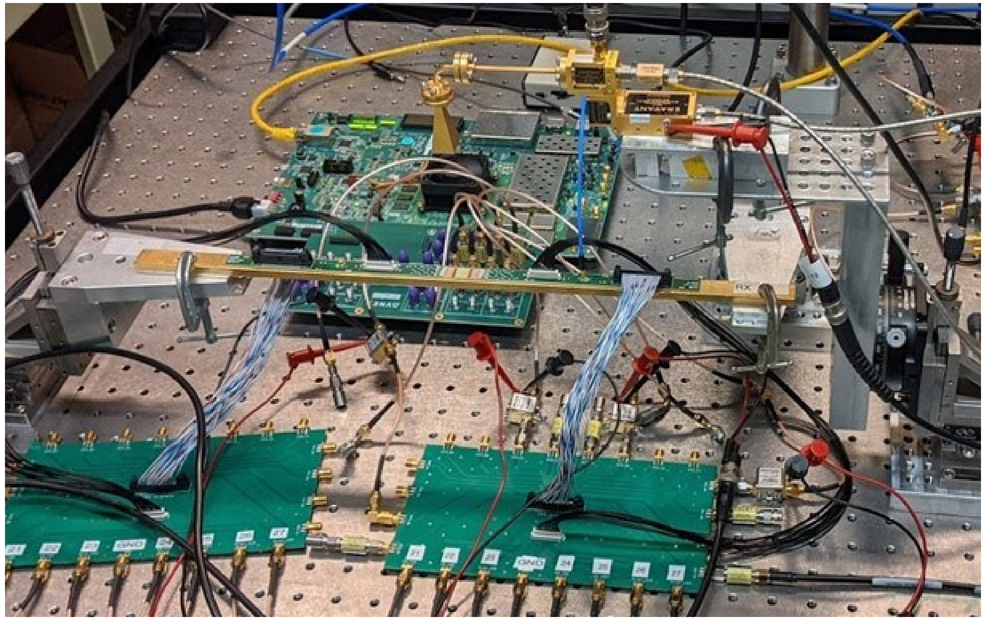
PCB provides I/Q , LO reference, DC connections

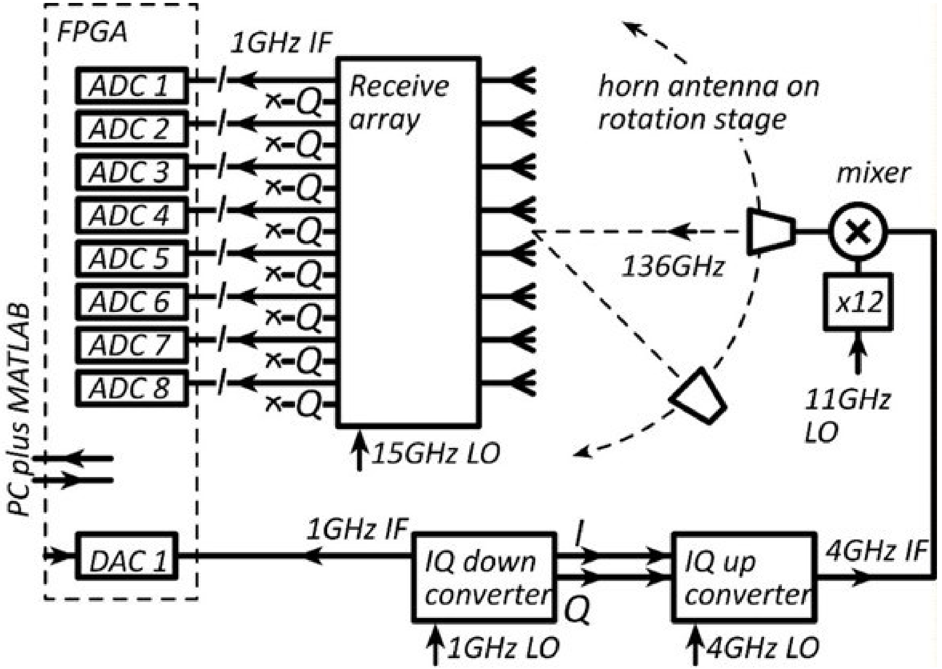






Receive module testing





Rx module connected to ZCU-111 for array calibration and beamforming.

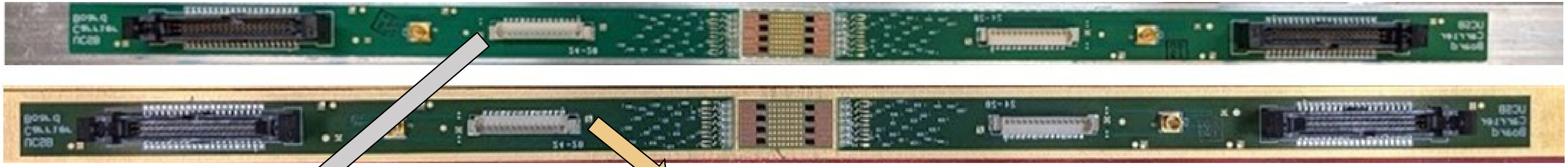
Test transmitter mounted at 15cm distance on a rotating arm.

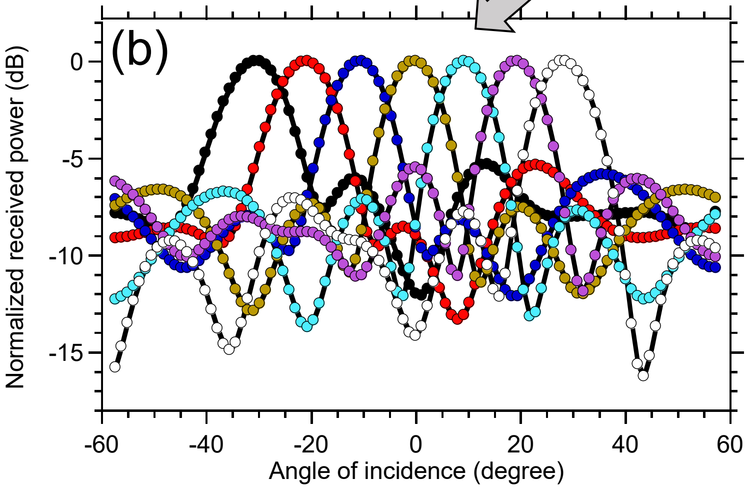
Wideband 1-GHz OFDM signal used for array calibration

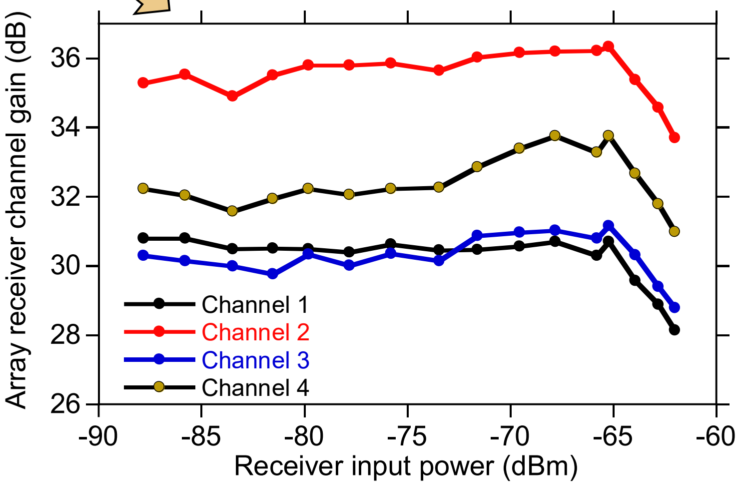
https://github.com/pi-radio/Pi-Radio-v1-NRT

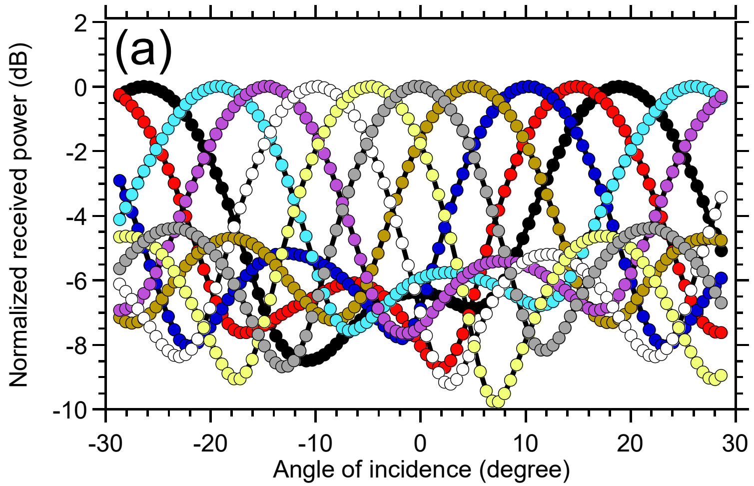
https://dl.acm.org/doi/abs/10.1145/3411276.3412195

Conversion gain, radiation pattern









8 working channels: good patterns

Poor ground: limits data rate

4 working channels: patterns with sidelobes

good ground: data transmission experiments

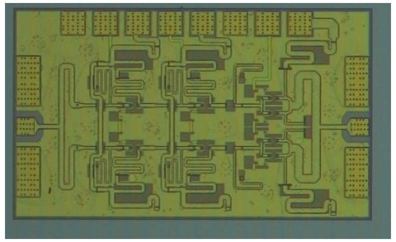
135GHz 8-channel MIMO hub array tile modules

140GHz MIMO hub receiver array modules,
4-element, 8-element
MIMO beamforming
Data transmission up to 1.9Gb/s

140GHz MIMO hub transmitter array modules,
8-element
38.5dBm EIRP
Data transmission up to 1.9Gb/s
Performance limited by assembly yield.
Data rate limited by connector.

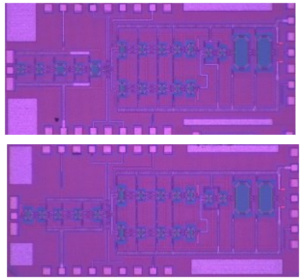
Link demonstration to be reported

110mW InP PA
20.8% PAE

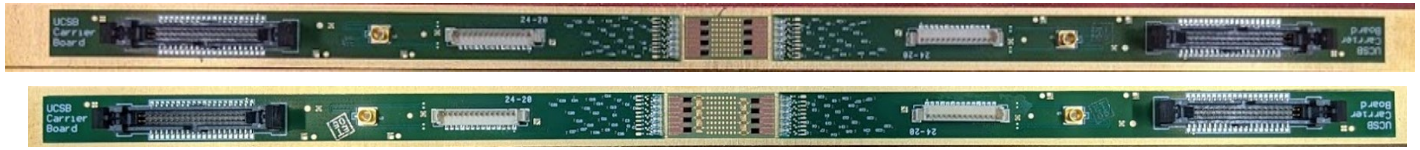


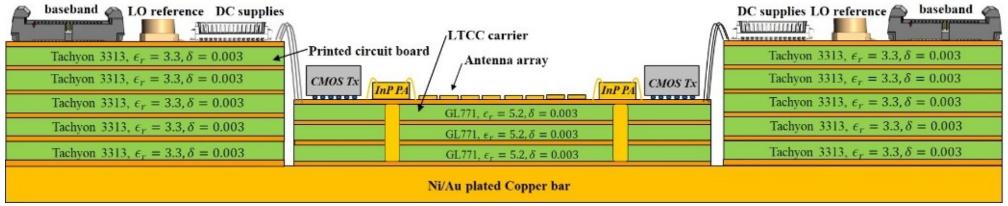
Teledyne 250nm InP HBT

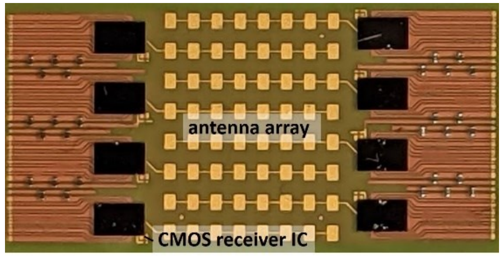
CMOS TX, RX ICs
GlobalFoundries
22nm SOI CMOS.

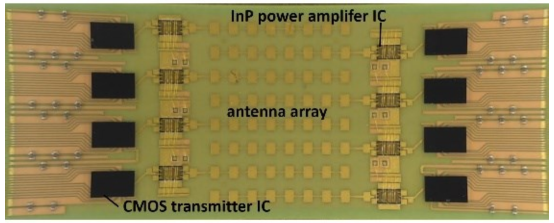


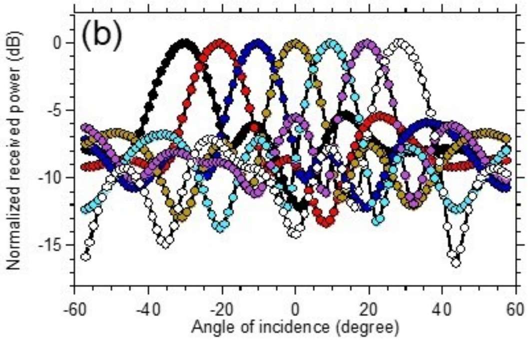
Receiver: A. Farid, 2021 BCICTS; Transmitter: in review

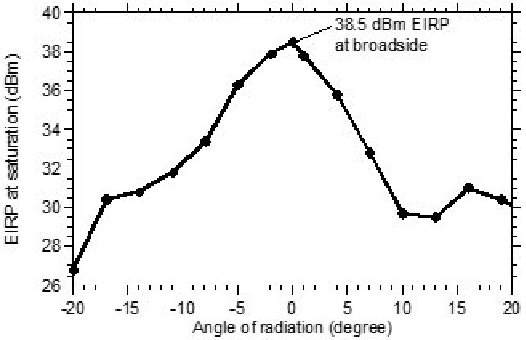


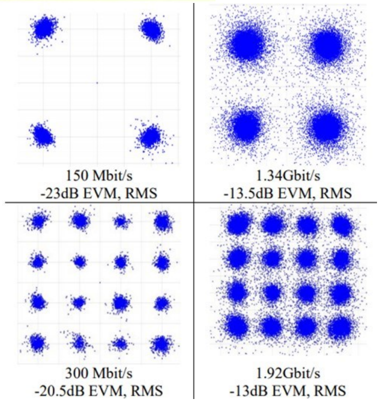












Gen-II 140GHz MIMO hub modules

Gen I 140 GHz CMOS+InP modules

low assembly yield: 50 μm Cu stud too small for LTCC

used in Samsung link demo; to be announced.

Gen II 140 GHz CMOS+InP modules

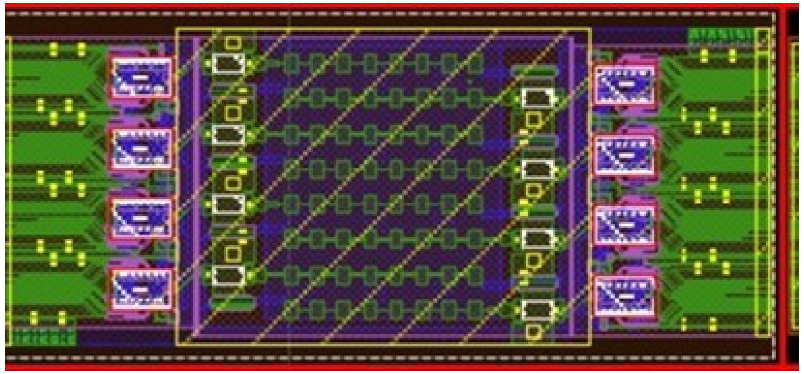
change to C4 solder bonds: more easily assembled on LTCC

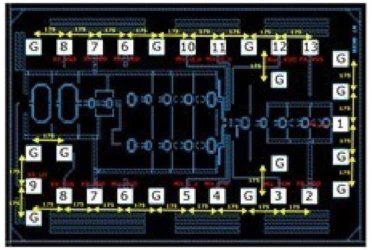
ICs re-fabricated with C4 bonds

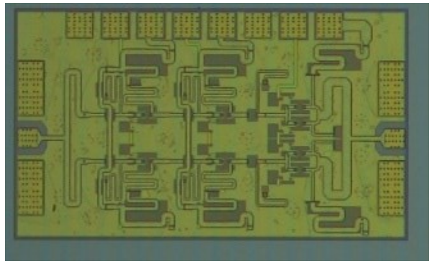
LTCC carriers re-designed for C4 bonds

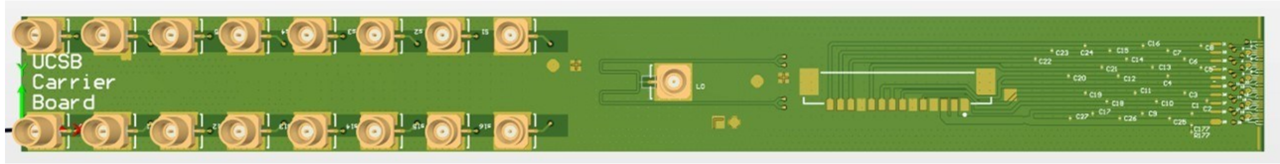
PCB has higher-bandwidth baseband IQ connectors: 10Gb/s.

Assembly planned in Winter 2022.





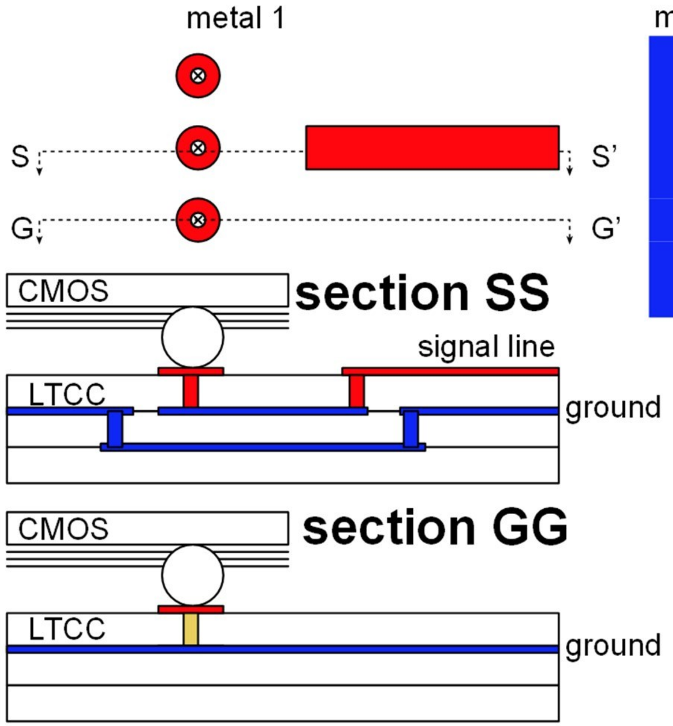


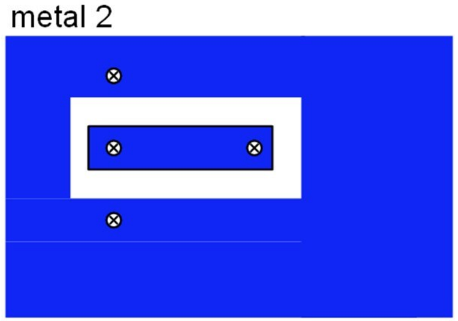


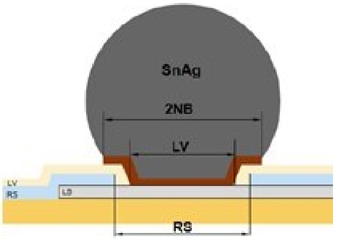
140 GHz C4-LTCC Transition Design

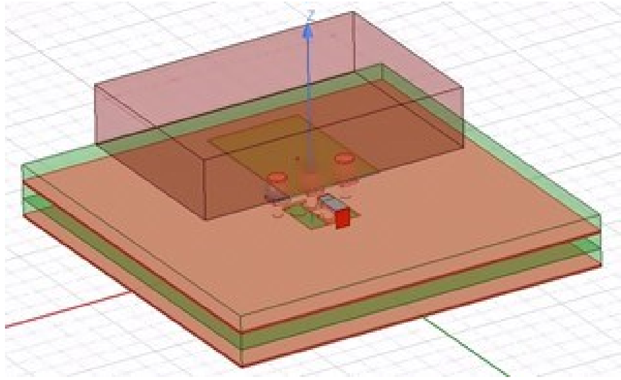
Simulated 1.3 dB insertion loss at 140 GHz.

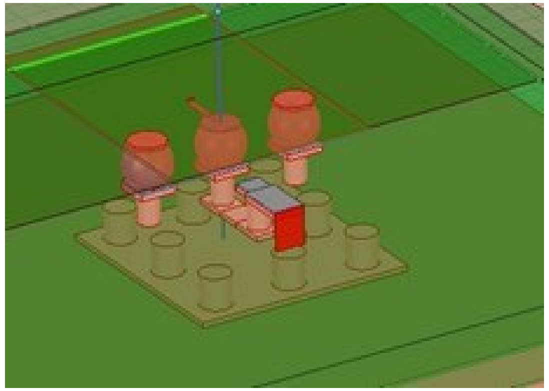
C4 has better assembly yield with LTCC than 50 μm Cu studs

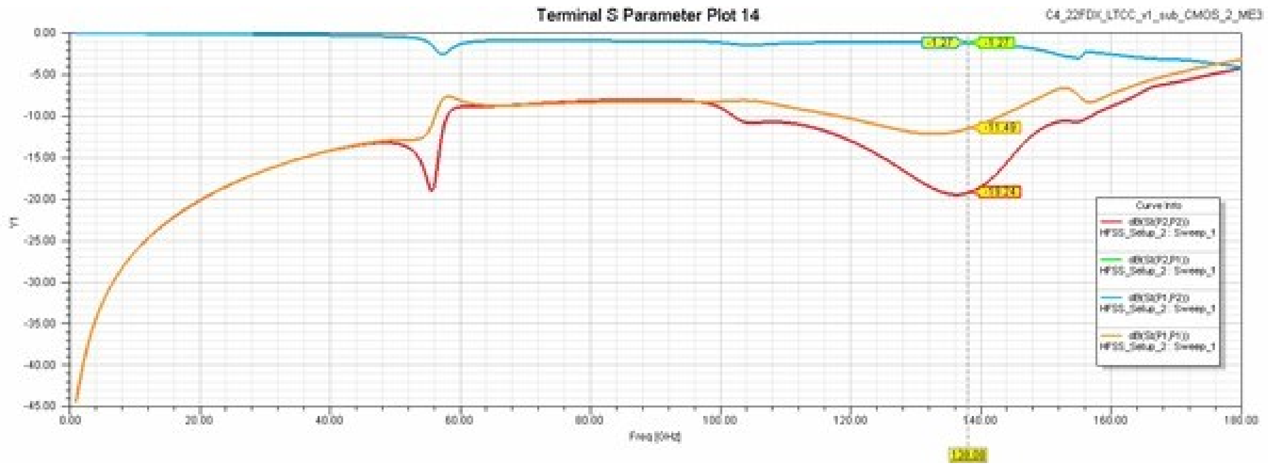






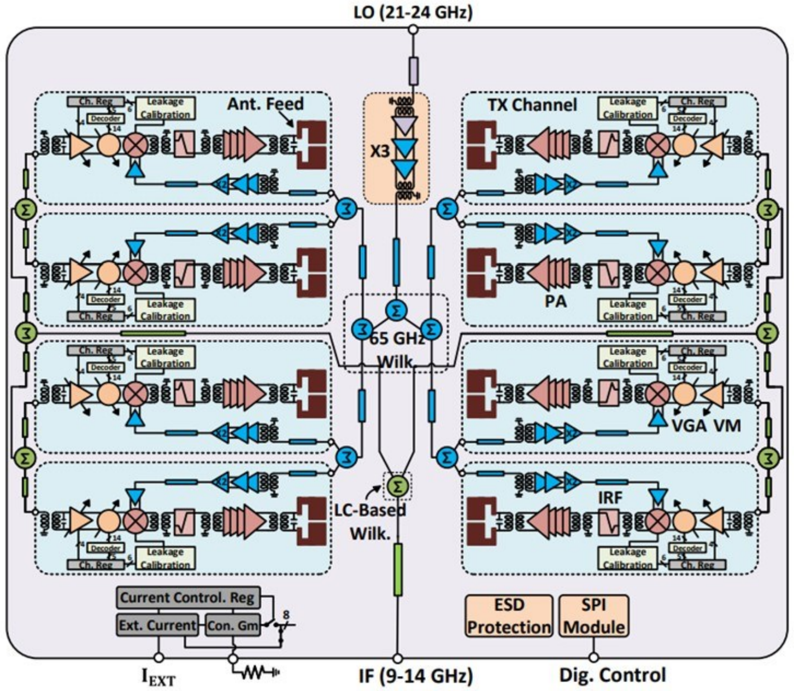


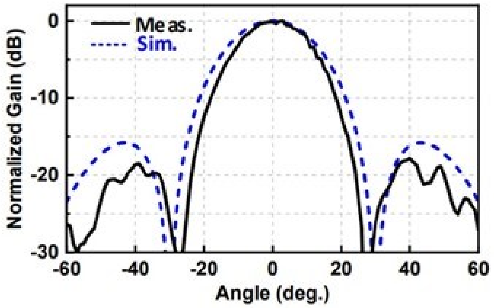


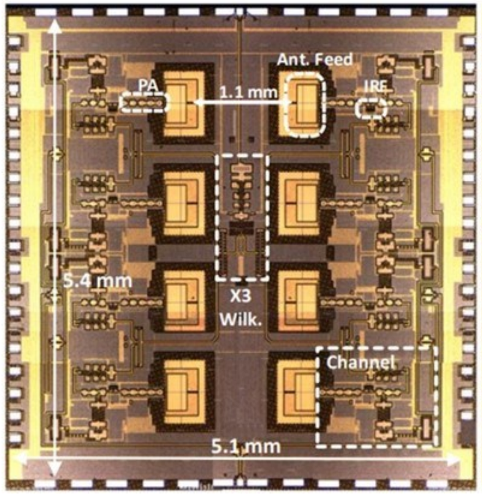


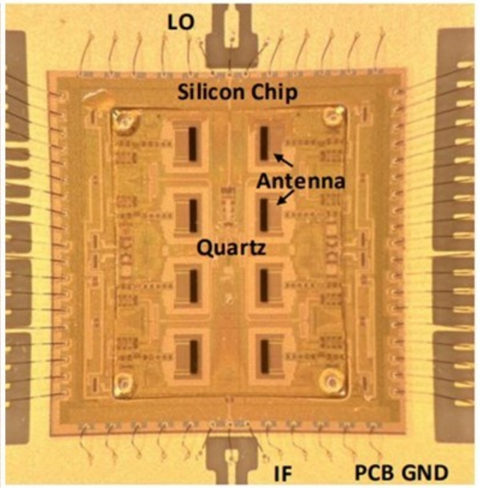
140 GHz IF Beamforming Phased-Array Transmitter

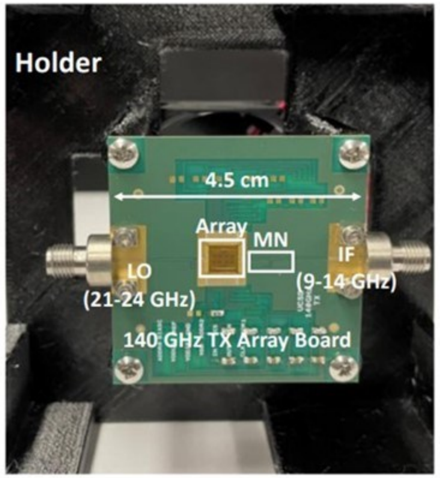
Siwei Li, 2021 IEEE IMS: Rebeiz Group, UCSD

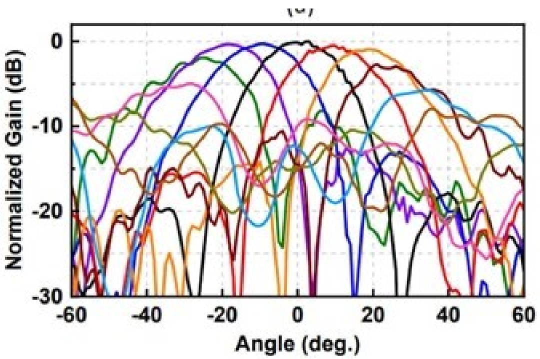




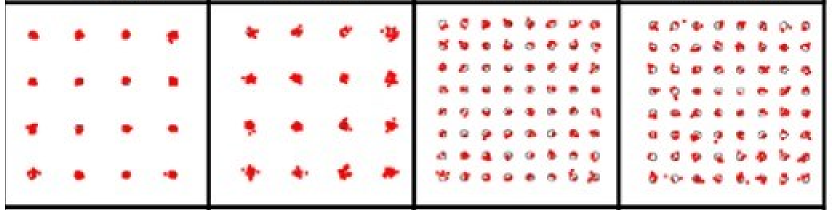








Pout: 3.5dBm /6dB BO		Pout: 1.5dBm /8dB BO	
4 Gb/s	16 Gb/s	6 Gb/s	21 Gb/s



4.1%	5.6%	3.9%	5.1%

Beamspace digital beamformer IC

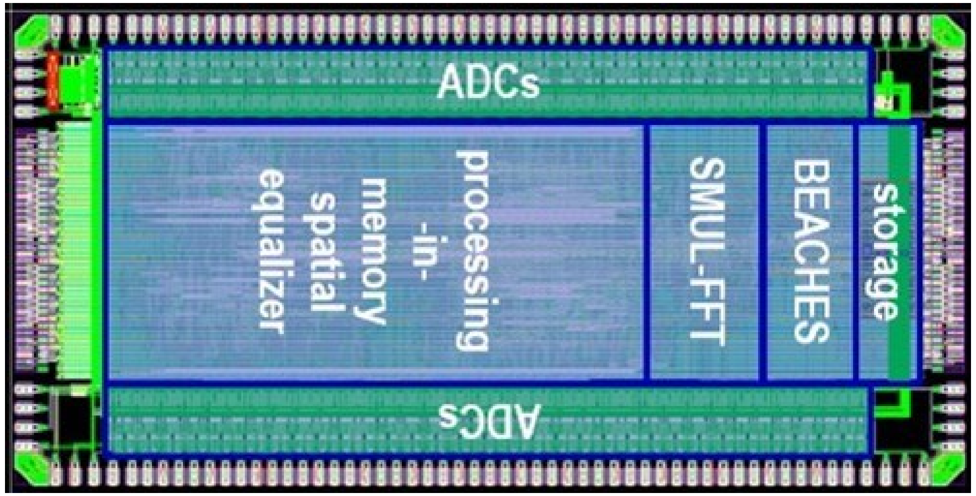
All-digital receive beamformer ASIC in 65nm CMOS

Beamspace algorithm

Supports 32 antennas and 1 to 16 users

20GB/s throughput given
16 simultaneously transmitting users
under conditions requiring 3-bit ADC resolution

Record 9.98GB/s throughput given
16 simultaneously transmitting users
under conditions requiring 6-bit ADC resolution

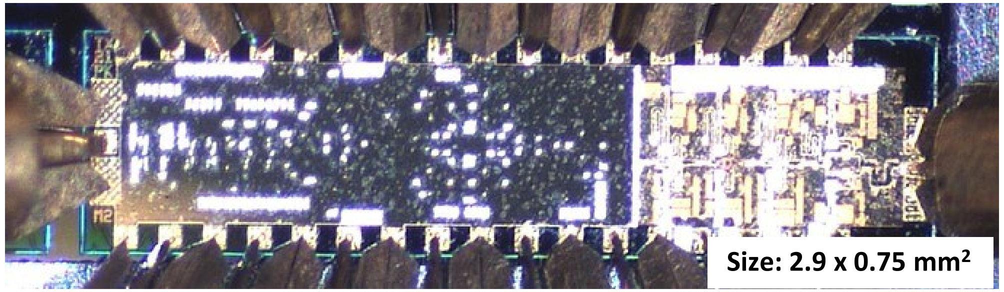


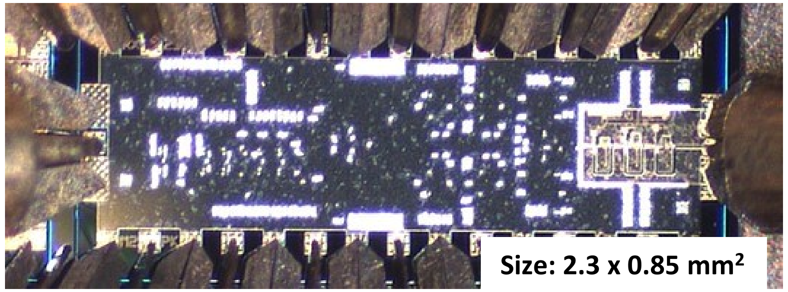
Castaneda Fernandez 2021 ESSCIRC.
Studer Group, Cornell/ETHZ
Molnar Group, Cornell

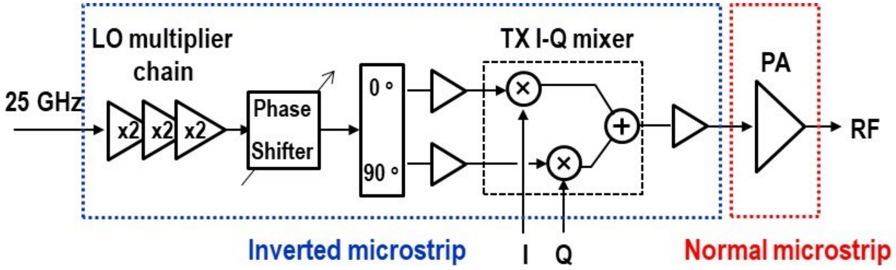
ICs and Modules: 210 GHz & 280 GHz

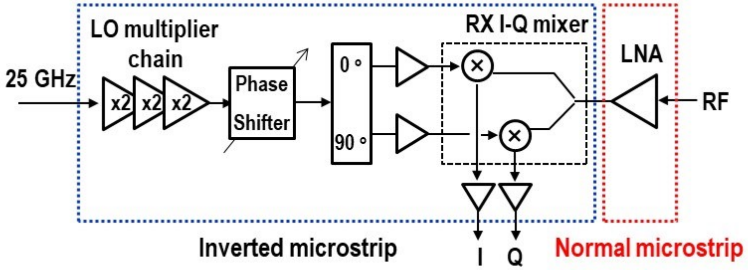
210 GHz Transmitter and Receiver ICs

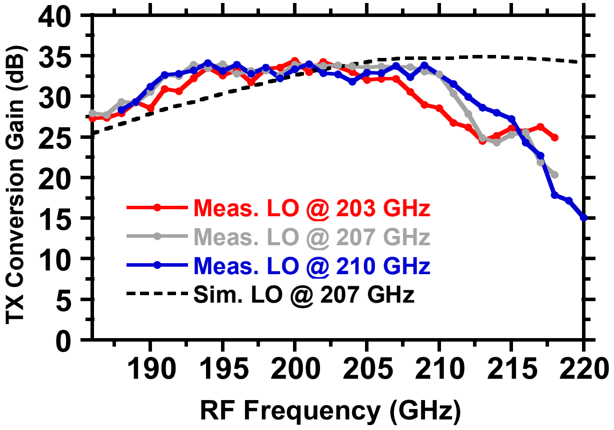
M. Seo et al, 2021 IMS; Teledyne 250nm InP HBT

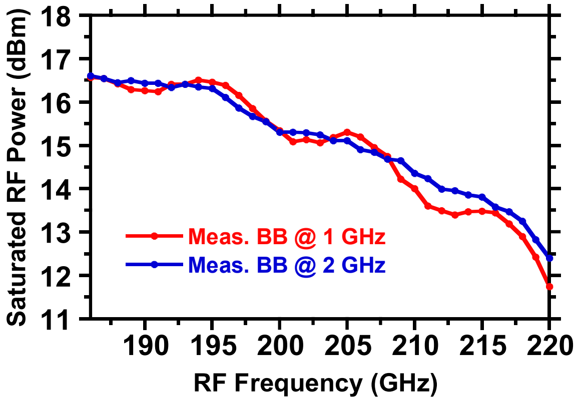


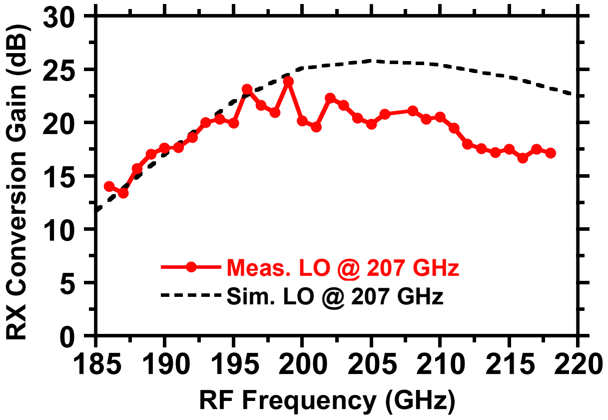


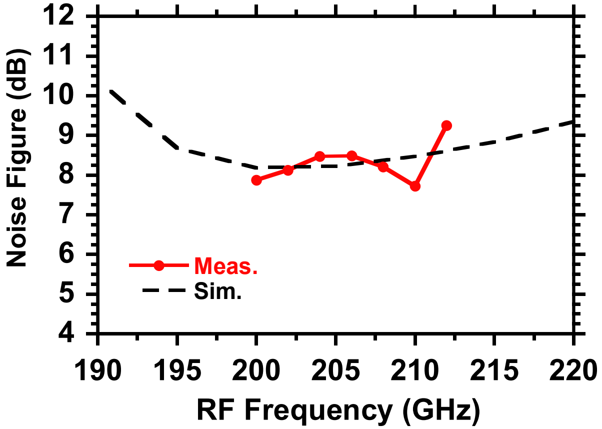










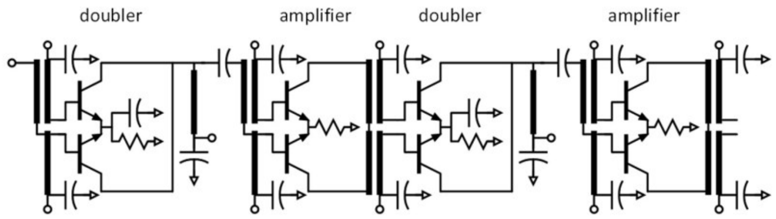


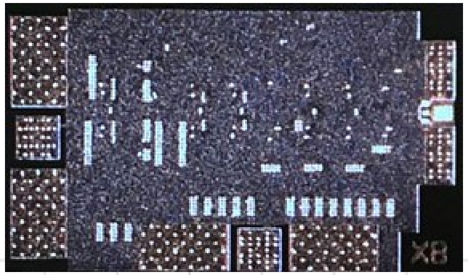
LO multiplier: 25 GHz to 200 GHz

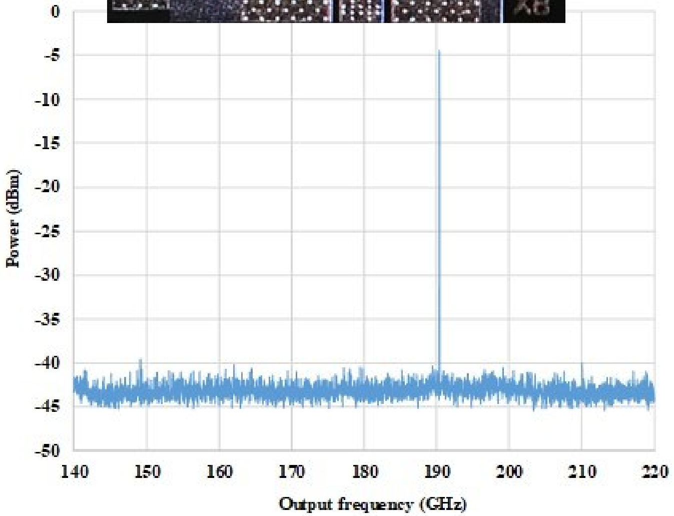
M. Seo et al, 2021 IMS; Teledyne 250nm InP HBT

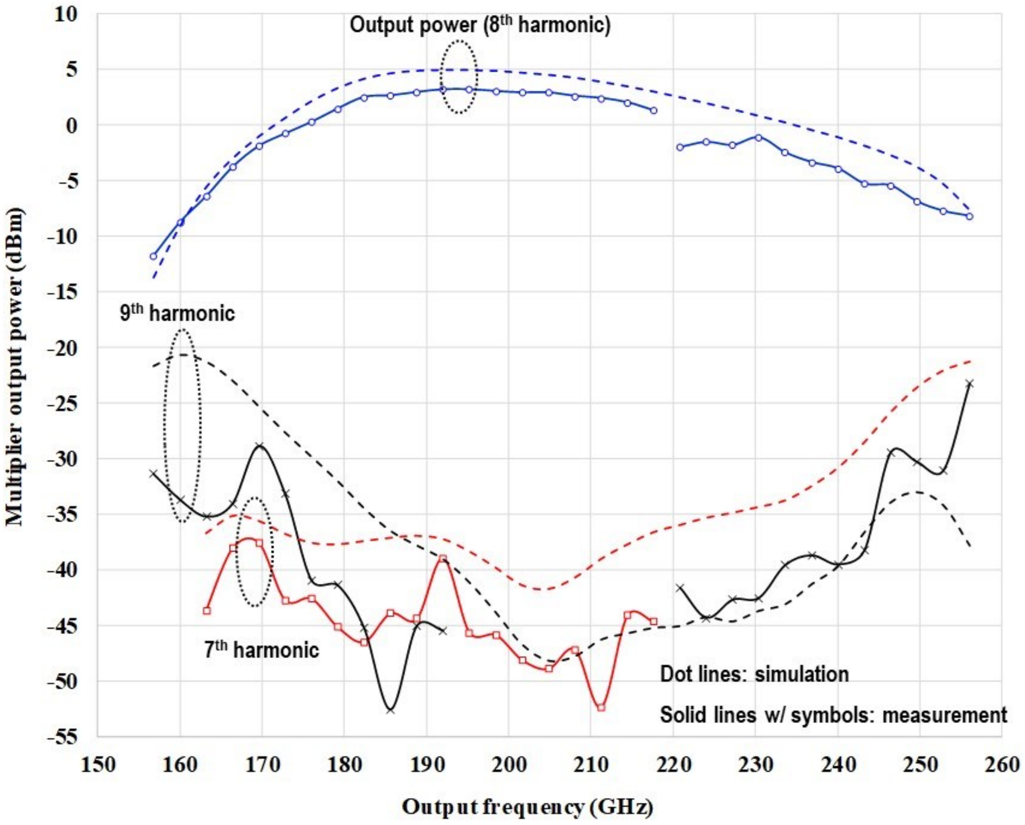
multiplier design by M. Seo

P_{out} > -5 dBm over 165 - 240 GHz
Spurious < -40 dBc over 180-230 GHz
P_{DC} = 282 mW
0.58 mm x 0.4 mm





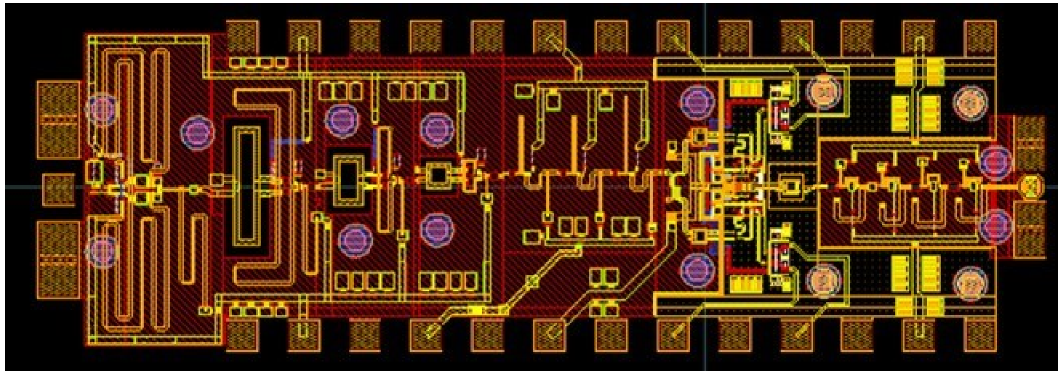




280GHz transmitter, receiver IC designs

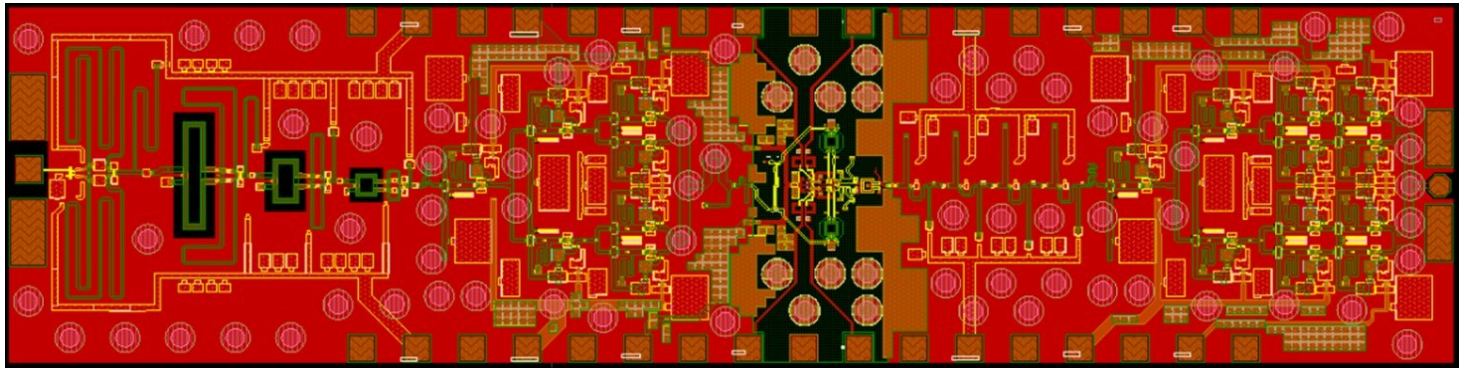
Solyu, Alz, Ahmed, Seo; UCSB/Sungkyunkwan
Teledyne 250nm InP HBT technology

Receiver



simulations: 11dB noise figure, 40GHz bandwidth

Transmitter

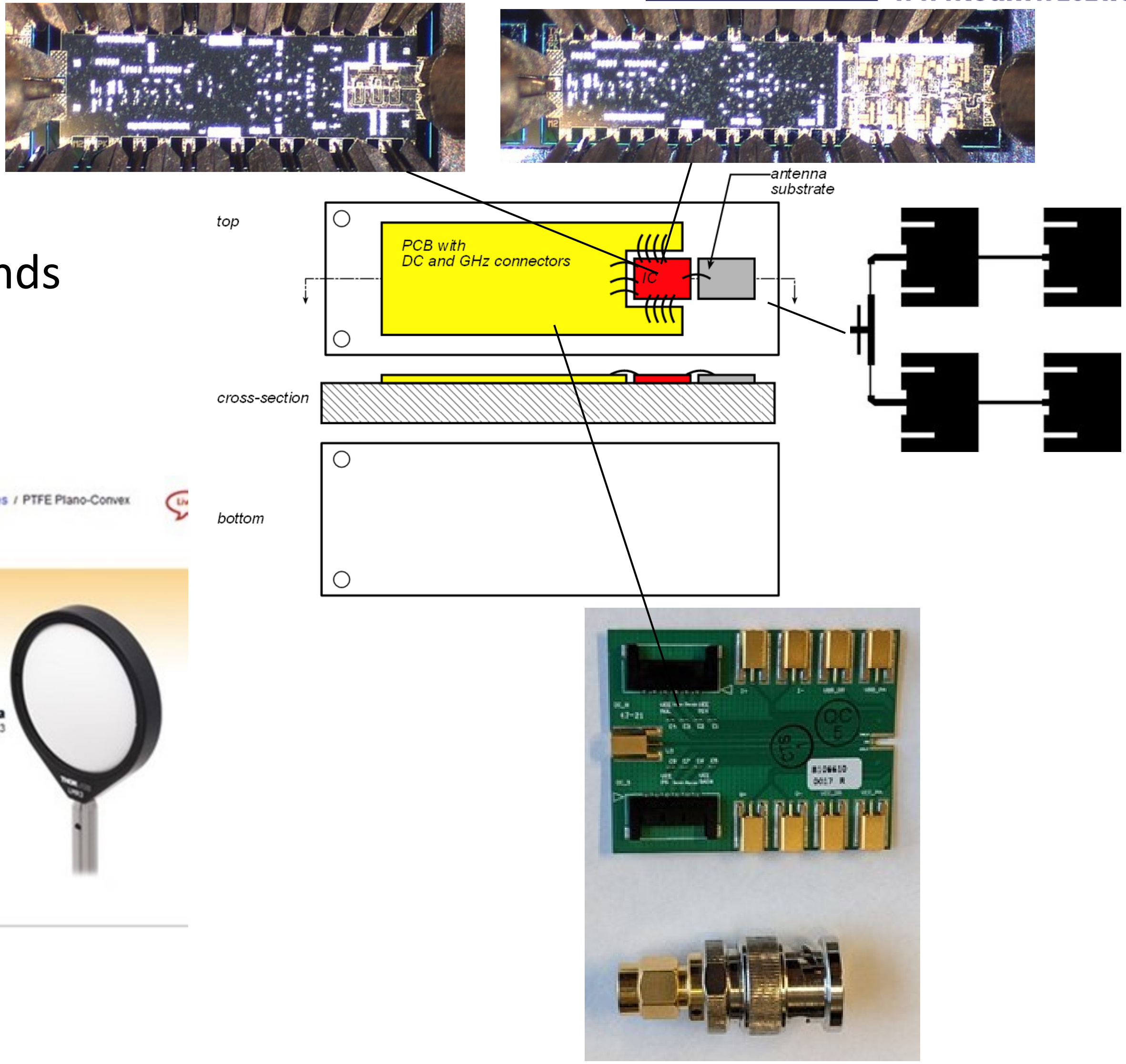


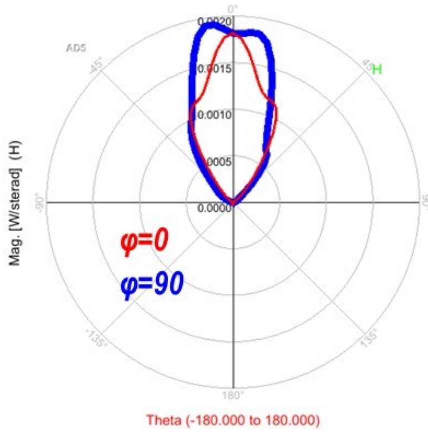
simulations: 17dB saturated output power.

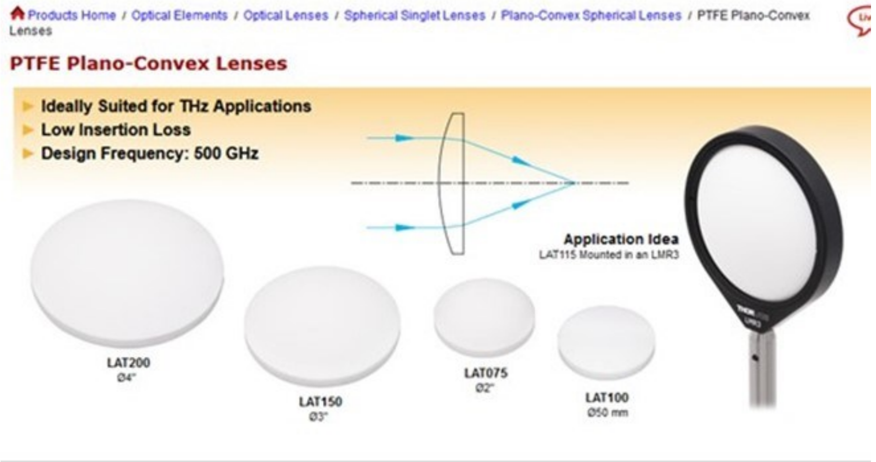
Application: point-point MIMO backhaul links

210, 280 GHz MIMO backhaul modules

Single-channel modules (simplicity)
210 GHz InP TX, RX ICs
2x2 patch antenna feed on fused silica substrate
Primary antenna: 200 mm Teflon lens
Assembly: 200 GHz ribbon bonds, low-frequency ball-bonds
280 GHz modules will be similar







100-300GHz Wireless

100-300GHz Wireless

Massive capacities
large available bandwidths
massive spatial multiplexing in base stations and point-point links

Very short range: few 100 meters
short wavelength, high atmospheric losses. Easily-blocked beams.

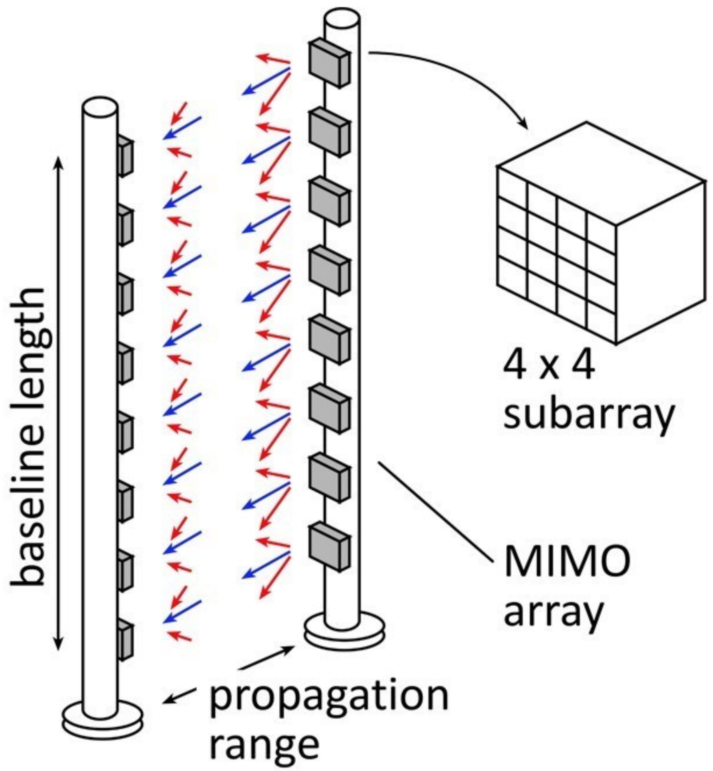
IC Technology
All-CMOS for short ranges below 200 GHz.
SiGe or III-V LNAs and PAs for longer-range links. Just like cell phones today
SiGe or III-V frequency extenders for **20**0GHz and beyond

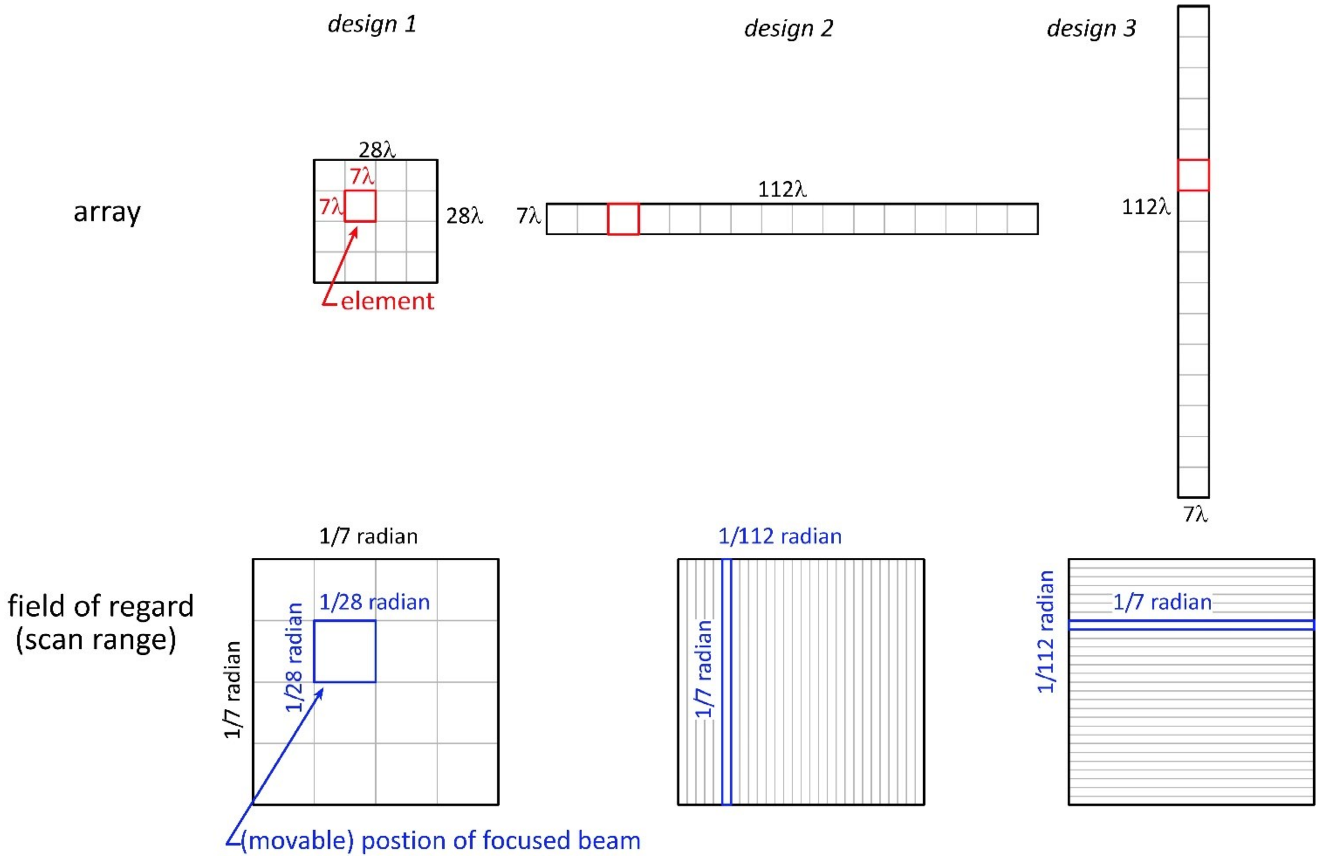
The challenges
digital beamformer computational complexity
packaging: fitting signal channels in very small areas
mesh networking to accommodate beam blockage
driving the technologies to low cost

Backup slides

1D or 2D subarray for backhaul ?

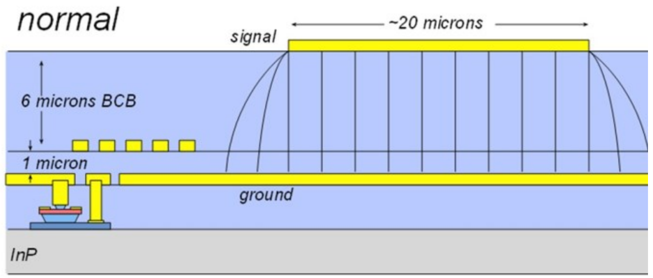
Should we use 4x4 array, 1x16, or 16x1 array ?
All provide same system link budget, same # RF channels, same angular scanning range.

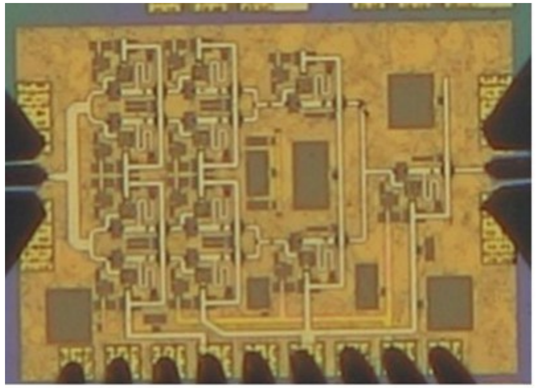




Normal & inverted microstrip

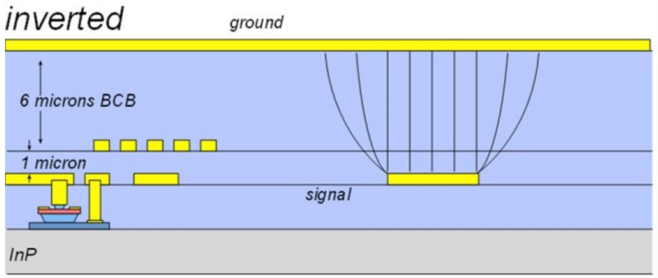
Normal: PAs, LNAs
smaller skin-effect losses ✓
ground-plane holes at transistors ✗

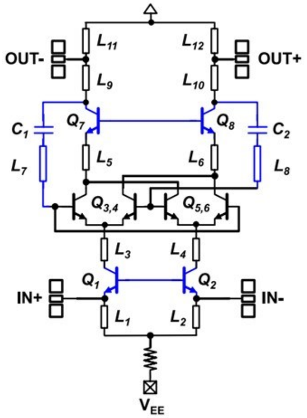


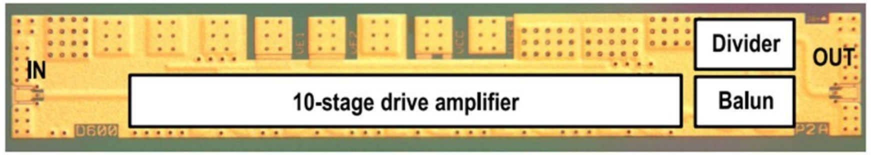


266GHz, 16.8dBm PA: A. Ahmed et. al, 2021 IMS

Inverted: high-density blocks (mixers, phase shifters,…)
higher skin-effect losses ✗
no ground-plane breaks: better ground integrity ✓



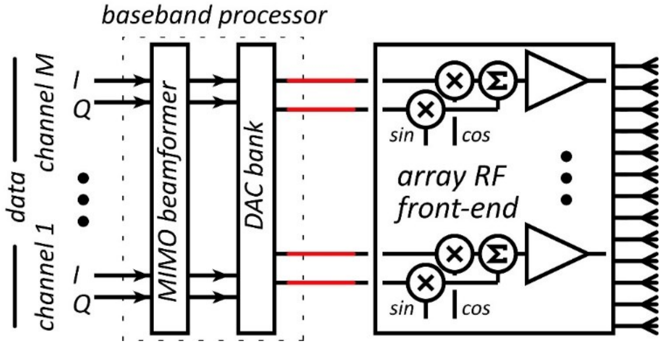




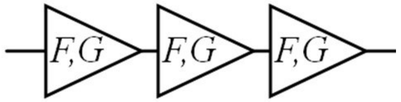
529GHz dynamic divider: M. Seo et al, IEICE Electronics Express, Feb. 2015

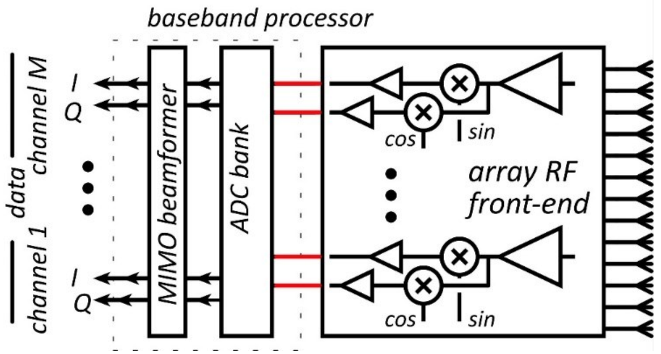
100-300GHz wireless: transistor requirements

Transmitters need:
high power-added efficiency $PAE = (P_{out} - P_{in})/P_{DC}$
high added power density $(P_{out}$-$P_{in})$/(gate width, emitter length)

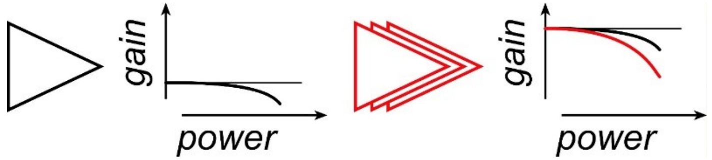


Receivers need:
low cascaded noise $F_{casc} = F + (F-1)/G + (F-1)/G^2 + \cdots$





Need reasonable gain/stage.
die area, power,
accumulated gain compression



(gain in PAs, LNAs is less than MAG/MSG, U, ...)

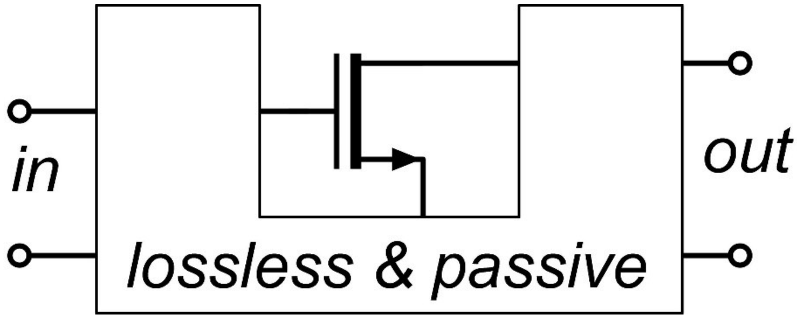
Where the IC designer can't help

mm-wave transistor gain is low: gain-boosting is common
Common-source vs. common-gate.
Capacitive neutralization. Unconditionally stable positive feedback (Singhakowinta, Int. J. Electronics, 1966)

Such circuits don't improve the parameters that matter the most.

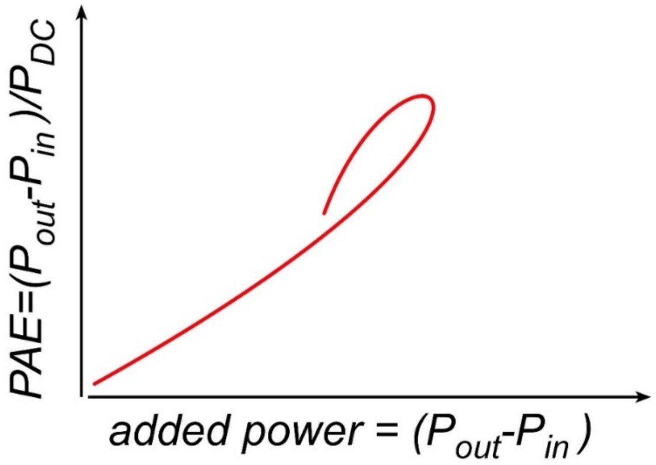
The circuit* doesn't change the transistor minimum cascaded noise figure. (Haus, Adler, Proc. IRE, 1958)

The circuit* doesn't change the transistor maximum efficiency vs. added power curve.



$$F_{casc} = 1 + M = F + (F-1)/G + (F-1)/G^2 + \cdots$$

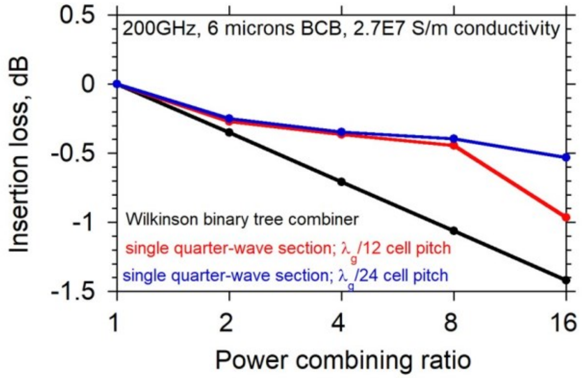
*If lossless, and given the correct source and load impedances.

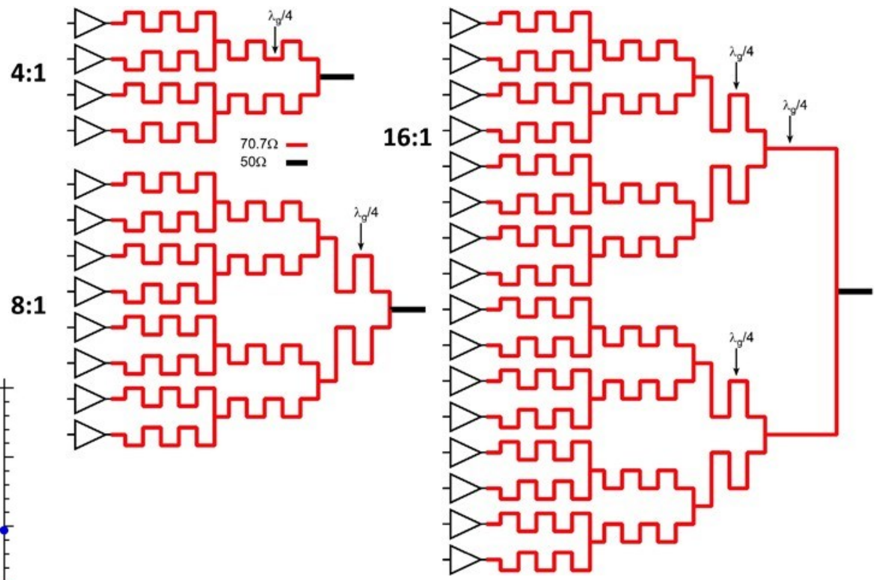


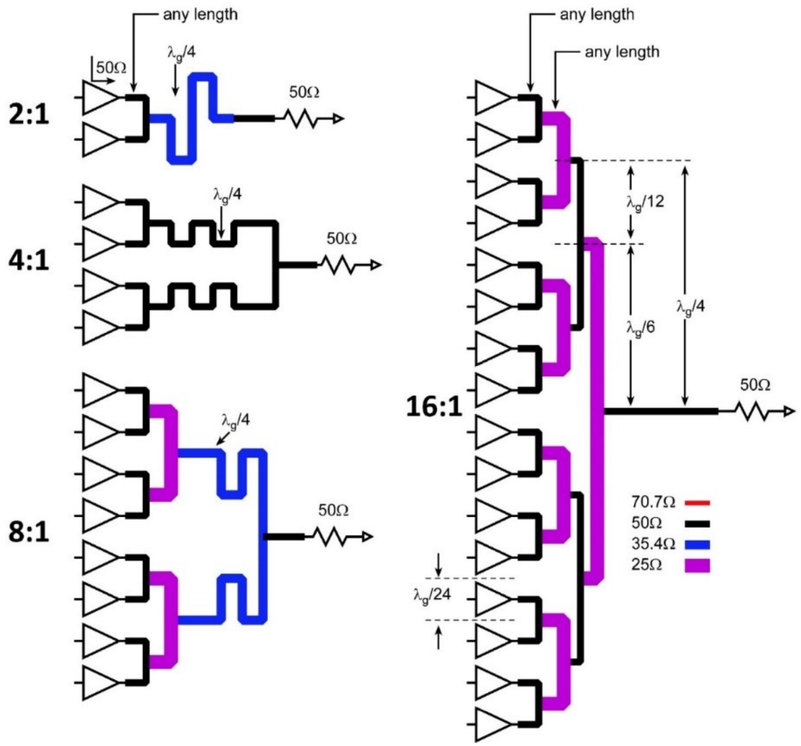
Low-Loss 100-300GHz Corporate Combining

Wilkinson trees are lossy:
Signal passes through *many* 70.7Ω, λ/4 lines.
λ/4 lines are long.
70.7Ω lines are narrow…and lossy→ High loss.

Single-(λ/4) combiners are much less lossy
Each design uses a single *effective* λ/4 section.
Shorter lines, low-Z_o lines → lower loss
But, low loss only if transistor cells fit.

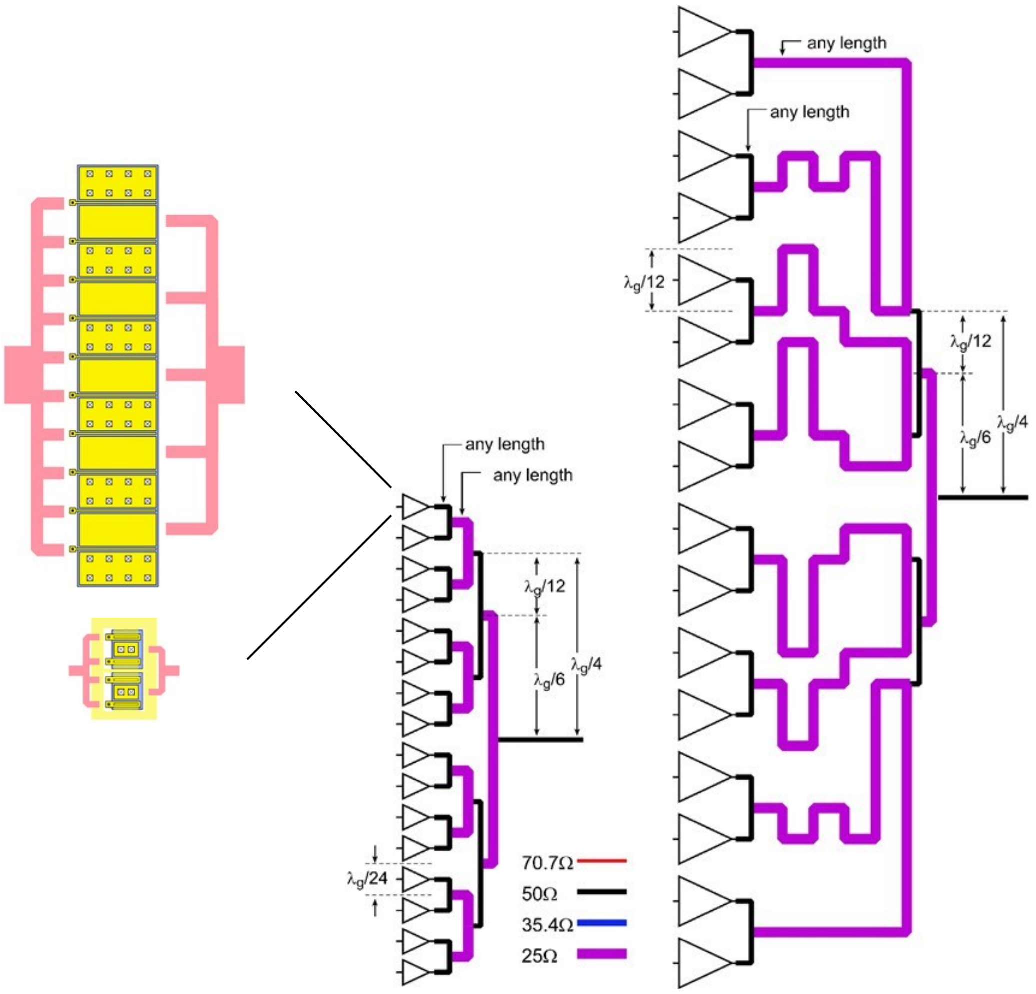




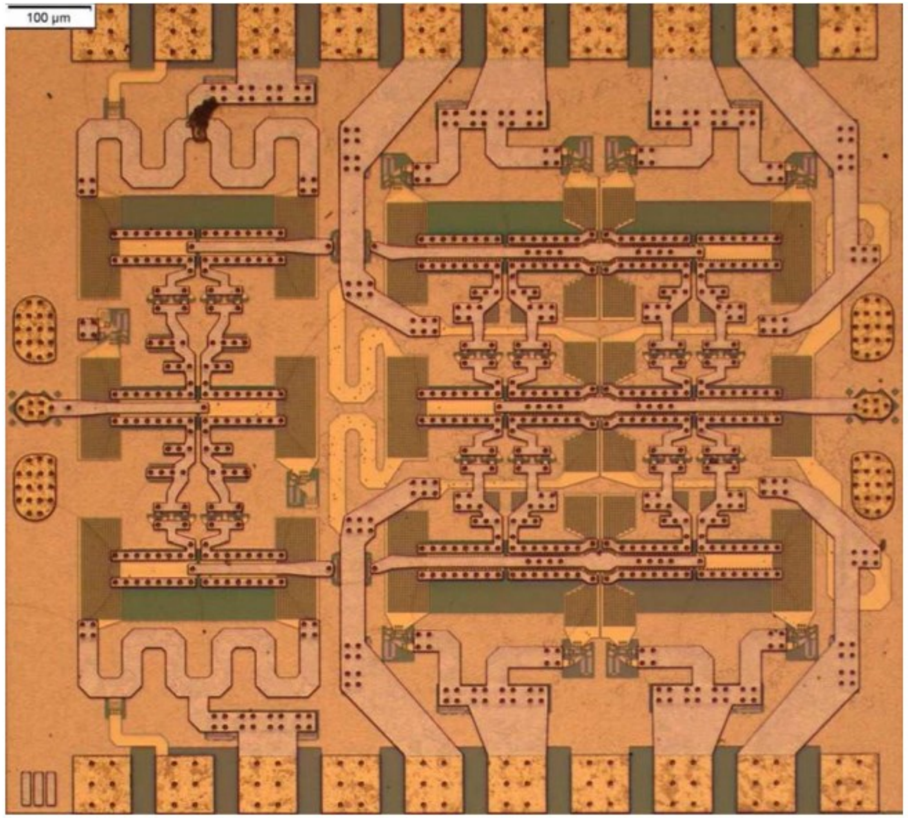


Denser Integration: higher PAE at high Power

Compact multi-finger transistor layouts
→ Shorter combiner lines
→ Less loss
→ Higher PAE.

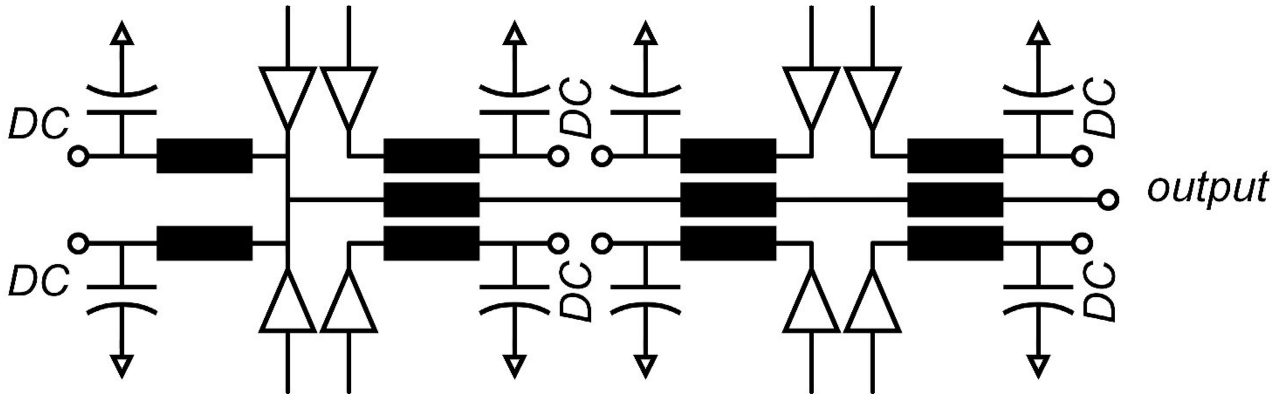


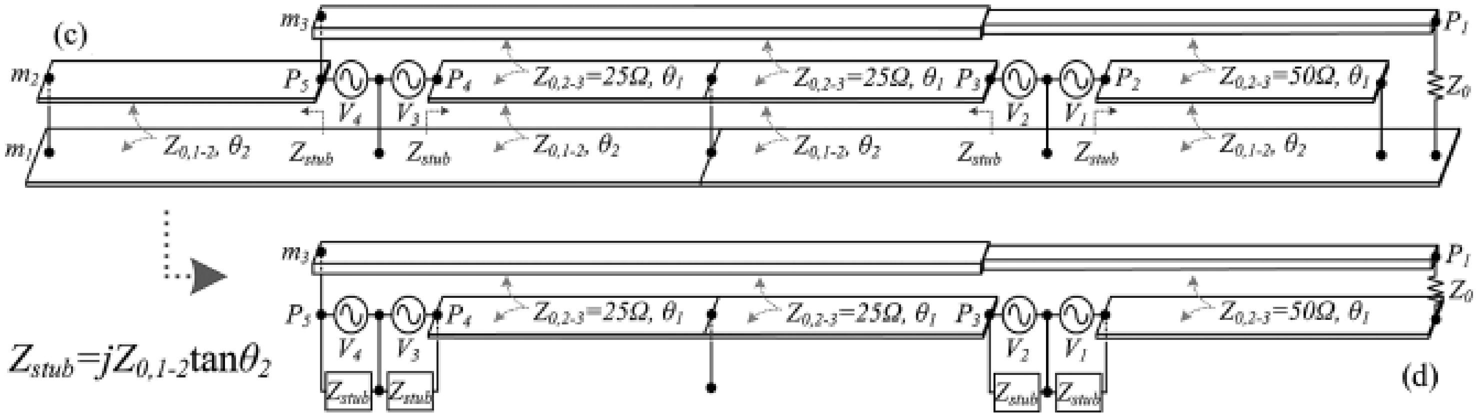
Series combining using sub-λ/4 baluns



81GHz, 17 dB Gain
470 mW P_{sat} , 23% PAE
Teledyne 250 nm InP HBT
2 stages, 1.0 mm^2(incl pads)

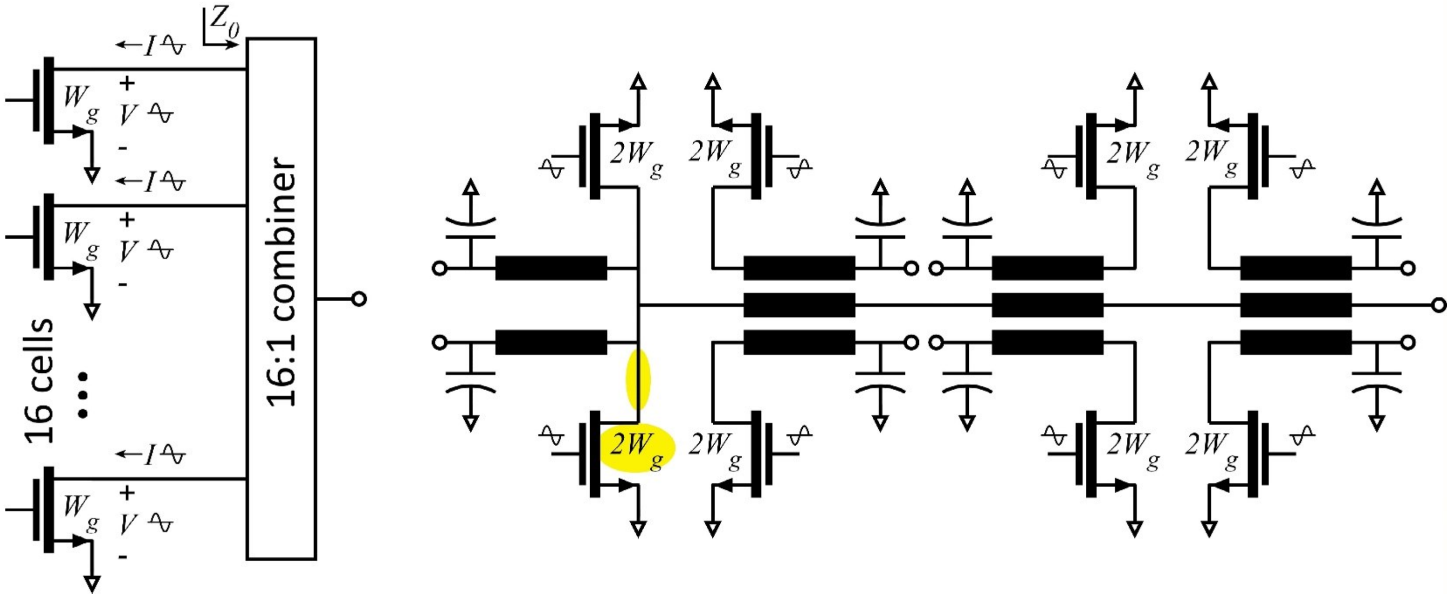
λ/4 baluns: Y. Yoshihara, 2008 IEEE Asian Solid-State Circuits Conference **(Toshiba)**
sub-λ/4 baluns: H. Park, et al, IEEE JSSC, Oct. 2014 **(UCSB)**





$Z_{stub}=jZ_{0,1\text{-}2}\tan\theta_2$

Sub-λ/4 Balun Combiners. Why ? Why not ?



	Lower frequencies	Higher frequencies
Corporate combining	length ∝ $1/f$ → large die area ✗ dB loss ∝ $1/\sqrt{f}$ → high loss ✗	length ∝ $1/f$ → small die area ✓ dB loss ∝ $1/\sqrt{f}$ → low loss ✓
Sub-λ/4 Balun	more transistor fingers per cell → ok ✓	more transistor fingers per cell → parasitics ✗ impedance shift of transistor-balun interconnect ✗

On-Wafer Interconnect Losses

Interconnects in packages and on PCBs:

$H \propto 1/\text{frequency}$ (to control radiation loss)

$\text{loss (dB/mm)} \propto (\text{frequency})^{3/2}$

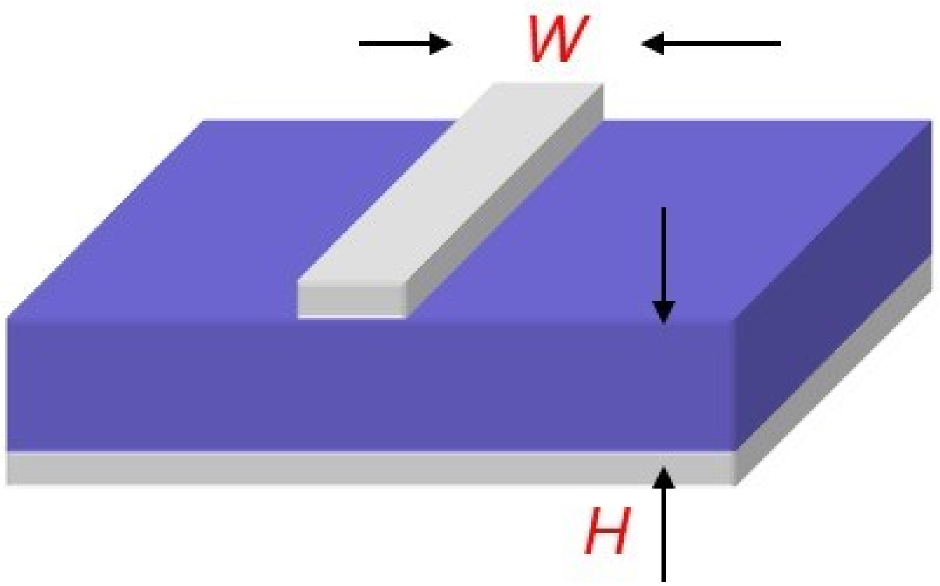
$\text{loss (dB/wavelength)} \propto \sqrt{\text{frequency}}$

Interconnects in ICs:

H is independent of frequency

$\text{loss (dB/mm)} \propto \sqrt{\text{frequency}}$

$\text{loss (dB/wavelength)} \propto 1/\sqrt{\text{frequency}}$

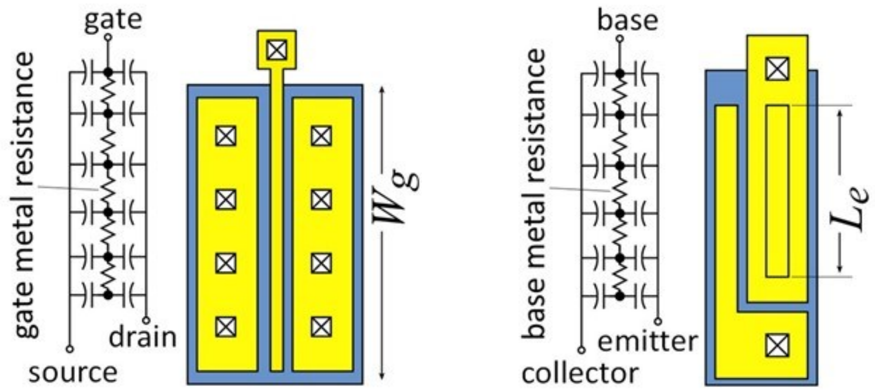


Current density, finger pitch limit cell output power

Electrode RC charging time $\propto$ (finger length)^2

Maximum finger length $\propto 1/\sqrt{\text{frequency}}$

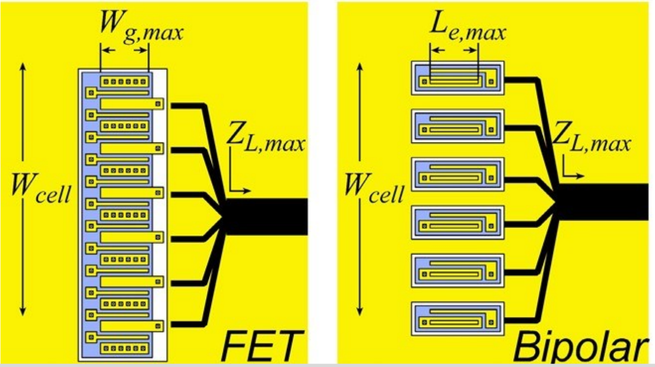
Current per finger $\propto 1/\sqrt{\text{frequency}}$



Maximum cell width $\propto 1/\text{frequency}$

Maximum number fingers $\propto 1/\text{frequency}$

Maximum current per cell $\propto 1/\text{frequency}^{3/2}$



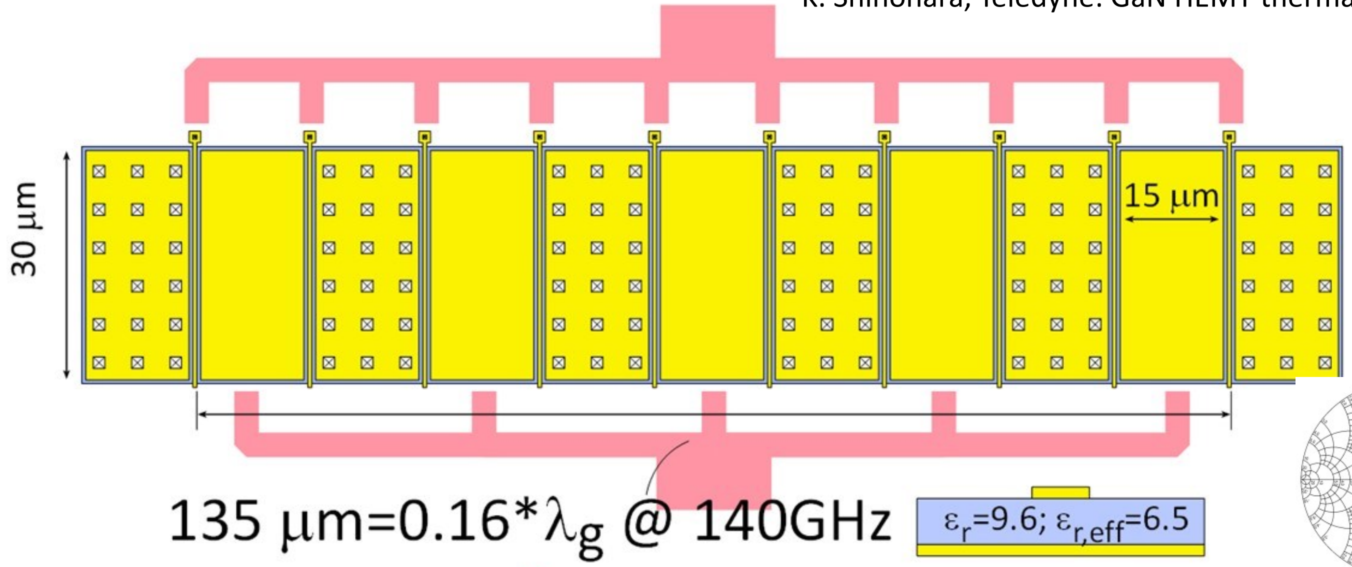
Maximum RF power per cell $\propto (\text{maximum load resistance}) \cdot (\text{maximum current})^2 \propto 1/(\text{frequency})^3$

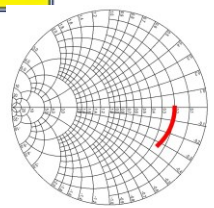
Compare to Johnson F.O.M.: maximum power per cell $\propto (\text{maximum voltage})^2 / (\text{minimum load resistance}) \propto 1/(\text{frequency})^2$

Current density, finger pitch limit cell output power

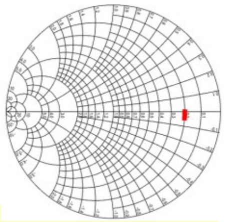
K. Shinohara, Teledyne: GaN HEMT thermal analysis

50Ω GaN PA cell @ 140GHz (1.6W)
25V swing, 1.67mA/µm,
gates: 30 µm width, 15 µm pitch





50Ω InP HBT PA cell @ 280GHz (40mW)
4V swing, 3.3mA/µm,
emitters: 6 µm length, 6 µm pitch

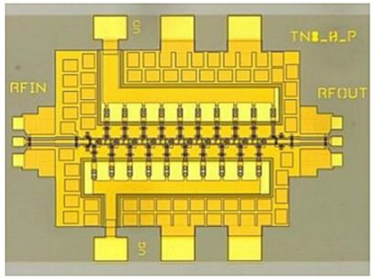


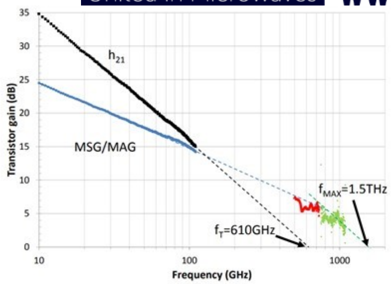
High V_{br}, low I_{max} ? Device sized to drive 50Ω might approach $\lambda_g/4$ width.
Small finger pitch is critical; limited by thermal design

Summary: InP transistors & ICs

InP HEMTs: 1.5THz f_{max}, 1.0THz amplifiers

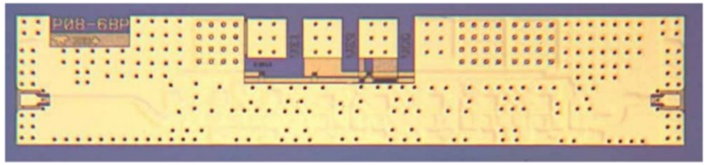
W. Deal et al, 2016 IEDM (Northrop-Grumman)

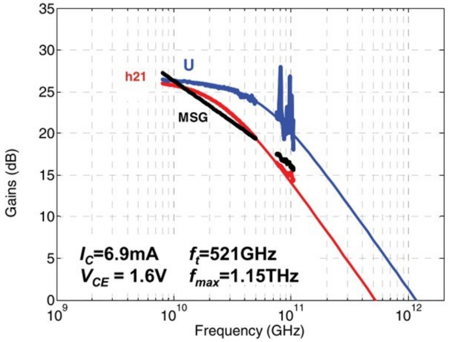


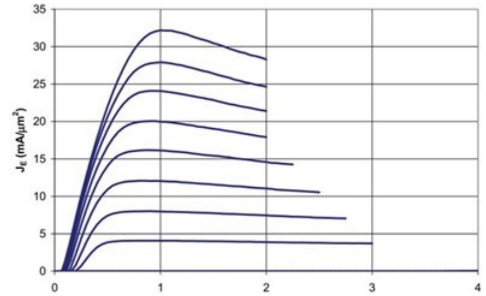


130nm InP HBTs: 1.1THz f_{max}, **3.5V.** 670 GHz amplifiers

M. Urteaga, et al, IEEE Proceedings June 2017 (Teledyne)



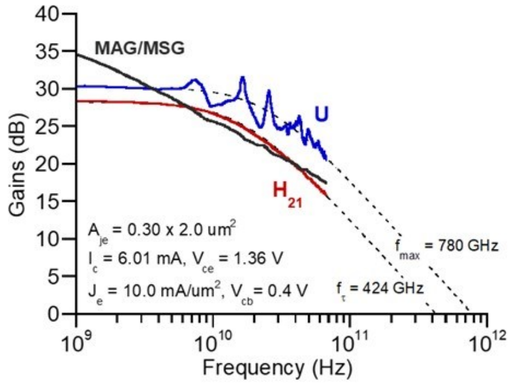


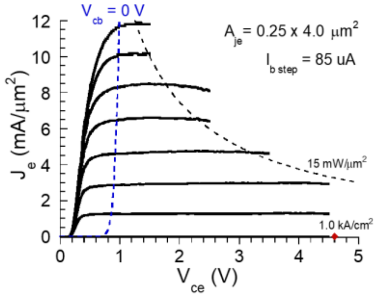


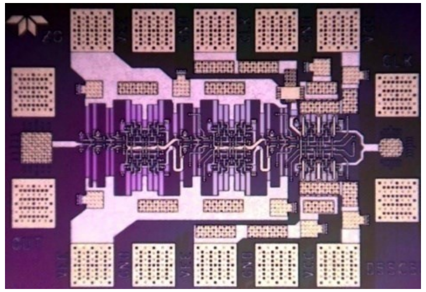
250nm InP HBTs: 650GHz f_{max}, **4.5V.**

Z. Griffith et al, 2007 IPRM conference (UCSB)

M. Urteaga, et al, IEEE Proceedings June 2017 (Teledyne)







204 GHz static frequency divider
Z. Griffith et al, 2010 IEEE CSICS