End-to-end 6G Terahertz Wireless Platform with Adaptive Transmit and Receive Beamforming

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***Abstract*— 6G is envisioned to provide ultimate experience for all through hyper-connectivity involving humans and everything, with unprecedented requirements and expectations [1]. In this vision, terahertz (THz) technology is a leading candidate to realize the 6G requirements. This paper presents the latest development and results of a terahertz wireless prototyping platform, which is being developed in Samsung research lab. The platform currently supports real-time transmission of 6 Gbps of data over a 2 GHz channel centered around 135 GHz with adaptive beamforming at the transmitter and receiver. The modem is designed to handle data-rate up to 36 Gbps, supports two MIMO streams, and aggregates two 2GHz channels. This paper also presents the specifications of the current RF units and discusses the challenges faced during the design and fabrication of these units.**

Keywords— 6G, Terahertz, wireless, platform, prototype, beamforming.

I. INTRODUCTION

Fast growth in artificial intelligence (AI), robotics, and automation are some trends that indicate an increase in the demand for throughput. Samsung in their 6G-vision white paper [1], envisage that machines will be the dominant consumers of the communication networks. Moreover, some of these machines might take the form of a truly immersive extended reality (XR), high-fidelity mobile hologram, or digital replica. These high-end machines will require communication links with nearly terabit-per-second (tbps) speeds. Where can we get such capacity?

Various new technologies are emerging to enhance system capacity and user experience. One of the leading candidates is to utilize the THz band. In this work, the THz band is defined as the frequencies ranging from 0.1 THz to 10 THz, which aligns with some publications such as [2]. The THz band includes enormous amount of available bandwidth, which will enable extremely wideband channels with tens of GHz-wide bandwidth. This could potentially provide a means to meet the 6G requirement of tbps data rate.

To realize stable THz communications in practice is not straight forward, and a handful of fundamental and technical challenges need to be overcome. Commonly, this band is often referred to as the terahertz gap that is mainly due to the lack of efficient devices, which generate and detect signals in these frequencies. In this band, the device dimensions are significant relative to the signal wavelength, and this result in high losses due to dielectric skin-depth and surface roughness losses. Also devices show low efficiency due to significant impact of parasitics on the device performance. The severe path-loss and atmospheric absorption add to the challenge of utilizing this band. On the positive side, in the past 10 years a lot of research and development has been done on: 1) designing RF circuits operating at the lower THz band [3], and 2) utilizing large antenna arrays to mitigate path-loss. Scaling up this technology to extremely large phased arrays will be essential to realize a reliable THz link.

Recognizing the potential of THz spectrum, global regulatory agencies such as Japan's Ministry of Internal Affairs and Communications (MIC), Conference of European Postal and Telecommunications (CEPT), the Federal Communications Commission (FCC), and England's OFCOM have adopted rulemakings and have opened up the spectrum above 100 GHz [4]. For example, a total of 102 GHz spectrum in the range between 95 GHz and 300 GHz is being made accessible for licensed fixed point-to-point and mobile services through the Spectrum Horizon program [5]. Accordingly, the extremely wideband THz channels with tens of GHz-wide bandwidth could potentially support the Tbps communication envisioned by the future 6G standard.

In [6], we presented the initial phase of Samsung's THz prototyping platform. The initial platform supported up to 6 Gbps end-to-end throughput using a single 2 GHz single-input-single-output (SISO) channel. Also, the RF units had several limitations: the beamformer TX had linearity issue, and limited transmit power. In this work, a more powerful platform is developed. The Samsung Terahertz REsearch Advanced Modem (STREAM) platform supports up to 36 Gbps end-to-end throughput, and can aggregate two 2 GHz channels, each one is a 2x2 multi-input-multi-output (MIMO) channel. Also, new RF units are developed, which provides good linearity at both transmit and receive units. The new RF is able to provide 15 dB more output power by including Indium Phosphate (InP) power amplifiers (PA). Note, the lab results provided in this paper are

for a single MIMO stream, a single 2GHz-carrier, and up to 16-QAM modulation. This lab setup achieves 6 Gbps at 30-meter distance, and 2.3 Gbps at 120-meter distance. The modem, however, is designed to support up to 64-QAM, and when configured to two MIMO streams and two 2GHz-carriers, the achieved rate is 36 Gbps.

Following are other state-of the-art publications, which demonstrate multi-channel links in the D-band (110-170 GHz) : In [7], a 140 GHz link was tested over WR-6 waveguide, and it achieved a data-rate of 30 Gbps using 64-QAM modulation. 4-channel TX and RX chips were developed. The chips were fabricated in 130 nm SiGe BiCMOS. The TX has a maximum output power of 12 dBm. In [8], a 140 GHz over-the-air link was demonstrated. A data-rate of 16 Gbps over 30 cm distance was achieved using 64-QAM modulation. 8-channel 140 GHz TX chip was developed. The chip was fabricated in CMOS, and it has on-chip antennas. The chip has 1-D scanning range of ±30°. The chip has a maximum EIRP of 32 dBm. In [9], a 130 GHz over-the-air link was demonstrated. A data-rate of 32 Gbps over 40 cm distance was achieved using QPSK modulation and 2x2 LoS-MIMO. 2-channel TX and RX chips were developed. The chips were fabricated in 55nm BiCMOS. The TX has a maximum output power of 2.5 dBm, and it has a maximum EIRP of 28 dBm, which was achieved by utilizing on-package lens antennas.

The paper is organized as follows: In Section II, the overall system description is presented. In Section III, the architecture and capabilities of the STREAM platform are shown. In Section IV, the specifications of the RF modules are shown. In Section V, the specifications for the baseband modem and waveform design is presented. In section VI, the baseband modem architecture and signal processing is shown. In Section VII, the experimental setup and results are presented.

II. Overall System Description

The system architecture for the 36 Gbps prototyping platform is shown in Fig. 1. The transceiver consists of three parts, the STREAM platform, the analog and baseband unit (ABU), and the RF units (RFU).

The STREAM platform runs the baseband modem, where the data get encoded, modulated, and mapped to the frame structure. The platform has 400 Gbps streaming interface to data-convertors on the ABU, and it is capable of processing up to 50 Gbps of PHY throughput. The ABU performs the filtering, digital beamforming, and data-conversion between analog and digital domains. The RFU convert the signal between the baseband analog signal and the RF signal at 135 GHz. TX (or, RX) RF module contains 8 RF channels.

III. The STREAM Platform

The architecture of the STREAM platform is shown in Fig. 2. The platform consists of four FPGAs from the Xilinx Zynq Ultrascale+ RFSoC family, namely the ZU21DR. Each of these FPGAs consists of Programmable Logic (PL) and a Processing System (PS). The PL contains eight Soft Decision Forward Error Correction (SD-FEC) cores, 4272 DSP slices and 930K system logic cells for signal processing, 38 Mb of BRAM for storage and 16 GTY transceivers for high speed serial data transmission between devices. The PS includes a Quad-core ARM Cortex A53 Application Processing Unit (APU) and a Dual-core ARM Cortex R5 Realtime Processing Unit. The PS-PL interface is based on AMBA AXI4 interface for primary data communication. The STREAM platform also consists of one Xilinx Virtex Ultrascale+ VU13P FPGA. This FPGA contains 12288 DSP slices, 3780K system logic cells, 94.5 Mb of BRAM and 128 GTY transceivers and is used for low-PHY processing such as channel estimation, equalization, and MIMO detection. As shown in Fig. 2, these five FPGAs are interconnected via the GTY transceivers to support high speed data transfer between different processing blocks. Each FPGA also has external end-point connectors via QSFP and ODI to enable data communication with other external devices such as a host PC, ABU, or another STREAM platform. The platform is shown in Fig. 3.

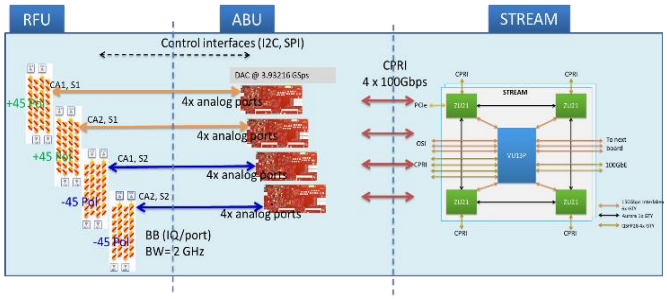

Fig. 1. Architecture of the 36 Gbps THz prototyping platform

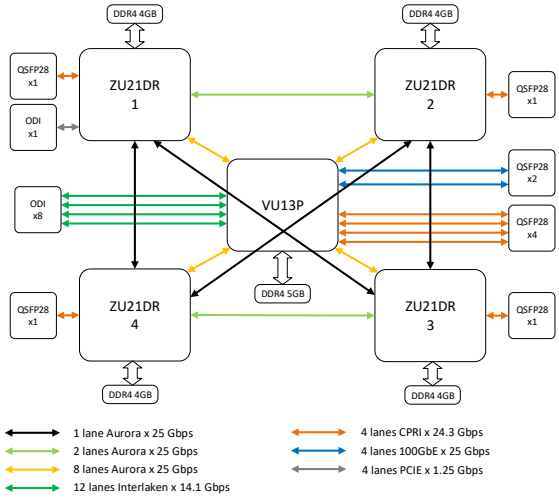

Fig. 2. Architecture of the STREAM platform.

IV. RF Specifications

At the transmitter side, two RF options were used. First, a CMOS based TX beamformer was used which is based on the 22nm CMOS RFICs developed by the University of California, Santa Barbara (UCSB). Second, InP PA based TX beamformer, which is based on the 22nm CMOS RFICs and additional InP PAs to reach longer distance. [10]-[13]

Fig. 3. STREAM platform for baseband modem implementation.

The TX beamformer includes eight CMOS transmitter ICs with InP HBT power amplifiers as well as linear microstrip patch antennas on Kyocera LTCC substrate. The transmitter ICs, which were fabricated using Global Foundries 22nm SOI process, are direct conversion transmitters, and they generate 135GHz RF signal using differential baseband IQ signals. The multiplier, which consists of two series tripler, generates the 135GHz signals from external 15GHz signals. The InP HBT power amplifier has three common-base stages and a low-loss 4:1 transmission-line output power combiner. It was fabricated with the 250nm InP HBT technology. The amplifier has 20.5 dBm peak saturated output power with 20.8% PAE and 15dB associated large-signal gain at 135 GHz. The CMOS ICs have 50 um Cu pillars on the pads, they were assembled using flip-chip process, and they were directly attached to the LTCC substrate. The InP PAs are attached to the LTCC substrate and the pads are connected using wire-bonding process [13].

Fig. 4 shows the large signal power measurement and simulation results for the InP PA. At 140GHz, the amplifier has saturated output power of 20.5dBm with 20.8% PAE and 15dB associated gain. At 1-dB gain compression, the amplifier has 17dBm output power and 9.7% PAE. [16]

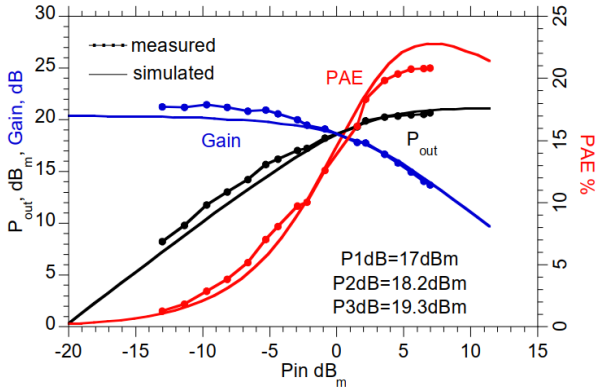

Fig. 4. Measured and simulated output power, PAE, and gain versus the input power at 140GHz.

In the single MIMO-stream TX beamformer, the I/Q baseband signal is replicated 8 times, each replica is rotated using the digital phase-shifter, processed to apply the transmitter I/Q imbalance and phase calibration, then fed to the digital-to-analog convertor (DAC). Note that this part is implemented using two ABUs, each ABU processes four I/Q channels. The system architecture is shown in Fig. 5. The I/Q channels are then directly up-converted to 135 GHz using the CMOS TX RFIC. Each RFIC has one channel, which has an output power of -6 dBm per channel with 6 dB back-off (CMOS based) and output power of 10 dBm per channel (InP PA based) at the input of the antenna. The TX beamformer module, which was made using conventional PCB fabrication process, is shown in Fig. 6 (Left) carrying the CMOS RFICs, InP PA ICs and the antenna array.

The single MIMO-stream RX beamformer consists of CMOS receiver ICs with linear microstrip patch antennas on Kyocera LTCC substrate as well. The direct conversion receivers were implemented with a wideband fully differential LNA at the front end, using a cross-coupled pair with capacitive neutralization, followed by a linear double balanced passive mixer and broadband pseudo-differential trans-impedance amplifier.

The RX beamformer has similar structure as that of the TX as shown in Fig. 6 (Right). The 135 GHz is directly down-converted to the I/Q baseband signal using the CMOS RX RFIC. A total of eight RFICs are used, each has one channel. The I/Q signals are sampled using the 4 Gsps analog-to-digital convertors (ADC) on the ABU board (see, the architecture in Fig. 5). The digitized signals are rotated using digital-phase shifter, then combined and passed to the baseband modem.

A 64-element antenna array, which was made using Kyocera LTCC fabrication process, is used at the TX beamformer. A similar array is used at the RX beamformer. The array is developed to achieve 20 dBi gain with a scanning range of +/-40 degree in azimuth direction. The array is shown in Fig. 7, and it has dimensions of 9.3 mm by 7.2 mm. The simulated beam patterns of the array steered in different azimuth angles are shown in Fig. 8. The array includes 8 sub-arrays. Each sub-array consists of 8 radiating patch antennas. The elements of the sub-array are serially fed rectangular patches.

TABLE I shows the link-budget for two different variations of the setup. In the first setup (labeled: CMOS based), eight beamformed channels from CMOS are used at the TX and eight channels at the RX. The TX beamformer can provide EIRP of 23 dBm. This can support a spectral efficiency of 5.02 b/s/Hz at a distance of 5 meters. In the second setup (labeled: InP based), eight beamformed channels with additional InP PAs are used at the TX and eight channels at the RX to achieve EIRP of 39 dBm. This EIRP can support a spectral efficiency of 4.7 b/s/Hz at a distance of 30 meters. Same RX RF modules were used for both setups.

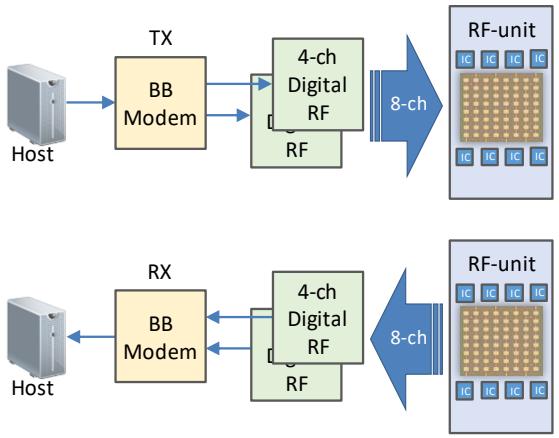

Fig. 5. System architecture for the single MIMO-stream transmitter and receiver digital beamformers.

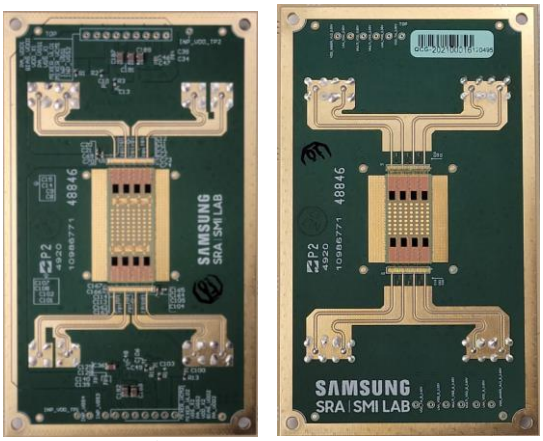

Fig. 6. The TX beamformer module with eight channel 135 GHz RFICs and the antenna array (Left). The RX beamformer module (Right).

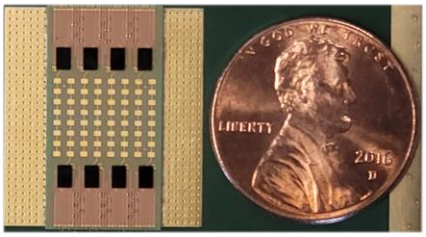

Fig. 7. Antenna array with 8 RF channels at 135 GHz carrier frequency.

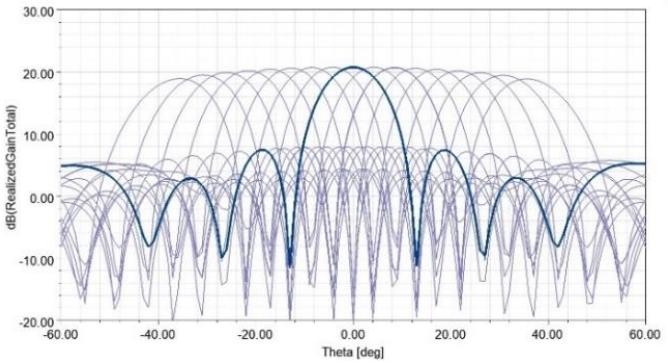

Fig. 8. Antenna pattern shows 20 dB of realized gain and +/-40 degree steerability.

In the spectral efficiency calculations, the line-of-sight (LoS) free-space path-loss model is used, which is given by:

$$PL = 32.45 + 20\log(d) + 20\log(f),$$

where d is distance in meter, and f is the frequency in GHz. Moreover, the Shannon capacity formula is used after applying a margin of around 10 dB for other losses. These losses include algorithmic losses in the baseband modem, but more importantly it also accounts for hardware impairments, losses due to routing the 135 GHz signal between the RFIC and the antennas, and the imperfections in the array calibration.

TABLE I. SYSTEM LINK-BUDGET

Parameter	CMOS based	InP based
RF Frequency (GHz)	135	135
Bandwidth (GHz)	2	2
Number of RF TX Channels	8	8
Number of RF RX Channels	8	8
RFIC TX Output Power (dBm/Channel)	-6	10
TX Antenna Gain (dBi)	20	20
RX Antenna Gain (dBi)	20	20
EIRP (dBm)	23	39
RX LNA Noise Figure (dB)	10	10
Distance (m)	5	30
Path-Loss (dB)	90	106
Margin for other TX/RX losses (dB)	10	10
Max. spectral efficiency [b/s/Hz]	4.7	4.7
Theoretic max. throughput [Gbps]	9.4	9.4
Modulation	16-QAM	16-QAM
Achieved throughput [Gbps]	6.3	6.3

V. BASEBAND MODEM SPECIFICATIONS

The baseband modem implements a single-carrier waveform, which has low peak-to-average power ratio (PAPR), especially when used with QPSK modulation. This choice aligns well with the limited output-power capabilities of current RF devices. Recall that a single-carrier QPSK waveform, when transmitted at peak output power, doesn't suffer from EVM degradation. However, a back-off of 3dB from the peak output power is needed to prevent spectral re-growth. On the other hand, for a single-carrier 16-QAM waveform a back-off of 6 dB is necessary to avoid significant degradation in EVM. For comparison, a multi-carrier waveform such as orthogonal frequency division multiplexing (OFDM) waveform requires around 8 dB back-off, when used with a crest factor reduction algorithm.

The waveform frame structure is similar to that in [6], and its main features are captured in Fig. 9 and Fig. 10. For a more detailed description, the reader is advised to refer to [6]. Also note that, in this work, the channel estimation field (CEF) is updated to support two MIMO streams. The CEF structure is similar to that used in IEEE802.11ay [14], in which two orthogonal complimentary Golay sequences are used for the different MIMO-streams.

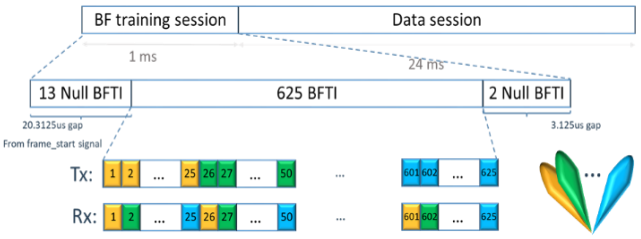

Fig. 9. Frame structure of the used single-carrier waveform and exhustive beam cycling algorithm to check all 625 beam-pair combinations.

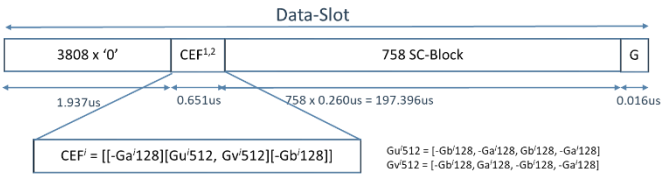

Fig. 10. Data-Slot structure in the data session and the structure of the two orthogonal sequences $CEF^{1,2}$.

Given the EVM limitation of the current RF front-end, the highest modulation that can be supported is 16-QAM. And so, a 16-QAM with coding rate of 11/12 was designed to show 6.39 Gbps throughput per MIMO stream and 2 GHz carrier bandwidth. This rate is the highest possible with current RF. Also, two QPSK modulation and coding schemes (MCS) were used to demonstrate longer distances transmissions. In particular, QPSK with coding rates of 1/2 and 11/12. These MCSs achieve throughputs of 1.74, and 3.19 Gbps, respectively. Moreover, in anticipation for a higher quality RF front-end, a 64-QAM and coding rate of 11/12 MSC was implemented. This MCS can achieve 9.56 Gbps throughput per MIMO stream.

The waveform numerology is the same as that in [6], and it is summarized in TABLE II.

TABLE II. SINGLE-CARRIER WAVEFORM NUMEROLOGY.

Parameter	Value	Unit
Chip-Rate	1.96608	G Chip/s
Chip-Duration	0.508626302	*ns*
SC-Block length	512	Chip
Guard-block length	32	Chip
Data-block length	480	Chip
Guard-block duration	16.27604167	*ns*
Data-block duration	244.140625	*ns*
SC-Block duration	260.4166667	*ns*

VI. BASEBAND MODEM ARCHITECTURE

The baseband modem architecture in the STREAM platform is shown in Fig. 11. Also, the architecture of the digital-front-end on the ABU is shown in Fig. 12.

On the transmitter side: The host PC generates up to four streams of data, and sends each data-stream to one of the ZU21DR FPGAs on the STREAM platform. A ZU21DR FPGA runs the bit-processing (denoted H-PHY) of a single data-stream. The H-PHY processing include CRC insertion, LDPC encoding, and scrambling. The scrambled data is sent to the VU13P FPGA via the high speed Aurora interface.

The VU13P FPGA runs two 2GHz-carrier modules (CA1, and CA2). Each CA module processes two MIMO streams. The CA module modulates the scrambled data, and generates the data frame. The data frame is sent to the ABU via the CPRI interface, where it gets resampled and filtered using a root-raised-cosine (RRC) filter with roll-off factor 0.2. After that, the signal is replicated four times, each replica is rotated using the digital phase-shifter, processed to apply the transmitter I/Q imbalance and phase calibration, then fed to the DACs. Finally, the analog I/Q signals are sent to the RF-units. Note in the case of single MIMO-stream the same signal is sent to two ABUs to generate the analog signals for eight beamformed channels.

On the receiver side: The analog baseband signals from the RF-unit are digitized using the ADCs in the ABU, four channels at each ABU. Each channel is corrected for I/Q imbalance and phase-mismatch, then rotated using digital-phase shifters according to a preloaded beamforming table. The four channels are then combined, and filtered using the matching filter. The output of the matching filter is sent to the VU13P FPGA via CPRI. The received signal is then passed to the synchronization module, channel estimation module, and the equalizer. The synchronization module signals the start of a CEF in a data-slot to the channel estimation module. The channel estimation module captures the received CEF and estimates the channel, then passes the estimation to the equalizer. The equalizer converts the time-domain channel to the frequency domain using 512 FFT, then uses it to equalize the received SC-block one-by-one in the frequency domain. The equalizer implements a fractionally spaced equalizer (FSE) with 2x oversampling to alleviate the receiver sensitivity to sampling offset impairment. More details on the used equalizer can be found in [15]. The equalized symbols are processed using the phase-noise tracking module, which corrects for the common phase-error in the SC-block. The output of the phase-noise module is demodulated into soft log-likelihood-ratios (LLRs). The LLRs are sent to the ZU21DR FPGA, which descrambles and decodes the LLRs. The recovered information bits are packaged into IP packets, then sent to the host PC at the receiver side.

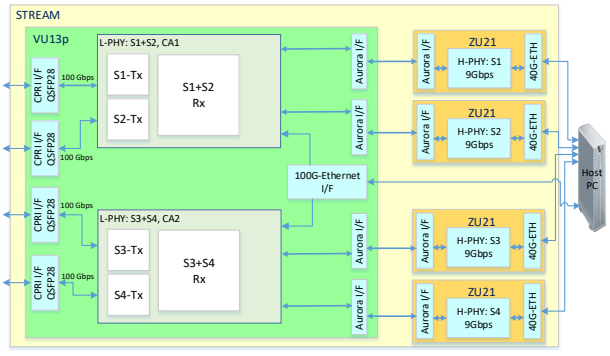

Fig. 11. Baseband modem architecture in STREAM platform.

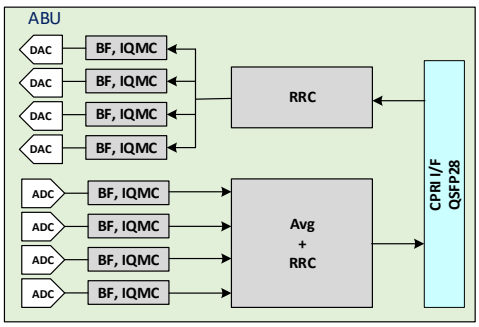

Fig. 12. Digital-front-end architecture in the ABU.

VII. System Setup and Lab Measurements Result

The lab setup is shown in Fig. 13. In this setup the TX was placed at distance *d* from the receiver, where *d* was set to 8.5 m, 30 m, or 120 m. In all cases, the InP PA based TX beamformer was used. Note similar experiments were conducted with the CMOS based TX beamformer at 1 m distance from the RX, however in the following we limit the results to the InP PA based TX beamformer. Also note, only 5 TX channels and 4 RX channels were beamformed due to hardware status.

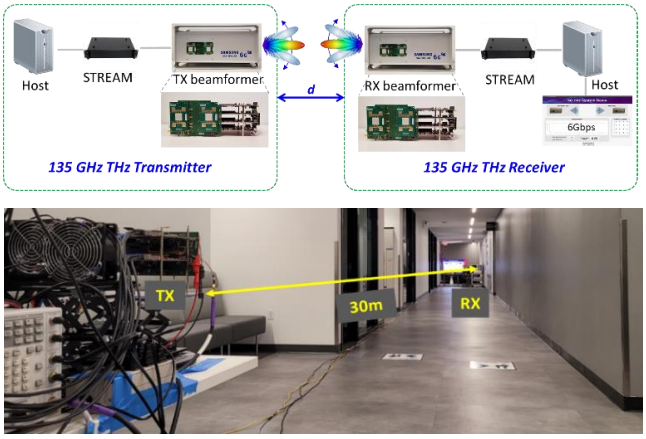

Fig. 13. TX and RX adaptive beamforming indoor setup.

At distance 8.5 m between TX and RX, Fig. 14 shows the RSSI values obtained during the beamforming session for all 625 TX-RX beam-pairs, when the TX and RX beamformers are facing each other. The selected beam, which has the maximum RSSI, is at BFTI index 313. This index corresponds to the beams pointing toward the broadside of the array. It is also interesting to note the unsymmetrical RSSI profile for the directions to the left and right of the direct LoS direction. Specifically, the RSSI values corresponding to BFTI indices 1 to 100 compared to that for indices 525 to 625. There was a bench and measurement instruments, which have similar height as the TX and on a direction that aligns with indices 1 to 100. Also observed, as one rotates the TX, RX, or both, the BFTI index with the maximum RSSI changes in correspondence with the rotation direction, which result in the modem selecting different beams for the data-session.

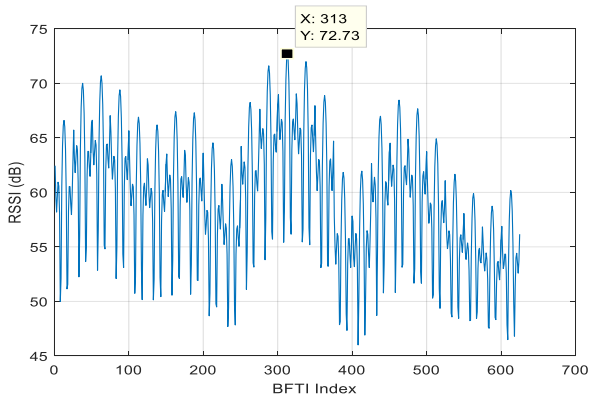

Fig. 14. RSSI scan recorded during BF training session for all TX-RX beam pairs.

At distance of 8.5 m, we also evaluated the end-to-end link throughput as a function of the signal-power backoff at the input of the TX beamformer. The results for the 2nd and 3rd MCSs are shown in Fig. 15. For QPSK, the MCS full rate of 3 Gbps was maintained with backoff in the range from -23 dB to 0 dB. On the other hand, for 16QAM the MCS full rate of 6 Gbps was maintained with backoff in the range -13 dB to -7 dB. This implies that the 16QAM MCS has 6 dB of margin, which can be used to double the distance to 17 meters while maintaining the full rate. Similarly, the QPSK MCS has 23 dB of margin, which potentially can increase the distance to 120 meters while maintaining the full rate. Note, the QPSK MCS not only has 10 dB SNR advantage over the 16QAM MCS, but also it tolerates higher level of PA nonlinearity. This tolerance gives the QPSK MCS another 6 dB advantage. Off course this comes at the cost of bandwidth, as pushing the PA into saturation causes spectrum regrowth.

At distance of 30 m between TX and RX, a lens antenna was placed in front of the RX array, which provided 9 dB of gain. This was necessary to substitute for the missing TX and RX channels, and to close the link-budget at 30 m. Fig. 16 shows 6 Gbps end-to-end throughput maintained while rotating the TX and RX.

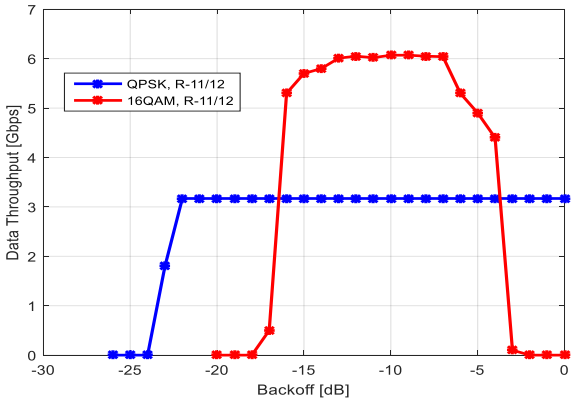

Fig. 15. End-to-end thrpugput vs TX backoff.

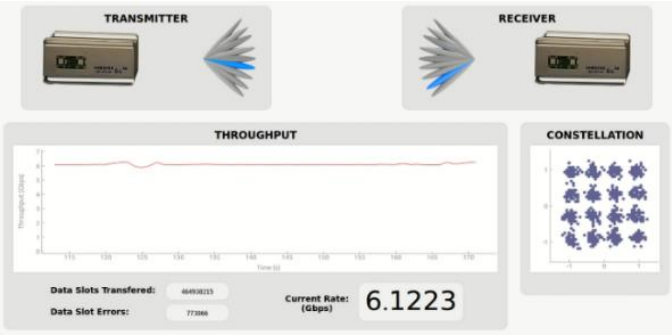

Fig. 16. Maintained 6 Gbps throughput (per single-stream and one 2GHz carrier) while rotating TX and RX.

At distance 120 m, the setup is shown in Fig. 17. This experiment was done outdoor, where the TX was placed on the second floor of the parking garage, and the RX was placed in the parking lot 120 m away from the TX. There was a clear line-of-sight path between the TX and RX. There were also few lamp-posts and small trees, which may have resulted in some non-line-of-sight signal components. The QPSK, rate 11/12, MCS was used, and a lens antenna was placed in front of the RX array. Among the received packets, 27% were in error, and got discarded. Accounting only for successful packets, the achieved rate was stable at around 2.3 Gbps. Note, no erroneous packets were observed with QPSK, rate 1/2, MCS. The later MCS achieved a stable 1.74 Gbps. It is expected that QPSK, rate 3/4, MCS can achieve error-free 2.3 Gbps data-rate. However, in the prototype, coding rates between 1/2 and 11/12 were not implemented.

VIII. Conclusion

In this paper, the latest progress on Samsung's 6G THz wireless platform is presented. The platform was used to demonstrate a real-time end-to-end link with adaptive TX and RX beam steering with data-rate of 6.3 Gbps at 30-meter distance, and 2.3 Gbps at 120-meter distance. In both cases, 2 GHz of channel bandwidth was used and achieved spectral efficiencies of 3.15 and 1.15 bit/sec/Hz, respectively at 135 GHz. The platform is designed to support two MIMO-streams and aggregates two 2GHz-carriers. Future work will demonstrate these capabilities and show improved spectral efficiency.

Fig. 17. Outdoor setup with 120 m distance between TX and RX.

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