A 280 GHz (x8) Frequency Multiplier Chain in 250 nm InP HBT Technology

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***Abstract*— We report a 280 GHz x8 frequency multiplier chain in 250 nm InP HBT technology. Emitter coupled pair in push-push configuration act as a balanced frequency doubler. The x8 frequency multiplier chain consists of three cascaded frequency doublers. Passive transformers are used to generate single-ended to differential conversion. At 280 GHz, the multiplier chain generates -0.6 dBm output power with 3-dB bandwidth of 48 GHz with input power of -2 dBm at 35 GHz. The unwanted harmonics are suppressed by more than 28 dBc over the frequency range of interest. It consumes 112 mW of DC power and occupies 0.4 mm^2 of the chip area. To the authors' knowledge, these results demonstrate record spectral purity for H-band frequency multipliers working around 280 GHz with low DC power consumption.**

Keywords—H-band, millimeter wave, frequency multiplier, balanced frequency doubler, high spectral purity, indium phosphide (InP), double heterojunction bipolar transistor (DHBT).

I. Introduction

There is increasing interest in the 200-300 GHz frequency band as millimeter-wave communications permit high data rates due to the available wide spectrum [1]. Frequency multipliers are important components in the transceiver since spurious harmonics generated by the frequency multiplication negatively affect the signal-to-interference ratio in direct-conversion transceivers. The implementation of low phase-noise oscillators becomes difficult as the operation frequency increases. Using a frequency multiplier with a high multiplication factor preceded by a low frequency voltage-controlled oscillators (VCO) would be an ideal case to generate local oscillator (LO) signal. Advanced technologies with high power gain cut off frequency (f_{max}) are necessary to generate moderate power and high harmonic suppression at H-band frequencies [2]-[10].

Here we report an H-band x8 frequency multiplier chain (FMC). It consists of three cascaded frequency doublers. The key design features are 1) doubler area scaling and 2) single-ended to differential conversion with low phase/amplitude imbalance. At 280 GHz, FMC shows -0.6 dBm output power with 48 GHz of 3-dB bandwidth when -2 dBm of input power is applied. The spurious harmonics are suppressed by more than 28 dBc over the frequency range of interest. Input power can be decreased for higher harmonic suppression at the cost of reduced operation bandwidth.

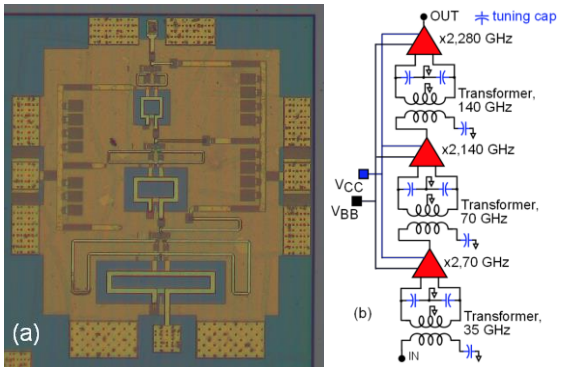

Fig. 1. (a) die photo, area including DC routing and pads is 0.8 mm x 0.92 mm. Core area, without DC routing or pads, is 0.56 mm x 0.7 mm and (b) frequency multiplier chain block diagram.

II. Frequency Multiplier Chain Design

The FMC is fabricated in Teledyne 250 nm InP HBT technology [11]. The HBT has a maximum 650 GHz power gain cut-off frequency (f_{max}), a maximum 3 mA/μm current density, and the 4.5 V BV_{CEO}. The technology provides four Au interconnect layers, 50 Ω/square thin film resistors, and 0.3 fF/μm^2 MIM capacitors.

A. Frequency Multiplier Chain Block Diagram

The x8 frequency multiplier is implemented by cascading three stages of frequency doublers in push-push configuration (Fig. 1b). The frequency doublers are preceded by a 1:1 passive transformer. Since each transformer is designed based on the input frequency of the associated frequency doubler, they act as a bandpass filter and help suppress spurious harmonics. The bias condition and the HBT emitter length of 280 GHz frequency doubler are chosen such that the output power generated at the 2nd harmonic has higher power than the required input drive power. Therefore, when the same bias condition and HBT emitter length are implemented for preceding frequency doubler stages, cascaded frequency doublers will have enough output power to drive the proceeding frequency doubler without any buffer amplifier in between. This design procedure helps us to minimize total DC power consumption. Using a single-ended input to differential output amplifier with a high common-mode rejection ratio (CMRR) may provide better spurious harmonic rejection at expense of DC power consumption.

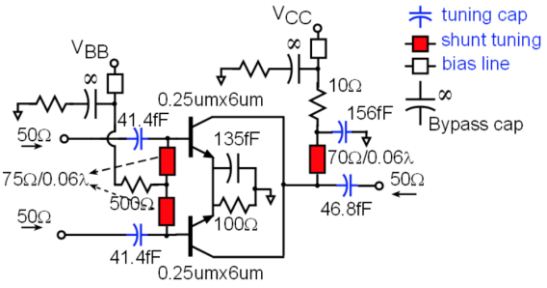

Fig. 2. Schematic diagram of 280 GHz frequency doubler.

B. *Balanced Frequency Doubler Cell*

The balanced frequency doubler cell consists of emitter-coupled pair in push-push configuration [12]. The transistor size is 0.25μm·6μm with 140 GHz large signal input impedance matched to 50 Ω and the output is class-B load line matched to 50 Ω at 280 GHz under the bias condition of 0.8 mA/μm and V_{CB}=0.8 V. Fig 2 shows the schematic diagram of the 280 GHz frequency doubler. The simulated output power of the 280 GHz frequency doubler integrated with the140 GHz transformer is +1 dBm with -1 dBm input power. RC network is implemented at the emitter node to improve the Pin vs Pout response. The capacitor value is set to provide AC ground. At low frequency, the emitter degeneration resistor increases CMMR.

C. *Transformer*

Single-ended to differential conversion is achieved using 1:1 passive transformer (Fig. 3a). The transformer is implemented with the top two metal layers to minimize the loss. The length and the width of the transmission lines are chosen to match 50 Ω. The 140 GHz transformer has a simulated phase imbalance of 8-12° and amplitude imbalance of 0.3-0.1 dB from 120 to 160 GHz with 0.5 dB loss at 140 GHz. Fig. 4 shows the schematic diagram of the frequency doubler integrated with the 1:1 transformer.

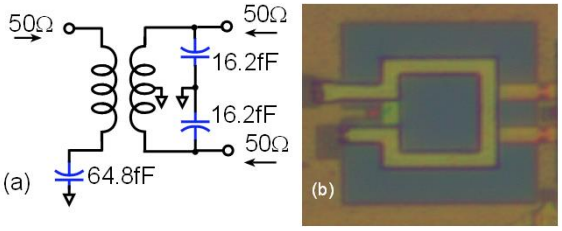

Fig. 3. 140 GHz 1:1 transformer: (a) schematic and (b) die photo.

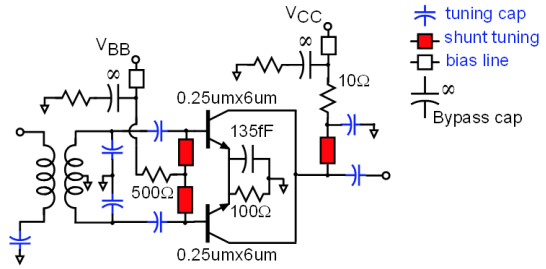

Fig. 4. Schematic diagram of the frequency doubler with 1:1 transformer.

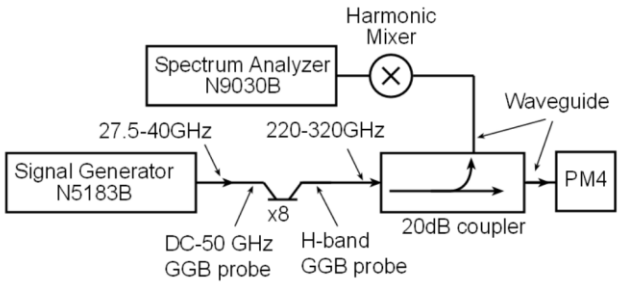

Fig. 5. Power measurement setup.

III. Measurement Results

The measurement is performed on the 3-mil thinned die (Fig 1a). Fig 5 shows the power measurement setup. The output power spectrum is monitored using a 20 dB H-band directional coupler followed by an H-band harmonic mixer (M03HWD) and a spectrum analyzer (N9030B). The through port goes to the Erickson power meter (PM4). The same setup is used in the calibration phase, and the FMC generates the spurious-free tone to calculate the cross-calibration coefficient between the spectrum analyzer and power meter reading. Since broadband FMC is used during the calibration phase, the frequency range of the measurement is not limited by a commercial narrowband power source. To characterize the performance of an FMC, closest spurious harmonics should be measured accurately. The high-order passive harmonic mixer (M03HWD) limits the minimum detectable signal power. Fig 8. shows the noise floor of the measurement setup.

The FMC is biased by DC probes at (V_{CCx8}=2.9V, V_{BBx8}=1.9V, I_{CCx8}=29.8mA, I_{BBx8}=1.2mA). At 280 GHz (Fig 6), the FMC has -0.6 dBm output power with -2 dBm input power and the 7th and 9th harmonics are below the noise floor of the measurement setup. The first measured 7th harmonic power is -31 dBm with -1.2 dBm input power, and the first measured 9th harmonic power is -28.3 dBm with +3.3 dBm input power. Fig 7 shows the measured 8th harmonic power versus input power at various input frequencies. At 280 GHz, the measured 8th harmonic power is -0.8 dBm with 0 dBm input power which is 1.7 dB less than the simulated value. At 300 GHz, measured 8th harmonic power is 3.3 dBm with 0 dBm input power which is 3 dB less than the simulated value. This discrepancy be might due to inaccurate large-signal device modelling at high frequencies.

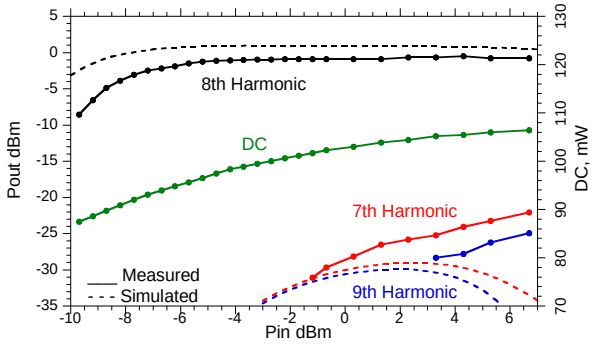

Fig. 6. Measured output power at 8th, 7th and 9th harmonics with 35 GHz input source versus input power.

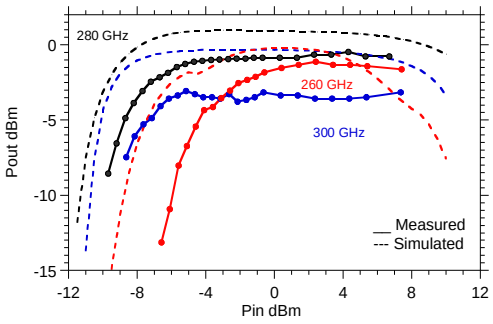

Fig. 7. Measured power at 8th harmonic versus Pin at various frequencies.

Fig 8 shows the measured output power at 7th, 8th and 9th harmonics with different input power levels. When -6 dBm input power is applied, 7th (Fig 9b) and 9th (Fig 9c) harmonics are below the noise floor. Using a H-band fundamental mixer would increase the dynamic range of the measurement set-up. At 280 GHz, the measured 8th harmonic power is -0.6 dBm with 3-dB bandwidth of 48 GHz with -2 dBm input power. When applied input power is increased to +2 dBm, 3-dB bandwidth increases to 60 GHz, the harmonic suppression decreases by 8 dB. Input power can be tuned for high spectral purity or wider operating bandwidth.

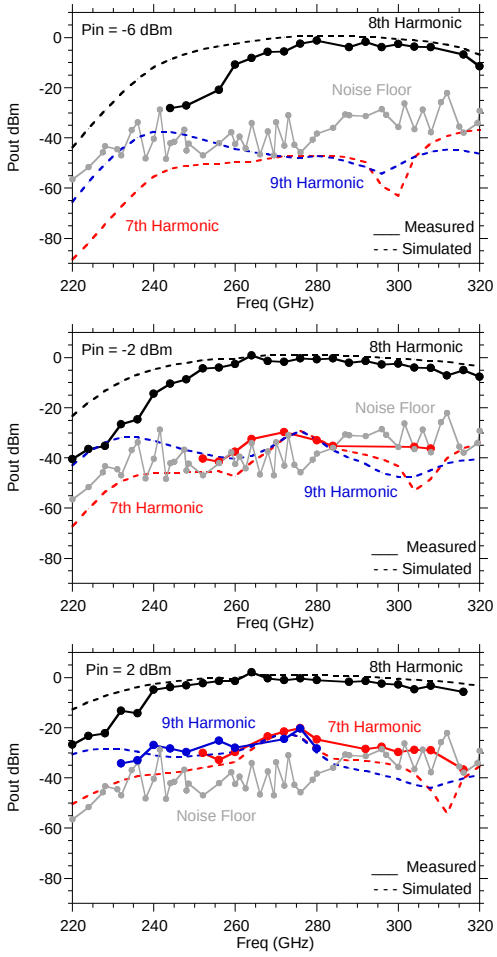

Fig. 8. Measured output power, at 8th, 7th and 9th harmonics with different input power levels vs 8th harmonic frequency.

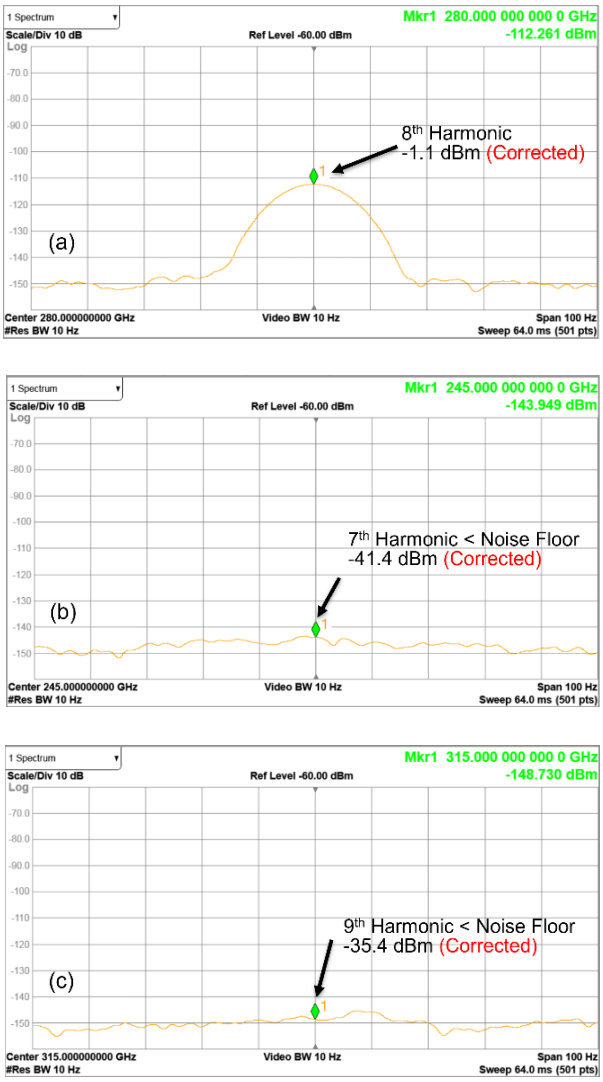

Fig. 9. Frequency multiplier chain output spectrum with -6 dBm input power at 35 GHz. 7th and 9th harmonics are below the noise floor.

IV. Conclusion

In this paper, a broadband 280 GHz x8 frequency multiplier IC with high spectral purity is presented. The FMC generates -0.6 dBm output power with 3-dB bandwidth of 48 GHz. The unwanted harmonics are suppressed by more than 28 dBc over the frequency range of interest with an input power of -2 dBm. The frequency multiplier chain could be integrated with a power amplifier [13] to be used as a high-power source.

Acknowledgment

This work was supported by ComSenTer, a JUMP program sponsored by the Semiconductor Research Corporation. The authors thank Teledyne Scientific & Imaging for the IC fabrication.

Table 1. State-of-the-art H-band frequency multipliers.

Ref	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]	**This work**
Freq, GHz	240	159	244.5	260	252	250	255	300	300	**280**
Multiplication	x18	x6	x8	x8	x4	x6	x16	x3	x8	**x8**
BW_{3dB}, GHz	41	48[c]	81	100	48	45	40	22	127	**48**
P_{out}, dBm	6.2	4.6	-7.7	2.5	5.5	5	-6	2.3	2.3	**-0.6**
P_{DC}, W	429	100	240	-	270	124.8	300	410	537	**112**
Chip Size, mm^2	0.28	0.25	0.86	3.25	0.29[d]	2[d]	0.7	1.85[d]	1[d]	**0.4**
Spurious Harmonic Suppression, dBc	25	13	28	< 10[a]	20	-	30[b]	-	16[b]	**28**
Technology	130-nm SiGe BiCMOS	250-nm InP HBT	130-nm SiGe BiCMOS	GaAs mHEMT	130-nm SiGe BiCMOS	InP HEMT	130-nm SiGe BiCMOS	40 nm CMOS	130-nm SiGe BiCMOS	**250-nm InP HBT**

[a]graphically estimated, [b]simulated, [c]BW_{5dB}, [d]including pads

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