A 280 GHz (x8) Frequency Multiplier Chain in 250 nm InP HBT Technology

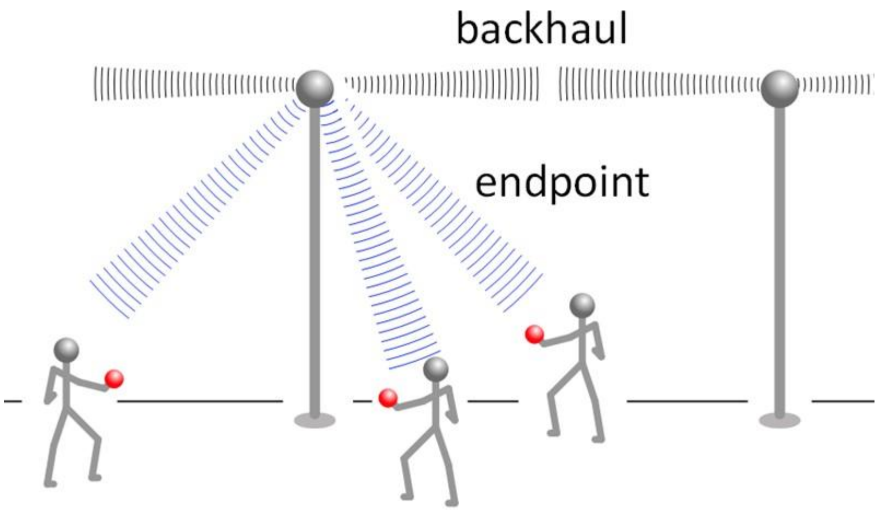
Utku Soylu[1]
Amirreza Alizadeh[1], Munkyo Seo[2], Mark J. W. Rodwell[1]
[1]ECE, University of California, Santa Barbara, USA
[2]ECE, Sungkyunkwan University, South Korea

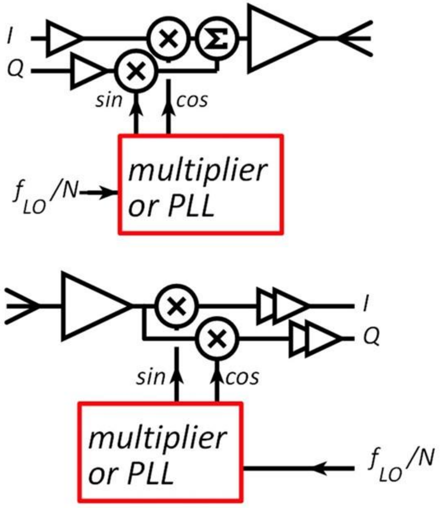
200-300 GHz Wireless Backhaul

Growing demand for wireless communications: endpoint and backhaul

200-300 GHz backhaul: 100+ Gb/s feasible over ~km range.

→ develop 200-300 GHz transceivers





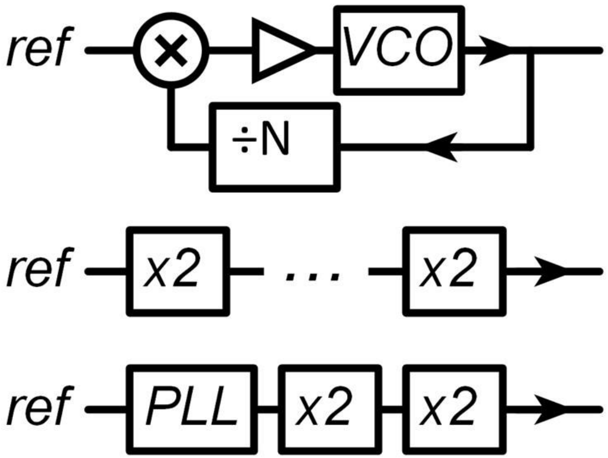
mm-wave LO generation

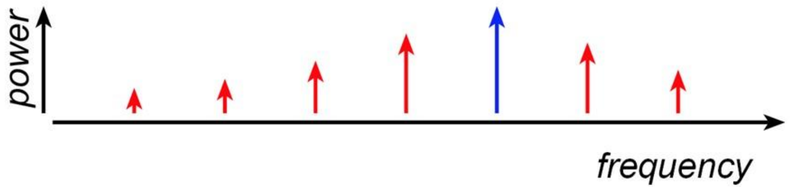
PLLs:

- in-band phase noise: $N^2 \times$ reference (plus additive noise)
- out-of-band phase noise: VCO
- challenge: low-noise mm-wave VCO

Multipliers:

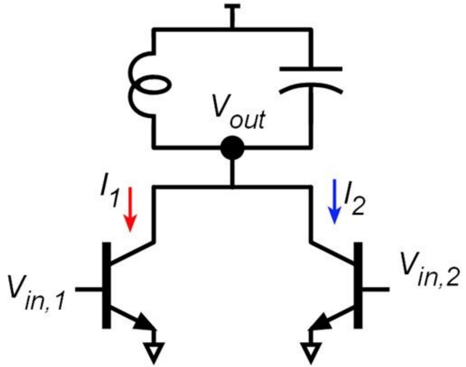
- phase noise: $N^2 \times$ reference (plus additive noise)
- spurious harmonics: out-of-band response

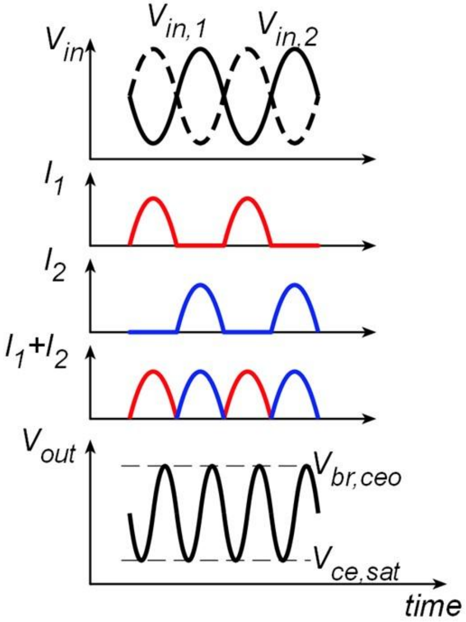


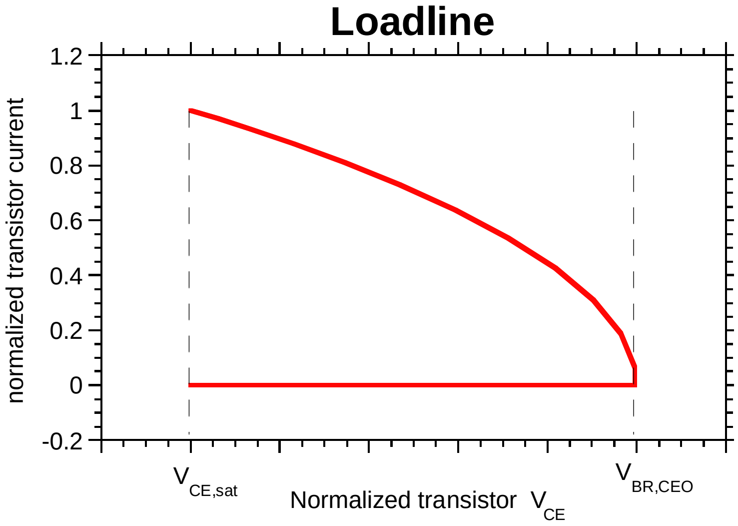


Push-Push Frequency Doubler

Push-push: odd harmonic suppression.
Maximum P_{out} design: voltage swing between $V_{ce,sat}$ and $V_{br,ceo}$.
Here: loadline instead tuned for maximum PAE (smaller V_{max}).



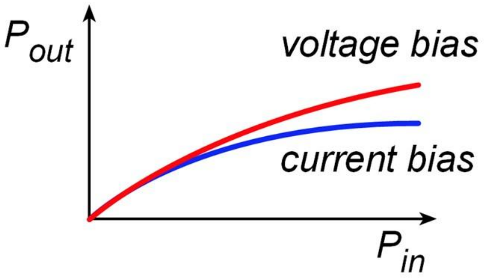


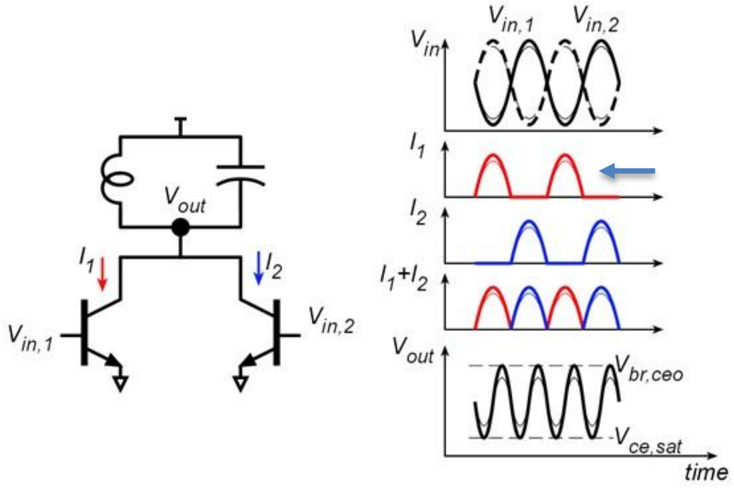


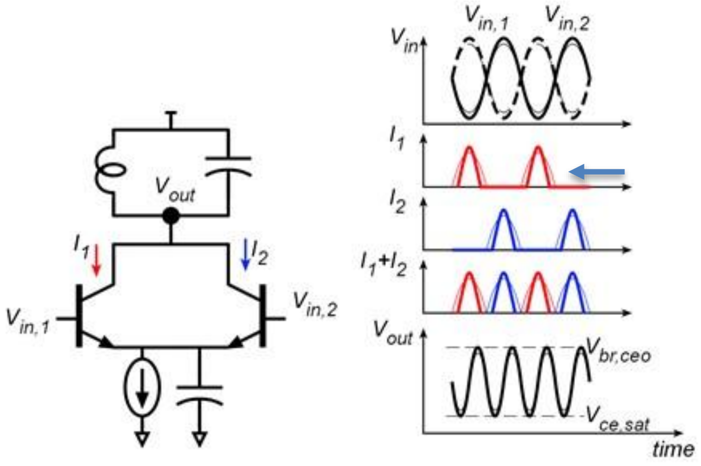
Doubler: Voltage vs. Current Bias

Voltage bias: output current & charge increase with P_{in}.

Current bias: output <u>charge</u> independent of P_{in}.
→ less variation of P_{out} with P_{in}.







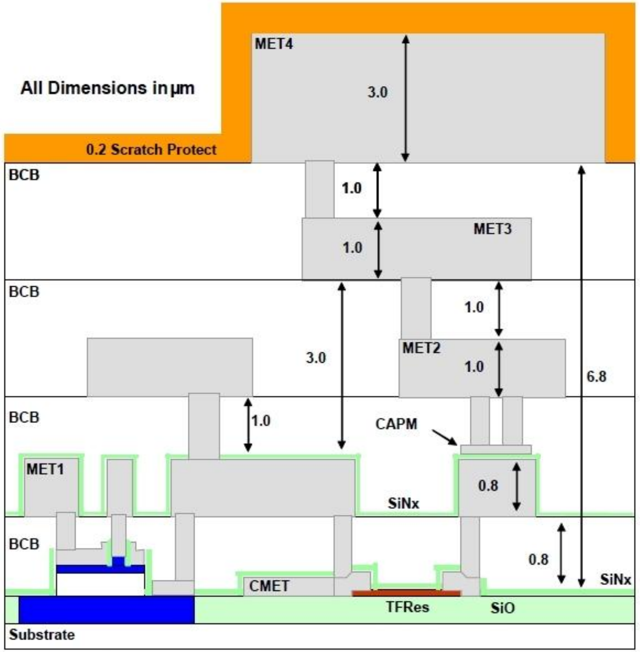
Teledyne 250 nm InP HBT

f_{max} = 650 GHz.
J_{max} = 3 mA/µm.
B_{VCEo}= 4.5 V.

Four interconnect levels

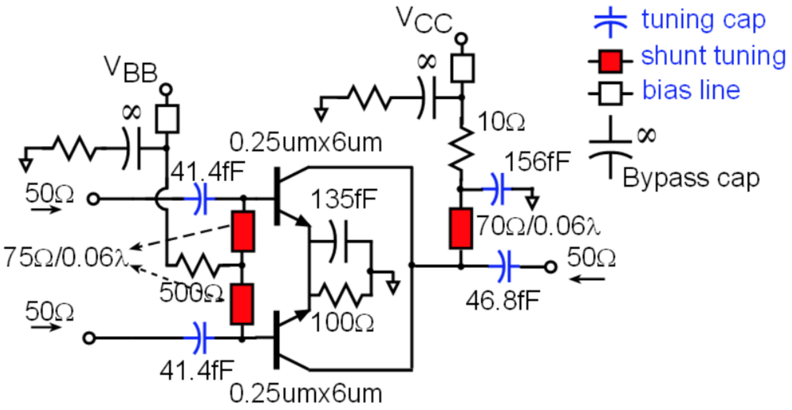
Microstrip lines (M4 signal, M1 ground)
1.0 dB/mm @ 280 GHz

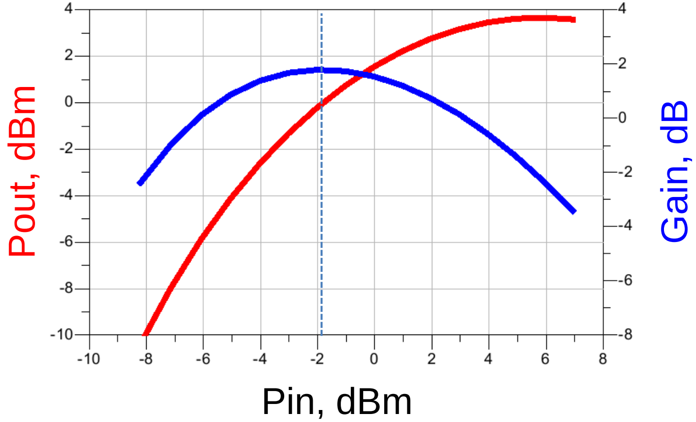
Resistors: 50 Ω/square
MIM capacitors: 0.3 fF/µm^2



Representative cross-section of TSC250 IC technology. Drawing is not to scale.

Doubler Area Scaling/Bias Condition





HBT emitter length set such that P_{out} > P_{in}.

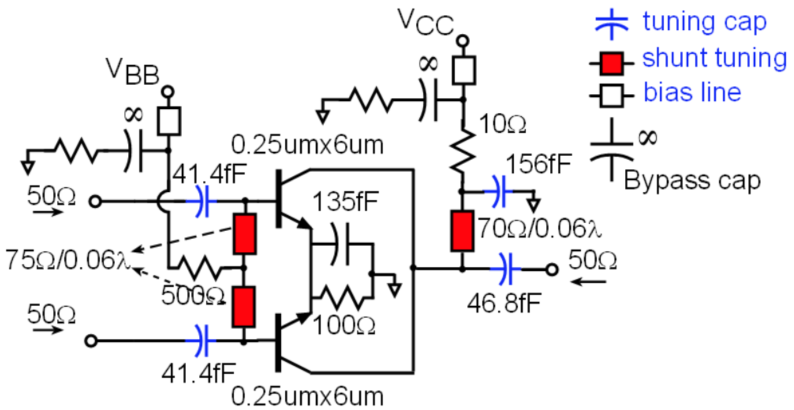
→ Cascaded doublers don't need inter-stage amplifiers .

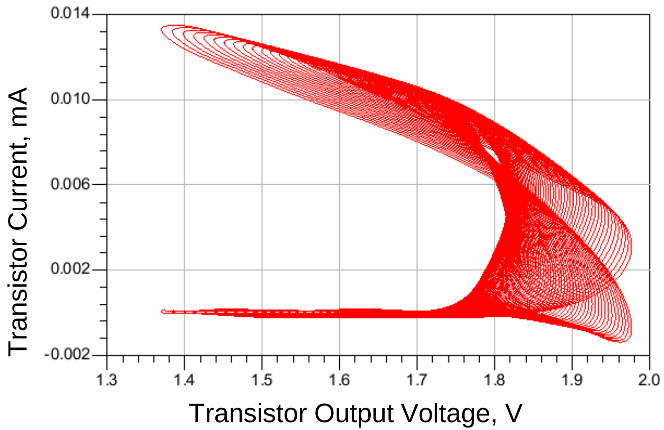
Input/Output Matching

140 GHz input tuning: 50 Ω large-signal match

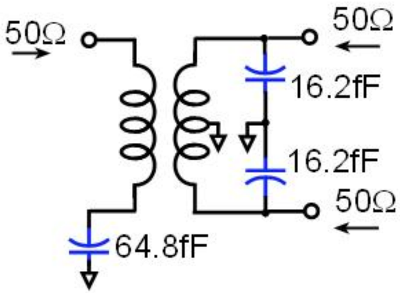
280 GHz output (50 Ω load):
current swing at HBT safe limits (2.3 mA/μm)
voltage swing below HBT (V_{BRCEO}-$V_{CE,sat}$) limits:
less saturated ouput power but greater gain.

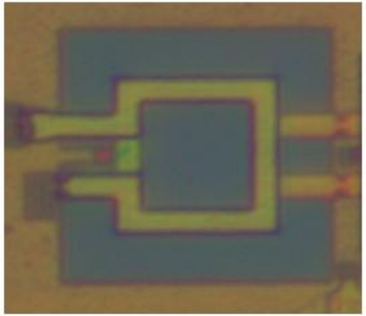
Emitter RC network improves low-frequency common-mode stability.

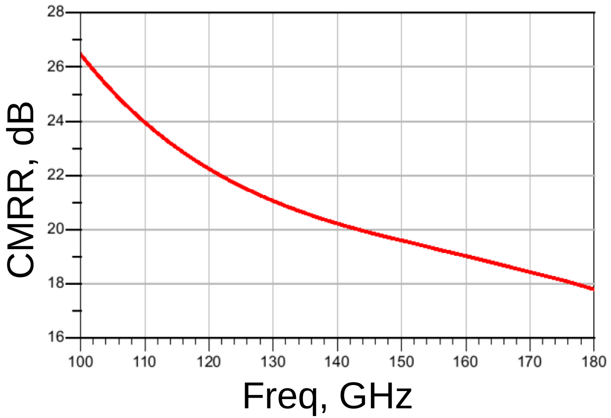




Single-ended to Differential Conversion





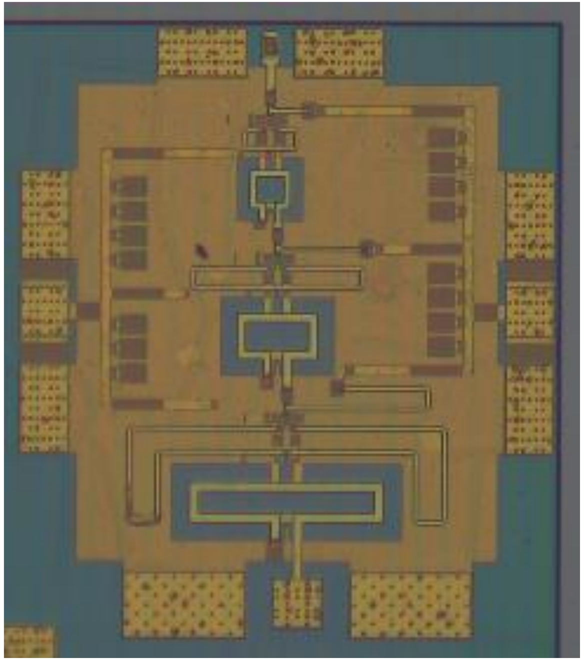


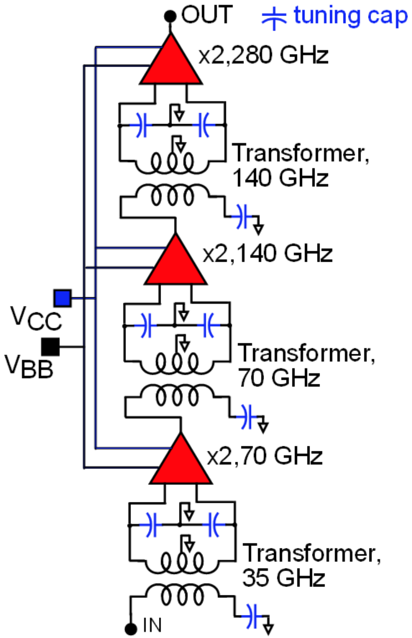
0.5 dB loss at 140 GHz.

Simulated phase imbalance: 10^{o} & Simulated amplitude imbalance: 0.2 dB

Single-ended input to differential output amplifier with high CMRR:
Better spurious harmonic rejection at the expense of DC power consumption.

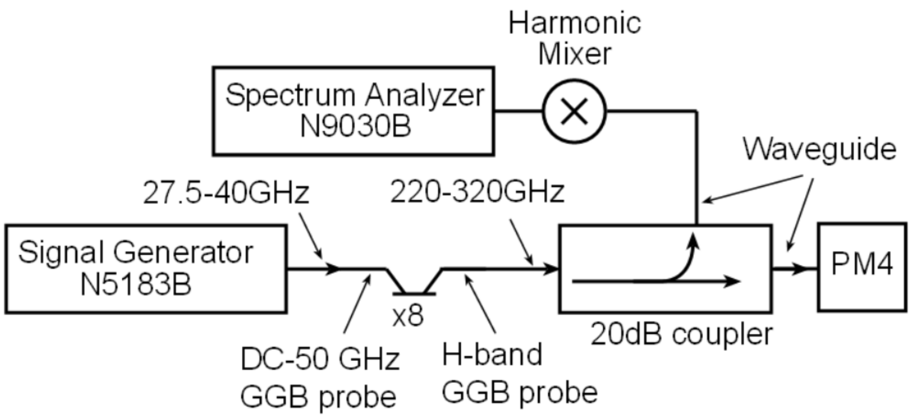
x8 Frequency Multiplier Chain

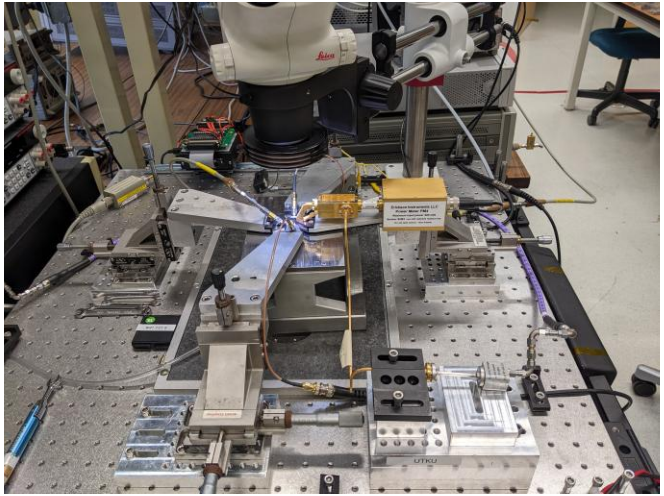




280GHz Pin = -2 dBm	0.25um x 6um, 3 cascaded x2
Multiplication	x8
BW_{3dB}	48 GHz
P_{out}	-0.6 dBm
P_{DC}	112 mW
Die Area	0.4 mm^2
Spurious Harmonic Suppression	**28 dBc**

Power Measurement Setup



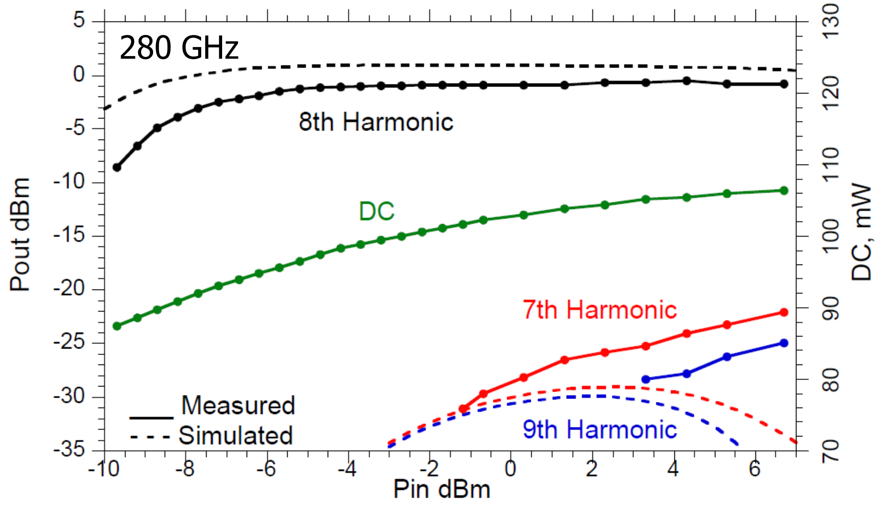


Simultaneous power and spectrum measurement.

Spurious-free tone to calculate cross-calibration coefficient generated by FMC.

High-order passive harmonic mixer limits minimum detectable signal power.

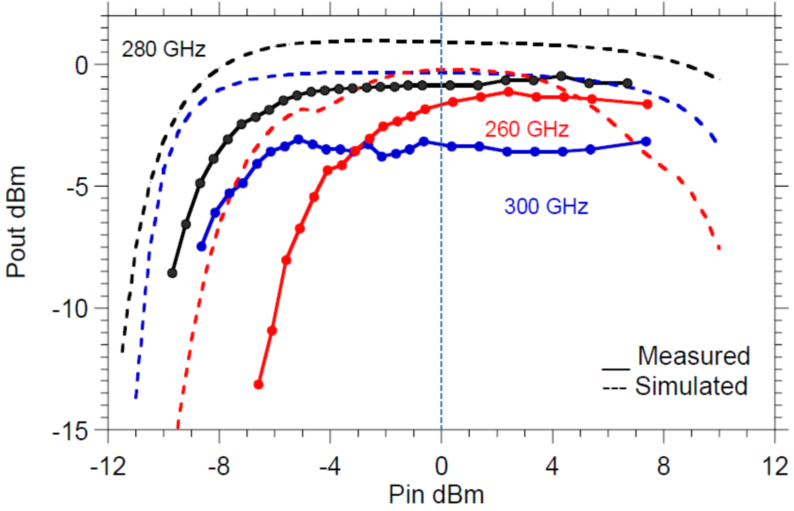
Measurement Results: Pout vs Pin



P_{in} = -1.2 dBm → $P_{out(@7th\ harmonic)}$ = -31 dBm

P_{in} = 3.3 dBm → $P_{out(@9th\ harmonic)}$ = -28.3 dBm

Measurement Results: Pout vs Pin



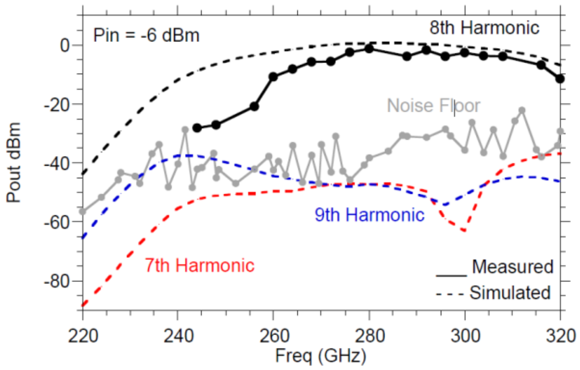
P_{in} = 0 dBm:

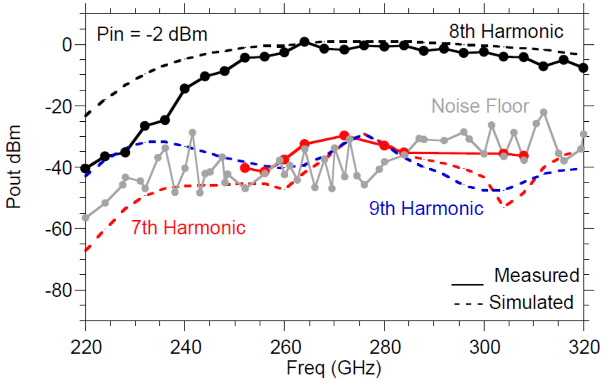
280 GHz: Measured P_{out} : -0.8 dBm, Simulated P_{out} : 0.9 dBm

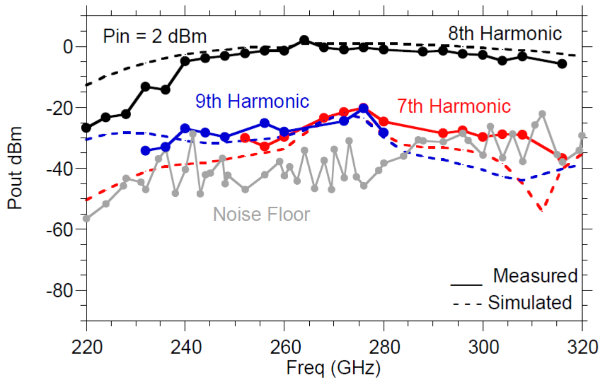
300 GHz: Measured P_{out} : -3.3 dBm, Simulated P_{out} : -0.3 dBm

Inaccurate large-signal device modelling at high frequencies.

Measurement Results: Pout vs freq







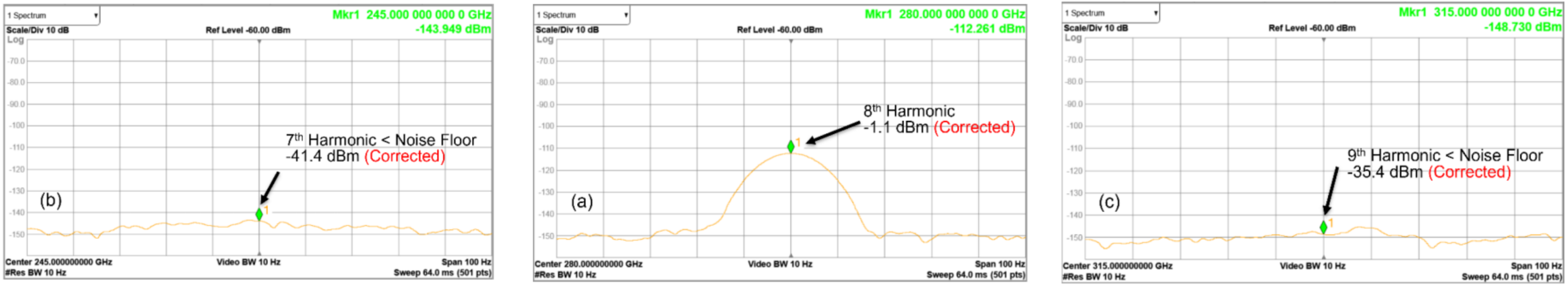
P_{in} = -2 dBm → 2 dBm:

3-dB bandwidth: 48 GHz → 60 GHz.

Harmonic suppression: 28 dBc → 20 dBc

Set P_{in} for high spectral purity or wider operating bandwidth.

Measurement Results: Output Spectrum

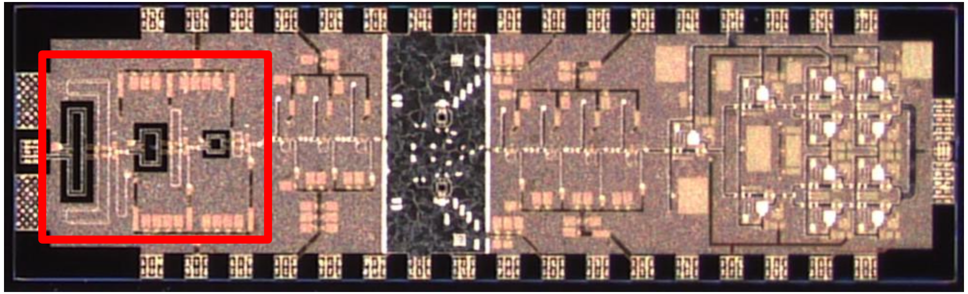


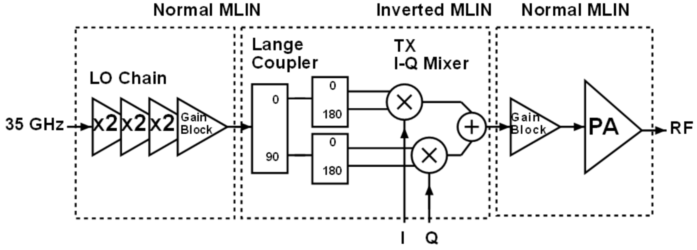
P_{in} = -6 dBm: Spurious harmonics are below the noise floor.

Low order/fundamental mixer → better dynamic range.

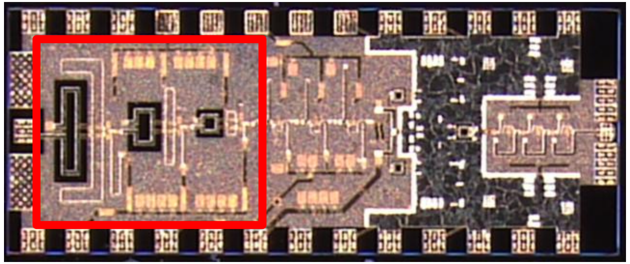
Transmitter/Receiver with x8 FMC

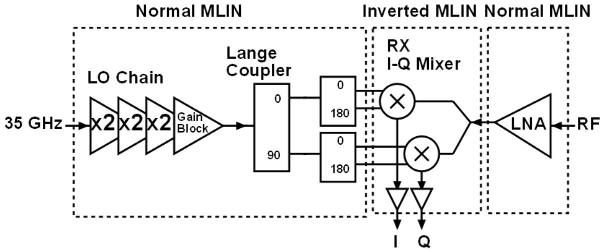
280 GHz direct-conversion TX





280 GHz direct-conversion RX





Performance Comparison

Table 1. State-of-the-art H-band frequency multipliers.

Ref	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]	This work
Freq, GHz	240	159	244.5	260	252	250	255	300	300	**280**
Multiplication	x18	x6	x8	x8	x4	x6	x16	x3	x8	**x8**
BW_{3dB}, GHz	41	48[c]	81	100	48	45	40	22	127	**48**
P_{out}, dBm	6.2	4.6	-7.7	2.5	5.5	5	-6	2.3	2.3	**-0.6**
P_{DC}, mW	429	100	240	-	270	124.8	300	410	537	**112**
Chip Size, mm^2	0.28	0.25	0.86	3.25	0.29[d]	2[d]	0.7	1.85[d]	1[d]	**0.4**
Spurious Harmonic Suppression, dBc	25	13	28	< 10[a]	20	-	30[b]	-	16[b]	**28**
Technology	130-nm SiGe BiCMOS	250-nm InP HBT	130-nm SiGe BiCMOS	GaAs mHEMT	130-nm SiGe BiCMOS	InP HEMT	130-nm SiGe BiCMOS	40 nm CMOS	130-nm SiGe BiCMOS	**250-nm InP HBT**

[a]graphically estimated, [b]simulated, [c]BW_{5dB}, [d]including pads

This work shows **record spectral purity** among H-band frequency multipliers.

Acknowledgement

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THANK YOU

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Power Measurement Setup (Pictures)