D-Band Power Amplifier with 27 dBm Peak Output Power and 14.9% PAE in 250-nm InP HBT Technology

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***Abstract*— We present a *D*-band power amplifier (PA), implemented in Teledyne (TSC)-250-nm InP technology, that produces 27.2 dBm output power and 14.9% associated PAE at 150 GHz. The measured saturated output power exceeds 26 dBm over 126-150 GHz. The output stage power-combines sixteen 24-μm common-base cells, each having capacitive series feedback that increases the real part of the input impedance, reducing inter-stage matching losses. Each power cell is independently biased by an adaptive bias network that prevents thermal runaway and increases bias currents with increased RF power to maintain nearly constant gain. The IC consumes 3 mm^2.**

***Keywords*— Adaptive bias network, analog pre-distortion, *D*-band, InP HBT, power Amplifiers, thermal compensation.**

I. Introduction

6G wireless systems may provide up to 100 Gbs user data rates, enabling new mobile applications [1], [2]. 100–300-GHz links can provide very high capacity [3] because of the wide spectrum and because short wavelengths readily support massive MIMO. Given high atmospheric attenuation and high λ^2/R^2 path losses, such links require either highly directional antennas or arrays having many elements. If the transmitter RF power is increased, fewer array elements are needed for a given range. Power amplifiers (PAs) will thus be key blocks in 6G links, with their output power determining range, and their efficiency determining power consumption.

In *D*-band (110–170 GHz), CMOS and SiGe offer superior integration capability [6], [7], but have limited output power and efficiency due to low breakdown voltages. GaN HEMTs offer superior power density below 100 GHz, but their efficiency drops above 100-GHz [8], [9]. InP transistors provide moderately output power and high efficiency due to their high $f_{\max}$ and moderate breakdown voltage ($V_{\mathrm{BR,CEO}}$).

Here, we present (Fig. 1) a half-watt PA in Teledyne 250-nm InP HBT process, wich has $V_{\mathrm{BR,CEO}} = 4.5$ V [4] and 650 GHz $f_{\max}$ when the reference plane is at top metal layer. Adaptive bias networks (ABNs) operate the transistors in deep class-AB. The PA produces 27.2 dBm output power and 14.9% associated PAE at 150 GHz. The measured saturated output power exceeds 26 dBm over 126-150 GHz. To the authors' knowledge, this is the highest reported output power for *D*-band PAs in any technology.

II. Circuit Design

In class-A amplifiers the collector bias current is independent of the output power. This can be achieved by providing e.g., a fixed base bias current through a large bias resistance. In an ideal class-B amplifier, the time-average collector current is proportional to the RMS RF output current, and hence proportional to the square root of the output power. Either an ABN must adjust the bias current as a function of RF power, or the base-emitter must be biased just above the cutoff voltage. Fixed-V_{BE} bias is prone to electrothermal instability, which leads to transistor destruction. Class-AB designs require a variation of collector current with RF power intermediate between class-A and class-B.

In the presented ABN (Fig. 2), the RF transistor Q_1, with C_3 and C_{cb3} providing series RF feedback, is biased by a current mirror (Q_2, R_1, R_2, and diode-connected transistors Q_3 and Q_4). Common-base topology is preferred over common-emitter due to its higher maximum available gain ($G_{\max}$) at *D*-band. Variation in the reference current (I_{ref}) from thermal variations in V_{BE3} and V_{BE4} is negligible if the

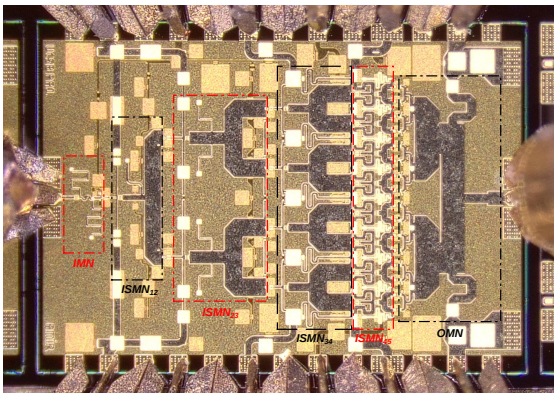

Fig. 1. Photograph of the 5-stage power amplifier. The rectangles identify interstage matching networks. The die is 2 mm by 1.5 mm.

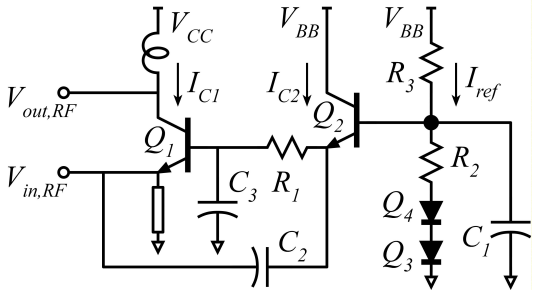

Fig. 2. *D*-band power-transistor gain cell with adaptive dc bias. Q_1 is the RF transistor with C_3 providing base capacitive series feedback, while Q_3 and Q_4 are diode-connected transistors. Impedance matching networks are not shown.

dc voltage across R_3 is large. Assuming $I_c = I_s \exp(V_{be}/V_t)$ for all transistors, with $V_t = nkT/q$, given no RF drive,

$$\left[\frac{nkT}{q}\right] \ln\left[\frac{I_{C1}^2 I_{S3} I_{S4}}{\beta I_{ref}^2 I_{S1} I_{S2}}\right] = I_{ref} R_2 - \frac{1}{\beta} I_{C1} R_1. \qquad (1)$$

Setting $I_{S1}/\gamma = I_{S2} = I_{S3} = I_{S4}$, where $\gamma = I_{C1}^2/\beta I_{ref}^2$, gives $I_{C1}/I_{ref} = \beta R_2/R_1$, a temperature-independent design.

An ideal diode, biased at a constant dc current and driven by an RF voltage $v_p \cos(\omega t)$ generates a dc bias voltage shift of $\delta V_{diode} \approx -v_p^2/4V_t$ to leading order. In the ABN of Fig. 2, unlike [5], both the RF transistor Q_1 and the reference transistor Q_2 are driven by the RF voltage, and both produce $\delta V_{BE} \approx -v_p^2/4V_t$ shifts upon RF drive. Neglecting transistor RF parasitics, I_{C1} varies approximately as

$$I_{C1} \approx I_{ref} \frac{\beta R_2}{R_1} + \frac{2(v_p^2/4V_t)}{R_1/\beta + 2V_t/I_{C1}}. \qquad (2)$$

I_{C1} has a fixed component and a component varying in proportion to the RF power. Given that $R_1/\beta >> 2V_t/I_{C1}$, reducing R_1 increases the rate of variation of I_{C1} with RF power. If C_2 was removed so that only Q_1 produced RF rectification, R_1 would have to be 2:1 smaller for given desired variation of I_{C1}. This is important for electrothermal design.

The ABN of Fig. 2 will be stable against electrothermal runaway if $\beta_T < 1$, where

$$\beta_T \approx \left(\frac{-\partial V_{BE}}{\partial T}\right)\left(\frac{V_{CE1}\theta_{ja1}}{R_1/\beta + R_{E1} + 2V_t/I_{C1}}\right), \qquad (3)$$

$\partial V_{BE}/\partial T = -1.8\,\text{mV/K}$, $V_{CE1} = 2.5\,\text{V}$, $R_{E1} \approx 1\,\Omega$ is the parasitic emitter resistance of Q_1, and $\theta_{ja} \approx 2.33\,\text{K/mW}$ is the thermal resistance of Q_1. Electrothermal stability is poorest when I_{C1} is large (high P_{out}) hence when V_T/I_{C1} is negligible. Therefore, for $\beta \approx 24$ of the HBT transistors in the technology, (3) stipulates $R_1 > 39\,\Omega$ to avoid thermal runaway. Increasing R_1 would provide larger margin for process variations, but would reduce the variation of I_{C1} below that desired. The design uses $R_1 = 75\,\Omega$, giving $\beta_{T\text{-min}} \approx 0.6$ and $R_2 = 53\,\Omega$.

In the designed PA, a class-AB biased 24-μm (4×6 μm) transistor is used as the RF device (Q_1 in Fig. 2), and it provides about 17 dBm output power and 35% power added efficiency (PAE) at 150 GHz. Fig. 3 compares simulated P_{out}, gain, and PAE of a 24-μm common-base transistor biased with ABN, to a design where the transistor base is dc-biased with a fixed resistor such that the two designs operate with the same I_{C1} at a P_{out} level corresponding to 1 dB gain compression of the design with ABN. The two designs, using the same capacitive series feedback (C_3), show similar peak PAE and P_{out} at the peak PAE, but the design with ABN shows smaller gain variation, with only 0.5 dB gain compression at peak PAE.

Fig. 4 shows the IC block diagram, where the 5th (output), 4th, 3rd, 2nd, and 1st stages employ 16, 8, 4, 2, and 1 transistors. The output stage transistors have 24-μm (4×6-μm) emitter periphery; all others have 32-μm (4×8-μm). Each four-finger transistor operates in common-base with capacitive feedback. This series feedback increases $\Re\{Z_{in}\}$, reducing input matching losses, and provides significant

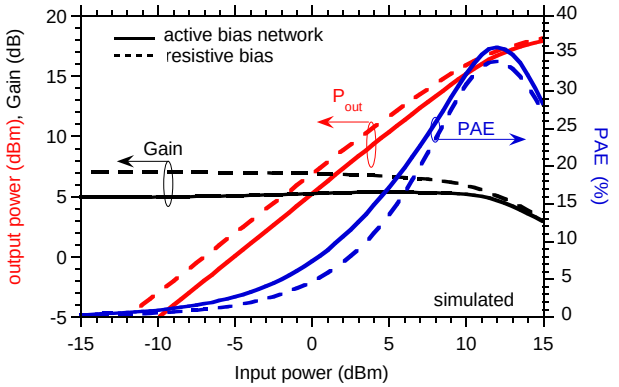

Fig. 3. Simulated P_{out}, gain, and PAE of a 24-μm transistor in the common-base topology when the base node is biased using: a) the ABN of Fig. 2, and b) a fixed 100-Ω resistor.

cascade power-combining [12], with about 25% of P_{out} being produced by the driver (4th) and preceding stages. To prevent electrothermal instability, each four-finger transistor is biased by a separate ABN. Each ABN was adjusted to tailor the overall P_{out}-vs.-P_{in} characteristics of the 5-stage amplifier.

The output and four interstage matching networks (ISMNs) load each transistor with its optimum large-signal load impedance (Z_{LP}), which is determined by load-pull (LP) simulations when the transistor is matched to conjugate of its input impedance (Z_{in}). The input matching network (IMN) and ISMNs should preset $Z_{in}^{\star}$ to each transistor. The IMN at its input port is matched to 50 Ω. MN design in its general form is a passive filter-design problem, where each MN, when terminated to Z_{in} and $Z_{LP}^{\star}$ at its input and output ports, should provide better than 15 dB return losses while minimizing the insertion loss. All passive structures were EM-simulated using FEM engine in Keysight ADS and their layout drawings were optimized in multiple steps to compensate for the coupling effects and phase difference between different paths.

The foundry transistor model includes interconnect parasitics up to the M1 layer. Interconnects between the four 6-μm or 8-μm fingers in each 4-finger transistor were also EM-simulated to characterize their parasitic effect. M1, the micro-strip line ground plane, is also used for transistor contacts, hence a hole must be made in the M1 ground plane for every RF and dc-bias transistor. This complicates design of microstrip lines as the holes, if carelessly placed, produce discontinuities in ground current return paths. These issues were carefully modeled in EM-simulations, and the layout appropriately adjusted.

III. Measurements

The die was bonded to a copper heat sink using a material with 29 W/(m.K) thermal conductivity. Fig. 5 shows the *S*-parameters of the PA, where there is a close agreement between the measured and simulated data. For $V_{CC} = 2.4\,\text{V}$, the 3-dB bandwidth is 43.6 GHz (118.8–162.4 GHz), showing a fractional BW of 31% around 140.6 GHz. For the same collector current, the measured S_{21} at 140 GHz is 1 dB lower

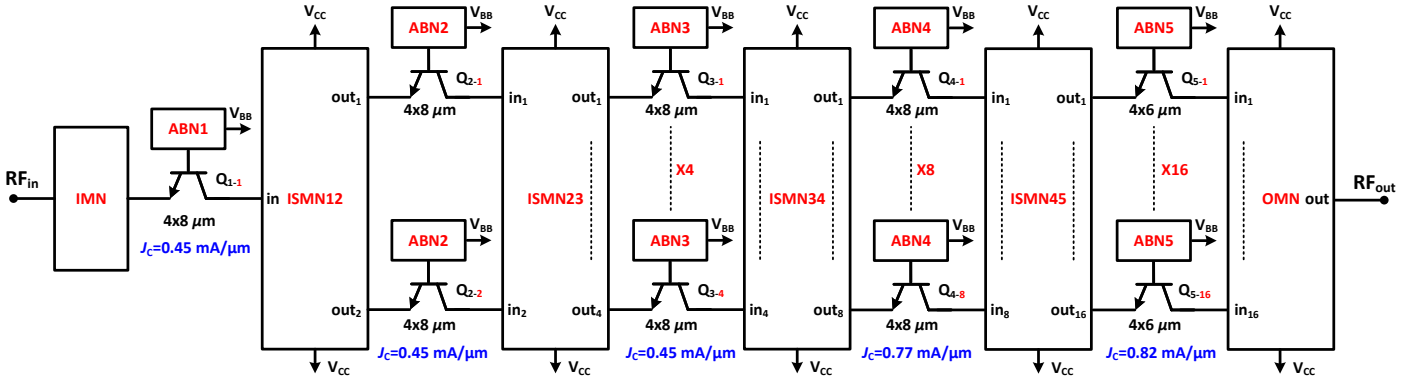

Fig. 4. Architecture of the the *D*-band half-watt PA. The third, fourth, and fifth stages employ 4, 8, and 16 transistors in parallel. The supply voltage is 2.6 V.

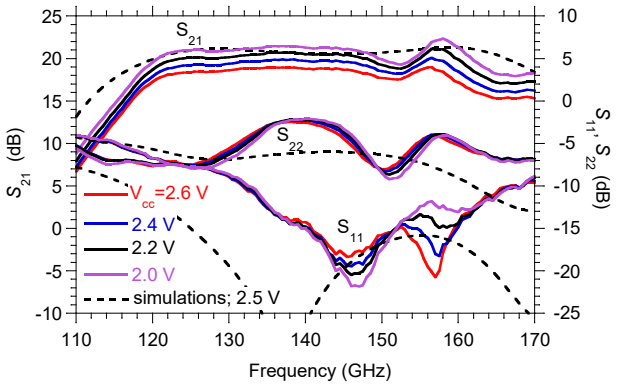

Fig. 5. Power amplifier small-signal *S*-parameters.

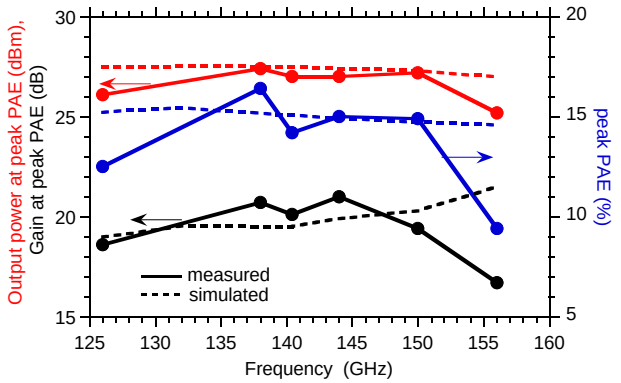

Fig. 6. Maximum PAE, with the associated gain and P_{out} vs. frequency.

than its simulated counterpart. This can be due to heating, calibration errors, or the modeling and simulation inaccuracies.

For power measurements, a synthesizer and 12:1 frequency multiplier (VDI AMC-333) generated the input signal, which passed through a directional coupler and a 140-220 GHz GGB wafer probe, whose waveguide cutoff is 116 GHz. The coupler -20 dB port, connected to a harmonic mixer and spectrum analyzer, monitored the input power; before IC testing, this P_{in} monitor was calibrated against a VDI/Erickson power-meter. The IC output was contacted using a second, identical probe.

Connecting the meter directly to the output probe overloads the meter (200 mW limit). As a high-power attenuator, a 40-cm waveguide was placed between the output probe and the power-meter after first measuring its loss. Six measurements of the waveguide loss showed 0.33 dB reproducibility (σ). Probe loss (3.07, 2.85, 3.02, 2.51, 2.24, and 2.51 dB per probe at 126, 138, 140.4, 144, 150, and 156 GHz) was estimated by measuring the attenuation of the two probes connected by a 100 μm CPW line (0.08 dB simulated loss). The probe loss measurement reproducibility σ was < 0.07 dB. Because the 2.24 dB probe loss correction at 150 GHz is smaller than at other measurement frequencies, we subsequently focus on 150 GHz power and PAE measurements. All on-wafer *D*-band power measurements without vector-corrected calibration have $\sigma \approx 1$ dB uncertainty in measurement of P_{out}; in this high-power measurement, the output attenuator correction introduces an additional 0.33 dB reproducibility (σ).

Fig. 6 depicts the maximum PAE versus frequency, together with the associated gain and P_{out}, while Fig. 7 shows the simulated and measured PAE, P_{out}, and gain versus P_{in} at 150 GHz. The peak saturated output power is 27.3 dBm with 14.6% associated PAE, while the peak PAE is 14.9% with 27.2 dBm associated output power. The measured saturated output power exceeds 26 dBm over 126-150 GHz. The measured collector bias currents (Fig. 8) at 138 GHz show the expected linear variation with P_{out}; the disparity between simulation and measurement may be from model errors or process variations.

Table 1 compares the present and prior results for *D*-band PAs. The IC here reported establishes new records, in any technology, for P_{out}, gain variation with output power, efficiency at 1 dB gain compression, and power density.

IV. Conclusion

A 5-stage *D*-band PA, in a 250-nm InP HBT technology, operating on a 2.6 V supply, with peak 27.2 dBm output power and 14.9% associated PAE is presented. The measured saturated output power exceeds 26 dBm over 126-150 GHz. Multiple transistors are power combined at each PA stage to increase the output power, where all active cells employ a common-base topology with capacitive base degeneration. Each transistor is biased using an adaptive bias network, which

Table 1. Summary of the state-of-the-art integrated PAs with >100-mW saturated output power at *D*-band.

Reference[◇]	Technology	V_{DD} (V)	P_{out} (dBm)	PAE (%)	Gain[†] (dB)	Freq. (GHz)	BW (%)	A (mm^2)	$P_{den}^{‡}$ (W/mm^2)
MWCL-2021 [6]	SiGe HBT 90-nm	3.25/4	17.6-21.9	4.9-12	12	110-145	27.4	1.7	0.09
ISSCC-2022 [7]	SiGe HBT 130-nm	4	22-22.7	16-18.7	15-16	107-135	23.1	1.11	0.17
TMTT-2019 [8]	GaN HEMT 100-nm	15	21-26.4	3-11.5	21-26.4	110-140	24	7.5	0.06
EuMIC-2022 [9]	GaN HEMT 40-nm	12	23.5	7.9	6	136	NA	4.25	0.05
IMS-2019 [10]	InP HBT 250-nm	2.5	23.2-24	5.8-7	14-16	110-150	30.8	1.89	0.13
IMS-2019 [10]	InP HBT 250-nm	2.5	20.3-21.3	6.8-8.9	13-15	55-135	84.2	1.19	0.12
MWCL-2019 [11]	InP HBT 250-nm	2.5	21-21.8	8.2-10.5	15-17.5	115-150	26.4	0.75	0.2
IMS-2020 [12]	InP HBT 250-nm	2.5	18.9-20.5	14.3-20.8	12.3-15.9	125-150	18.2	0.69	0.16
EuMIC-2021 [13]	InP HBT 250-nm	2.5	22.3-23	15-17.8	13-16.5	127-151	17.3	1.34	0.15
MWCL-2022 [14]	InP HBT 250-nm	2.5	20.2-21	12.5-16.2	16-18	150-180	18.2	0.77	0.16
This Work	InP HBT 250-nm	2.6	26-27.4	13-16.4	19-21	126-152	18.7	3	0.18

[◇]Spec values for other works were extracted from their text or otherwise estimated from the the plots. [†]Gain at power saturation. [‡]Power density.

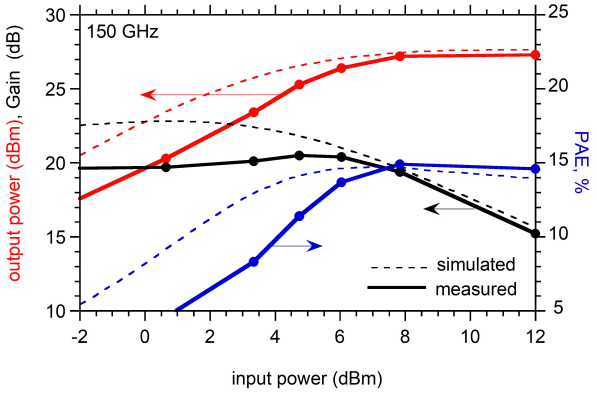

Fig. 7. Simulated and measured PAE, P_{out}, and gain of the PA versus P_{in} at 150 GHz.

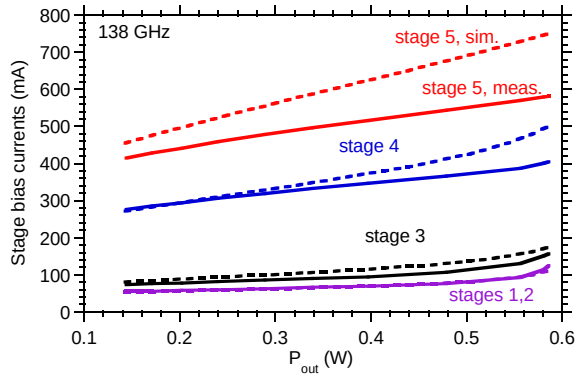

Fig. 8. Measured and simulated collector current of each PA stage versus P_{out} at 138 GHz.

adjusts the bias point based on the input RF power. The ABN also acts as an analog pre-distorter and engineers the P_{in}–P_{out} curve. The PA occupies 2×1.5 mm^2 die area, including pads, and consumes 3.47 W dc power at peak PAE.

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