Self-Aligned InGaAs Channel MOS-HEMTs for High Frequency Applications

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Overview

A gate to link self-aligned, L_g = 20 nm, $In_{0.80}Ga_{0.20}As$ MOS-HEMT exhibiting f_t = 525 GHz and f_{max} = 709 GHz at V_{DS} = 1.00 V, V_{GS} = 0.20 V, and I_{DS} = 0.624 mA/μm is reported. Also, a self-aligned, L_g = 36 nm, $In_{0.80}Ga_{0.20}As$ MOS-HEMT exhibiting f_t = 479 GHz and f_{max} > 1 THz, at V_{DS} = 0.9 V, V_{GS} = 0.20 V, and I_{DS} = 0.528 mA/μm is reported. f_t = 525 GHz and f_{max} exceeding 1 THz are both the highest report for III-V MOSFETs. The typical T-gate formation via bilayer resist is replaced with a V-gate via a regrown, sacrificial InP support that is later etched in dilute HCl, and the traditional thick topside modulation doped link is replaced by a thin $Si:In_{0.53}Ga_{0.47}As$ (4.0 x 10^{19} cm^{-3}) layer. An $Al_xO_yN_z$ / ZrO_2 high-k gate dielectric is used with a 6.0 nm $In_{0.80}Ga_{0.20}As$ channel. At 16 nm L_g, low $g_{ds,e}$ = 0.13 mS/μm at V_{DS} = 1.00 V, V_{GS} = 0.20 V was achieved. At L_g = 1000 nm, V_{DS} = 0.10 V, SS_{min} = 82 mV/dec is observed. High frequency performance of the present device is limited by $g_{m,e}$ < 2 mS/μm.

Device Fabrication

The starting epitaxial structure was purchased from Intelligent Epitaxy. From substrate to air the grown layers are: 100 nm UID-$In_{0.52}Al_{0.48}As$ buffer, 3 nm modulation doped $Si:In_{0.52}Al_{0.48}As$ (1.2 x 10^{19} cm^{-3}), 3 nm UID-$In_{0.52}Al_{0.48}As$ spacer, 7 nm strained UID-$In_{0.80}Ga_{0.20}As$ channel, 3 nm $Si:In_{0.53}Ga_{0.47}As$ (4.0 x 10^{19} cm^{-3}) topside doping, 3 nm UID-$In_{0.53}Ga_{0.47}As$ cap. After alignment marks, a HSQ "dummy link" hard mask was defined using E-Beam lithography, and 50 nm of $Si:In_{0.53}Ga_{0.47}As$ (4.0 x 10^{19} cm^{-3}) was grown. Next a HSQ "dummy gate" hard mask was defined, and a 5 nm UID-$In_{0.53}Ga_{0.47}As$ etch stop layer and an 80 nm UID-InP sacrificial layer were grown similar to Egard *et al.* [1]. The double regrowth definition is novel in that the order is reversed, and gates are written in the 001 direction instead of the $0\bar{1}1$ and $0\bar{1}\bar{1}$ directions to maximize the undercut etch rate of the InP [2].

After regrowths, the cap and doped layers of the link are digitally etched through before the bi-layer high-k is deposited using 9 cycles of $Al_xO_yN_z$ (0.83 nm) and 30 cycles of ZrO_2 (1.71 nm). The gate is defined using EBL and 30 nm Ni / 300 nm Au are deposited. A 30 nm SiN PECVD deposition followed by a vertical CF4/O2 dry etch sidewalls the gate prior to the InP sacrificial removal. The InP layer is then removed in a 2-minute dilute HCl etch. After the mesas are defined by wet etching, ohmics (Pd/Ti/Pt/Au 9/15/15/100 nm) are E-beam evaporated. 30 cycles of ZrO_2 (1.71 nm) passivation are then followed by wet etched vias and pad metal (Ti/Au 20/500 nm) E-beam evaporation. The device fabrication flow can be seen in **fig. 1** and TEMs of an 18 nm gate length device can be seen in **fig. 2**.

Results

RF testing follows [2]. Output characteristics can be seen in **fig. 3**. f_τ, f_{max} are determined by fitting the -20 dB/dec roll off of current gain H21 and unilateral power gain U from 22-66 GHz and 40-67 GHz respectively. H_{21} and U fit for a L_g = 20 nm and a L_g = 36 nm device are shown in **fig. 4a** and **fig 4b**. Open-Short de-embedding is the most common way to extract FOM in academia, but as we reach higher f_{max}, it would be advantageous to adopt TRL calibrations and move to higher frequency measurements to validate these results [3]. The 20 nm gate length small signal equivalent circuit model used to fit the measured S-parameters can be seen in **fig. 5a**, and the measured and modeled S-parameters can be seen in **fig. 5b**.

A gate length series of equivalent circuit parameters via automated fitting are seen in **fig. 6** [4]. $C_{GS,end}$ < 0.40 fF/μm and $C_{GD,end}$ < 0.10 fF/μm is a large improvement on previous MOS-HEMTs [2]. $g_{m,e} \leq$ 2 mS/μm is worse than state of the art most likely due to lower strain in the channel [2,5,6]. Low $g_{ds,e}$ = 0.13 mS/μm was demonstrated even at gate lengths down to 16 nm. f_τ is greater than 500 GHz for devices 26 nm and shorter.

Conclusions

Improved C_{GS} and C_{GD} were accomplished by thinning the link and switching to a self-aligned process. The inclusion of the high-k gate dielectric improved electrostatics and therefore, $g_{ds,e}$ is approximately 46% lower than published state of the art HEMT technology [6]. High frequency performance was limited by lower $g_{m,e} \leq$ 2 mS/μm due to worse epi design. Significant improvement in high frequency performance could be achieved if the self-aligned process were run with high performance epi.

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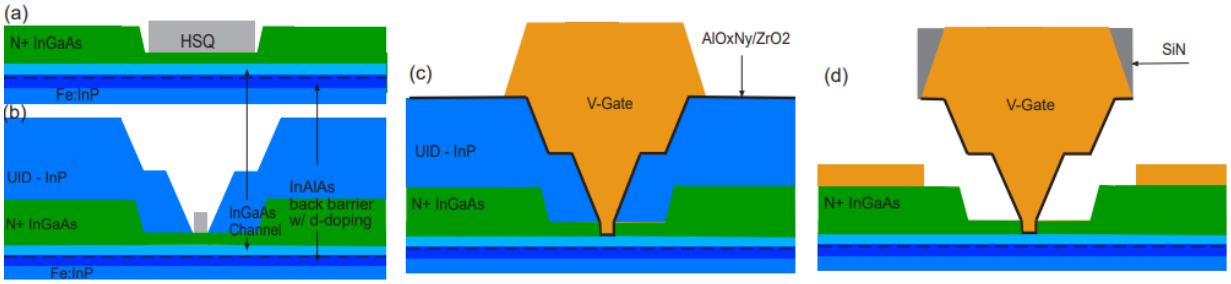

Fig. 1: process flow (a) Epi, dummy link, contact regrowth (b) dummy gate, sacrificial regrowth (c) etch N+ link, high-k deposition, gate metal deposition (d) high-k etch, SiN sidewall, InP removal, ohmic contact deposition

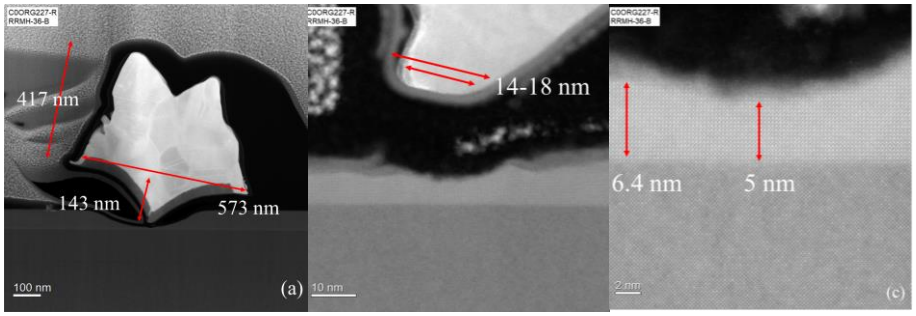

Fig. 2: 18 nm Lg TEM cross section. Note: the gate was dislodged from channel during FIB.
(a) full device
(b) gate length
(c) channel thickness

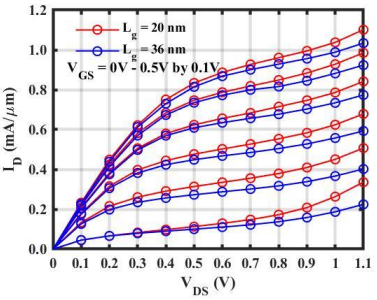

Fig. 3: 20 & 36 nm L_g I_D vs V_{DS}

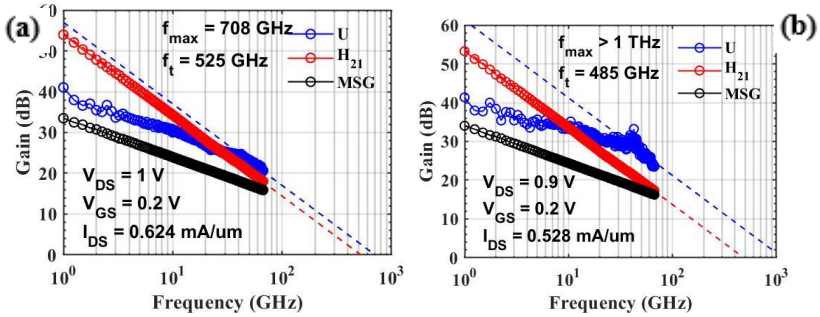

Fig. 4. High frequency FOM extraction at (a) Lg = 20nm (b) Lg = 36 nm

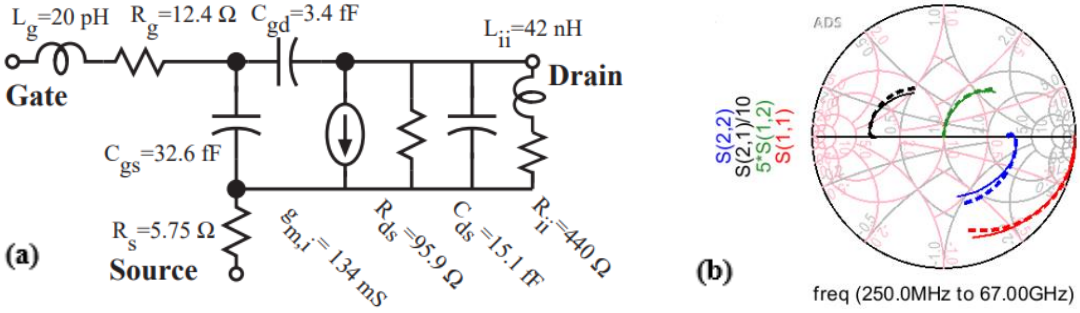

Fig. 5 20 nm Lg (a) equivalent circuit (b) measured / modeled S-parameters

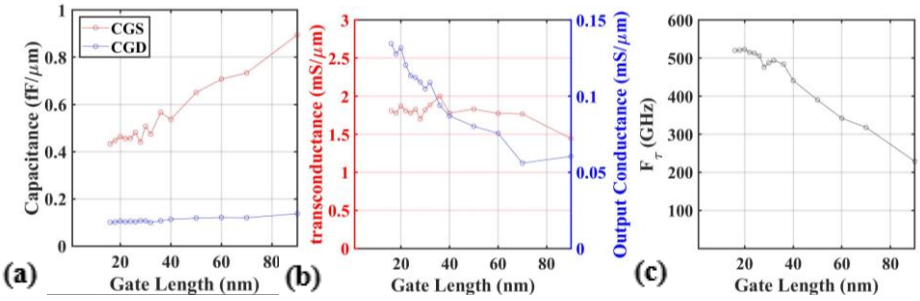

Fig. 6: Gate length series of extracted common-source SSEC elements.
(a) C_{GS}, C_{GD}
(b) $g_{m,e}$, $g_{ds,e}$
(c) $f\tau$