



UNIVERSITY OF CALIFORNIA SANTA BARBARA
ELECTRICAL AND COMPUTER ENGINEERING

Self-Aligned InGaAs Channel MOS-HEMTs for High Frequency Applications

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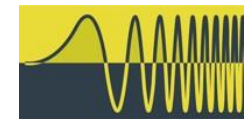
Advisor: Prof. Mark Rodwell

Funding: SRC & DARPA



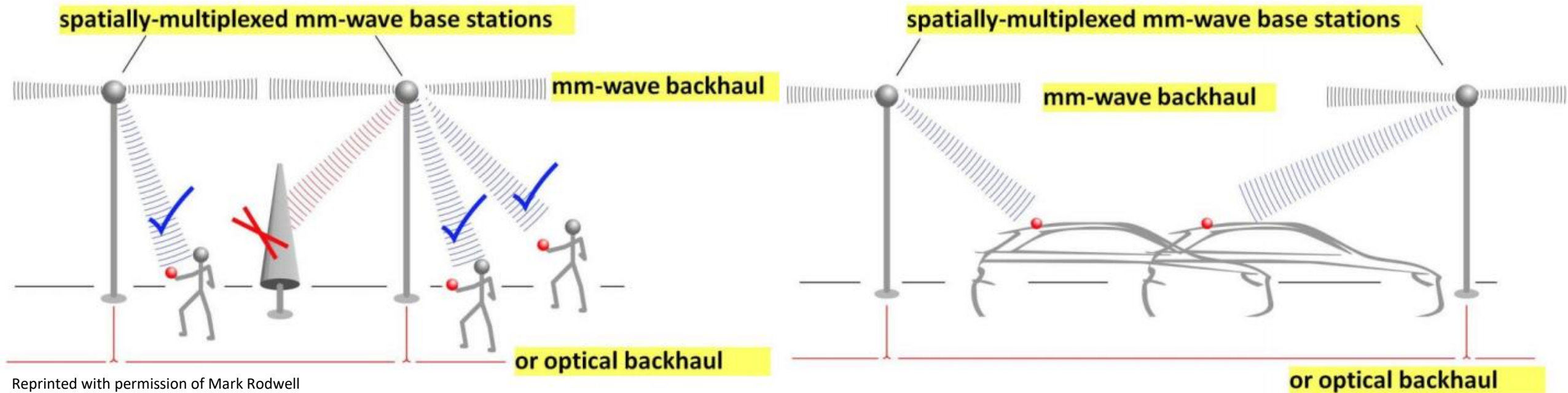
JUMP

Joint University Microelectronics Program



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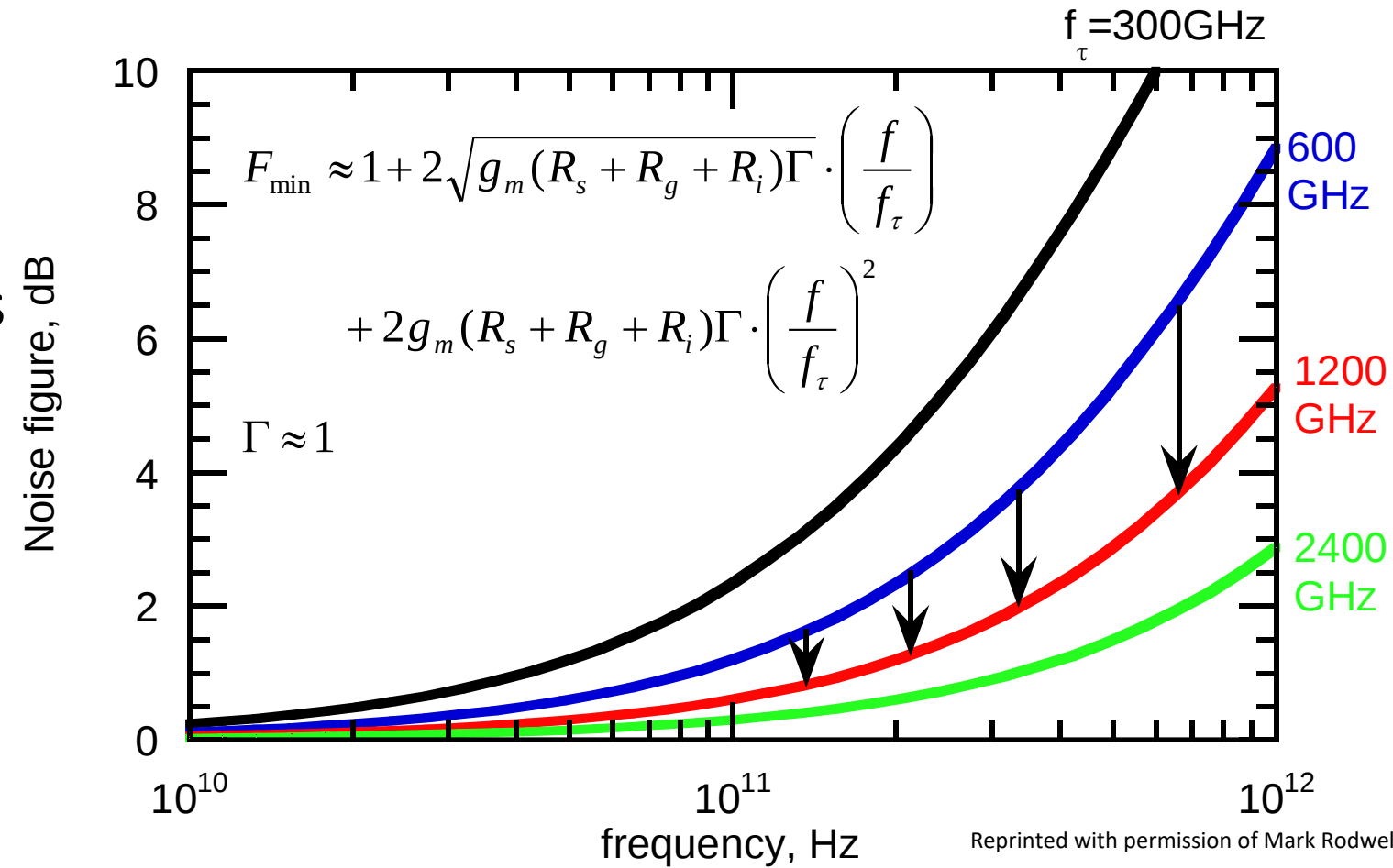
Motivation – Beyond 5G



- Industry currently introducing 5G (20-80 GHz)
- Beyond 5G requires 100-300 GHz communication systems
 - More bandwidth
 - Higher data rates
- Requires transistors operate “easily” at these frequencies:

FETs – Reduce Noise Figure

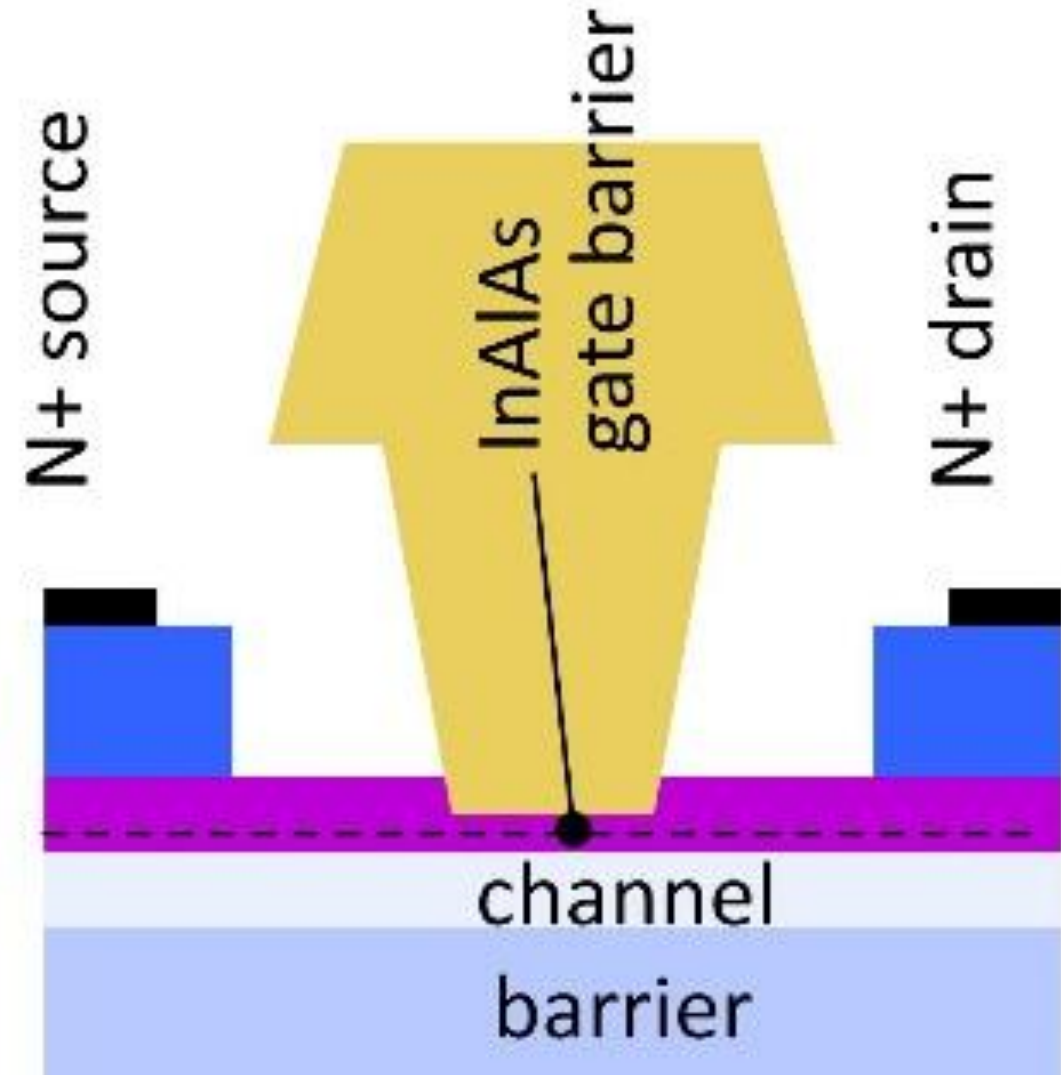
- Increase in f_τ :
- Current frequency
 - Improved noise
- higher-frequency systems
 - Same noise



Why not HEMT?

$$f_{\tau} \approx \frac{g_{m,e}}{2\pi(C_{gs} + C_{gd})}$$

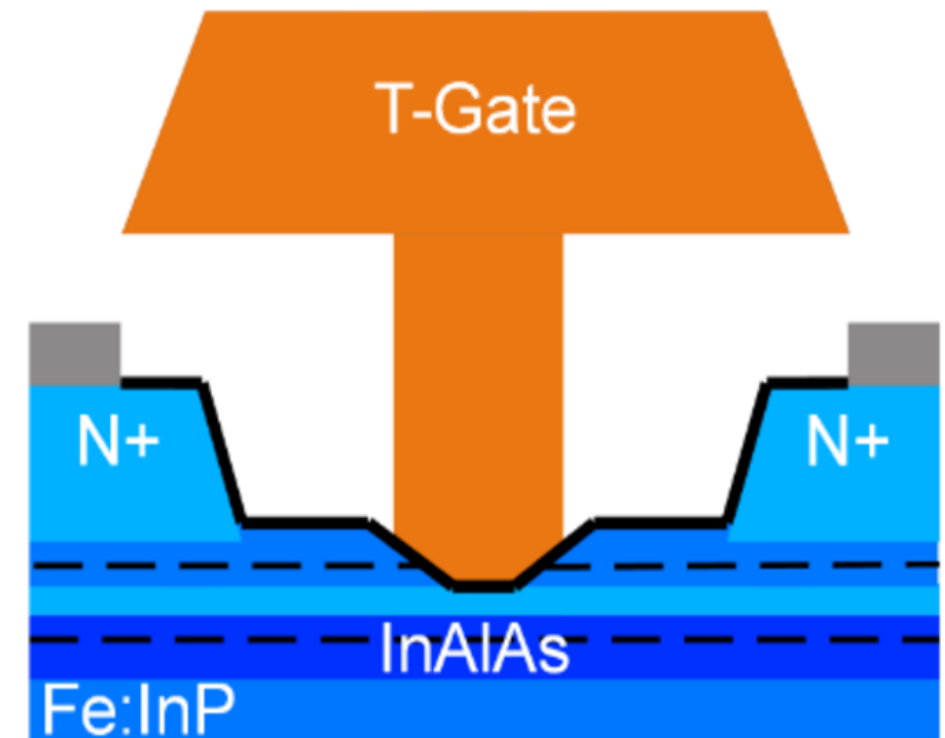
- Increasing f_{τ} by reducing $C_{GS,i}$
- Reduced C_{GS}/C_{GD} hurts g_{ds}
- Scaling laws say thin gate insulator
- InAlAs – InGaAs CBO ~ 0.5 eV
- High gate leakage



MOS-HEMTs

Institution	L_g (nm)	$g_{m,e}$ (mS/ μm)	$g_{ds,e}$ (mS/ μm)	C_{GS} (fF/ μm)	C_{GD} (fF/ μm)	f_T (GHz)	f_{max} (GHz)
Markman <i>et al.</i>	40	2.9	0.15	0.8	0.2	403	594

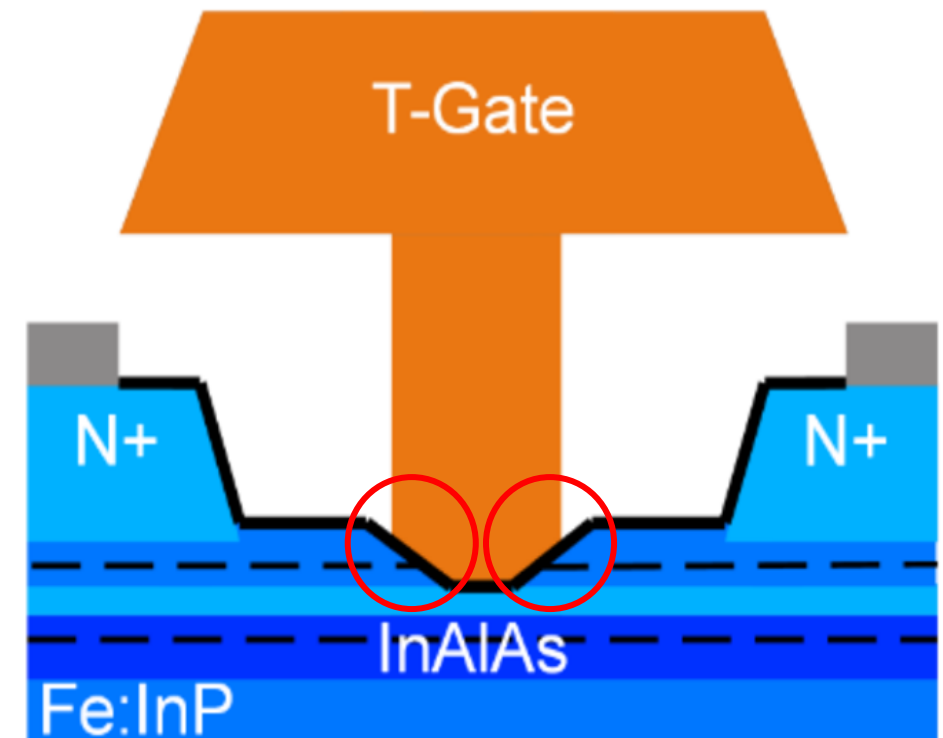
- Add gate dielectric
- Improve C_{GS} / C_{GD}
- Improve g_{ds}



MOS-HEMTs

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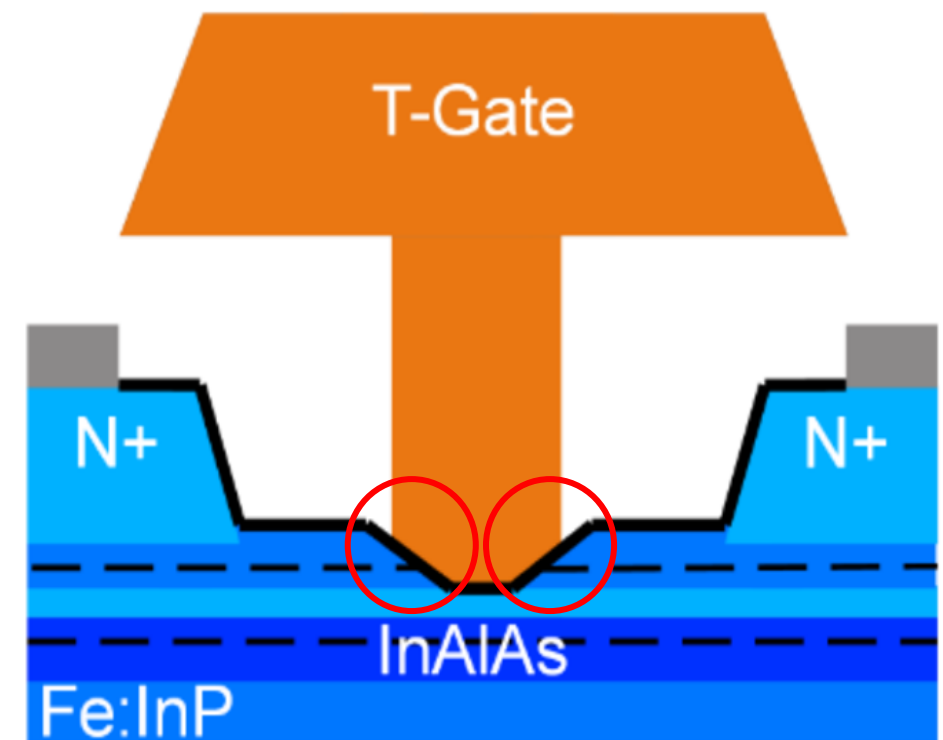
- f_t , f_{max} limited by C_{GS} , C_{GD}
- Fringe capacitance from gate-link overlap
 - T-gate filling
 - Gate alignment
- Extra capacitance from thick link



MOS-HEMTs

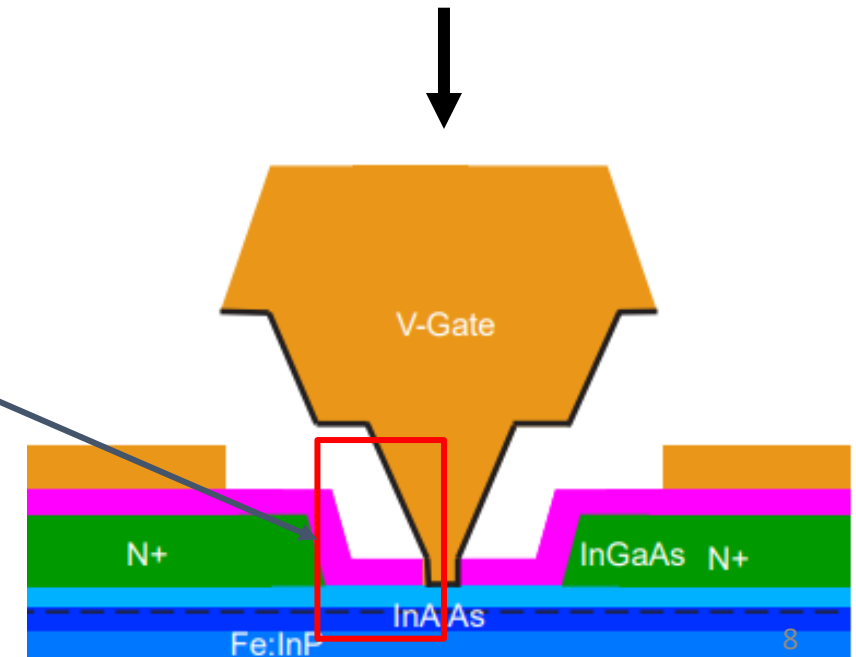
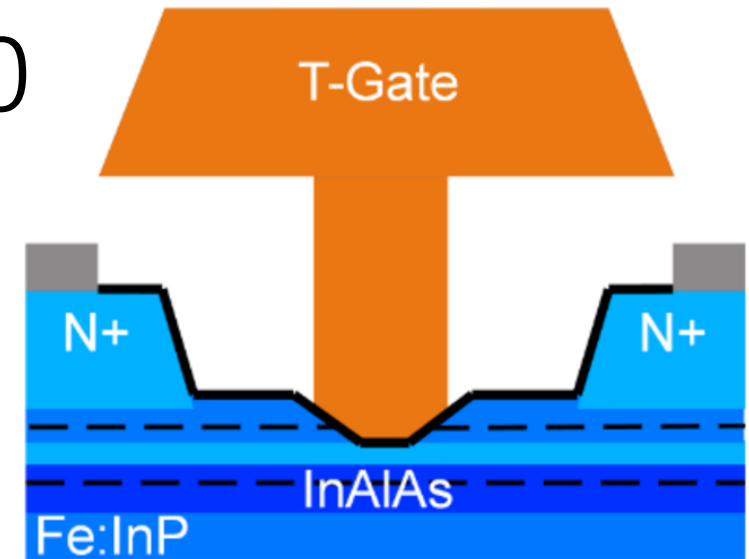
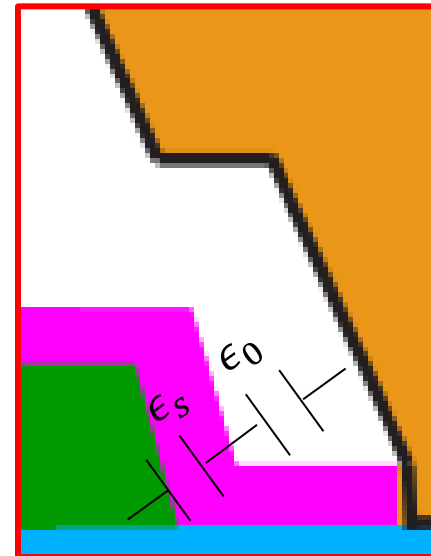
Institution	L_g (nm)	$g_{m,e}$ (mS/ μm)	$g_{ds,e}$ (mS/ μm)	C_{GS} (fF/ μm)	C_{GD} (fF/ μm)	f_T (GHz)	f_{max} (GHz)
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- f_t , f_{max} limited by C_{GS} , C_{GD}
- Fringe capacitance from gate-link overlap
 - T-gate filling
 - Gate alignment
- Extra capacitance from thick link
- Need:
 - Self aligned process
 - Structure that's easier to fill
 - Thinner Link



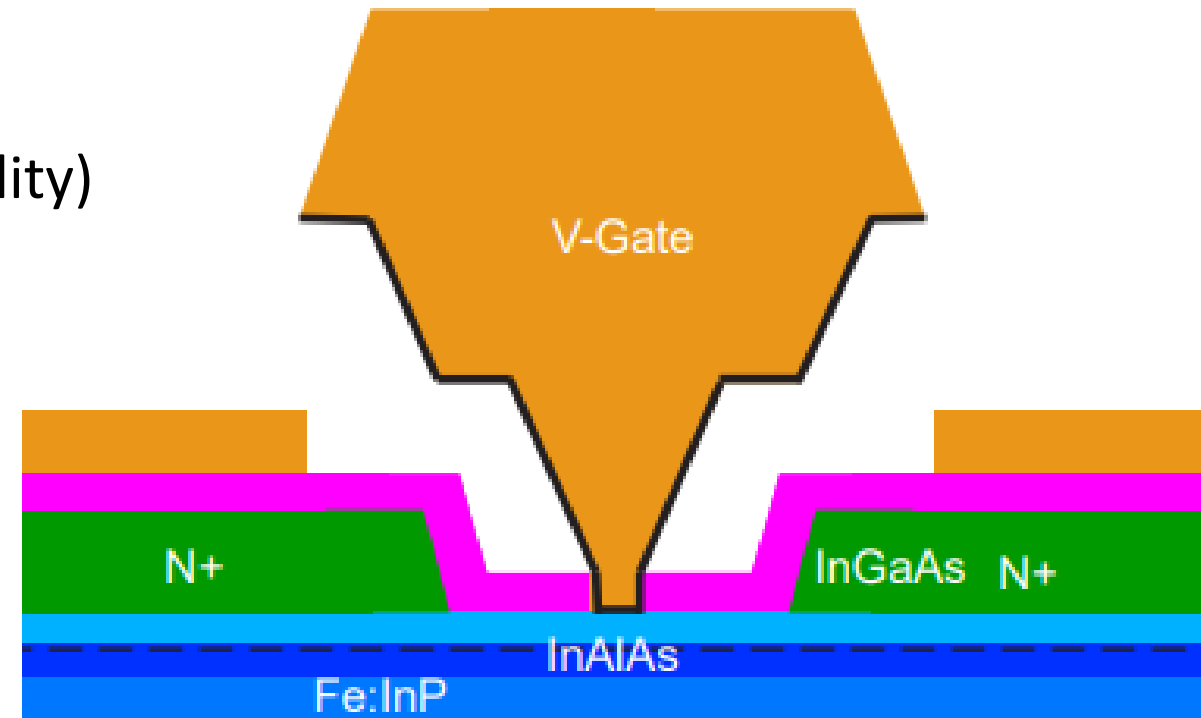
MOS-HEMTs 2.0

- Self aligned
 - Removes gate-link overlap
 - Reduces $C_{GS,f}$
- V-Gate
 - Easier to fill with metal
 - Better L_g scaling
- Thin link
 - More ϵ_0
 - Less ϵ_s
 - Reduces $C_{GS,f}$



What is my variable?

1. Link thickness
 1. 3 nm minimum (source starvation)
 2. 20 nm maximum (maximized mobility)



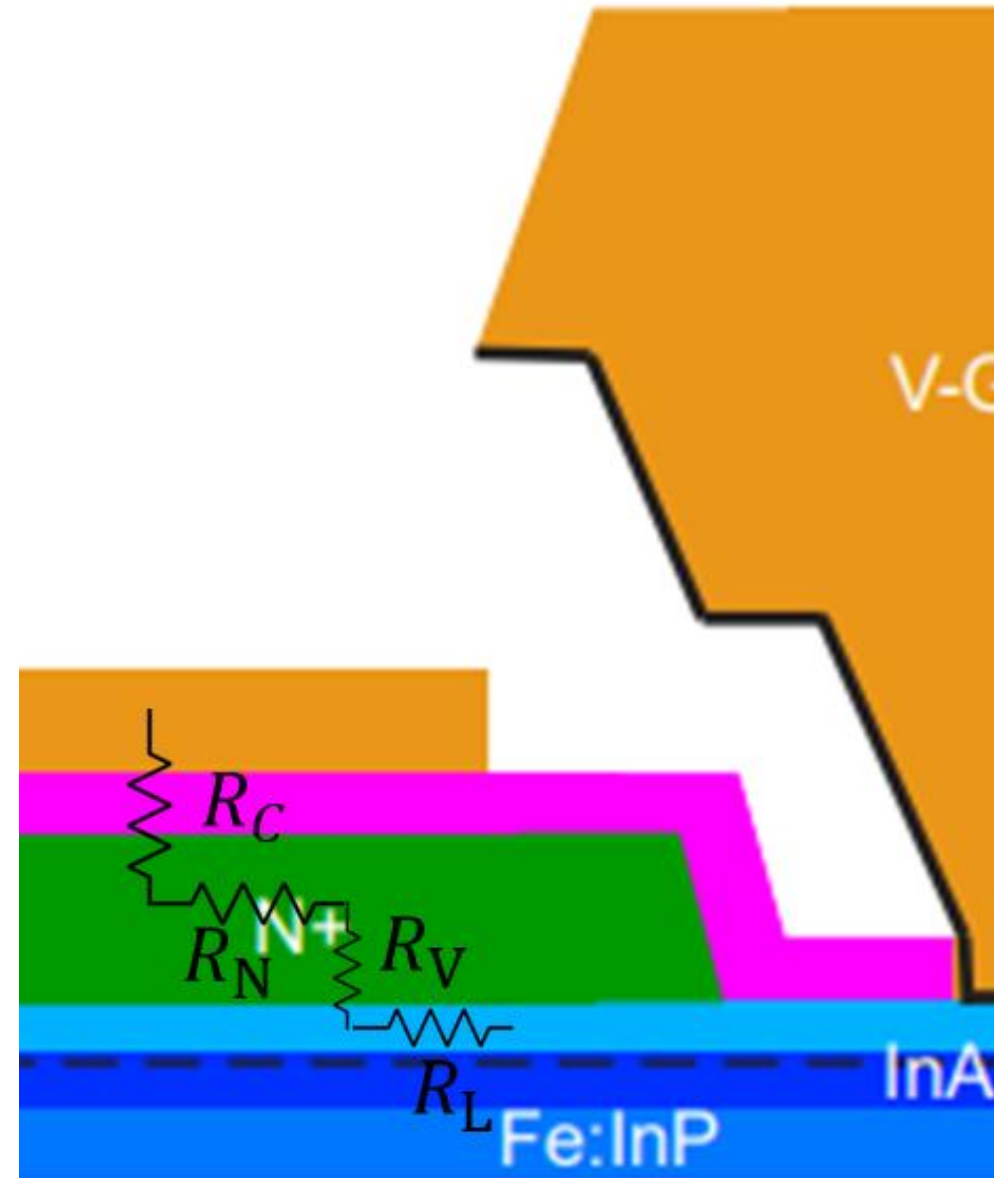
Rs breakdown

$$R_S = R_C + R_N + R_V + R_L$$

$$R_{sheet} = (q * \mu_{Link} * n_{link})^{-1}$$

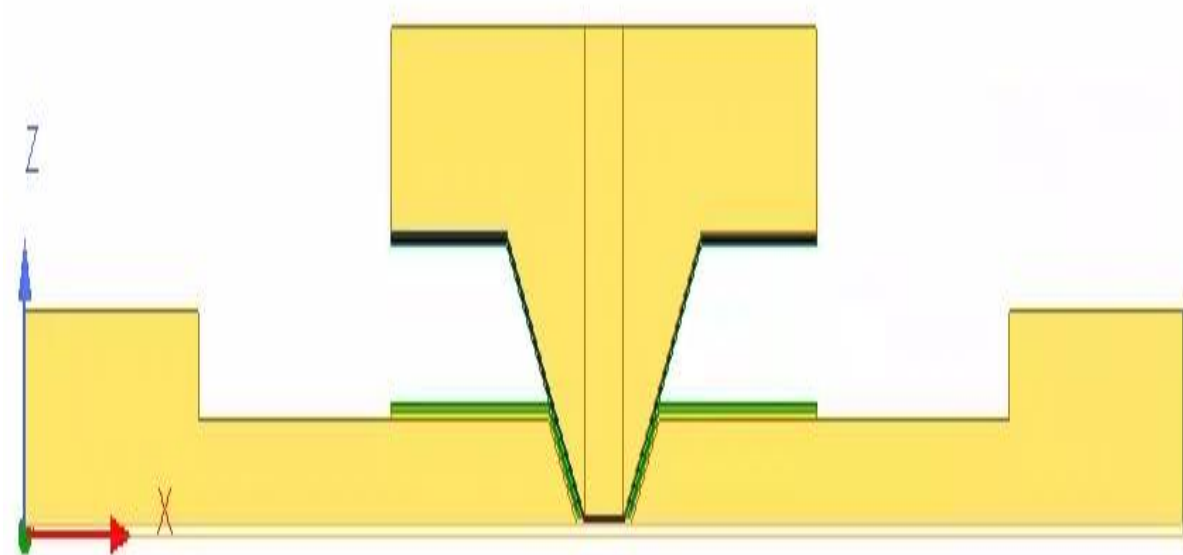
$$R_L = R_{sheet} * L_{sg}$$

$$t_{link} \downarrow \rightarrow \mu_{link} \downarrow$$



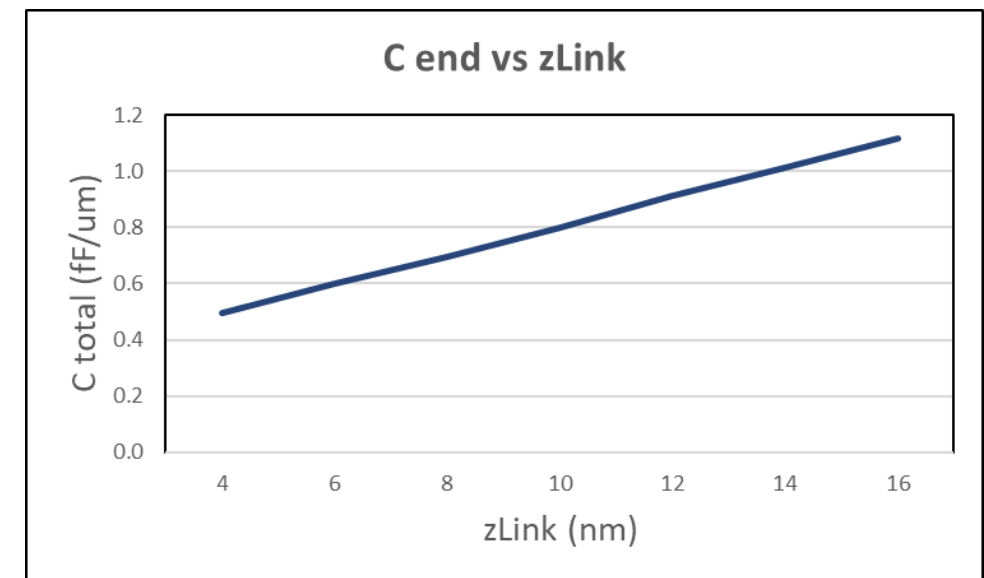
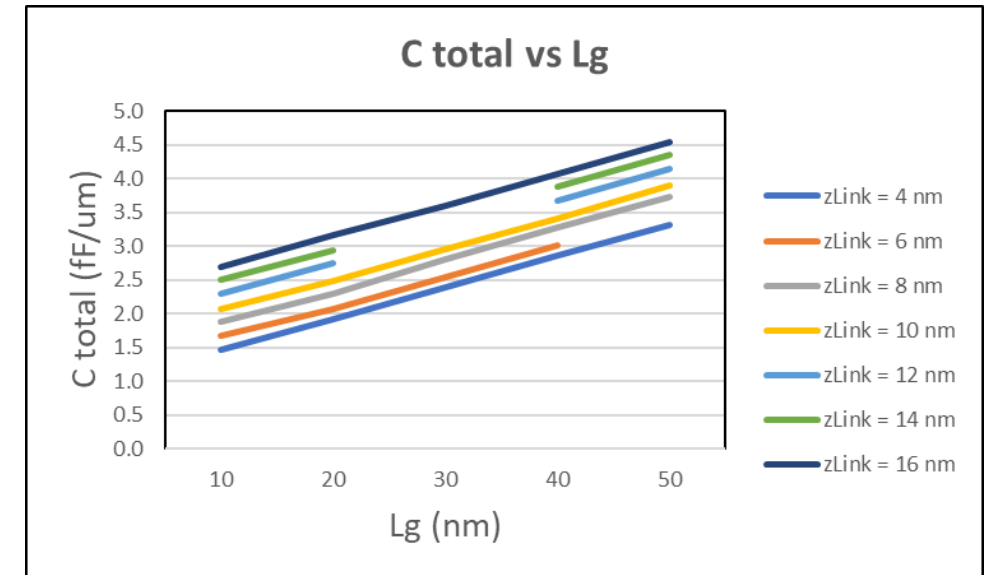
Capacitance

1. Create model in HFSS
2. Find capacitance of the model
3. Vary L_g
4. Find y intercepts
5. Divide by 2 to find CGS
6. Repeat with variations on the model



C_{gs} end vs Link Thickness

- Vary the thickness of the link
 - Assume channel is perfectly conducting (pessimistic)
 - Assume topside link doping is a perfect insulator (optimistic)
 - Results in a **STRONG** linear relationship between link thickness and end capacitance
- Thinner (low mobility) links could be better?



So What?

- *Ideal: Transit Time*

$$f_{\tau} \approx \frac{g_{m,e}}{2\pi(C_{gs} + C_{gd})}$$

$$\begin{aligned} \frac{1}{g_{m,e}} &= \frac{1}{g_{m,i}} + R_S \\ \frac{1}{g_{m,e}} &= \frac{1}{g_{m,i}} + R_C + R_N + R_L \end{aligned}$$

So What?

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$$\frac{1}{g_{m,e}} = \frac{1}{g_{m,i}} + R_S$$

$$\frac{1}{g_{m,e}} = \frac{1}{g_{m,i}} + R_C + R_N + R_L$$

	traditional regrown link	"LEMT" link
link thickness (nm)	16.0	3.0
Rsheets (ohm/sq)	225.0	700.0
link distance (um)	0.05	0.05
Rlink (ohm*um)	11.3	35.0
Rs-Rlink (ohm*um)	65.0	65.0
Rs (ohm*um)	76.3	100.0
gmi (mS/um)	4.0	4.0
gme (mS/um)	3.07	2.86
change in gme		7%

So What?

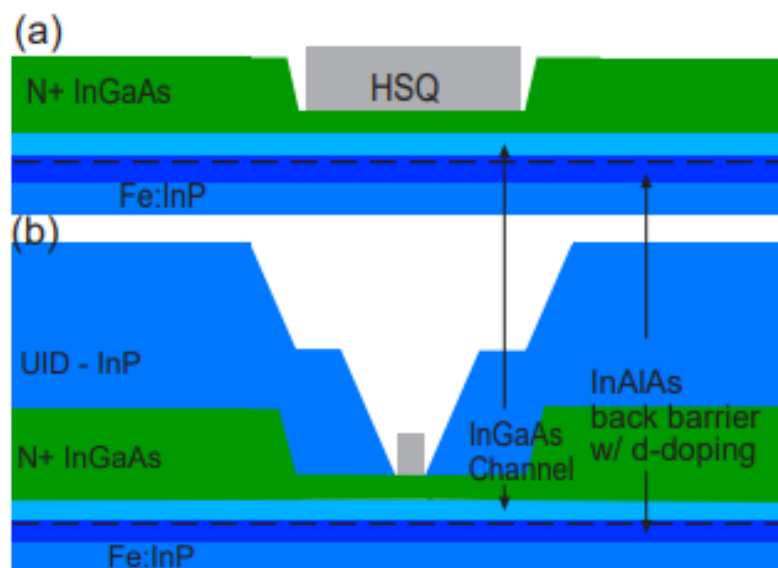
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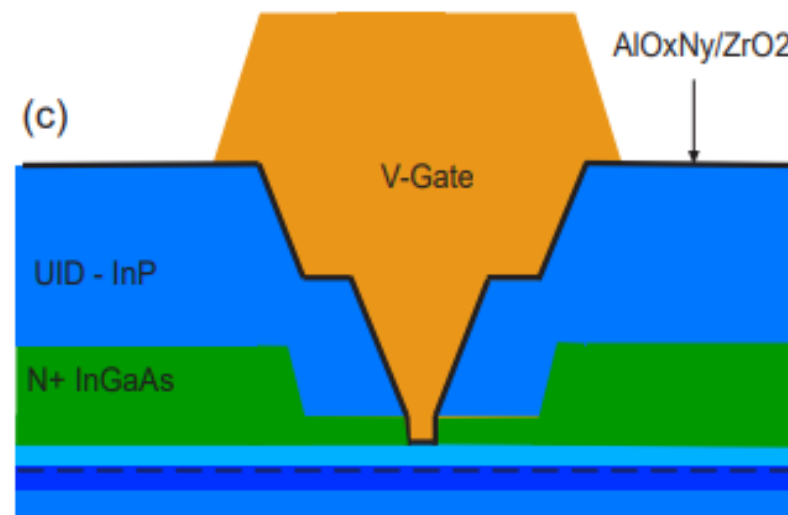
	traditional regrown link	"LEMT" link
link thickness (nm)	16.0	3.0
C _{ch} (fF/um)	0.3	0.3
CGD (fF/um)	0.3	0.3
CGS end (fF/um)	1.1	0.4
CGS + CGD (fF/um)	1.7	1.0
change in capacitance		41%

Process Flow

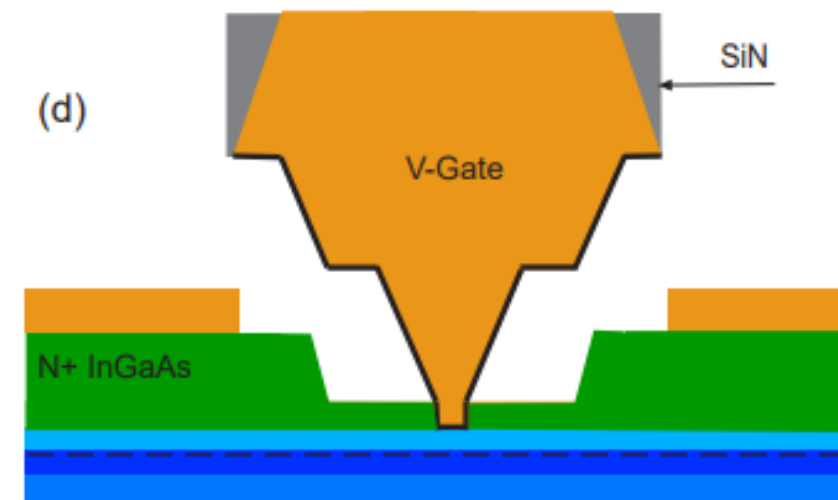


a) Epi + Regrowth 1

b) Regrowth 2

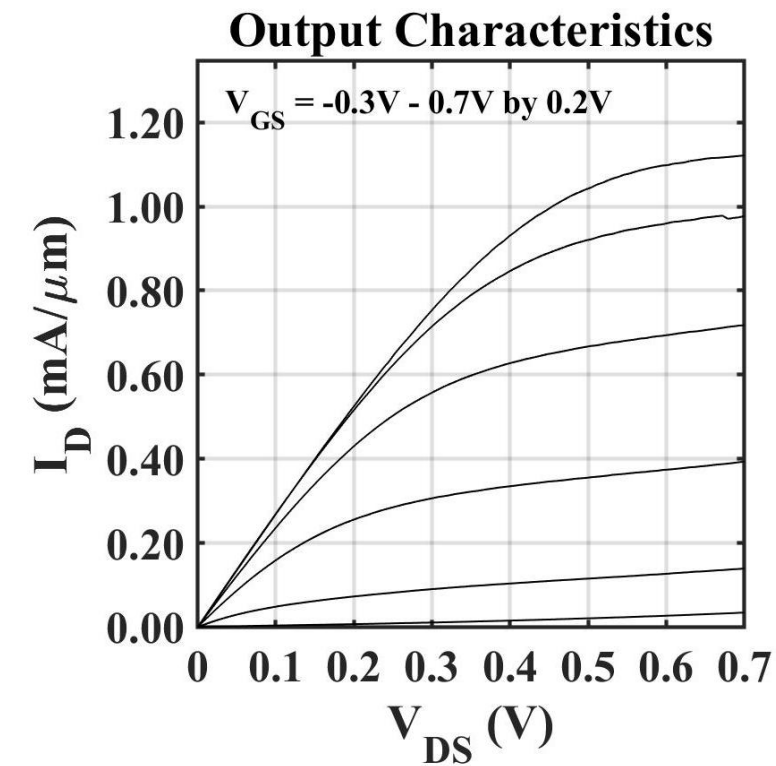
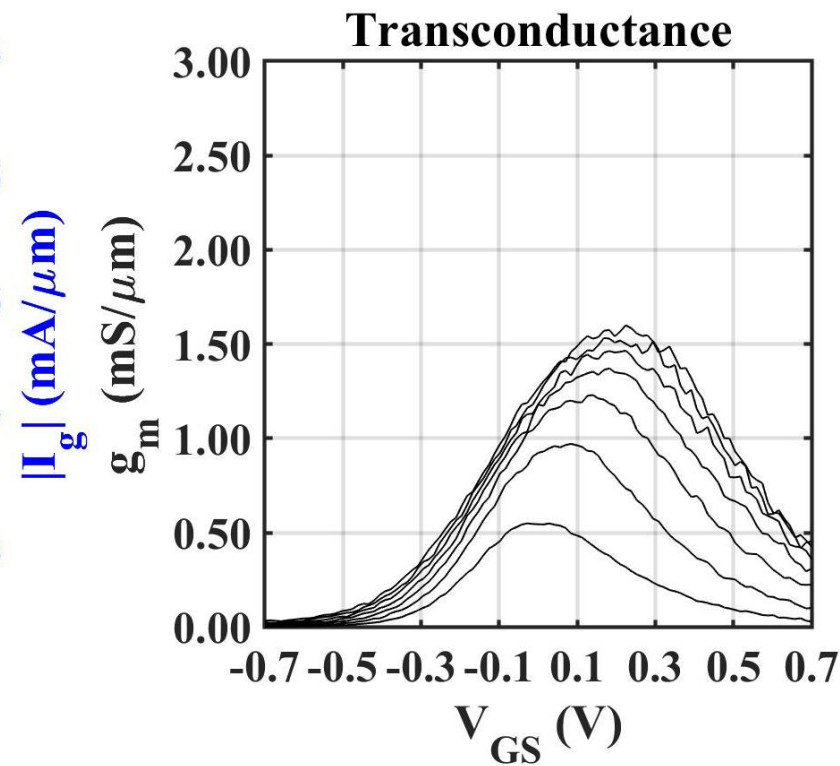
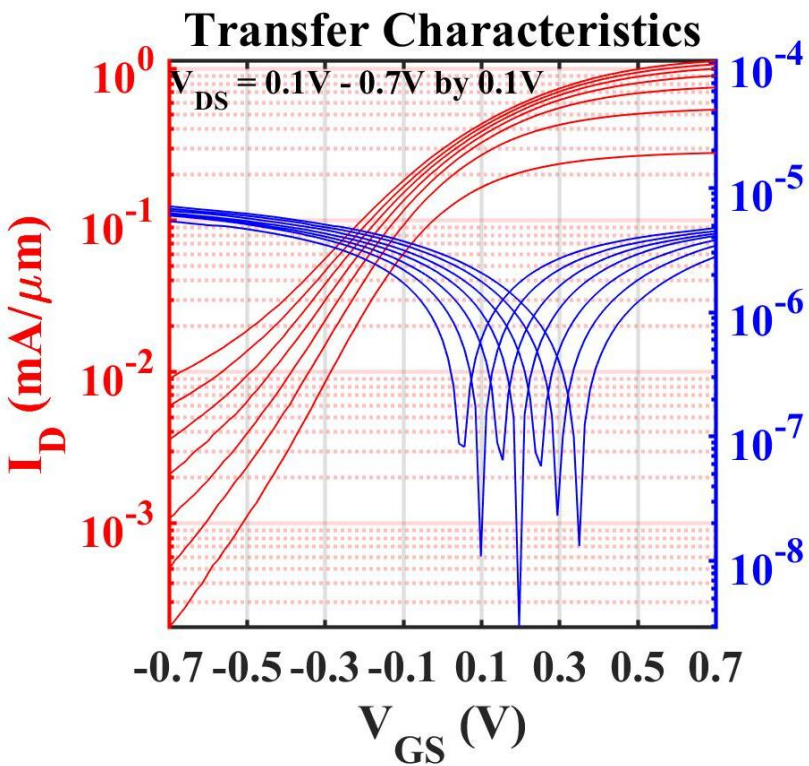


c) Digital etch, high-k,
and gate metal

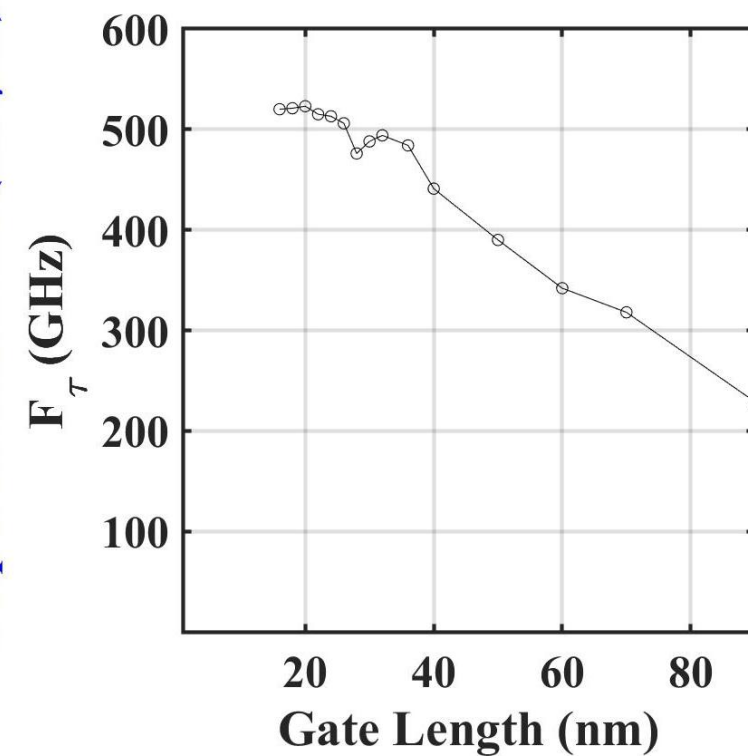
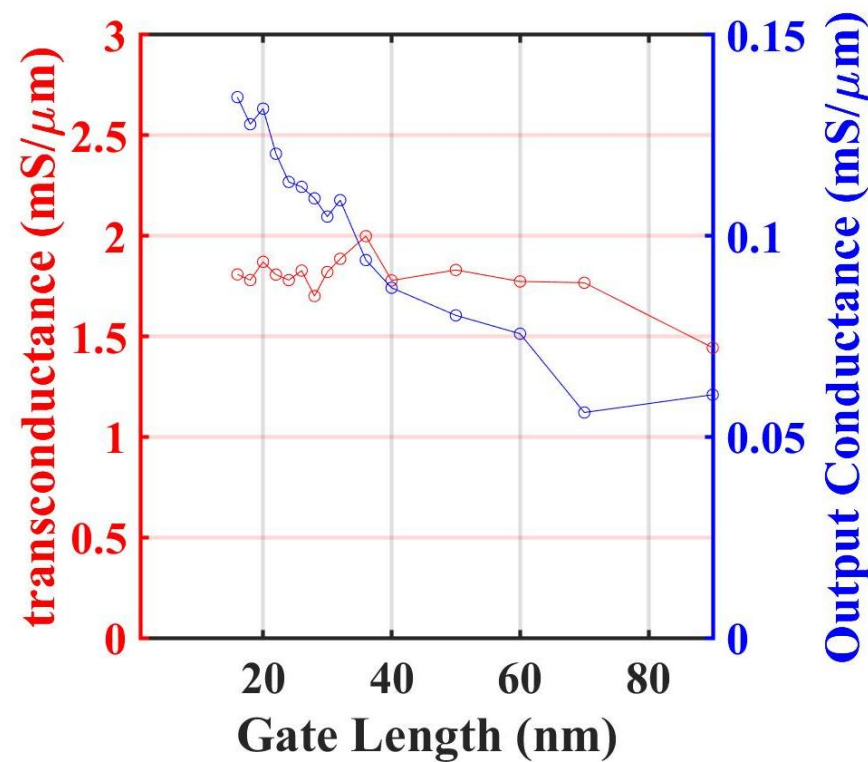
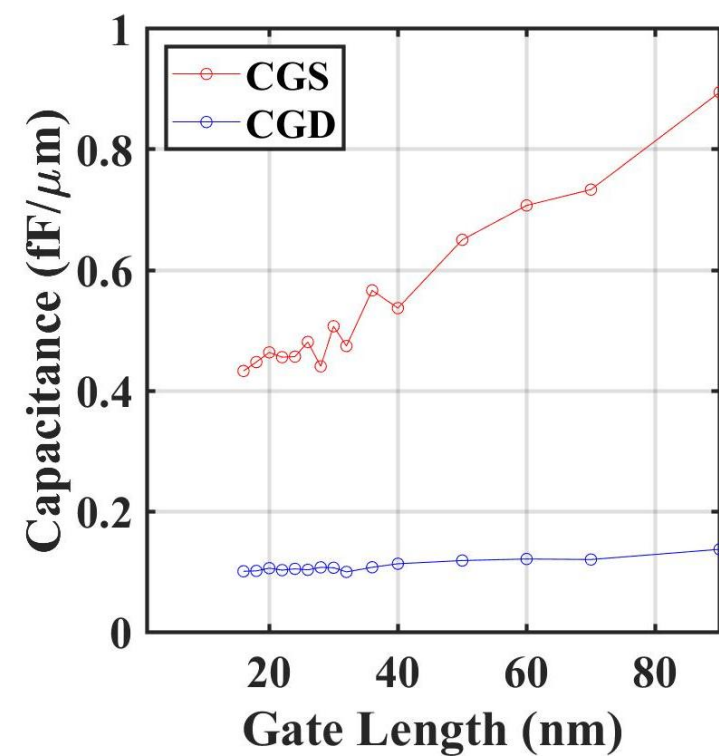


d) high-k etch, sidewall,
sacrificial etch, mesa
isolation, and contacts

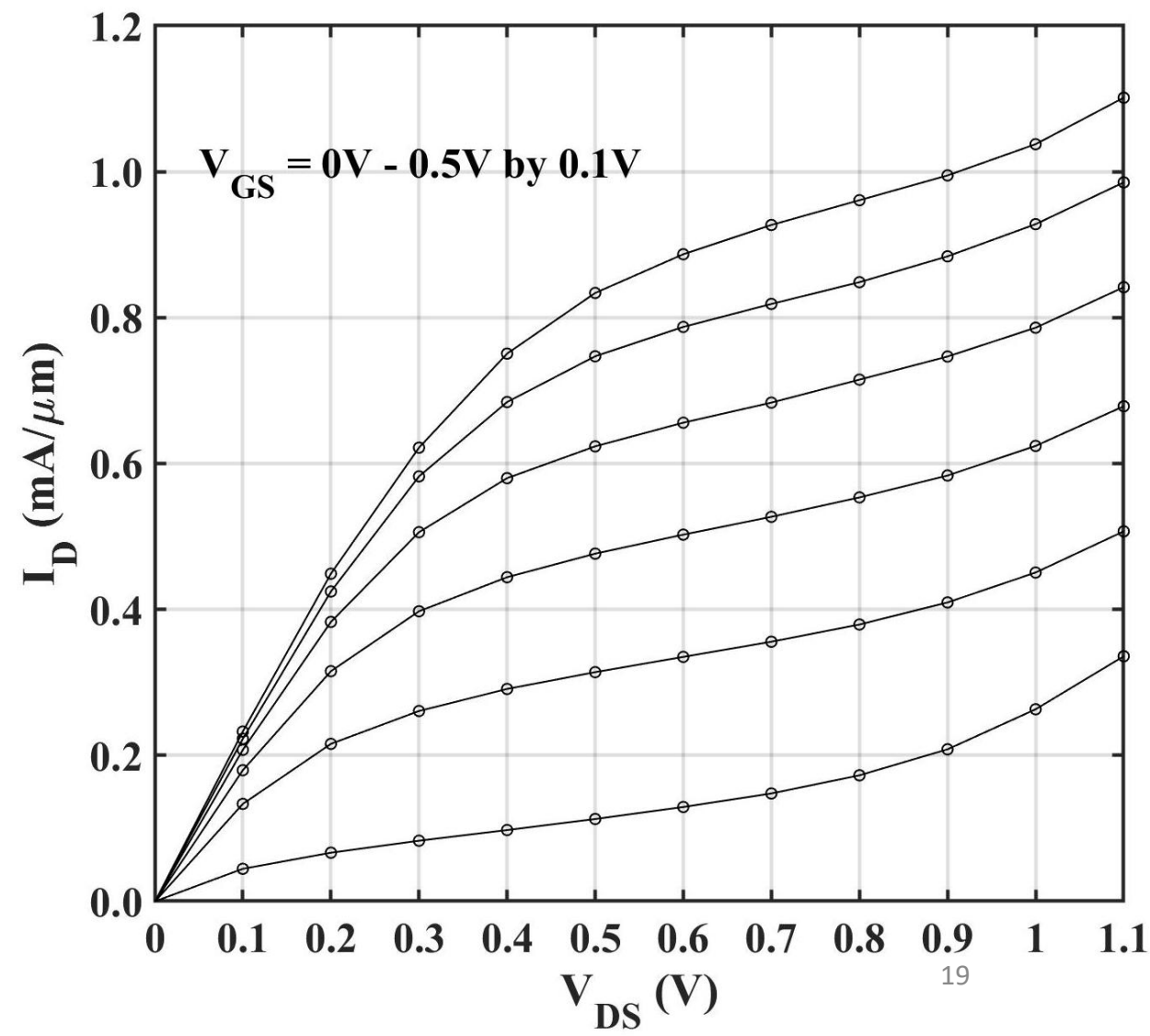
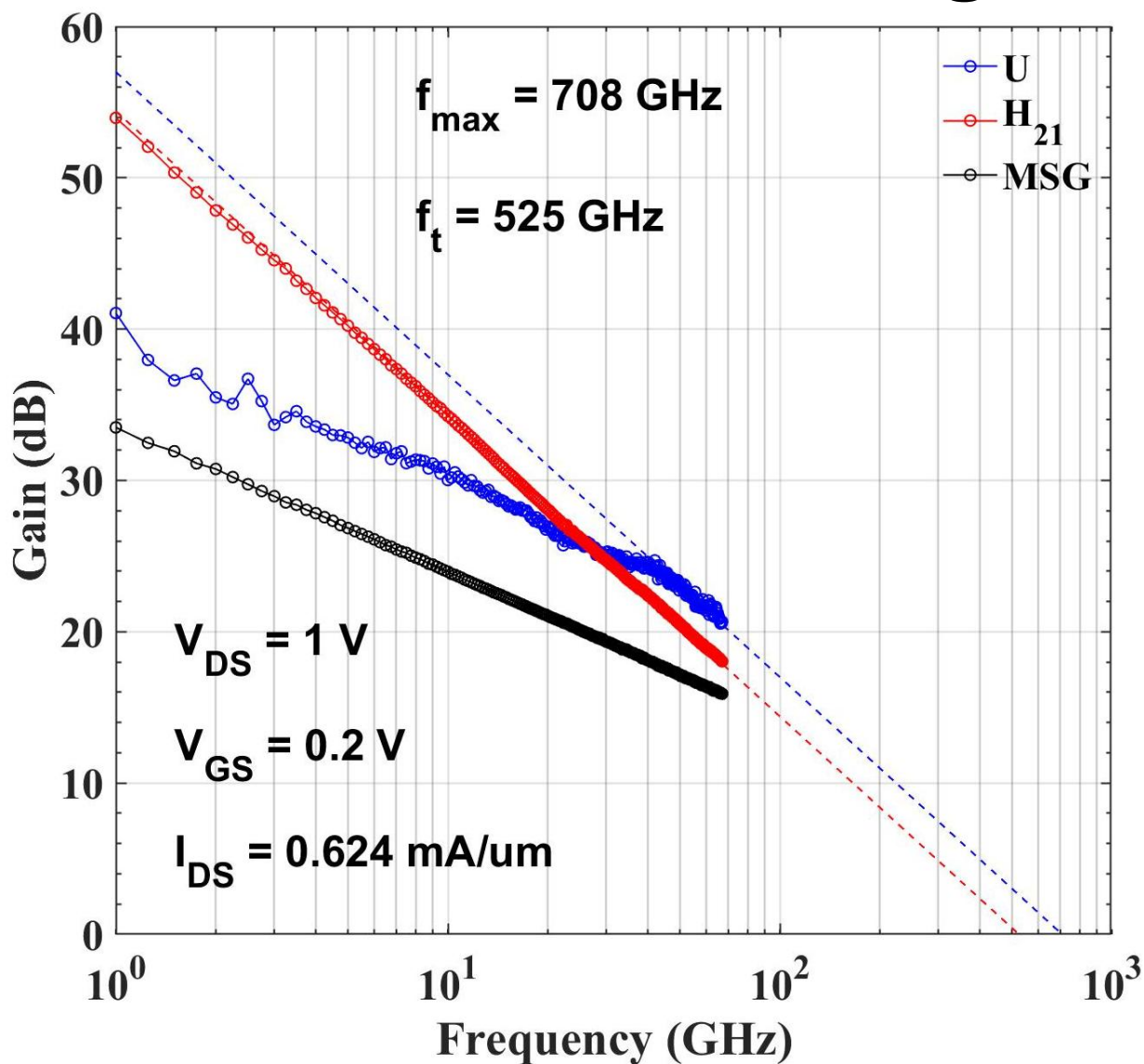
DC results – $L_g = 22$ nm

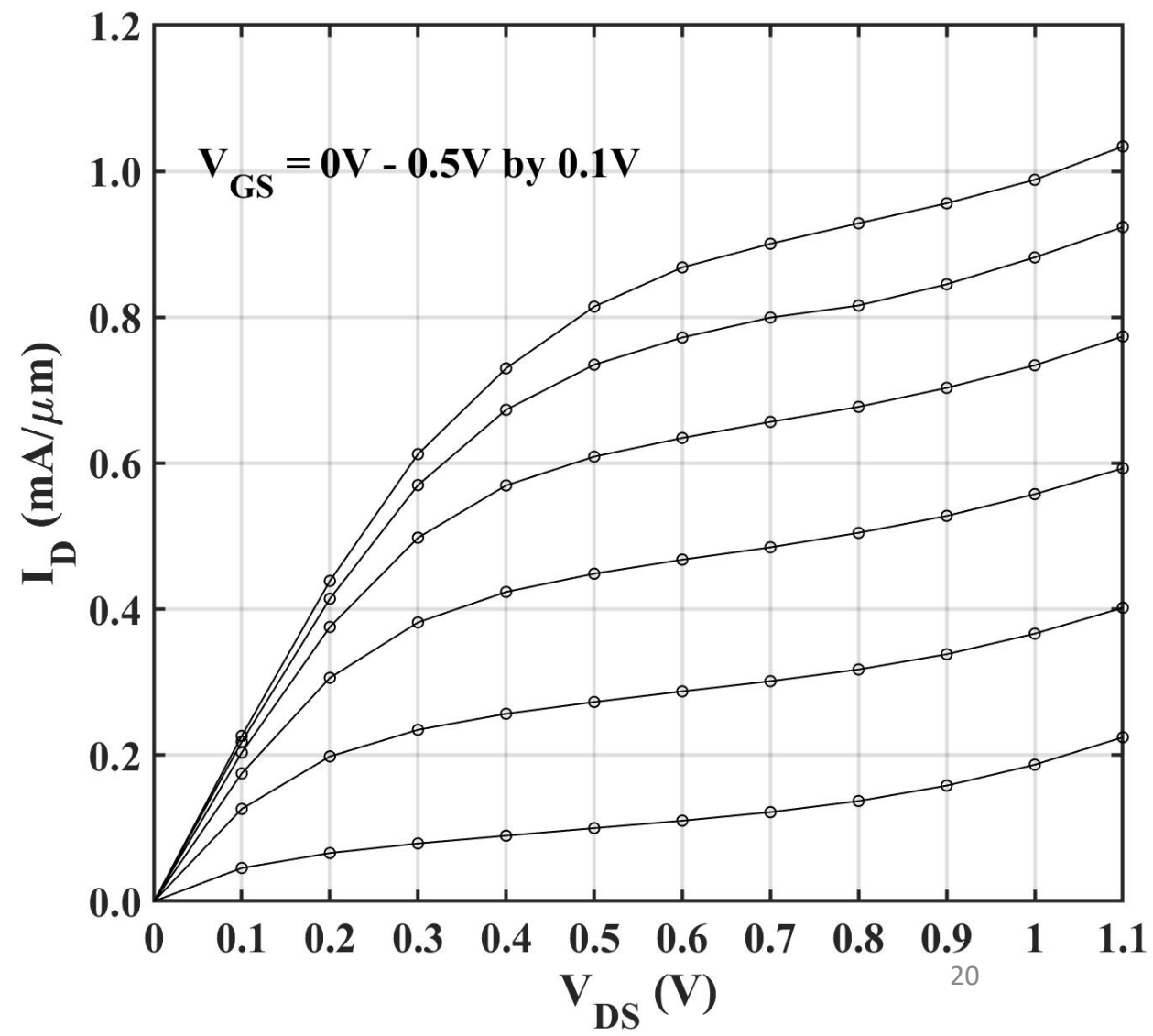
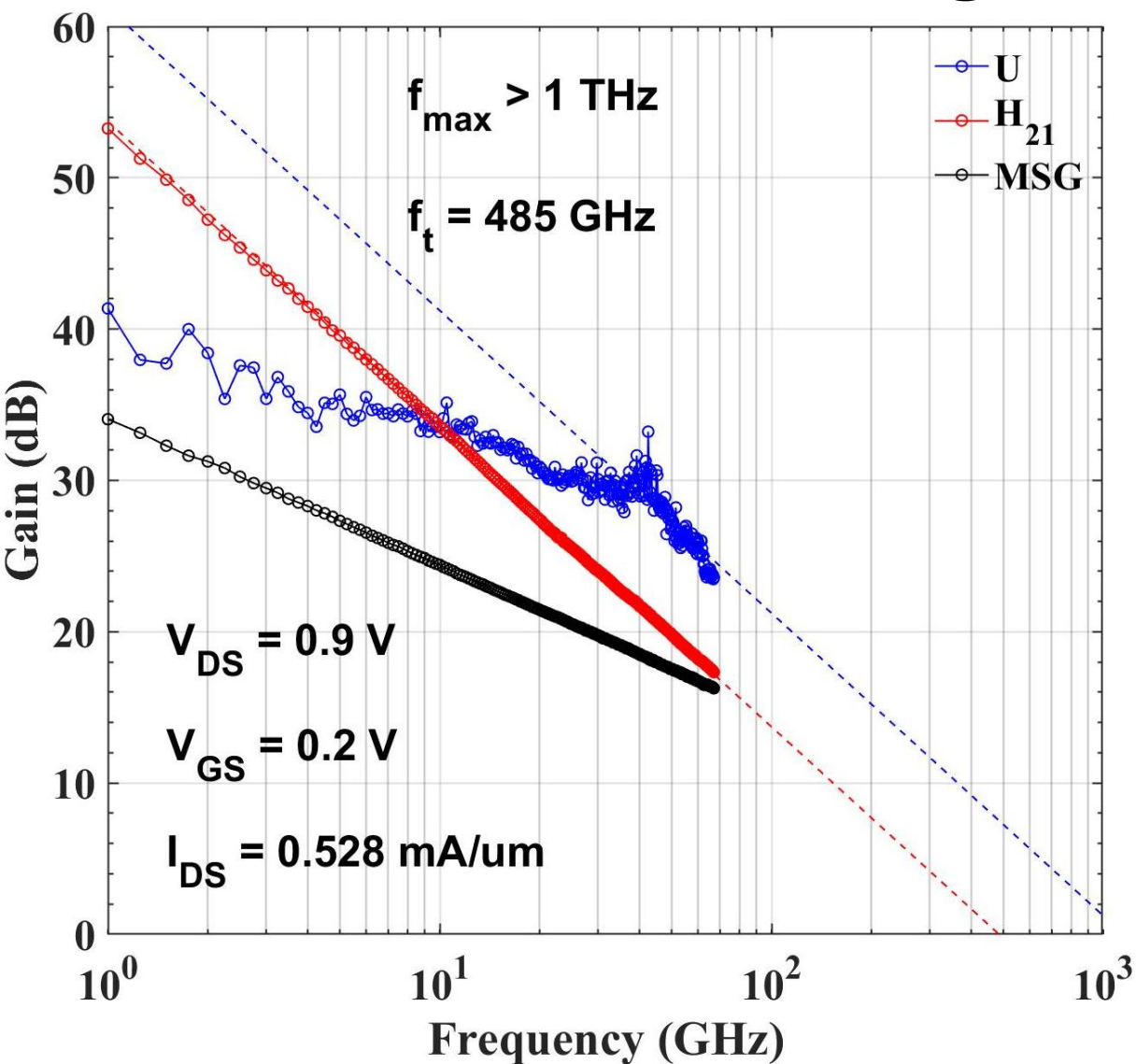


RF results vs Gate Length

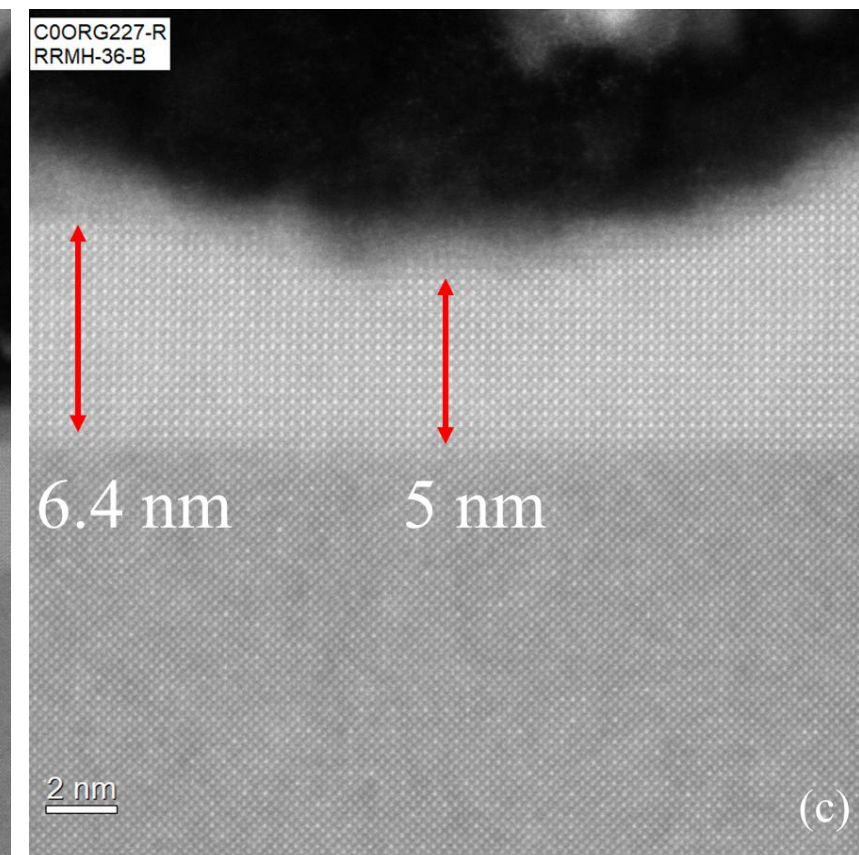
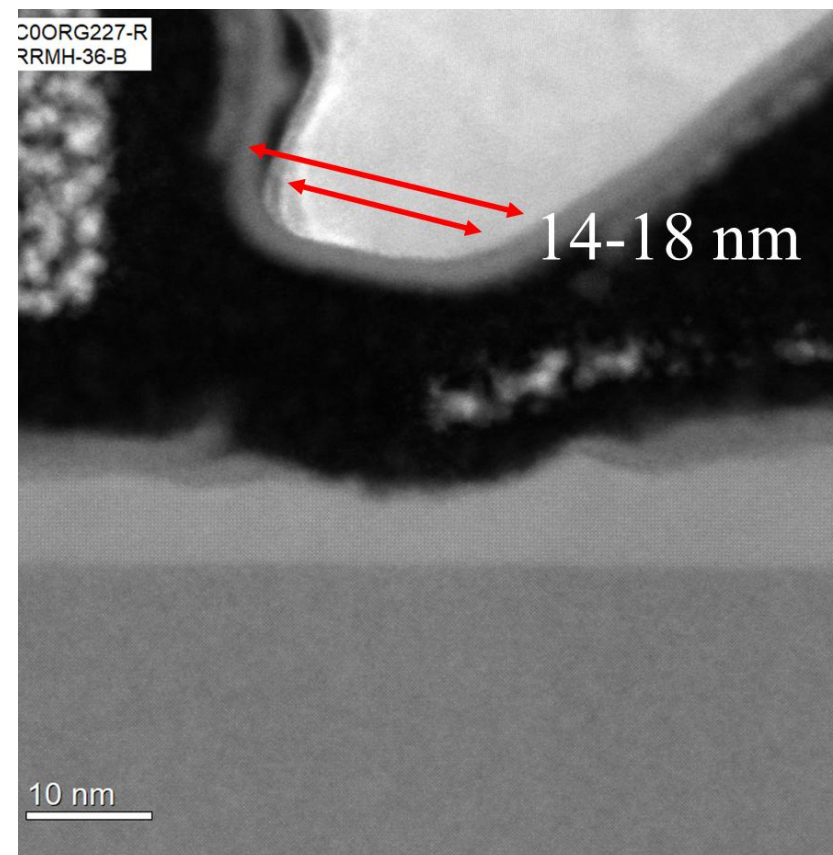
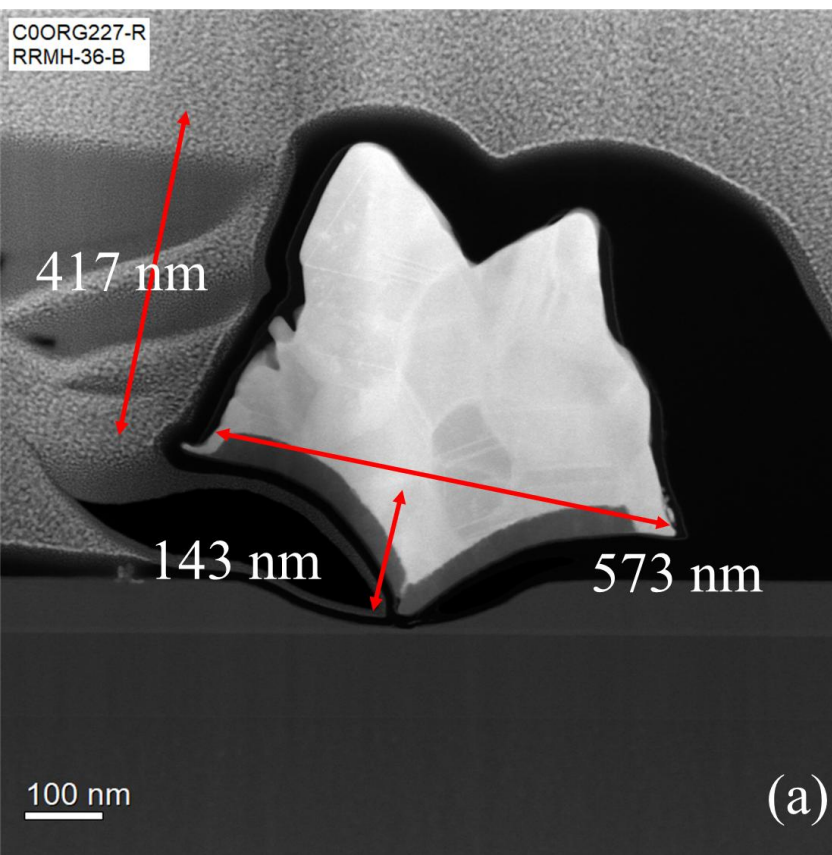


Mixed Results – $L_g = 20$ nm



Mixed Results – $L_g = 36$ nm

TEM – Lg = 18 nm



Acknowledgements

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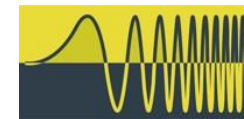
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References

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