280-GHz Frequency Multiplier Chains in 250-nm InP HBT Technology

Utku Soylu, *Member, IEEE*, Amirreza Alizadeh, *Member, IEEE*, Munkyo Seo, *Senior Member, IEEE*, and Mark J. W. Rodwell, *Fellow, IEEE*

***Abstract*— We report 280 GHz 8:1 and 16:1 frequency multipliers in 250-nm indium phosphide (InP) HBT technology. The 8:1 multiplier uses three cascaded push-push emitter-coupled-pairs serving as balanced frequency doublers, with 1:1 transformers at 35, 70, and 140 GHz providing single-ended to differential conversion; the 16:1 multiplier has an additional input emitter-coupled push-push doubler whose drive signal is generated by a transistor differential input stage. With −2 dBm input power, the 8:1 multiplier generates −0.6 dBm output power at 280 and has 48-GHz 3-dB bandwidth. Spurious harmonics are suppressed by >28 dBc over the 3-dB bandwidth. With −13 dBm input power, the 16:1 multiplier generates −0.6 dBm output power at 280 and has 44-GHz 3-dB bandwidth. Spurious harmonics are suppressed by >26 dBc over the 3-dB bandwidth. The 8:1 and 16:1 multipliers consume 102- and 162-mW dc power and occupy 0.4- and 0.75-mm^2 die area, respectively. To the authors' knowledge, these results demonstrate record spectral purity for frequency multiplier chains operating near 280 GHz.**

***Index Terms*— Balanced frequency doubler, double heterojunction bipolar transistor (DHBT), frequency multiplier, *H*-band, high spectral purity, indium phosphide (InP), mm-wave, spurious harmonic rejection.**

I. Introduction

THERE is increasing interest in the 200-300-GHz frequency band due to its potential for high-speed wireless communication links with capacities well above 100 Gb/s [1]. One key transceiver design challenge [Fig. 1(a)] is local oscillator (LO) generation. The LO can be directly generated by a phase-locked loop (PLL) whose output is at the LO frequency [Fig. 1(b)]. Because the resulting phase noise, outside the PLL loop bandwidth, is then that of the voltage-controlled oscillator (VCO), the main challenge is to design a VCO with adequately low phase noise. Alternatively, the LO can be generated by a lower-frequency PLL followed by an N:1 frequency multiplier [Fig. 1(c)]. Although this increases the PLL phase noise by 20log(N) dB, the resulting phase noise can nevertheless be lower than that of a PLL operating directly at 200–300 GHz. Selecting a larger multiplication factor N results in a lower input frequency, facilitating transceiver IC packaging; selecting a smaller N increases the frequency separation of spurious harmonics generated by the multiplier chain, making it easier to suppress these by filtering. These spurious LO multiplier harmonics will cause receivers to receive signals, and transmitters to radiate signals, at frequencies other than those intended, thereby causing interference. Key design objectives for such multipliers are a strong rejection of spurious harmonics for better signal-to-interference ratios and low dc power consumption for better efficiency.

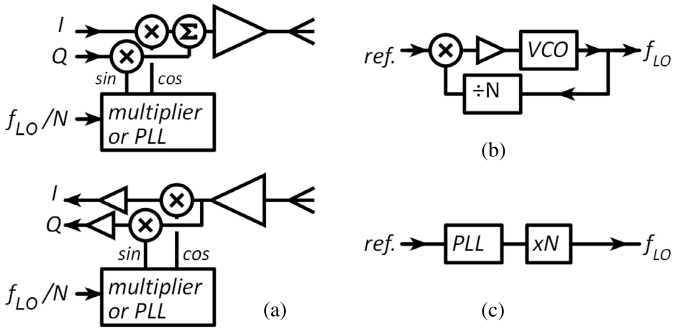

Fig. 1. (a) Millimeter-wave transceiver architectures with (b) PLLs and (c) multiplier chains for on-chip LO generation.

Integrated frequency multiplier chains operating near 280 GHz have been demonstrated [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17] in several technologies, these showing excellent performance (Table I). Here we report *WR*-3 band 8:1 and 16:1 frequency multipliers with record spectral purity for designs operating near 280 GHz. The 8:1 multiplier uses three cascaded push-push emitter-coupled-pairs serving as balanced frequency doublers, with 1:1 transformers at 35, 70, and 140 GHz providing single-ended to differential conversion; the 16:1 multiplier has an additional input emitter-coupled push-push doubler whose drive signal is generated by a transistor differential input stage. As is well understood [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], key design features include the selection of the transistor load-line for high efficiency and single-ended to differential conversion with low phase and amplitude imbalance for strong spurious harmonic suppression.

With −2 dBm input power, the 8:1 multiplier generates −0.6 dBm output power at 280 and has 48-GHz 3-dB bandwidth. Spurious harmonics are suppressed by >28 dBc

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Utku Soylu, Amirreza Alizadeh, and Mark J. W. Rodwell are with the Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA 93117 USA (e-mail: utkusoylu@ucsb.edu).

Munkyo Seo is with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 440-746, South Korea.

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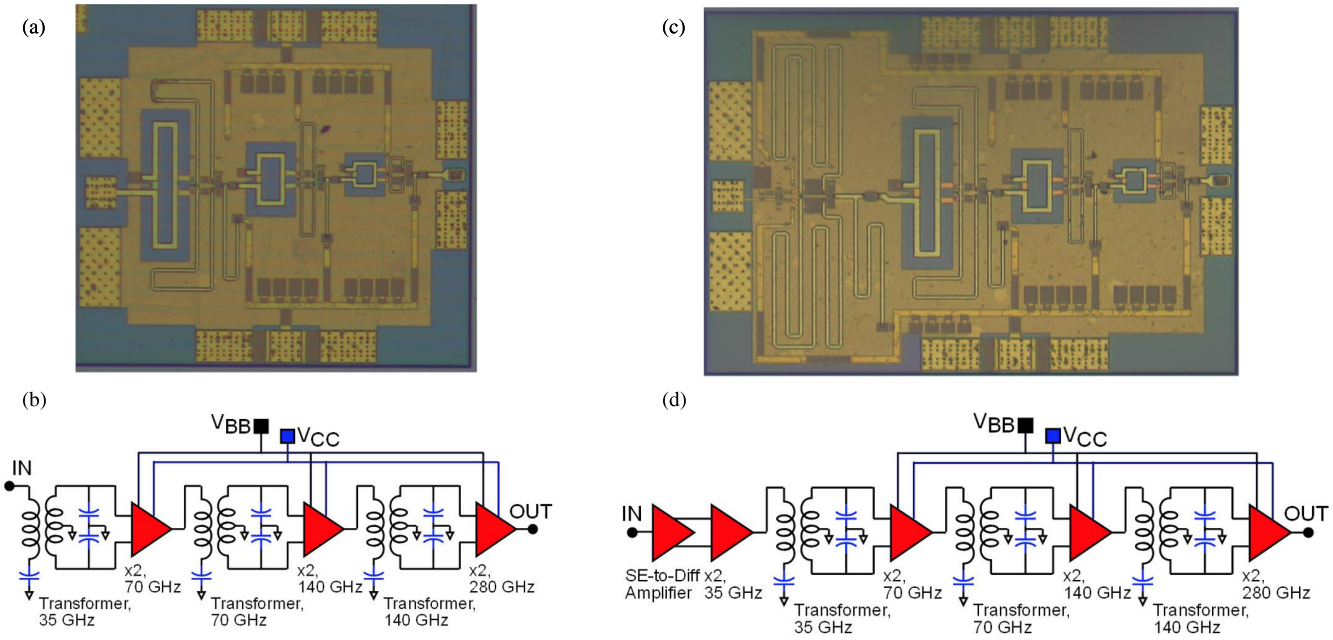

Fig. 2. (a) Die photograph and (b) block diagram of the 8:1 frequency multiplier; the die area is 0.92 × 0.8 mm, while the core area, without dc routing and pads, is 0.7 × 0.56 mm. (c) Die photograph and (d) block diagram of the 16:1 frequency multiplier; the die area is 1.2 × 0.8 mm, while the core area, without dc routing and pads, is 1 × 0.75 mm.

over the 3-dB bandwidth. With −13 dBm input power, the 16:1 multiplier generates −0.6 dBm output power at 280 and has 44-GHz 3-dB bandwidth. Spurious harmonics are suppressed by >26 dBc over the 3-dB bandwidth. The 8:1 and 16:1 multipliers consume 102 and 162-mW dc power and occupy 0.4 and 0.75-mm^2 die area, respectively. Reducing the RF input power further improves the suppression of spurious harmonics but reduces the multipliers' bandwidth. Although the 16:1 multiplier consumes greater dc power and occupies a greater die area, the lower (17.5 versus 35 GHz) input frequency makes IC packaging less difficult.

II. Frequency Multiplier Chain Design

The frequency multipliers were fabricated in Teledyne 250-nm indium phosphide (InP) HBT technology [18], this having a maximum 650-GHz power gain cut-off frequency (f_{max}) at the top metal layer, a maximum 3-mA/μm current density, and 4.5-V $V_{BR,CEO}$. The technology provides four Au interconnect layers, 50-Ω/square thin film resistors, and 0.3-fF/μm^2 metal-insulator-metal (MIM) capacitors.

As shown in Fig. 2(a) and (b), the 8:1 frequency multiplier uses three cascaded doublers to generate 280 from a 35-GHz input. Each active doubler cell has a differential input but a single-ended output; the necessary single-ended to differential conversion is provided by interstage transformers, not transistor differential amplifiers, as transformers provide better amplitude and phase balance at high frequencies and consume no dc power. Shown in Fig. 2(c) and (d), the 16:1 frequency multiplier has an additional input frequency doubler and generates 280 from a 17.5-GHz input. To save die area, this doubler uses a transistor differential amplifier instead of an input transformer.

A. Multiplier Chain Spurious Harmonics

If each frequency doubler in the 16:1 frequency multiplier generated only the 2nd harmonic of its input frequency, with input frequency f_{in} the successive stage output frequencies would be $2f_{in}$, $4f_{in}$, $8f_{in}$, and $16f_{in}$. Each doubler will however generate spurious output signals at the other harmonics. As we will see below, spurious harmonics generated by the first several doubler stages will produce multiplier chain spurious output harmonics that are closest to the desired output harmonic, and therefore of greatest design concern. Once these spurious harmonics are generated by a given stage, further intermodulation between them and the desired harmonic will generate additional sum and difference frequencies.

In the 16:1 frequency multiplier (Fig. 3) driven at f_{in} = 17.5 GHz, spurious harmonic outputs from the first frequency doubler at frequencies f_{in} and $3f_{in}$ will, after passing through the second, third, and fourth doubler, produce spurious outputs of the 16:1 frequency multiplier chain at the frequencies (f_{in}, $2f_{in}$, ..., $24f_{in}$), with the spurious harmonics $15f_{in}$ and $17f_{in}$ separated in frequency from the desired output harmonic $16f_{in}$ by $\pm f_{in}$. In contrast, spurious harmonic outputs from the second frequency doubler at frequencies $2f_{in}$ and $6f_{in}$ will, after passing through the third and fourth doubler, produce spurious outputs of the 16:1 multiplier chain at frequencies ($2f_{in}$, $4f_{in}$, ..., $24f_{in}$), with the spurious harmonics $14f_{in}$ and $18f_{in}$ separated in frequency from the desired output harmonic $16f_{in}$ by $\pm 2f_{in}$. This trend continues, with spurious harmonics of the third doubler stage producing spurious outputs of the 16:1 multiplier chain whose separation from the desired output harmonic is at least $\pm 4f_{in}$, whereas for the fourth stage, its spurious outputs produce, at the 16:1 multiplier chain output, spurious signals that are separated from the desired harmonic by at least $\pm 8f_{in}$. As spurious harmonics having frequencies

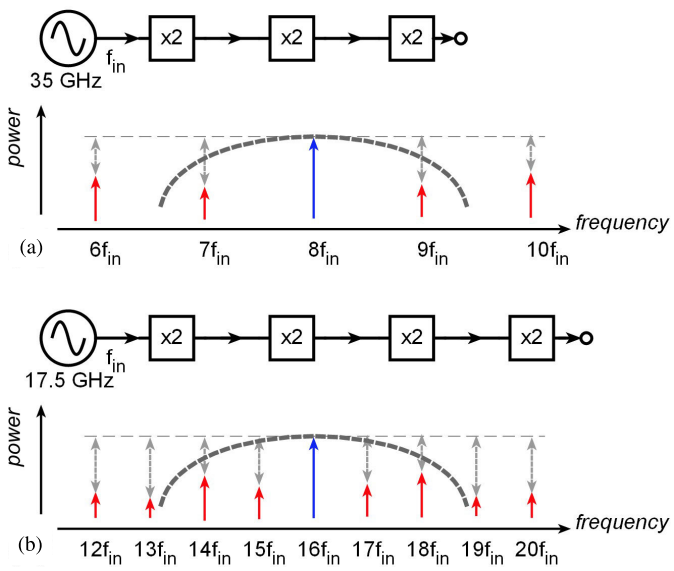

Fig. 3. The output spectrum of (a) ×8 FMC and (b) ×16 FMC.

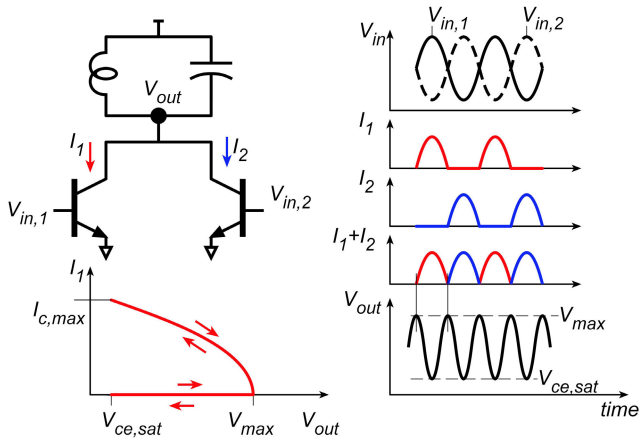

Fig. 4. Balanced frequency doubler voltage waveforms, current waveforms, and transistor loadline.

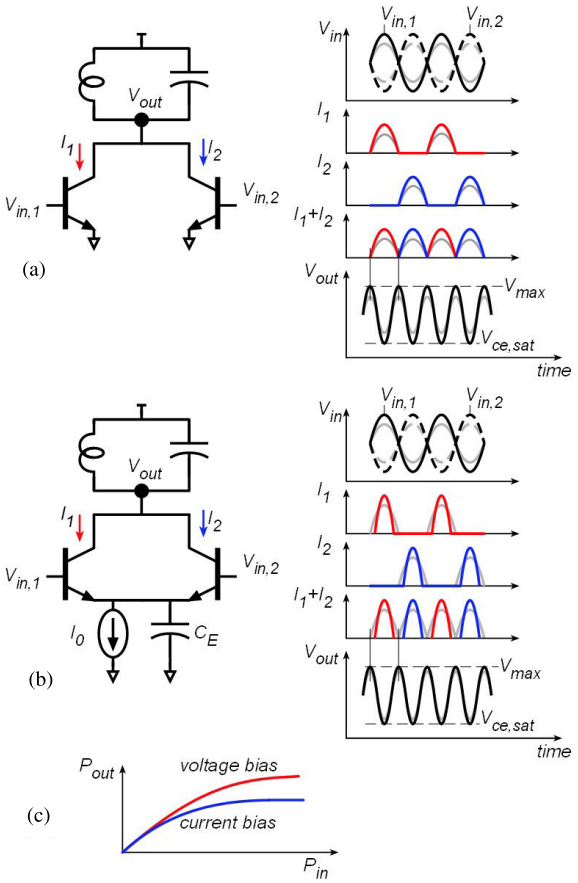

Fig. 5. Balanced frequency doubler with voltage and current waveforms with varying drive power for designs with (a) fixed voltage bias and (b) fixed emitter current bias. The fixed emitter current bias design shows a smaller variation (c) of output power with variations of input power.

far from the desired harmonic can be readily suppressed by bandpass filters in the transmitter or receiver, spurious harmonics generated by the first several multiplier stages are of greatest concern.

Within each frequency doubler stage, the adjacent fundamental and 3rd spurious harmonics would be suppressed by the differential circuit if it were perfectly symmetrical. Transistor or bias circuit mismatch, or unbalanced drive signals, will break this symmetry and thus will produce spurious harmonics. The interstage networks provide not only single-ended to differential conversion and impedance transformation, but also bandpass filtering, and thereby improving spurious harmonic suppression.

The frequency doublers rely on symmetry to suppress spurious odd harmonic outputs. Fabrication process variations will lead to circuit imbalances hence odd spurious harmonic generation. The foundry design kit does not provide statistical models of these variations. In simulations of the stage producing a 70-GHz output from a 35-GHz input, a 1.2:1 fractional imbalance of the emitter lengths of the two transistors in the doubler results in a spurious fundamental (35 GHz) output suppressed by only 20.5 dB relative to the power in the desired 70-GHz output.

B. Balanced Frequency Doubler Cell

The push-push emitter-coupled pair [19], if fabricated with identical transistors and provided with symmetric dc bias and RF drive signals is symmetric and hence will not generate spurious odd harmonics. Fig. 4 shows the circuit, its voltage and current waveforms, and the transistor loadline. The output tuning network of amplifiers can be designed for either the largest small-signal gain, or, for power amplifiers, for the largest saturated output power, the latter case having a load-line between the points, i.e., ($I_c = I_{c,max}, V_{ce} = V_{ce,sat}$) and ($I_c = 0$ A, $V_{ce} = V_{BR,CEO}$). Similarly, the multiplier output can be tuned for the greatest conversion gain or for the greatest saturated output power. If tuned for the greatest saturated output power, the loadline is as in Fig. 4, with

$$V_{ce} = \left(V_{max} - V_{ce,sat}\right)\left(1 - (I_c/I_{max})^2\right) + V_{ce,sat} \qquad (1)$$

and with $V_{max} = V_{BR,CEO}$, this expression is a consequence of I_c being a half-wave-rectified cosine wave at frequency f_0, and V_{ce} a cosine wave at frequency $2f_0$. The designs reported here use the above load-line, but with $V_{max} = 2.0$ V, which is smaller than $V_{BR,CEO}$. This reduced output voltage decreases the doubler's saturated output power but increases its gain,

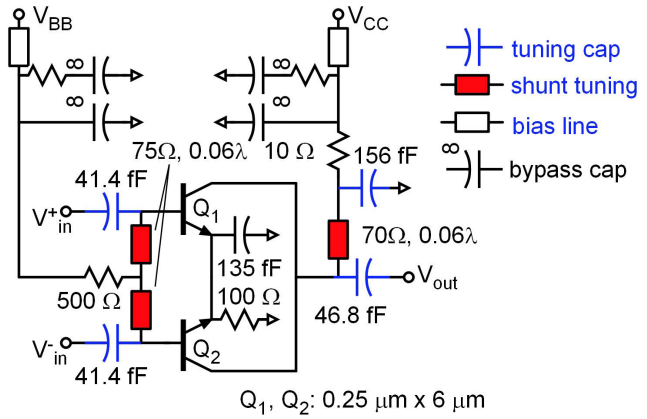

Fig. 6. Schematic of the 140–280-GHz frequency doubler with input and output matching networks.

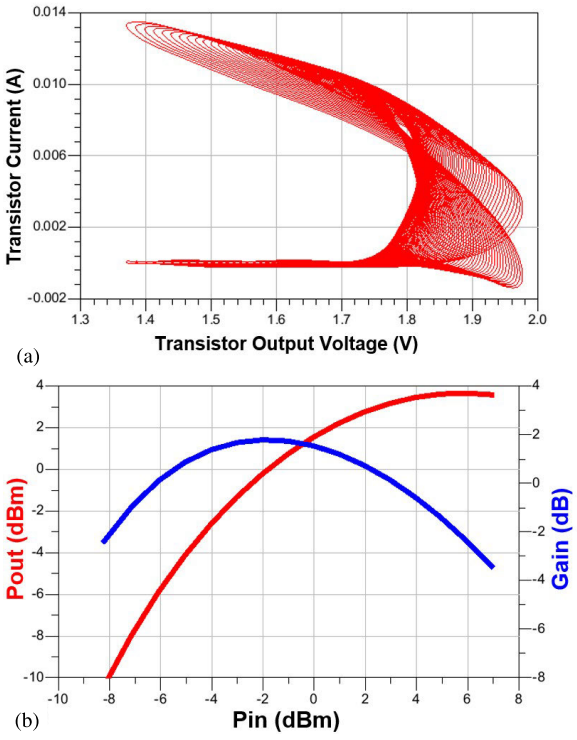

Fig. 7. (a) Simulated loadline (I_c versus V_{CE}) where P_{in} is swept from −12 to 2 dBm. (b) Simulated P_{out} versus P_{in} characteristics of the 140-280-GHz frequency doubler. The transistor current displayed in the loadline includes only the collector electron transport current and not the $C_{cb}dV_{cb}/dt$ displacement current associated with the collector base capacitance.

balancing output power and gain to maximize the doubler's power-added efficiency.

With maximum current densities set near the maximum safe value for the technology, this giving high transistor bandwidth, transistor emitter stripe lengths in the output doubler stage are adjusted to set the output power at the desired value. Preceding stages are similarly sized so that each stage has sufficient output power to drive the subsequent stage, avoiding the need for interstage amplifiers and hence avoiding their added power consumption.

Driven at f_{in}, the doubler produces outputs at not only $2f_{in}$ but also at dc. Depending on the bias circuit design, this RF to dc conversion can shift the transistors' dc bias,

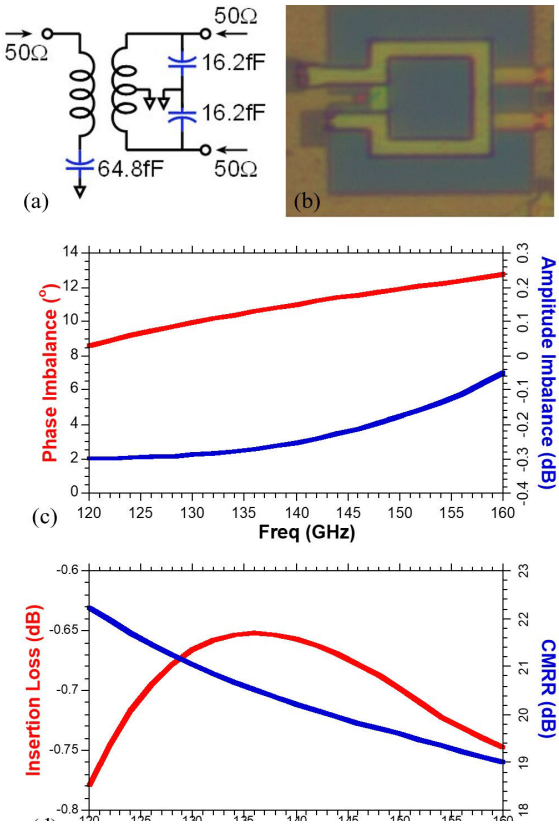

Fig. 8. 140-GHz transformer balun (a) schematic, (b) die photograph, (c) simulated phase and amplitude imbalance, and (d) simulated insertion loss and CMRR.

thereby changing the doubler's output power at $2f_{in}$. Fig. 5(a) shows that if the emitter-coupled pair is biased with a fixed dc voltage V_{BE} (using, e.g., a current mirror) then increasing the RF input power will, over the $1/2f_{in}$ conduction period of each transistor, increase the total charge delivered by each transistor to the output resonant circuit. The amplitude of the RF output voltage at $2f_{in}$ will therefore increase. If, instead [Fig. 5(b)], the emitter-coupled pair is dc biased with a constant dc current source I_0, this bypassed to ground with a low impedance at f_{in} by C_E, then, over the $1/2f_{in}$ conduction period of each transistor, each transistor will deliver a charge $I_0/2f_{in}$ to the output circuit, independent of the amplitude of the RF input signal. The transistor peak collector current amplitude, occurring at low V_{CE}, is limited by the Kirk effect. This regulation of the pulse charge delivered to the output resonator reduces the variation of doubler output power with variations of input power, as depicted in Fig. 5(c).

Because implementing the current source I_0 with a transistor would require increased supply voltage, the emitter-coupled pair is instead biased through a $R_B = 500\ \Omega$ base resistor and a $R_{EE} = 100\ \Omega$ resistor (Fig. 6). This establishes a dc bias current $I_0 = (V_{BB} - V_{BE,dc})/(R_{EE} + R_B/\beta)$, providing a nearly constant bias current because variations in the input RF drive power cause only small variations in $V_{BE,dc}$. At low frequencies, R_{EE} provides common-mode stability.

Fig. 6 shows the schematic of the 140-280-GHz frequency doubler. Each transistor has a $0.25 \times 6 - \mu$m emitter-base junction and is biased at $J_E = 0.8$ mA/μm and $V_{CB} = 0.8$ V.

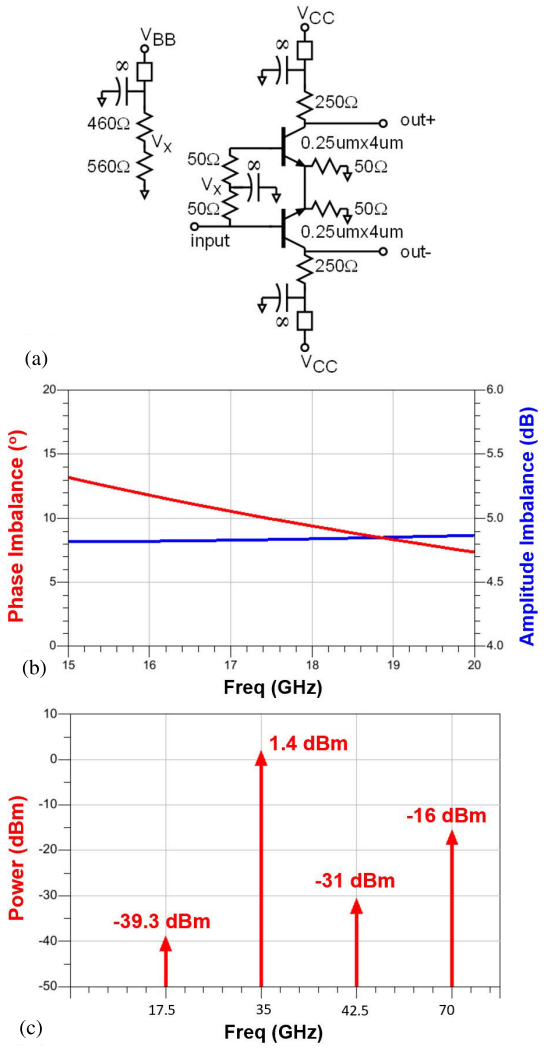

Fig. 9. Active balun (a) schematic and (b) simulated phase and amplitude imbalance. (c) Shows the simulated output spectrum of the 1st doubler stage integrated with the active balun, with $P_{in} = -13$ dBm.

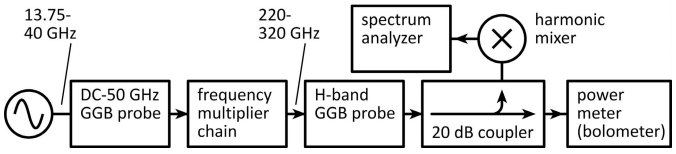

Fig. 10. Experimental setup for characterizing the frequency doubler.

To achieve the maximum P_{out}, the load line can be tuned to swing between V_{CEsat} and $V_{BR,CEO}$. Here, the load line is instead tuned with a smaller V_{max} for maximum PAE, with the output network tuned to provide this transistor load line when the external load is 50 Ω at 280 GHz. The large signal input impedances at V_{in}^{+} and V_{in}^{-} are tuned to 50 Ω at 140 GHz. Fig. 7(a) shows the simulated load line, while Fig. 7(b) shows the simulated output power as a function of input power; the simulation includes the input transformer. The simulated P_{out} is 1 with -1 dBm input power, hence, given similar characteristics for all doublers in the chain, interstage amplifiers are not necessary.

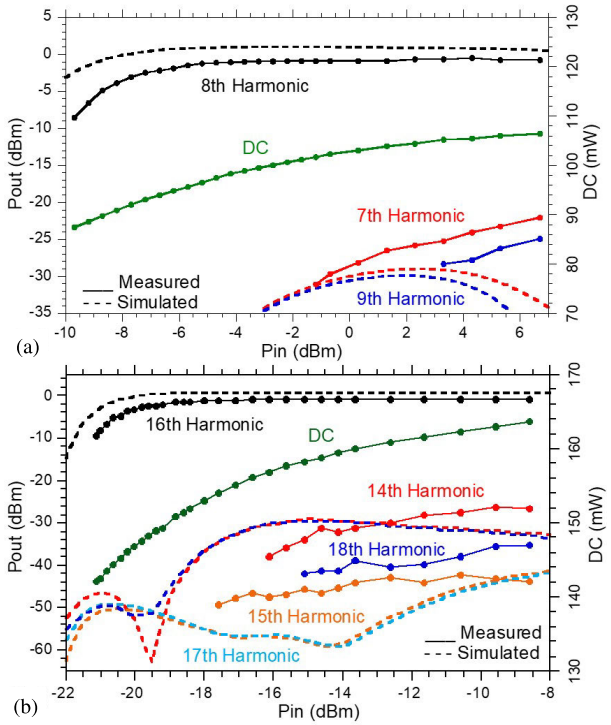

Fig. 11. Measured P_{out} versus P_{in} for the desired and spurious harmonics for (a) 8:1 multiplier with a 35-GHz input and (b) 16:1 multiplier with a 17.5-GHz input.

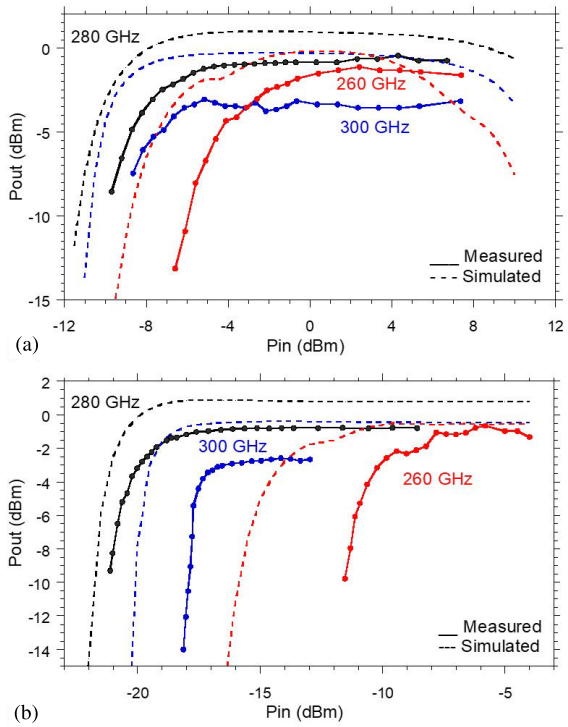

Fig. 12. Measured P_{out} versus P_{in} at 260, 280, and 300 GHz for (a) 8:1 multiplier and (b) 16:1 multiplier.

C. Single-Ended to Differential Conversion

Except for the first doubler in the 16:1 multiplier chain, differential input signals for all frequency doublers are generated using 1:1 passive transformers, as illustrated in Fig. 8(a). The transformers are implemented with the top two

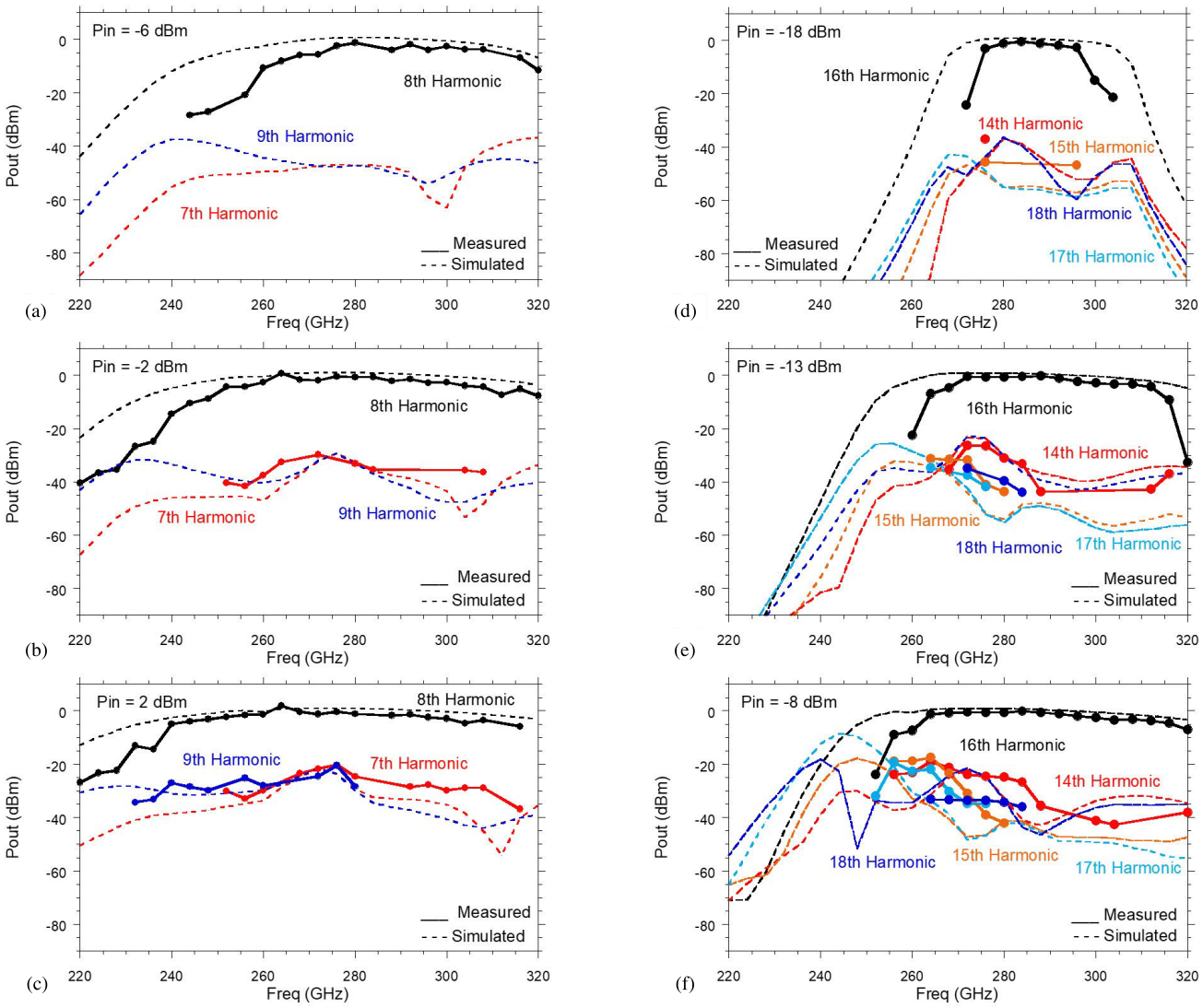

Fig. 13. Measured and simulated output power at the 7th, 8th, and 9th harmonics of the input frequency, for the 8:1 frequency multiplier chain, at (a) −6 dBm, (b) −2 dBm, and (c) 2-dBm input power. Measured and simulated output power at the 14th through 18th harmonics of the input frequency, for the 16:1 frequency multiplier chain, at (d) −18 dBm, (e) −13 dBm, and (f) −8 dBm input power.

metal layers to minimize loss [Fig. 8(b)]. Transformer line dimensions and the three capacitors are adjusted so that the transformer input impedance is 50 Ω when its two output ports are both loaded in 50 Ω. The 140-GHz transformer has a simulated phase imbalance of 8.5°–12.8° and an amplitude imbalance of 0.1–0.3 dB from 120 to 160 GHz, as shown in Fig. 8(c). At 140 GHz, the simulated insertion loss and CMRR are 0.6 and 20.2 dB, respectively [Fig. 8(d)].

The first doubler in the 16:1 multiplier chain uses a transistor differential pair for single-ended input to differential conversion [Fig. 9(a)]. This is because a transformer at this frequency would be physically very large and would consume excessive integrated circuit die area. The simulated phase imbalance is 7.3°–13.1° while, because of the small emitter resistive loading, the amplitude imbalance is poor at 4.7–4.8 dB from 15 to 20 GHz [Fig. 9(b)]. Despite this poor drive amplitude imbalance, in simulations [Fig. 9(c)] the adjacent odd-order spurious harmonics are suppressed by more than 32 dBc. The 4th harmonic is suppressed by 17.4 dBc. Current mirror biasing of the active balun would have provided better amplitude balance, but adequate spurious harmonic suppression was obtained from the first doubler stage even with resistive biasing. Because the active balun has considerable power gain, the required drive power for the 16:1 frequency multiplier chain is considerably smaller than that required for the 8:1 frequency multiplier chain.

III. Measurement Results

Fig. 10 shows the measurement setup. The output power spectrum is monitored by using a 20 dB *WR*-3 band directional coupler followed by an *WR*-3 band harmonic mixer (Oleson M03HWD) and a signal analyzer (Keysight N9030B). An Erickson PM4 power meter monitors the power at the through port of the 20-dB coupler. Before using this setup to characterize the frequency multiplier chains, the harmonic mixer and spectrum analyzer are calibrated by driving the input to the directional coupler with a 220-330-GHz swept-frequency tone from the 8:1 frequency multiplier chain, and then comparing the measurements of the power meter and of the spectrum analyzer's measurement of the 8th harmonic.

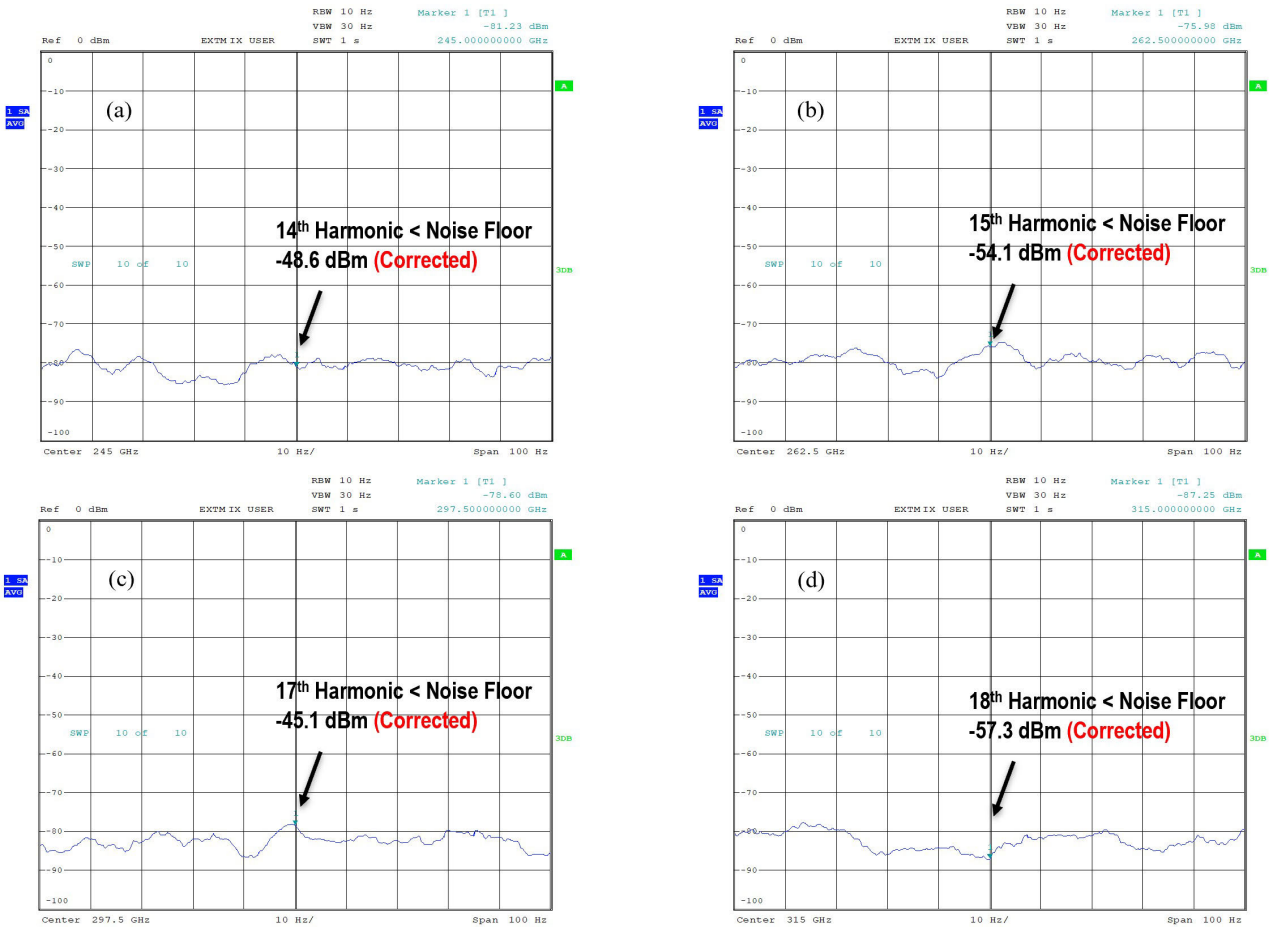

Fig. 14. Output spectrum of the 16:1 frequency multiplier chain, as measured by the harmonic mixer and spectrum analyzer, given −18 dBm input power at 17.5 GHz. (a) 14th Harmonic, (b) 15th harmonic, (c) 17th harmonic, and (d) 18th harmonic. All spurious harmonics within the 220–330 GHz band are below the instrument noise.

Because the spurious harmonics from the multiplier chain are suppressed by more than 25 dBc, more than 99% of the power measured by the power meter is in the 8th harmonic, hence the spurious harmonics only negligibly degrade the calibration accuracy. While subsequently characterizing the 8:1 and 16:1 multiplier chains, spurious harmonic power is measured using the harmonic mixer and spectrum analyzer. The mixer noise figure, high because of high-order harmonic mixing, limits the minimum detectable signal power of the spurious harmonics.

The 8:1 frequency multiplier was biased by dc probes at $V_{CC\times 8} = 2.9$ V, $V_{BB\times 8} = 1.9$ V, $I_{CC\times 8} = 29.8$ mA, and $I_{BB\times 8} = 1.2$ mA. A 2.9-V supply was selected as the frequency multiplier to be used in a 280-GHz transmitter whose power amplifier uses the same 2.9-V supply. At 280-GHz, the 8:1 multiplier has −0.6 dBm output power when −2 dBm input power is applied. With this input power, the 7th and 9th harmonics are below the instrumentation noise floor [Fig. 11(a)]. By increasing the input power to −1.2 dBm, the 7th harmonic power increases above the instrument noise to −31 dBm, while the input power must be increased to 3.3 dBm for the 9th harmonic power to be observed, at −28.3 dBm, above the instrument noise. The total dc power consumption is 102 mW, when −2 dBm input power is applied [Fig. 11(a)] and the core die area is 0.4 mm^2, as shown in Fig. 2(a).

The 16:1 frequency multiplier was also biased by dc probes at $V_{CC\times 16} = 2.9$ V, $V_{BB\times 16} = 1.9$ V, $I_{CC\times 16} = 45.1$ mA, and $I_{BB\times 16} = 3.6$ mA. At 280 GHz, the 16:1 multiplier has −1.1 dBm output power when −18 dBm input power is applied. With this input power, spurious harmonics are below the noise floor of the instrumentation [Fig. 11(b)]. Increasing the input power, first to −16.1 dBm, allows the 15th harmonic to be observed above the instrumentation noise at −47.4 dBm, then to $P_{in} = -14.6$ dBm allows the 14th harmonic to be observed above the instrument noise at −31.2 dBm, and finally increasing P_{in} to −13.6 dBm allows the 18th harmonic to be observed above the instrument noise at −38.7 dBm. The total dc power consumption is 162 mW, when −13 dBm input power is applied [Fig. 11(b)] and the core die area is 0.75 mm^2, as depicted in Fig. 2(c).

Fig. 12 shows the output power, at the desired harmonic, as a function of input power, with the input frequency tuned to give outputs at 260, 280, and 300 GHz. For the 8:1 multiplier operating with a 280-GHz output [Fig. 12(a)], the measured 8th harmonic power is −0.8 with 0 dBm input power, 1.7 dB less than that simulated. For the 8:1 multiplier operating with a 300-GHz output, the measured 8th harmonic power is −3.3 with 0-dBm input power, 3 dB less than that simulated. The disparity may be due to inaccurate large-signal transistor models at high frequencies [18]. For the 16:1

TABLE I
STATE-OF-THE-ART *WR*-3 BAND FREQUENCY MULTIPLIERS

Refrence†	Technology	Process Node (nm)	Multiplication	Frequency (GHz)	3-dB BW (GHz)	Chip Area (mm^2)	P_{out} (dBm)	P_{DC} (mW)	HRR (dBc)
RFIT-2017 [2]	CMOS	40	x3	300	22	1.85	2.3	410	NA
IMS-2021 [3]	CMOS	40	x9	223	20	1.7	4.1	185	35
TMTT-2011 [4]	SiGe BiCMOS	130	x18	325	11	0.95	-3	162	NA
RFIC-2014 [5]	SiGe BiCMOS	130	x16	245	30	0.98	2.5	700	NA
JSSC-2016 [6]	SiGe BiCMOS	55	x2	245	40	0.25	5.5	238	NA
SiRF-2017 [7]	SiGe BiCMOS	130	x6	240	15	0.75	-4	900	14
IJMWT-2017 [8]	SiGe BiCMOS	130	x8	236	40	1.2	0	250	25
CICC-2019 [9]	SiGe BiCMOS	130	x4	284	39	0.66	2.5	384	NA
MWCL-2020 [10]	SiGe BiCMOS	130	x8	244.5	81	0.86	-7.7	240	28
TMTT-2020 [11]	SiGe BiCMOS	130	x8	300	127	1	2.3	537	16
IMS-2021 [12]	SiGe BiCMOS	130	x4	252	48	0.29	5.5	270	20
IMS-2022 [13]	SiGe BiCMOS	130	x8	270	50	0.4	-5	125	25
MWCL-2022 [14]	SiGe BiCMOS	130	x18	240	41	0.28	6.2	429	25
TMTT-2023 [15]	SiGe BiCMOS	130	x6	240	68	0.2	9	480	15
EuMIC-2014 [16]	GaAs mHEMT	35	x8	260	100	3.25	2.5	NA	10
IMS-2018 [17]	InP HEMT	80	x6	250	45	2	5	125	NA
This Work [20]	InP HBT	250	x8	280	48	0.4	-0.6	102	28
This Work	InP HBT	250	x16	280	44	0.75	-0.6	162	26

† Spec values for other works were extracted from their text or otherwise estimated from the plots.

multiplier operating with a 280-GHz output [Fig. 12(b)], the measured 16th harmonic power is −0.8 with −13 dBm input power, 1.5 dB less than that simulated. For the 16:1 multiplier operating with a 300-GHz output, the measured 16th harmonic power is −2.6 with −13 dBm input power, 2.2 dB less than that simulated.

Fig. 13(a)–(c) show the measured output power of the 8:1 frequency multiplier chain at the 7th, 8th, and 9th harmonics, given −6, −2, and 2-dBm input power. With −2 dBm input power at 35 GHz, the measured 8th harmonic power is −0.6 dBm at 280 GHz and the −3 dB bandwidth is 48 GHz, with spurious harmonics suppressed by more than 28 dBc over this bandwidth. When the input power is increased to 2 dBm, the −3-dB bandwidth increases to 60 GHz, but the spurious harmonic rejection decreases by 8 dB. The input power can be adjusted for either high spectral purity or wider operating bandwidth.

Fig. 13(d)–(f) illustrate the measured output power of the 16:1 frequency multiplier chain at the 14th through 18th harmonics, given −18, −13, and −8 dBm input power. With −18 dBm input power at 17.5 GHz, the 14th, 15th, 17th, and 18th harmonics are below the instrument noise (Fig. 14). With −13 dBm input power at 17.5 GHz, the measured 16th harmonic power is −0.6 dBm at 280 GHz and the −3 dB bandwidth is 44 GHz, with spurious harmonics suppressed by more than 26 dBc over this bandwidth. When applied input power is increased to −8 dBm, the −3 dB bandwidth increases to 52 GHz, but the spurious harmonic rejection decreases by about 10 dB.

IV. SUMMARY

In this article, broadband 280 GHz 8:1, and 16:1 frequency multiplier ICs with high spectral purity are presented. The 8:1 frequency multiplier chain generates −0.6 dBm output power and has a −3 dB bandwidth of 48 GHz. Spurious harmonics are suppressed by more than 28 dBc over the frequency range of interest. The 16:1 frequency multiplier chain generates −0.6 dBm output power and has a −3 dB bandwidth of 44 GHz. Spurious harmonics are suppressed by more than 26 dBc over the frequency range of interest. With reduced input power, both designs show better spurious harmonic rejection but decreased bandwidth. The 8:1 and 16:1 frequency multipliers can be integrated with a power amplifier [21] to be used as a high-power source. Characterization of these multipliers with a spectrum analyzer and a lower-order harmonic mixer would permit measurement of spurious harmonic suppression at lower input power levels.

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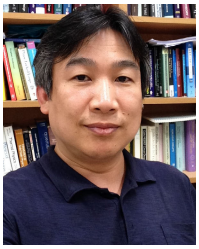
Utku Soylu (Member, IEEE) received the B.S. degree in electrical and electronics engineering from Boğaziçi University, İstanbul, Turkey, in 2018, and the M.S. degree in electrical and computer engineering from the University of California Santa Barbara, Santa Barbara, CA, USA, in 2019, where he is currently pursuing the Ph.D. degree.

In summer 2021, he joined Nokia Bell Labs, Murray Hill, NJ, USA, as an mm-Wave ASIC Research Intern. In summer 2022, he joined IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, as a Quantum Research Intern. His research interests include circuit, module, and system design for 200–300 GHz wireless communication links as well as cryo-CMOS circuit design for quantum computers.

Mr. Soylu received Analog Devices Inc. Outstanding Student Designer Award in 2022.

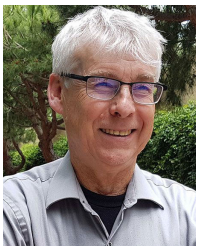
Amirreza Alizadeh (Member, IEEE) received the Ph.D. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2017.

From 2018 to 2019, he was an Assistant Professor with the Department of Electrical Engineering, Amir-Kabir University of Technology (Tehran Polytechnic), Tehran. From 2019 to 2021, he was a Post-Doctoral Research Scholar with the School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, USA, where he taught courses and performed research on full-duplex radios and phase noise of injection locked VCOs. From 2021 to 2023, he was a Staff Scientist with the Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA, USA, where he worked on realization of 210- and 280-GHz communication links. He is currently an Research and Development IC Design Engineer with Keysight Technologies, Santa Rosa, CA, USA. His research interests include RF and mm-wave integrated circuits and systems, mm-wave antennas in package, and mm-wave module design and packaging.



Munkyo Seo (Senior Member, IEEE) received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, South Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical engineering from the University of California at Santa Barbara (UCSB), Santa Barbara, CA, USA, in 2007.

From 1997 to 2002, he was an RF Engineer of designing microwave subsystems for wireless communication with LG Electronics Inc., Anyang, South Korea. From 2009 to 2013, he was with Teledyne Scientific Company, Thousand Oaks, CA, USA, where he worked on the design of various millimeter wave, terahertz, and high-speed mixed-signal circuits. In 2013, he joined the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, South Korea, where he is currently an Associate Professor.



Mark J. W. Rodwell (Fellow, IEEE) holds the Doluca Family Endowed Chair in electrical and computer engineering with the University of California at Santa Barbara (UCSB), Santa Barbara, CA, USA, and directs the SRC/DARPA ComSenTer Wireless Research Center. His research group develops high-frequency transistors, ICs, and communications systems.

Dr. Rodwell was a recipient of the 1997 IEEE Microwave Prize, the 1998 European Microwave Conference Microwave Prize, the 2009 IEEE IPRM Conference Award, the 2010 IEEE Sarnoff Award, the 2012 Marconi Prize Paper Award, and the 2022 SIA/SRC University Research Award.