A 272 GHz InP HBT Direct-Conversion Transmitter with 14.1 dBm Output Power

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***Abstract* — We report a fully integrated 272 GHz direct-conversion transmitter in 250 nm InP HBT technology. The transmitter has more than 18 dB conversion gain over 264-285 GHz, consumes 1.6 W, and has 14.1 dBm output power at 272 GHz. Its −3 dB bandwidth is 18 GHz, while its −6 dB bandwidth is 36 GHz. An internal 8:1 active frequency multiplier generates the local oscillator. To the authors' knowledge, the IC demonstrates record saturated output power for an integrated transmitter operating near 272 GHz.**

***Keywords* — direct-conversion, double heterojunction bipolar transistor (DHBT), H-band, high efficiency, indium phosphide (InP), millimeter wave.**

I. Introduction

The 200-300 GHz frequency range can support wireless backhaul links with capacities well above 100 Gb/s, serving future communications networks [1]. Integrated transmitters operating near 272 GHz have been demonstrated [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12] in several technologies. Key design objectives for such transmitters are high output power for increased link range and high bandwidth for high symbol rate hence high data rate. Here we report an integrated transmitter with a 14.1 dBm saturated output power, record for transmitters operating near 272 GHz. The transmitter −3 dB bandwidth is 18 GHz, while its −6 dB bandwidth is 36 GHz. With moderate post-equalization, this bandwidth should be sufficient to support 40 GSymbol/second QPSK data transmission.

II. Transmitter Design

The transmitter was fabricated in Teledyne 250 nm InP HBT technology [13], this having a maximum 650 GHz power gain cut-off frequency ($f_{\max}$) at top metal, a maximum 3 mA/μm current density, and 4.5 V $V_{\mathrm{BR,CEO}}$. The technology provides four Au interconnect layers, 50 Ω/square thin film resistors, and 0.3 fF/μm^2 MIM capacitors.

The transmitter has a broadband mm-wave power amplifier (PA), preceded by a PA buffer amplifier and up-conversion mixers for the in-phase (I) and quadrature-phase (Q) signals (Fig. 1). The mixers' local oscillators are generated by an 8:1 LO frequency multiplier, an LO buffer amplifier, and a passive LO quadrature phase generation circuit. In the PA, buffer amplifiers and frequency multiplier, the IC interconnects are microstrip lines (MSL's) using the lowest metal plane (M1) for ground. This provides lowest loss, hence best PA power-added efficiency (PAE). For the mixers, the interconnects are inverted

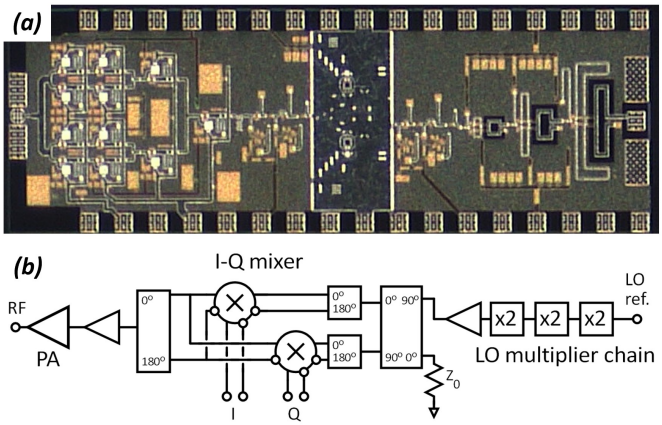

Fig. 1. 272 GHz direct-conversion transmitter: integrated circuit photograph (a), and block diagram (b). The IC is 2.8 mm x 0.92 mm.

microstrip lines (IMSL's), using the upper (M4) metal plane for ground. IMSL does not require holes in the ground plane where each transistor is placed. This minimizes ground-return parasitics in dense circuits having many transistors, such as (I, Q) Gilbert-cell mixers. At 272 GHz, 50 Ω MSL loss is 1 dB/mm while IMSL loss is 1.8 dB/mm. The simulated MSL to IMSL transition loss is less than 0.14 dB.

A. LO Multiplier (8:1)

The 272 GHz LO is generated from a 34 GHz input using three cascaded frequency doublers (Fig. 2a); the multiplier chain was earlier reported in [14]. Each balanced frequency doubler cell uses a push-push emitter-coupled pair. The chain has an input transformer balun. At 280 GHz, the measured 8th harmonic power is –0.6 dBm. With –2 dBm input power, the multiplier −3 dB bandwidth is 48 GHz. Adjacent harmonics are suppressed by better than 28 dBc; given the PA's and PA buffer amplifier's finite RF bandwidth, other LO harmonics will not result in significant transmitter spurious responses.

B. LO/PA Buffer Amplifier

The buffer amplifier increases the LO power to that necessary to drive the mixers. Though the DC bias circuit (Fig. 2b) is that of a pair of cascode stages, to provide the highest output power and PAE there is impedance tuning between the outputs of the common-emitter (CE) and the inputs of the common-base (CB) transistors. The buffer

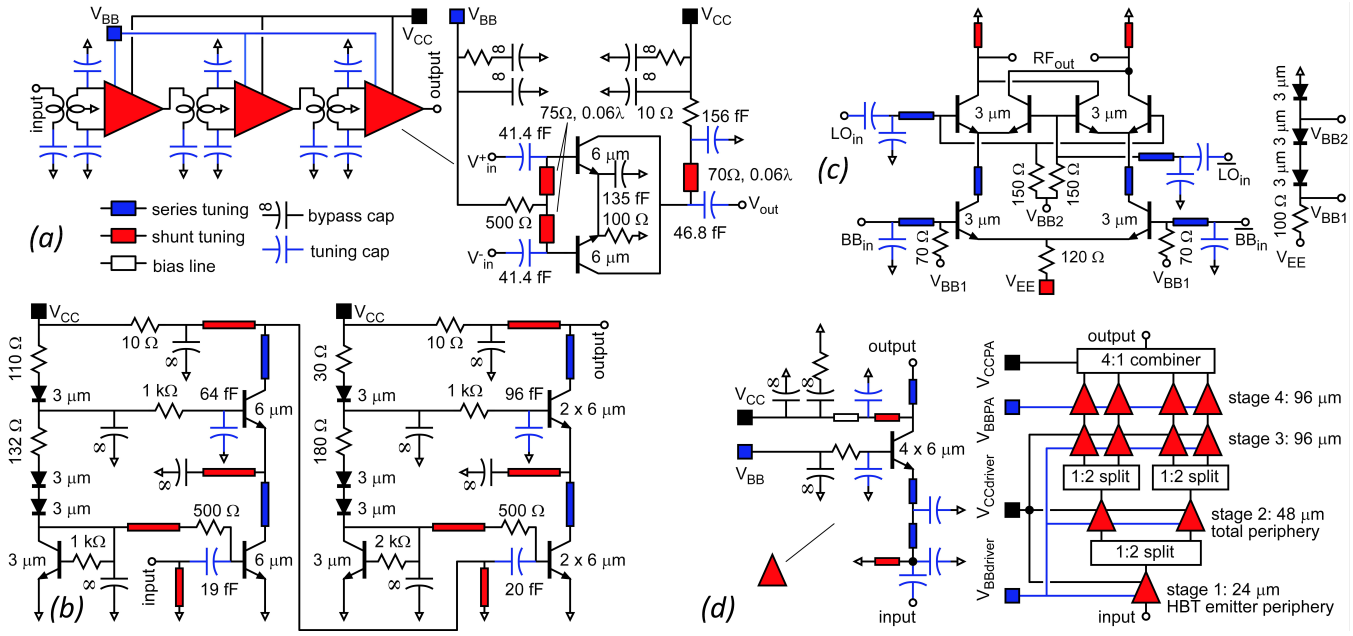

Fig. 2. Circuit schematics: (a) 8:1 LO frequency multiplier, (b) buffer amplifier for both the local oscillator and the power amplifier, (c) mixer, and (d) power amplifier.

amplifier is therefore best viewed as a four-stage (CE, CB, CE, CB) cascade. All inter-stage impedance tuning is for maximum saturated output power, given 0 dBm input power, not maximum small-signal gain. CE and CB transistors are individually stabilized, with the 500 Ω shunt resistors stabilizing the CE transistors and the finite base capacitance stabilizing the CB transistors. The finite base capacitance also provides significant cascade power combining between the CB and CE stages [15], [16]. In simulations, given 0 dBm input power, the output power is more than 7 dBm over 240-340 GHz. The simulated DC power is 160 mW. The same buffer amplifier is used to drive the PA.

C. I-Q Mixer

The LO driver amplifier output feeds a Lange coupler and a pair of transformer baluns, generating the four (0°, 90°, 180°, 270°) LO phases required for the I and Q mixers. Each mixer is double-balanced in the Gilbert configuration (Fig. 2c), with impedance-matching on the LO and RF ports and impedance-matching between the input BB and LO switching transistors. Series L, shunt C tuning networks increase the signal bandwidth on the baseband inputs. The I-Q mixers have a output inductive shunt tuning using short-circuited transmission-line sections. In the 272 GHz (I,Q) Gilbert cell mixer core, interconnect length imbalances will result in amplitude or phase imbalances between the I and Q channels; even a short 5-10 μm length interconnect will introduce 2-4° phase delay at 272 GHz. Transistor and interconnect spacings within the mixer core are therefore at the minimum allowed by the process design rules, and the layout was designed for minimum asymmetry between the I and Q paths

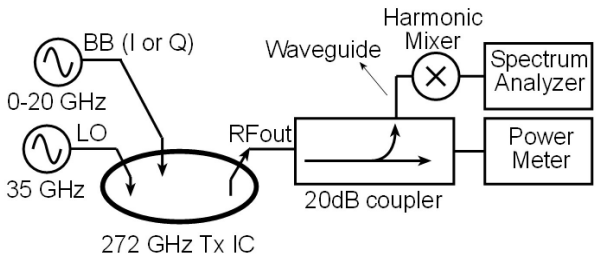

Fig. 3. Transmitter continuous wave (CW) testing setup.

D. PA

The PA uses four capacitively linearized common-base (CB) stages, designed for high efficiency and a compact layout (Fig. 2d), the PA was earlier reported in [17]. This design shows superior efficiency compared to common-emitter or grounded common-base at 1dB gain compression [16]. Four power cells (96 μm HBT periphery) are combined by a compact low-loss 4:1 transmission line network. Shunt inductive lines tune the transistor collector-base capacitances. Similar to transistor stacking, the capacitively linearized common-base stages provide significant cascade power-combining [15], with approximately 40% of the output power provided by stages 1-3. The measured saturated power of the reported PA [17] is 16.8 dBm at 270 GHz with greater than 4% PAE, while dissipating 1.09 W. In the version of the PA integrated into the transmitter, the shunt inductive transmission lines tuning the HBT output capacitances have been adjusted (made shorter) to provide peak saturated output power at 280 GHz.

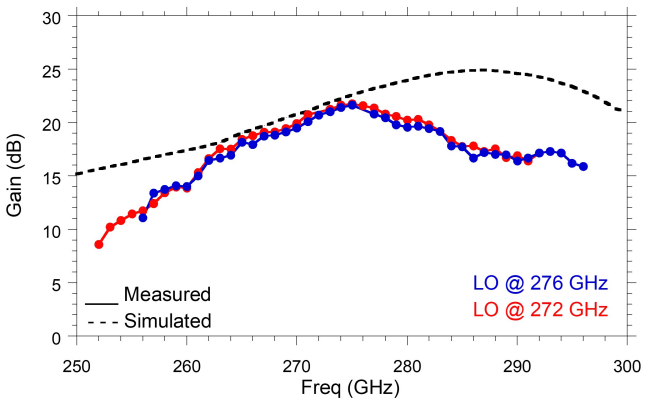

Fig. 4. Conversion gain vs. RF frequency at a fixed LO frequency.

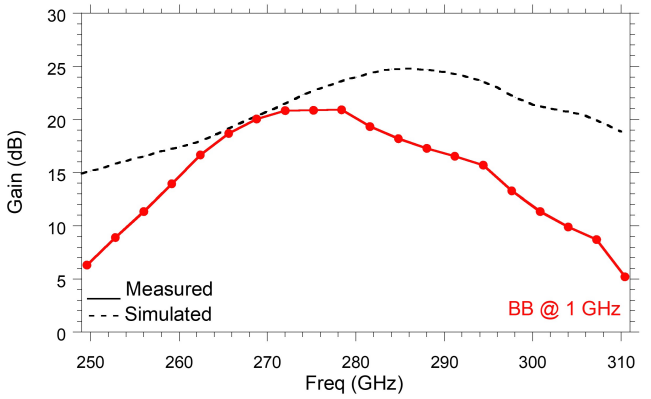

Fig. 5. Conversion gain vs. LO frequency at a fixed baseband frequency.

III. Measurement Results

Measurements (Fig. 3) were performed on a 3-mil thinned die (Fig. 1). Two synthesizers generated the LO and BB input signals, while the RF output signal was measured through a 220-330 GHz GGB wafer probe and a directional coupler. The coupler −20 dB port, connected to a harmonic mixer and spectrum analyzer, monitored the output power; before IC testing, this output power monitor was calibrated against a VDI/Erickson THz power meter. The transmitter output power was measured by a power meter and its spectrum was monitored by a spectrum analyzer. Measurements are corrected for the directional coupler and output probe loss using the losses stated on the datasheets.

In operation, the 8:1 multiplier was biased with V_{CCx8} = 2.9 V and V_{BBx8} = 2 V, drawing 31 mA and 1.51 mA respectively. The 4-stage PA was biased with V_{CCPA} = 2.5 V, $V_{CCdriver}$ = 3.15 V, V_{BBPA} = 2.3 V and $V_{BBdriver}$ = 1.76 V drawing 155 mA, 179 mA, 9.5 mA and 10.6 mA respectively. The LO buffer amplifier was biased with $V_{CCBuffer}$ = 5.2 V, and drew 42 mA. The PA buffer amplifier was biased with $V_{CCBuffer}$ = 5.2 V, and drew 41 mA from this supply. The mixers drew 22 mA from $V_{EEMixer}$ = −3.3 V. The DC power dissipation is 1.6 W.

The input baseband (BB) frequency was first swept with a fixed 272 and 276 GHz LO frequency (Fig. 4). The peak measured conversion gain was 21.7 dB, 3.2 dB less than simulated, and the frequency of peak conversion gain is 12 GHz less than simulated. The measured −3 dB bandwidth is 18 GHz, while the measured −6 dB bandwidth is 36 GHz. The LO frequency was then swept with a fixed 1 GHz BB frequency (Fig. 5). This showed 20.8 dB measured conversion gain at 272 GHz and ∼36 GHz LO tuning bandwidth at the −6 dB points.

To measure the transmitter saturated output power and 1 dB gain compression point, the input BB power at 1 GHz was swept while applying a 272 GHz local oscillator. The measured P_{in1dB} was -19 dBm (Fig. 6). The measured saturated output power was 14.1 dBm at 272 GHz (Fig. 7).

Table 1 compares the present and prior results for transmitter ICs operating in the 220 GHz - 330 GHz frequency band. The IC here reported establishes a new record, in any technology, for output power of an integrated transmitter operating near 300 GHz.

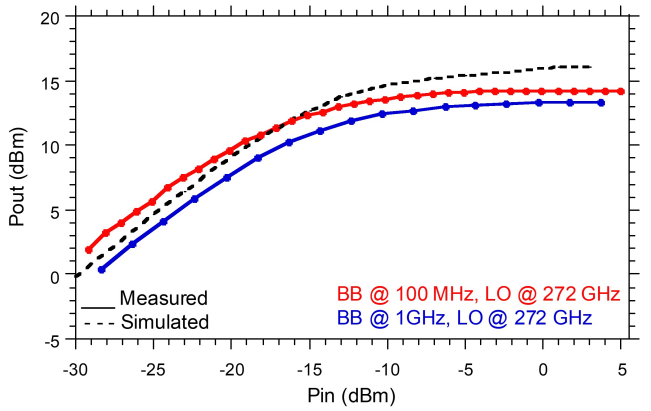

Fig. 6. RF output power vs. baseband input power.

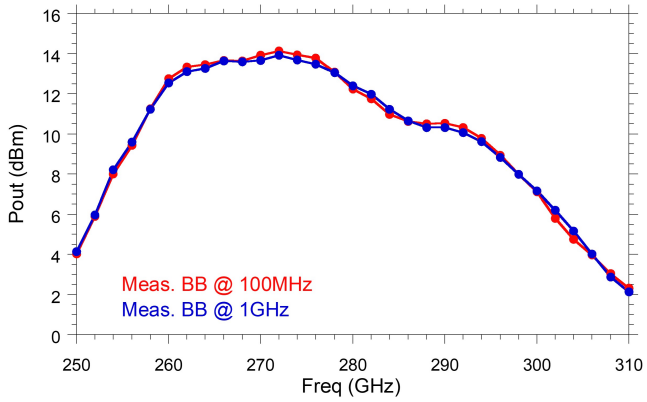

Fig. 7. Saturated RF output power vs. RF frequency.

IV. Conclusion

In this paper, a fully integrated 272 GHz transmitter with record output power is presented. The peak conversion gain is 21.7 dB with 36 GHz of −6 dB modulation bandwidth. The measured saturated output power is 14.1 dBm at 272 GHz with 1.6 W dissipation, and 1.6% DC-to-RF efficiency.

Table 1. Comparison of the recently reported integrated circuit transmitters operatig in the 220 GHz - 330 GHz frequency band.

Reference	**Technology**	**Circuit Blocks**	**Frequency (GHz)**	P_{sat} **(dBm)**	P_{DC} **(mW)**	**Efficiency (%)**
JSSC-2014 [2]	CMOS SOI 32 nm	LO VCO, OOK mod., PA, antenna	210	4.6	240	1.2
JSSC-2015 [3]	CMOS 65 nm	IQ mixer, tripler	240	-0.5	220	1.2
JSSC-2019 [4]	CMOS 40 nm	IQ-mixer, LO Multiplier (3:1)	265.68	-1.6	890	0.08
MWCL-2019 [5]	SiGe HBT 130 nm	IQ-mixer, LO Multiplier (16:1), PA	220-255	5	960	0.33
IMS-2020 [6]	SiGe HBT 130 nm	IQ-mixer, LO Multiplier (8:1), PA	240	12	1237	1.28
TMTT-2021 [7]	SiGe HBT 130 nm	Fund-mixer, LO Multiplier (4:1)	300	-4.1	300	0.13
TMTT-2011 [8]	GaAs mHEMT 0.1 μm	IF-mixer, LO Multiplier (2:1), PA, antenna	220	-6	110	0.23
IMS-2012 [9]	GaAs mHEMT 50 nm	IF-mixer, PA	240	1	N/A	N/A
JSSC-2020 [10]	InP HEMT 80 nm	IF-mixer, LO driver, PA	290	12	6600	0.24
TTST-2015 [11]	InP HBT 250 nm	IF-mixer, LO driver, LO oscillator	298.1	-2.3	452	0.13
IMS-2021 [12]	InP HBT 250 nm	IQ-mixer, LO Mult.(8:1), Phase Shifter, PA	200	15.3	1250	2.71
This work	**InP HBT 250 nm**	**IQ-mixer, LO Multiplier (8:1), PA**	**272**	**14.1**	**1600**	**1.6**

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REFERENCES

[1] M. J. W. Rodwell *et al.*, IC and array technologies for 100-300 GHz wireless, in *IEEE Custom Integrated Circuits Conference (CICC)*, Newport Beach, CA, USA, April 2022, pp. 1-5.

[2] Z. Wang *et al.*, A CMOS 210-GHz Fundamental Transceiver With OOK Modulation, in *IEEE Journal of Solid-State Circuits*, vol. 49, no. 3, pp. 564-580, March 2014.

[3] S. Kang, S. V. Thyagarajan and A. M. Niknejad, A 240 GHz Fully Integrated Wideband QPSK Transmitter in 65 nm CMOS, in *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2256-2267, Oct. 2015.

[4] S. Lee *et al.*, An 80-Gb/s 300-GHz-Band Single-Chip CMOS Transceiver, in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3577-3588, Dec. 2019.

[5] P. Rodríguez-Vázquez, J. Grzyb, B. Heinemann, and U. R. Pfeiffer, A 16-QAM 100-Gb/s 1-M Wireless Link With an EVM of 17% at 230 GHz in an SiGe Technology, in *IEEE Microwave and Wireless Components Letters*, vol. 29, no. 4, pp. 297-299, 2019.

[6] M. H. Eissa *et al.*, 100 Gbps 0.8-m Wireless Link based on Fully Integrated 240 GHz IQ Transmitter and Receiver, in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, Los Angeles, CA, 2020, pp. 627-630.

[7] J. Yu *et al.*, A 300-GHz Transmitter Front End With 4.1-dBm Peak Output Power for Sub-THz Communication Using 130-nm SiGe BiCMOS Technology, in *EEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 11, pp. 4925-4936, Nov. 2021.

[8] M. Abbasi *et al.*, Single-Chip 220-GHz Active Heterodyne Receiver and Transmitter MMICs With On-Chip Integrated Antenna, in *EEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 2, pp. 466-478, Feb. 2011.

[9] D. Lopez-Diaz *et al.*, A subharmonic chipset for gigabit communication around 240 GHz, in *2012 IEEE/MTT-S International Microwave Symposium Digest*, Montreal, QC, Canada, 2012, pp. 1-3.

[10] H. Hamada *et al.*, 300-GHz-Band 120-Gb/s Wireless Front-End Based on InP-HEMT PAs and Mixers, in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 9, pp. 2316-2335, Sept. 2020.

[11] S. Kim *et al.*, 300 GHz Integrated Heterodyne Receiver and Transmitter With On-Chip Fundamental Local Oscillator and Mixers, in *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 1, pp. 92-101, Jan. 2015.

[12] M. Seo *et al.*, A 200 GHz InP HBT Direct-Conversion LO-Phase-Shifted Transmitter/Receiver with 15 dBm Output Power, in *2021 IEEE MTT-S International Microwave Symposium (IMS)*, Atlanta, GA, USA, 2021, pp. 378-381.

[13] M. Urteaga *et al.*, InP HBT Technologies for THz Integrated Circuits, in *Proceedings of the IEEE*, vol. 105, no. 6, pp. 1051-1067, June 2017.

[14] U. Soylu, A. Alizadeh, M. Seo and M. J. W. Rodwell, A 280 GHz (x8) Frequency Multiplier Chain in 250 nm InP HBT Technology, in *2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Phoenix, AZ, USA, 2022, pp. 191-194.

[15] A. S. H. Ahmed, A. A. Farid, M. Urteaga and M. J. W. Rodwell, 204GHz Stacked-Power Amplifiers Designed by a Novel Two-Port Technique, in *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, Madird, Spain, 2018, pp. 29-32.

[16] A. S. H. Ahmed, *et al.*, A 140GHz power amplifier with 20.5dBm output power and 20.8% PAE in 250-nm InP HBT technology, in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, Los Angeles, CA, USA, 2020, pp. 492-495.

[17] A. S. H. Ahmed, *et al.*, A compact H-band Power Amplifier with High Output Power, in *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Atlanta, GA, USA, 2021, pp. 123-126.