A 200–250 GHz Low-Noise Amplifier in 130-nm InP HBT with 15.5 dB Gain and Record 5.3 dB Noise-Figure at 212 GHz

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***Abstract*— We present a low-noise amplifier (LNA) in Teledyne 130-nm InP technology, featuring peak 15.6 dB gain and better than 8 dB input return loss over the gain 3-dB bandwidth of 200–250 GHz. The designed LNA employs a cascade of five common-emitter stages and adopts a design procedure based on the minimum noise measure. The LNA achieves 5.75 ± 0.45 dB noise-figure (NF) in the measurement frequency range of 180–216 GHz. It consumes 0.25 mm^2 die area, including the DC bias pads, and dissipates 7.6 mW of DC power. To the authors' knowledge, this work demonstrates record NF results at 200 GHz and above for LNAs designed in any bipolar technology.**

***Keywords*— Indium phosphide (InP), heterojunction bipolar transistor (HBT), low noise amplifier (LNA), noise figure (NF).**

I. Introduction

The 100–300 GHz frequency band has drawn significant attention in recent years since the wide available spectrum leads to communication links with data rates up to 100 Gbs, and the short wavelengths enable greater integration levels [1]–[3] and hence larger capacities in multiple-input-multiple-output (MIMO) arrays. The signal-to-noise ratio (SNR) and the dynamic range (DR) of the mm-wave receivers are heavily dependent on the noise figure (NF) of the low-noise amplifiers (LNAs). Therefore, tremendous effort has been spent on improving the NF of the LNAs both at the device and circuit level, and LNAs implemented on high-electron-mobility transistor (HEMT) processes have exhibited NF values as low as 3.9 dB above 200 GHz [4]. LNAs on bulk and SOI CMOS technologies have achieved NF values of about 9 dB at 200 GHz [5], [6].

Although heterojunction bipolar transistors (HBTs) have noise performance inferior to that of HEMTs, THz InP HBTs have demonstrated yield and integration scales sufficient to realize fully integrated transmitters and receivers [7]. High-gain LNAs on SiGe HBT have shown 9–10 dB NF around 200 GHz [8], and 200-GHz InP HBT LNAs with about 7 dB NF have also been reported in the literature [9].

In this work, we present a 200–250 GHz LNA in Teledyne 130-nm InP HBT process (TSC130), which provides transistors with $V_{\mathrm{BR,CEO}} = 3.5$ V, $f_{\mathrm{T}} = 500$ GHz, and $f_{\max} = 1$ THz, when the reference plane is at top metal layer (M3) [10]. The LNA achieves NF of $\approx 5.75 \pm 0.45$ dB, peak gain of 15.6 dB, and gain 3-dB bandwidth of 200-250 GHz in measurements. To the best of the authors' knowledge, this work showcases record NF results at 200 GHz and above for LNAs designed in any bipolar technology, bridging the gap in competition with HEMT counterparts.

II. Circuit Design

The LNA design is focused on minimizing the noise measure (M), which sets a lower bound for the noise factor of an n-stage LNA with identical gain stages (F_{n}). Considering an available gain of G and noise factor of F for each stage,

$$\lim_{n\to\infty} F_{\mathrm{n}} = \frac{F - G^{-1}}{1 - G^{-1}} = 1 + M, \tag{1}$$

where $M = (F-1)/(1-G^{-1})$ [11], [12]. In theory, M is independent of the circuit topology (e.g., common-emitter vs. common-base) and embedding or pre-embedding circuits that might be used for gain boosting [13], provided that these embedding circuits are lossless and passive [11], [14].

Since, in the limit of lossless passive elements, M is independent of the stage configuration, the designer can choose between common-emitter (CE) and common-base (CE) topologies based on estimated layout losses, bandwidth requirements, and layout feasibility. For instance, due to its lower output impedance than the CB stage, the CE stage is more suitable for broadband designs [9]. On the other hand, CE stage is generally easier to implement, because, unlike the CB stage, there is no need for an additional capacitor in the base node to realize an ac ground.

One important point often neglected in CE vs. CB selection is that the interstage matching networks (ISMNs) employed between two neighboring stages in the chain introduce more loss for the CB selection. Fig. 1 shows these two scenarios, where for the CB case (Fig. 1(a)), an additional quarter wavelength ($\lambda/4$) short-circuit stub is required to provide a DC path for the emitter current. This stub introduces dissipative loss, particularly at mm-wave frequencies, and degrades the NF. In addition, due to the higher output impedance of the CB stage [9], its ISMN is often more lossy, particularly if a broadband design is targeted. Thus, here, we prefer the CE topology to implement the LNA.

At G-band frequencies, series DC-blocking capacitors show poor quality factors, and considering the low value of gain per stage (3 to 5 dB), they significantly impact the

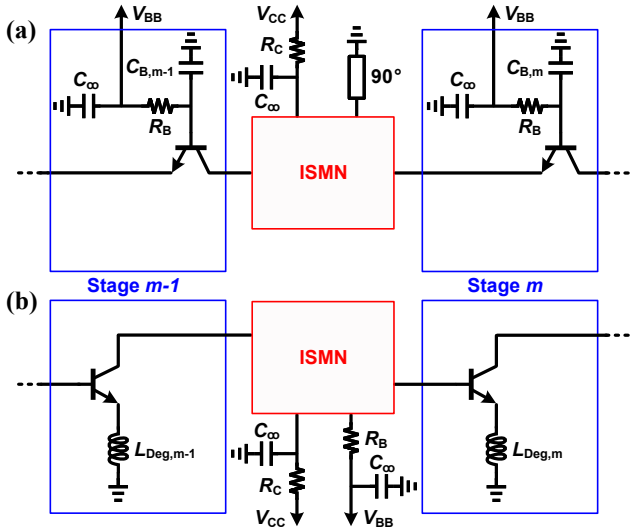

Fig. 1. Two neighboring stages of an LNA with (a) common-base and (b) common-emitter stages. ISMNs require a DC-blocking capacitor to separate the DC levels. R_B is large enough not to load the RF path.

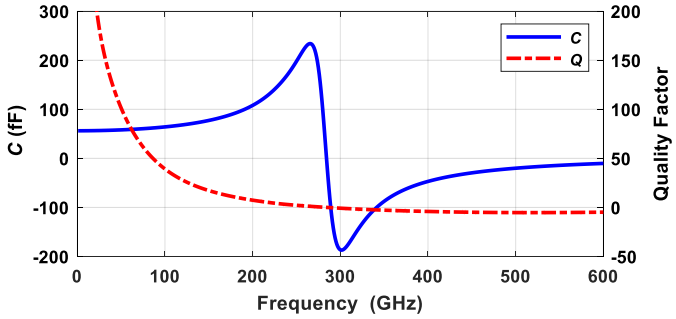

Fig. 2. Simulation results for the value and quality factor of a DC blocking series capacitor versus the frequency.

amplifier gain and noise performance. Fig. 2 features the frequency behavior and quality factor (Q_C) of a 56 fF series capacitor in the TSC130 technology, which shows impedance of $\approx 7.3\,\Omega$ at 200 GHz. With a self-resonance-frequency of 283 GHz, this capacitor achieves $Q_C \approx 7$ at 200 GHz. The low Q_C of series capacitors increase the dissipative loss and hence the NF. To avoid this, the series capacitor in the ISMN of Fig. 1(b) should be eliminated, which stipulates a DC-coupled design with $V_{CE} = V_{BE}$. It should be noted that the DC-coupled solution eliminates one of the feed lines in the ISMN (Fig. 1(b)), which also reduces the loss and improves the noise and gain performance.

Fig. 3 presents the F_n as a function of emitter current density (J_E) for an HBT with an emitter length (L_E) of 3 μm for collector-base voltage (V_{CB}) values of 0 and 0.2 V. At 200 GHz, the minimum F_n of 4.9 dB with associated gain per stage of 4 dB is achieved at $J_E \approx 0.4\,\text{mA}/\mu\text{m}$ and $V_{CB} = 0.2$ V. For a DC-coupled design (i.e., $V_{CB} = 0$ V), $J_E = 0.4\,\text{mA}/\mu\text{m}$ results in $F_n \approx 5.14$ dB with 3.2 dB gain per stage. The F_n for $V_{CB} = 0$ V is only 0.24 dB higher than the F_n for $V_{CB} = 0.2$ V. Since the gain per stage is low (4 dB for $V_{CB} = 0.2$ V), the loss introduced by series dc-blocking capacitors in ISMNs has

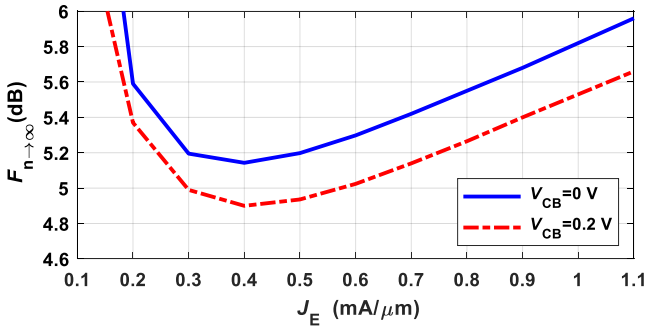

Fig. 3. Cascaded noise-figure vs. the emitter current density at 200 GHz for a 3 μm HBT biased at collector-base voltages of 0 and 0.2 V.

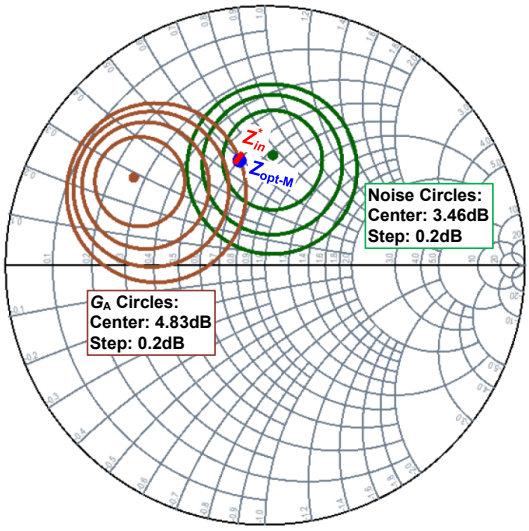

Fig. 4. Smith chart plot of the available gain (G_A) circles, noise circles, the source-plane impedance for the minimum noise measure ($Z_{opt\text{-}M}$), and the conjugate of the input impedance of the transistor (Z^*_{in}) at 200 GHz. The simulated device is an emitter-degenerated HBT (with $L_{Deg} = 11$ pH) in the CE topology, biased at $J_E = 0.4\,\text{mA}/\mu\text{m}$ and $V_{CB} = 0$ V.

a significant impact on the overall NF, and hence $V_{CB} = 0$ V is a wise choice to eliminate these capacitors. The F_n were also simulated for HBTs with 2, 4, and 5 μm emitter length, all resulting in a higher F_n compared to that for $L_E = 3\,\mu$m.

For a 3-μm HBT, $J_E = 0.4\,\text{mA}/\mu\text{m}$ is obtained for $V_{BE} \approx 0.83$ V, and the value of the emitter degeneration inductor (L_{Deg}) required for simultaneous gain and noise-matching is 10 and 11 pH for V_{CB} values of zero and 0.2 V, respectively. Fig. 4 shows the available gain (G_A) circles, noise circles, the source-plane impedance for the minimum noise measure ($Z_{opt\text{-}M}$), and the conjugate of the input impedance of the transistor (Z^*_{in}) on the Smith chart. The simulations are for an emitter-degenerated HBT ($L_{Deg} = 11$ pH) in the CE topology, biased at $J_E = 0.4\,\text{mA}/\mu\text{m}$ and $V_{CB} = 0$ V. All contours are shown in the plane of the source reflection coefficient.

Fig. 5(a) shows the schematic of the designed LNA. The LNA employs five inductively degenerated CE stages to achieve a gain of higher than 10 dB considering the loss of the matching networks. The design is DC-coupled with a supply voltage (V_{CC}) of 0.83 V and quiescent DC current of

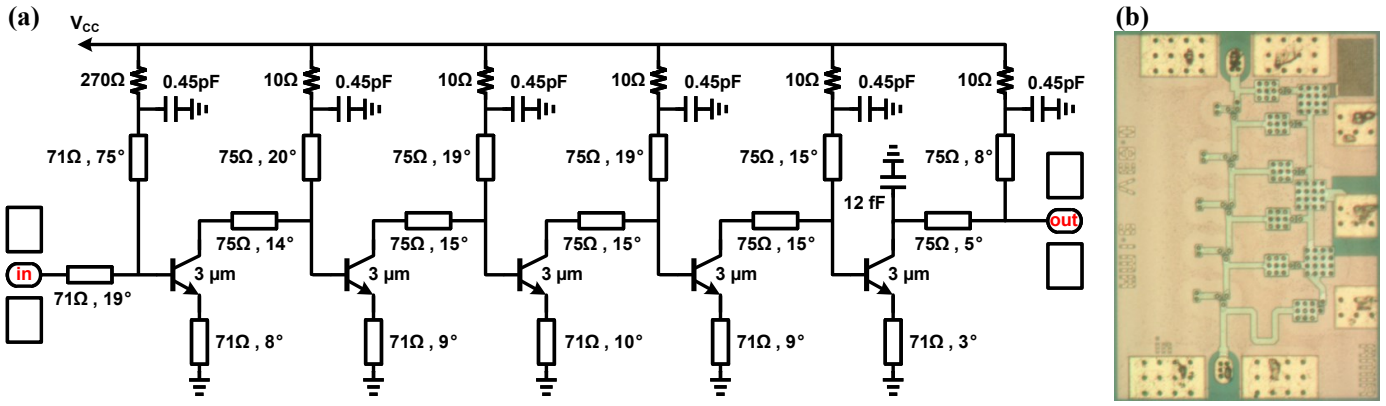

Fig. 5. (a) Circuit schematic and (b) die photo of the designed LNA in the 130-nm InP HBT technology from Teledyne Scientific. Design employs five DC-coupled common-emitter stages and consumes 0.6 mm × 0.41 mm die area.

$I_{CC\text{-}Q} \approx 9.1$ mA. The final design is optimized to achieve a broadband performance from 160 to 240 GHz, and therefore L_{Deg} values for different stages are slightly different. These inductors were replaced by short-circuit stubs in the final layout of the LNA.

The input matching network includes the input GSG RF pad and is designed to map the optimum noise-measure impedance (obtained from F_n simulations) to 50 Ω over 160–240 GHz frequency range. Since the LNA will be eventually used in a receiver with a direct on-wafer connection between the LNA and the down-conversion mixer, its output matching network has not been designed to feature a broadband matching to 50 Ω. All matching networks consist of a microstrip transmission line and a microstrip short-circuit stub that feeds the bias voltages. All passive structures were EM-simulated in Keysight RFpro.

III. Measurements

Fig. 5(b) features the die photo of the fabricated LNA in TSC130 technology. The chip area is 0.25 mm^2, including the bias and RF pads. On-wafer *S*-parameter characterization was performed using Oleson Microwave Lab (OML) 200–325-GHz VNA extenders (V03VNA2-T/R-A) with a Keysight PNA-X (N5245A). *S*-parameter calibration was performed using on-wafer multiline through-reflect-line (TRL) calibration standards with RF pads that matched the tested LNA.

Fig. 6 presents the simulated and measured *S*-parameters of the LNA biased at $V_{CC} \approx 0.83$ V and $I_{CC} \approx 9.1$ mA. There is a close resemblance between the simulated and measured *S*-parameters, but the measured S_{21} is higher than the simulated one. Given that the LNA uses five similar CE gain stages, 2.5 dB higher gain in measurements can be due to a slight gain increase (≈ 0.5 dB) in each CE stage.

The LNA noise figure is measured using the hot/cold *Y*-factor method. Fig. 7 shows the noise figure measurement setup. The VDI WR5.1 noise source was connected to the LNA input using a GGB WR-5 waveguide probe (220-GSG-75-BT). The probe loss of 1.54 dB at 200 GHz (from the probe manufacturer's measured data) was de-embedded from the measured noise figure. A low-noise post-amplifier (Mini

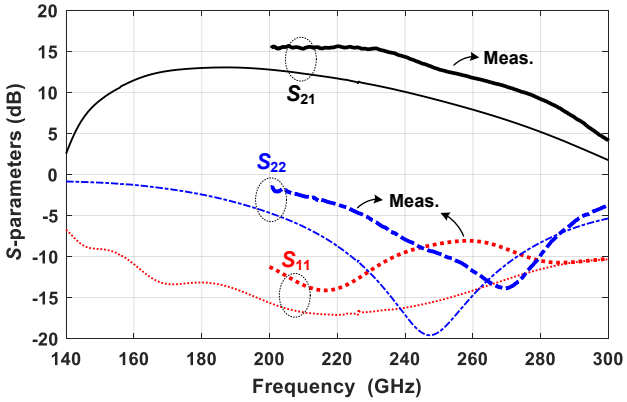

Fig. 6. Measured (thick lines) and simulated (thin lines) *S*-parameters of the five-stage LNA.

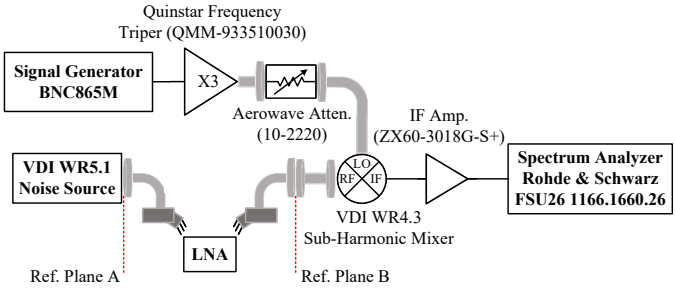

Fig. 7. Setup for noise-figure measurements. Based on probe manufacturer's measured data, the probe loss is 1.54 dB at 200 GHz.

circuit, ZX60-3018G+) was used to reduce the noise contribution of the spectrum analyzer.

Fig. 8 presents the simulated and measured NF. To plot this figure, the LNA gain values determined from NF measurements were compared to those from the measured S_{21}, and the NF data points were eliminated from the graph if the gain difference was more than ±1.5 dB. Above 200 GHz, the measured NF is smaller than the simulated counterpart. This can be due to higher LNA gain in measurements and hence suppressed noise contribution of the cascaded stages in the LNA. It is also worth mentioning that Teledyne's InP HBT processes have consistently shown a lower NF

Table 1. Performance Summary of Recently Published Low-Noise Amplifiers Operating Around 200-GHz.

Reference[◇]	Technology	Topology	3-dB Bandwidth (GHz)	Gain[†] (dB)	NF (dB)	P_{DC} (mW)	Area (mm^2)
EuMC-2022 [9]	250-nm InP HBT	2-stage CB	196–216	14.5	6.7–8.1	9.2	0.21
EuMC-2022 [9]	250-nm InP HBT	4-stage CE	196–216	13	6.8–7.6	19.2	0.28
EuMC-2021 [18]	130-nm SiGe BiCMOS	7-stage Cascode	236.8–250.8	28.5	13.7–14.2[‡]	97.2	0.45
IMS-2023 [8]	130-nm SiGe BiCMOS	3-stage Cascode	183–208	18.1	9–10	35	0.55
IMS-2019 [4]	25-nm InP HEMT	–	215–225	20	3.9–4.5	–	–
MWTL-2024 [19]	35-nm InP HEMT	4-stage CE	175–200	19.6	9.8–11.4	22	0.77
This Work	130-nm InP HBT	5-stage CE	200-250	15.6	5.3–6.2	7.6	0.25

[◇]Spec values for other works were extracted from their text or otherwise estimated from the plots. [†]Peak S_{21}. [‡]Simulation result.

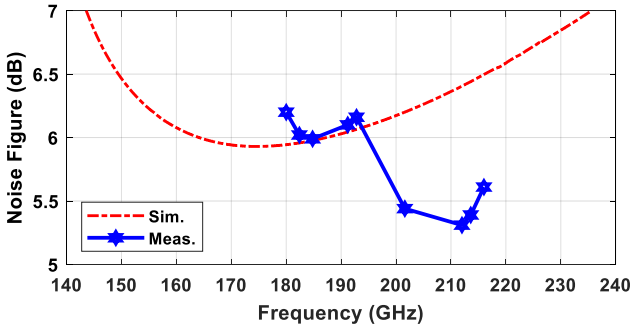

Fig. 8. Simulated and measured noise-figure of the LNA in 130-nm InP HBT.

in measurements than in the simulations. This includes the designs reported by UCSB [9], [15], Teledyne [7], [16], and other research groups [17].

A performance comparison between recently published LNAs [18], [19] operating around 200 GHz is presented in Table 1 where the presented LNA in this work achieves the lowest NF among the LNAs implemented on HBT processes.

IV. Conclusion

A five-stage common-emitter LNA is presented in this work, where each CE stage employs inductive degeneration to achieve simultaneous gain and noise matching. Since the series capacitors in the process have a relatively low quality factor at 200 GHz ($Q \approx 7$), the design is DC coupled, and thus no DC-blocking capacitors were used in the matching networks between the amplifying stages. This reduces the dissipative loss in the matching networks and improves the noise figure. To validate this idea, a proof-of-concept prototype was designed and fabricated in the 130-nm InP HBT process from Teledyne Scientific. The designed LNA achieves 15.4 dB peak S_{21} with 3-dB bandwidth of 200-250 GHz, noise-figure of $\approx$ 5.5 dB at 200 GHz, and DC power dissipation of 7.6 mW.

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