A 78-mW 220-GHz Power Amplifier With Peak 18.4% PAE in 250-nm InP HBT Technology

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***Abstract*— We report a three-stage power amplifier (PA), using 250-nm indium phosphide (InP) heterojunction bipolar transistors (HBTs), that achieves 18.4% peak power-added efficiency (PAE) with 18.8-dBm associated output power (P_{out}) and 13.8-dB associated power gain at 221.5 GHz. The amplifier has 19.5-dB peak S_{21} and 212–238-GHz 3-dB bandwidth. The output stage combines the output power of four power transistor cells, each cell being a capacitively degenerated common-base stage with four parallel HBTs, each HBT having 5-μm emitter length. Within each power transistor cell, separate base dc bias resistances for each emitter finger significantly increase the safe operation area (SOA), allowing dc bias at a greater collector current density at any given collector–emitter voltage. The increased SOA improves the amplifier P_{out} and power-added efficiency (PAE). The simulated loss of the 4:1 output power combiner is only 1 dB at 230 GHz. To the authors' knowledge, this is the highest published PAE for a transistor amplifier operating above 200 GHz.**

***Index Terms*— Common-base amplifier, hetero-junction bipolar transistor (HBT), high-efficiency amplifiers, indium phosphide (InP), mm-wave power amplifiers (PAs).**

I. Introduction

TRANSMITTERS and receivers operating at 220–330 GHz have potential applications in high-rate but short-range terrestrial wireless communications, airborne and satellite communications, synthetic aperture radar, and imaging systems for concealed weapons detection. In developing power amplifiers (PAs) for such systems, high output power, high power-added efficiency (PAE), high gain, and high power density (output power per unit IC die area) are key parameters. Because PAE and gain vary with output power, below we state the output power and gain reported at peak PAE. Above 200 GHz, all reported Si CMOS [1], [2], [3] and SiGe HBT [4], [5], [6] PAs have < 5% PAE. Higher PAE and output power have been reported with indium phosphide (InP) heterojunction bipolar transistor (HBT) technology. For instance, [7] reports a 202-GHz three-stage PA with 7.9% PAE, 18.3-dBm associated output power, and 15-dB associated power gain. [8] reports a three-stage PA with 4.1% PAE, 23.5-dBm associated output power, and 13.5-dB associated power gain at 200 GHz. [9] showcases a 200-GHz single-stage PA with 17.3% PAE, but both 12.7-dBm associated output power and 5.5-dB associated power gain are relatively low. [9] also presents a 200-GHz three-stage PA with 9% PAE, 17.8-dBm associated output power, and 15-dB associated power gain.

In this work, we report a 212–238-GHz PA in 250-nm InP HBT technology. At 221.5 GHz, the PA achieves 18.4% peak PAE, with 18.8-dBm (76 mW) associated output power and 13.8-dB associated power gain. To the authors' knowledge, this is the highest reported PAE for a transistor PA operating above 200 GHz.

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II. 250-nm InP HBT Process

The prototype PAs were fabricated in Teledyne's 250-nm InP HBT process [10], and PAs were designed using the Teledyne foundry design kit. HBTs with the reduced base–collector capacitance (C_{cb}) compared to baseline transistors in Teledyne's released process (TSC250) were made available for this fabrication run. The reduction in C_{cb} was primarily achieved through process modifications that allowed for scaling of the base contact pad area. For a 5-μm emitter length (L_E), an HBT with scaled base–collector mesa dimensions has about 20% reduction in extracted C_{cb} compared to a baseline TSC250 transistor. This results in f_{max} of 730 GHz for an $L_E = 5\,\mu$m reduced base post (RBP) transistor when compared to 650 GHz of the $L_E = 5\,\mu$m baseline transistor. The transition frequency (f_T) of a 5-μm RBP device biased at 1.5 mA/μm is 512 GHz.

III. Ballasted Multifinger Transistor Layout

The distribution of dc bias currents between fingers in a multifinger power transistor cell [Fig. 1(a)] is unstable [11], [12] if $\beta_T > 1$, where β_T is the electrothermal stability factor as

$$\beta_T \simeq \frac{V_{CE}\theta_{ja}}{R_B/\beta + R_{EX} + R_{EE} + kT/qI_C} \cdot \left.\frac{-\partial V_{BE}}{\partial T}\right|_{I_C} \quad (1)$$

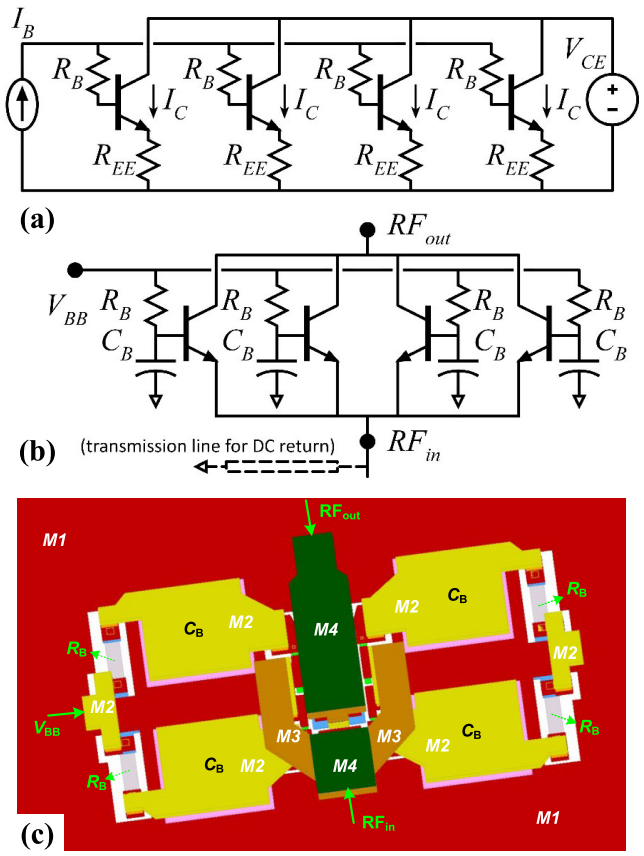

Fig. 1. (a) Distribution of dc bias currents between fingers in a multifinger power transistor cell as well as (b) circuit model and (c) layout of a $4 \times 5{-}\mu$m device in the common-base topology with base ballast resistors. ($C_B \approx 70$ fF and $R_B = 130\,\Omega$.)

in which $\partial V_{BE}/\partial T \simeq -0.8$ mV/K at 4 mA/μm^2 current density [11], and I_C, R_{EX}, and θ_{ja} are the dc current, parasitic emitter resistance, and thermal resistance of each emitter finger. Electrothermal instability can result in a disproportionally large fraction of the total dc bias current flowing in one emitter finger, with subsequent device failure. If the emitter fingers are sufficiently long, electrothermal instability can occur within a single finger, with a nonuniform dc current distribution along the finger, and, again, device destruction [11]. To avoid thermal instabilities within each finger, the emitter fingers should be kept sufficiently short. To avoid thermal instabilities between fingers, sufficient base (R_B) or emitter (R_{EE}) dc ballast resistance should be added to ensure that $\beta_T < 1$.

Because β_T increases with increased V_{CE}, in HBTs with long or multiple emitter fingers, electrothermal instability decreases the maximum V_{CE} that can be applied at a given dc bias current I_C; the safe operation area (SOA) is reduced. The present paper focuses on the IC design; a detailed characterization of the SOA of multifinger InP HBTs will be reported separately.

In the Teledyne 250-nm InP HBT technology, at $V_{CE} = 3$ V, an $L_E = 2\,\mu$m emitter length device fails at $J_C = I_C/L_E = 3.5$ mA/μm, but if ballasting is not added ($R_{EE} = R_B = 0\,\Omega$), a larger four-finger HBT with $L_E = 5\,\mu$m for each finger is observed to fail at a smaller $J_C = 1.75$ mA/μm at $V_{CE} = 3$ V. Adding ballasting [Fig. 1(b)], the $4 \times 5\,\mu$m HBT with $R_{EE} = 0\,\Omega$ and $R_B = 130\,\Omega$ is observed to fail at 2.7 mA/μm and

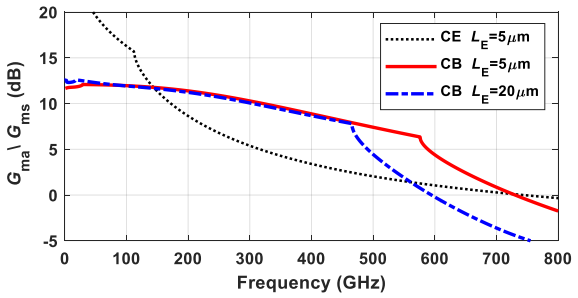

Fig. 2. Maximum available\stable gain ($G_{ma}\backslash G_{ms}$) of the $4 \times 5\,\mu$m device of Fig. 1(c) as well as $G_{ma}\backslash G_{ms}$ of a single-finger $5\,\mu$m device in the common-base topology. $G_{ma}\backslash G_{ms}$ of a 5-μm common-emitter device is also shown for comparison. All interconnect parasitics up to top-level metal (M4) were included in the electromagnetic simulations. For all devices, $V_{CC} = 2.5$ V and $J_C = 1.5$ mA/μm at zero RF input power.

$V_{CE} = 3$ V. Therefore, ballasting improves the SOA by more than 50%, and ballast resistances must be incorporated into the multifinger transistor layout without significantly reducing the transistor gain at 220 GHz. Fig. 1(c) shows the layout of a thermally ballasted $4 \times 5\,\mu$m HBT in common-base configuration. The capacitances C_B are adjusted to set the small-signal gain and gain compression characteristics [7].

Fig. 2 compares the maximum available\stable gain ($G_{ma}\backslash G_{ms}$), determined from the foundry single-finger HBT models and electromagnetic simulations (Keysight RF Pro) of the layouts, of an $L_E = 5\,\mu$m single-finger HBT in common-emitter and common-base configurations, and of the ballasted $4 \times 5\,\mu$m HBT. Simulations of all three devices include interconnect parasitics up to top-level metal (M4). Both the single-finger and four-finger common-base simulations employ $C_B = 70$ fF and $R_B = 130\,\Omega$ for each finger. In the simulations, $J_C = 1.5$ mA/μm at zero input power and $V_{CE} = 2.5$ V. The PA uses common-base stages because at 220 GHz these have significantly greater G_{ma} than the common-emitter stage. Note that the 595-GHz f_{max} of a 20-μm HBT is 83% of that of a 5-μm HBT (i.e., 730 GHz). This is due to resistive losses associated with the interconnects of the four-finger cell and resistive losses associated with the base capacitances C_B. Also, f_{max} simulated for the ballasted four-finger HBT is similar to that simulated for a four-finger unballasted design [7].

IV. Circuit Design

In addition to setting β_T, adjusting R_B and C_B also varies the stage gain, gain compression characteristics, and maximum modulation bandwidth. We examine these issues below.

A. Base Ballast Resistance (R_B)

If an ideal HBT is biased at a fixed dc current I_C while being driven by an ac base–emitter voltage $v_{be} = v_p \cos(\omega t)$, the transistor dc base–emitter voltage will, to leading order, vary as $V_{BE} = (nkT/q)\ln(I_C/I_S) - v_p^2/4V_t$, where n is the junction ideality factor, $V_t = nkT/q$, and I_S is the saturation current density. Note that the RF input power is proportional to v_p^2. Neglecting transistor RF parasitics, the bias current of the ballasted transistor [Fig. 1(b)] increases with RF drive power

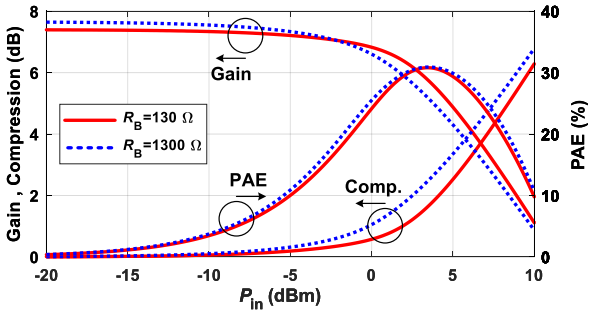

Fig. 3. Transducer power gain, PAE, and compression-level of a 5-μm common-base device with $C_B = 70$ fF versus P_{in} for $R_B = 130\,\Omega$ and $R_B = 1300\,\Omega$. In this simulation, $V_{CE} = 2.5$ V and $J_C = 1$ mA/μm at zero RF input power.

approximately as

$$I_C \approx I_{C,0} + \frac{v_p^2/4V_t}{R_B/\beta + R_{EX} + (nkT/q)I_{C,0}} \tag{2}$$

where $I_{C,0}$ is the dc collector current given no RF drive.

Fig. 3 shows the simulated transducer power gain, PAE, and gain compression, versus P_{in}, of a 5-μm common-base device with $C_B = 70$ fF, for $R_B = 130\,\Omega$ and $R_B = 1300\,\Omega$. Here, $V_{CE} = 2.5$ V and $J_C = 1$ mA/μm at zero RF input power. Larger values of R_B provide greater β_T, but smaller values of R_B provide a greater increase of I_C with increased RF input power, with consequently less simulated gain compression. The PA will distort signal modulation if the RF-induced changes in dc bias given by (2) adjust more slowly than the modulation symbol rate. The base bias circuit charging time is given by

$$\tau_{dc} \simeq R_B\left(C_B + \frac{1}{2\pi f_T}\left(R_{EX} + \frac{nkT}{qI_C}\right)^{-1}\right) \tag{3}$$

which is about 34 ps for $R_B = 130\,\Omega$. This value is sufficiently short for 1 GBaud but not 10 Gbaud modulation. As there is an RF potential at the HBT base node [Fig. 1(b)], very low values of R_B would result in significant RF dissipation in the resistor; this is negligible given $R_B = 130\,\Omega$.

B. Degeneration Capacitor (C_B)

Fig. 4 shows the simulated variation of P_{out}, PAE, and transducer power gain for a 5-μm common-base device with $R_B = 130\,\Omega$ and $C_B = 35$, 70, and 140 fF. In the simulations, $V_{CE} = 2.5$ V, while the base bias voltage V_{BB} is set such that $J_C = 1$ mA/μm when the RF input power is zero. Through input voltage division between C_{be} and C_B, and through shunt-series feedback between C_{cb} and C_B, nonzero impedance of the base degeneration capacitor (C_B) strongly reduces the stage small-signal gain, but has a much smaller effect on gain when the transistor is saturated, that is, $P_{in} \geq 7$ dBm in Fig. 4(a). Consequently, as C_B is reduced, the gain compression at peak PAE is reduced.

On the other hand, Fig. 4(b) shows that for low levels of gain compression (≤ 1 dB), a larger capacitor ($C_B = 140$ fF) results in a higher gain but inferior output power compared to a smaller capacitor ($C_B = 70$ fF). But, for operation at high levels of gain compression (≥ 3 dB), the value of C_B should be

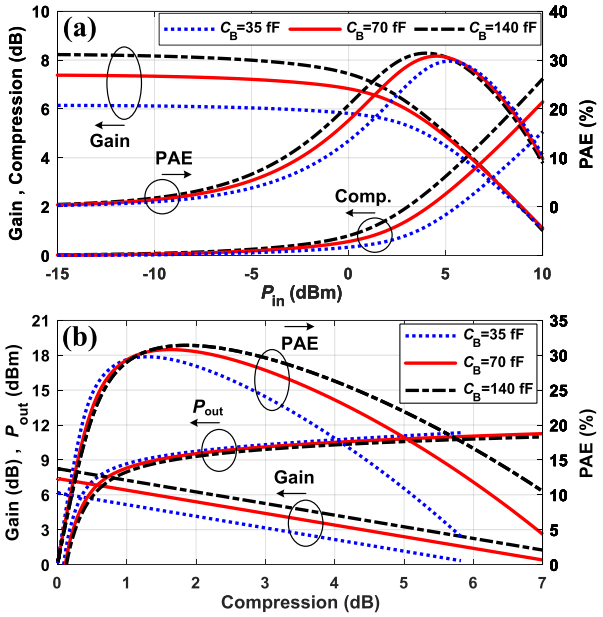

Fig. 4. (a) Transducer power gain, PAE, and compression level vs. P_{in}. (b) P_{out}, gain, and PAE vs. the compression level. The curves are plotted for a 5-μm common-base device with $R_B = 130\,\Omega$ and C_B values of 35, 70, and 140 fF. In the simulations, $V_{CE} = 2.5$ V, while the base bias voltage V_{BB} is set such that $J_C = 1$ mA/μm at zero RF input power.

increased to achieve enough gain at saturation. This extra gain comes at the cost of slightly lower output power. It is worth mentioning that, due to the series connection of feedback network (C_{cb}–C_B) at device input, the real part of the input impedance of the transistor decreases as C_B increases. This can increase the dissipative loss of the preceding passive network and thus degrade the overall PAE. Considering this, we choose $C_B = 70$ fF here to achieve an optimal PAE performance at ≤ 2-dB compression levels.

C. Stability Considerations

The stability of the transistor in the capacitively degenerated common-base structure is dependent on the values of R_B and C_B, and unconditional stability requires lowering of the quality factor of the base capacitance [9]. This is, however, not desired as it reduces the gain of the stage and hence the PAE. To achieve a higher gain, one can design the capacitively degenerated common-base stage to be conditionally stable. Fig. 5 presents the stability circles of the $4 \times 5\,\mu$m RBP transistor with $C_B = 70$ fF, $R_B = 130\,\Omega$, and $J_C = 1.5$ mA/μm, along with the optimal load and input impedances of the device. The transistor is conditionally stable, which results in a higher gain and hence PAE compared to an unconditionally stable design. Conditional stability is not an issue here since the input impedance (Z_{in}) and load–pull impedance (Z_{Load}) of the device are far from the unstable region in the Smith chart.

D. Optimum Bias Point

Fig. 6(a) shows, as a function of current density, the simulated PAE, P_{out}, and gain, at 2-dB gain compression, of the four-finger common-base device of Fig. 1(c). At each simulated bias current density J_C, the load admittance

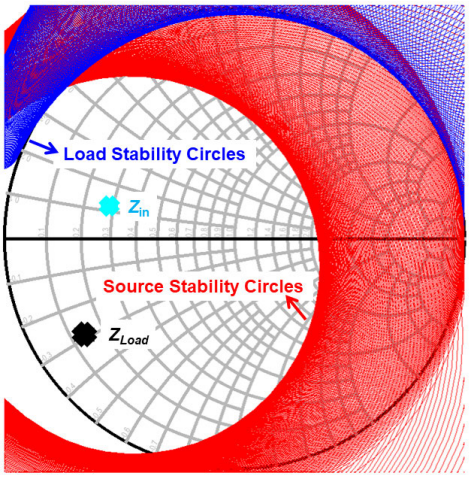

Fig. 5. Load and source stability circles of the 4 × 5 μm RBP transistor with $C_B = 70$ fF, $R_B = 130\,\Omega$, and $J_C = 1.5$ mA/μm, along with the optimal load and input impedances of the device.

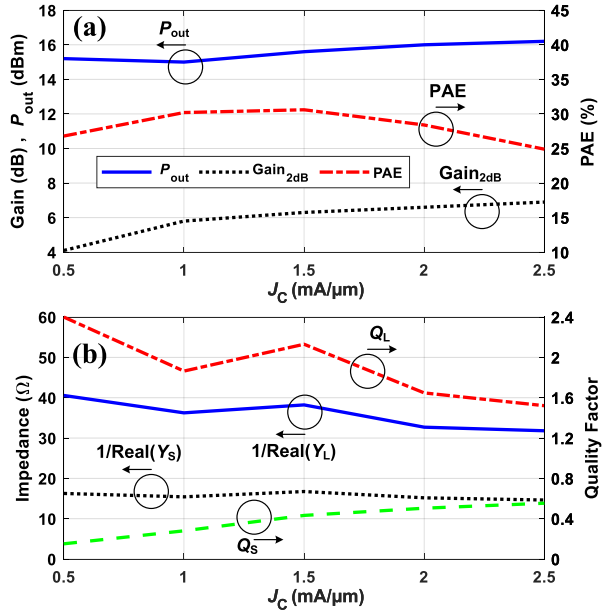

Fig. 6. (a) PAE, P_{out}, and transducer power gain of a 20-μm device shown in Fig. 1(c) at 2-dB compression point vs. the current density. (b) Quality factors of $Y_L = 1/Z_L$ and $Y_S = 1/Z_{in}^*$ as well as input and load-line resistances after resonating out the imaginary parts, that is, 1/Real(Y_L) and 1/Real(Y_S).

$Y_L = 1/Z_L$ is set at the value providing the greatest PAE, and the associated Z_{in} is found. Although the gain and P_{out} reach their maximum of 6.9 dB and 16.2 dBm, respectively, at $J_C = 2.5$ mA/μm, the greatest PAE (≈ 31%) is obtained at $J_C = 1.5$ mA/μm for which $P_{out} = 15.6$ dBm and gain is 6.3 dB. It is noteworthy that to study the performance of the 5-μm device, we run simulations at $J_C = 1$ mA/μm (Figs. 3 and 4). Nevertheless, due to higher interconnect parasitic and hence lower gain of the 20-μm device, $J_C = 1.5$ mA/μm was used in the IC design.

Fig. 6(b) shows the quality factors of Y_L and $Y_S = 1/Z_{in}^*$ (i.e., Q_L and Q_S), together with 1/Real(Y_L) and 1/Real(Y_S), which are the input and load-line resistances after resonating out the imaginary parts with parallel reactive elements (i.e., R_{in} and R_{out}). R_{in} is primarily set by the capacitive feedback and only weakly dependent on J_C, whereas R_{out} decreases as P_{out} increases. Moreover, Q_L is larger than Q_S and is the limiting factor if a broadband design is intended. For $J_C = 1.5$ mA/μm in this work, $Q_S \approx 0.4$, $Q_L \approx 2.1$, $R_{in} \approx 16.7\,\Omega$, and $R_{out} \approx 38.2\,\Omega$.

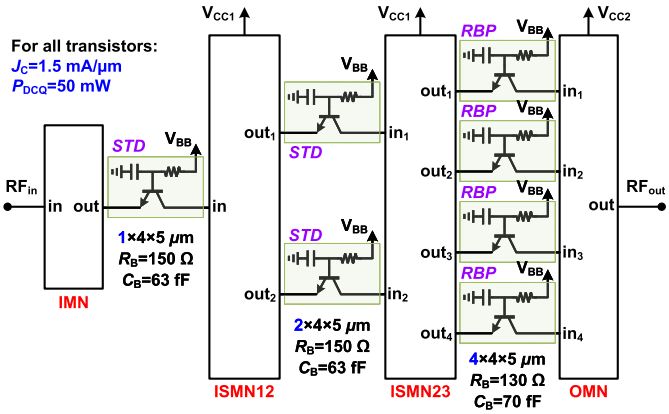

Fig. 7. System block diagram of the designed three-stage PA. The first-, second-, and third-stage transistors are compressed by 0.8, 1.2, and 2 dB, respectively. (STD: standard baseline transistor, RBP: reduced-base-post transistor.)

E. Multistage PA Design Considerations

The PA was designed with a target of 220-GHz center frequency, 10% bandwidth, ≥ 60 mW (17.8 dBm) output power with ≥ 20% associated PAE and ≥ 12-dB associated gain, ≥ 15-dB small-signal gain at 220 GHz, and better than 12-dB input return loss over the amplifier bandwidth. Given these design targets, the simulated 6–8-dB small-signal gain per stage [Fig. 4(b)], and c.a. 1-dB loss for each matching network (MN), the design uses three stages with a 2:1 staging ratio (Fig. 7). Given the target output power, and given anticipated 1-dB output matching and power-combining losses, the output stage uses four transistors, each four fingers with 20-μm total emitter length.

The total emitter periphery of the transistors in the second stage is determined by the drive requirement of those in the last stage. According to Fig. 4(a), a transistor with $C_B = 70$ fF and $R_B = 130\,\Omega$ needs $P_{in} = 4$ dBm at its 2-dB compression point. Therefore, four 4 × 5 μm transistors in the last stage of PA need $P_{in} = 16$ dBm. Considering 1-dB loss for the interstage matching network between stages two and three (ISMN23), transistors in the second stage must provide 17 dBm at a compression level (1.2 dB in this work) which is smaller than 2 dB. Fig. 4(b) suggests that a 5-μm device delivers minimum P_{out} of 8.4 dBm at its 1.2-dB compression (for all C_B values), and therefore two 20-μm transistors are sufficient to produce 17 dBm. Similarly, a 20-μm device in the first stage drives the transistors of the second stage while operating at its 0.8-dB compression point.

As mentioned above, the transistors in the first and second stages operate at their 0.8- and 1.2-dB compression, while the last-stage transistors are compressed by 2 dB, resulting in 4-dB compression of the three-stage PA. Because the RBP HBTs had not been extensively characterized, we used 4 × 5 μm standard (STD) baseline transistors in the driver stages with the same layout as the RBP device shown in Fig. 1(c).

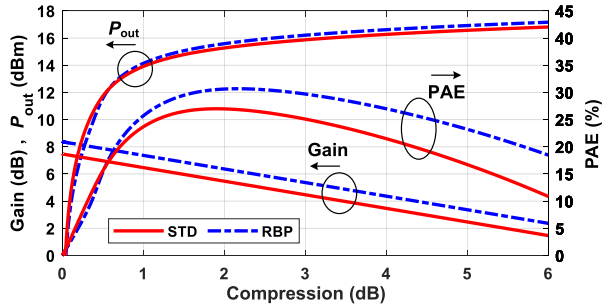

Fig. 8. P_{out}, transducer power gain, and PAE of a $4 \times 5\,\mu$m STD and RBP transistor, with a layout shown in Fig. 1(c), vs. the compression level. ($R_B = 130\,\Omega$, $C_B = 70$ fF, $J_C = 1.5$ mA/μm, and $V_{CC} = 2.5$ V.)

The simulated PAE, transducer power gain, and P_{out} of the $4 \times 5\,\mu$m STD transistor and its RBP counterpart are shown in Fig. 8 as a function of gain compression. The RBP and STD transistors have very similar P_{out} values with less than 0.3-dB difference, but the former has 1 dB more gain and superior PAE, particularly for $\geq$ 2-dB compression levels. Nevertheless, at the 0.8- and 1.2-dB compression levels required for the first- and second-stage transistors, the PAE difference is negligible.

The foregoing discussion suggests that the only drawback of using STD transistors instead of RBP ones in the driver stages is their lower gain. To compensate for this, while Fig. 4(b) indicates that the value of C_B should be reduced by 50% (i.e., from 70 to 35 fF) to improve the PAE at compression levels below 1 dB, we reduce the capacitor size by only 10% (to 63 fF) to achieve higher gain. The PAE penalty due to this choice is only 1%.

Once design of the active cells is finalized (L_E, R_B, C_B, and J_C values are chosen), the optimal load-line impedance and input impedance is calculated for each active cell of the three-stage PA and matching networks are designed based on these impedances. Finally, a circuit optimizer was used to achieve the best performance and compensate for the EM coupling between the different stages of the PA. The design of matching networks is explained below.

F. Output Matching Network

The OMN should combine the output powers of four transistors in the last stage of the PA with the least insertion loss possible. Furthermore, the mismatch loss of the OMN should be zero, which means that if a 50-Ω load is connected to the output port of the OMN, it should present the optimum load–pull impedance (Z_L) at its input ports. Z_L has a positive imaginary part (e.g., $Z_L = (6.9 + j14.7)\,\Omega$ at 220 GHz) to compensate for the parasitic collector–base capacitor (C_{cb}), necessitating the use of a shunt stub in the OMN. Considering this, there are four possibilities for the OMN, as shown in Fig. 9. The following points should be noted.

1) All four OMN circuits are symmetric with respect to the x-axis.
2) Output ground–signal–ground (GSG) pad is absorbed in the OMN and introduces about 0.2-dB loss.
3) L_{1b} and L_{2b} are determined by transistor spacing in layout and are not free parameters to optimize. The transistors should not heat each other, which is feasible if they are separated by a distance close to the substrate thickness (80 μm in this work).
4) The transmission lines (TLs) should be wide enough to handle the dc current of the transistors at power saturation. The top metal (M4) in the process carries 16 mA/μm and is used for TL implementation.

As the proposed power combiners do not guarantee port-to-port isolation, we have employed odd-mode resistors in between adjacent input ports to secure the odd-mode stability of the PA. To characterize the performances of the OMNs in Fig. 9, we developed an AEL script in Keysight ADS that generates the layout based on the given schematic and automatically runs EM simulation for it using the FEM engine. The script uses the least-mean-square (LMS) algorithm and adjusts the layout values to the point where all design goals are satisfied. For OMN simulations, we connect four input ports together and terminate them to $Z_L^*/4$ since ideally all ports have the same transfer function to the output port, which is connected to 50 Ω. Then, we run the AEL script to achieve input and output return losses of better than 15 dB at 200–250 GHz and S_{21} of greater than -0.2 dB at 225 GHz. This frequency is slightly higher than the target 220 GHz to compensate for the possible downward shift in the measurements.

The script simulated over 200 different layouts for each circuit in Fig. 9 and found the optimum solution. Fig. 10 presents the half-cell of the final layouts. Since the feed lines (L_{feed}) are close to the transistors in Fig. 10(a) and (b), the transistor spacing is increased to 124 μm to make room for L_{feed} between the neighboring transistors. In Fig. 10(c) and (d), L_{feed} is located far from the transistors and therefore the transistor spacing is 80 μm, which is slightly higher than the substrate thickness (75 μm) for effective heat dispersion.

Fig. 11 shows the insertion loss, return losses, and phase errors between the four input ports of the OMNs presented in Fig. 10. The OMN of Fig. 10(a) has the lowest insertion loss ($\approx$ 1 dB), wideband return losses that are better than 20 dB, and the best phase matching between its input ports.

The key observation here is that the shunt stub should be placed right next to the transistor since it transforms Z_L into an impedance with a higher real part and circumvents the need for low-impedance wide TLs after the point that the stub is connected. Wide TLs and hence wide bends and Tee junctions can excite higher-order evanescent modes at transmission-line junctions.

G. Interstage Matching Networks

Fig. 12(a) depicts the half-cell of the matching topology employed in ISMN12 and ISMN23. This circuit halves the P_{out} of the transistor connected to its input port and distributes it between the two transistors in the next stage. Two shunt stubs are necessary in the ISMN topology. The first stub (TL_1) is required to resonate out the parasitic C_{cb} and supply V_{CC}. The second stub (TL_3) provides a dc path for the emitter currents of CB transistors. Moreover, a series capacitor is also

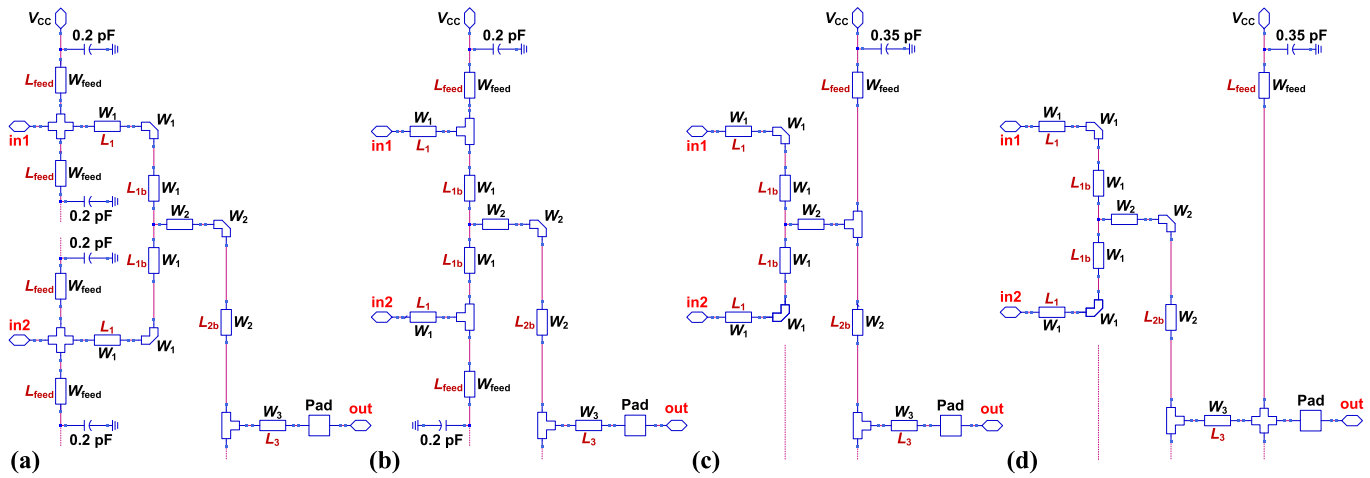

Fig. 9. Four possible OMN configurations. The output GSG pad is included in the OMN. (Half-cells are shown.)

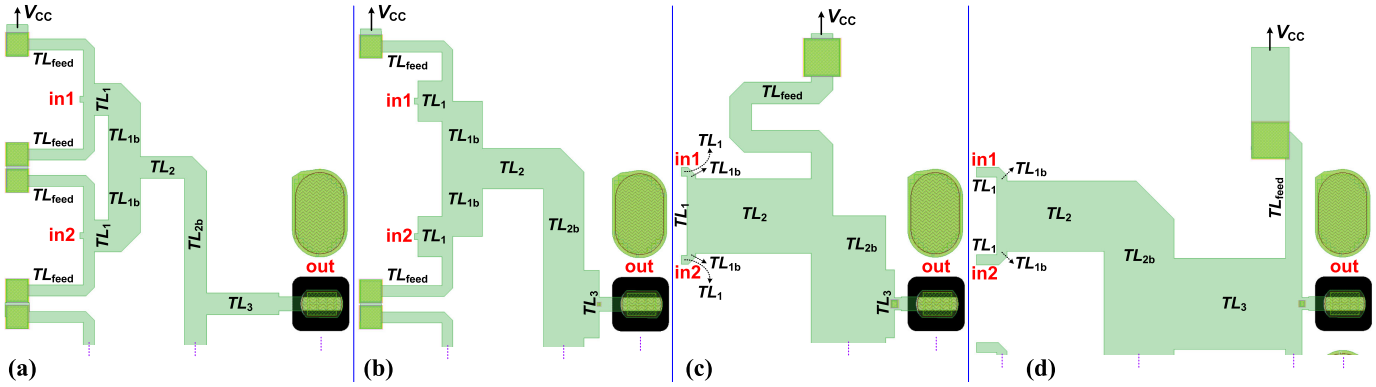

Fig. 10. Half-cell layouts of the OMN circuits shown in Fig. 9, each optimized for the best performance.

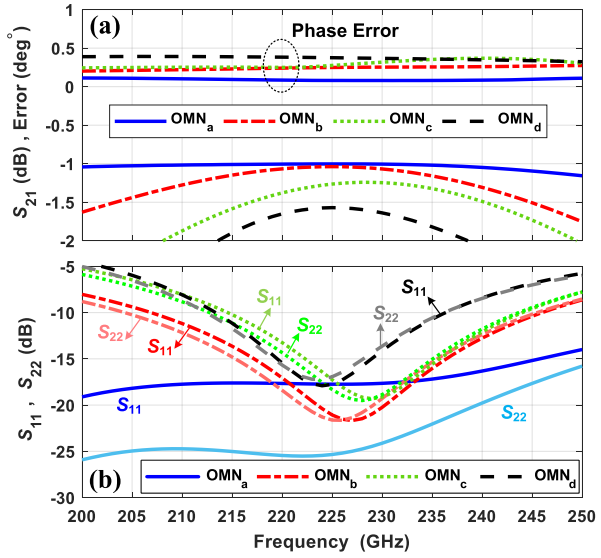

Fig. 11. (a) S_{21} and phase error between four input ports of the OMN. (b) Reflection coefficients at the input and output ports of different OMNs. Reference impedance at each input port is the complex conjugate of the load–pull impedance (Z_L^*) over 200–250-GHz bandwidth.

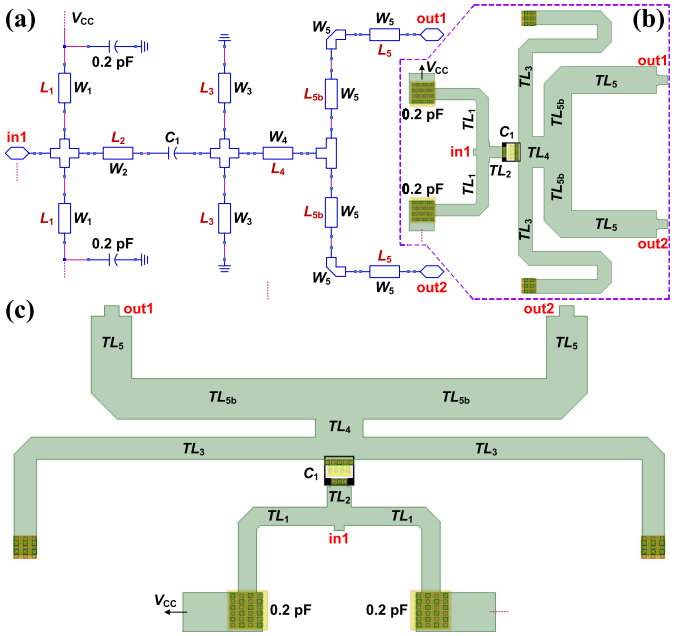

Fig. 12. (a) Half-cell schematic of the ISMNs. (b) Half-cell layout of ISMN23. (c) Half-cell layout of ISMN12.

needed in the ISMN half-cell to separate the dc levels of two subsequent stages. ISMN23 should preset $Z_{\text{LP-stg2}}$ (at 1.2-dB compression) at its input ports and $Z^*_{\text{in-stg3}}$ at each of its output ports. Similarly, ISMN12 should provide $Z_{\text{LP-stg1}}$ (at 0.8-dB compression) at its input port and $Z^*_{\text{in-stg2}}$ at each of its output ports. This impedance transformation must be done with the minimum insertion loss possible.

Fig. 13 illustrates the S_{21}, input and output reflection coefficients, and the phase mismatches of ISMN12 and

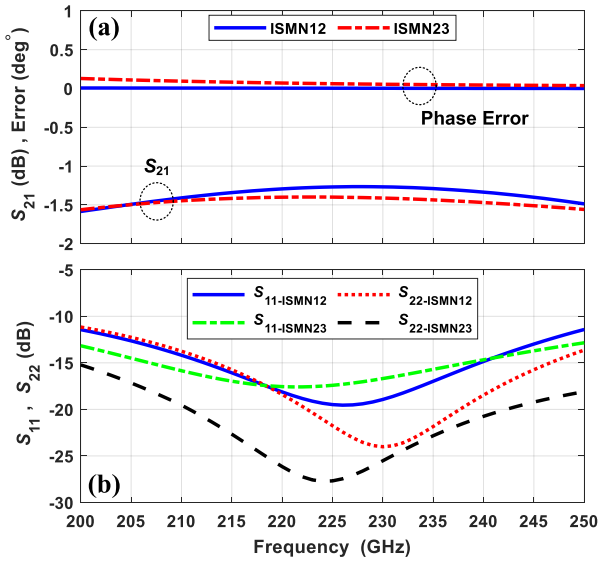

Fig. 13. (a) S_{21} and phase error of ISMNs. (b) Reflection coefficients at their input and output ports. The reference impedance at each input port is the complex conjugate of the load–pull impedance of the transistor at the preceding stage, while the input impedance of the transistor at the subsequent stage is used as the reference impedance at each output port.

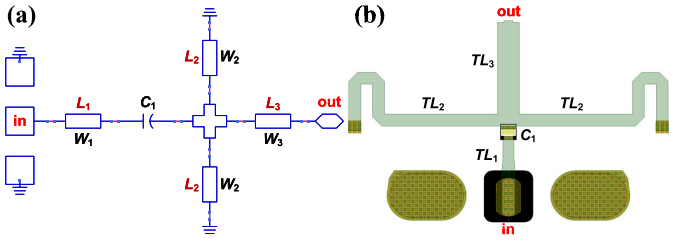

Fig. 14. (a) Circuit schematic. (b) Layout of the input matching network.

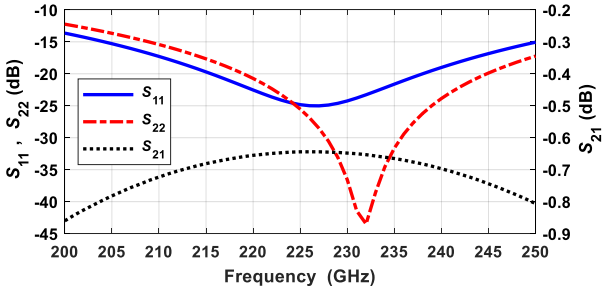

Fig. 15. S_{21} and reflection coefficients of the input matching network. The reference impedance at the input port is 50 Ω, whereas the input impedance of the first-stage transistor at 0.8-dB compression is used as the reference impedance at the output port.

ISMN23. Excluding 3-dB attenuation due to power splitting, ISMN12 and ISMN23 feature approximately 1.3 and 1.4-dB dissipative loss at 225 GHz. The mismatch loss is negligible since reflection coefficients are better than −17 dB at 225 GHz and lower than −12 dB over 200–250-GHz bandwidth. The ISMN loss is relatively high for CB amplifiers because the extra shunt stub that provides a dc path for the emitter current (TL_3) introduces about 0.5-dB loss.

H. Input Matching Network

Fig. 14 presents the circuit schematic and layout of the IMN. Similar to ISMNs, a shunt stub is necessary in the IMN topology to provide a dc path for the emitter current. The input GSG pad is also absorbed into the IMN, and the circuit is tuned to present 50 Ω and $Z^*_{\text{in-stg1}}$ at its input and output ports when the transistor in the first stage is compressed by 0.8 dB. The IMN loss and reflection coefficients are presented in Fig. 15. The average S_{21} is about 0.75 dB over the bandwidth, and the reflection coefficients are better than −12 dB.

V. Measurements

Fig. 16 shows the photograph of the implemented PA in 250-nm InP HBT process with a die area of 0.62 mm^2. On-wafer *S*-parameter characterization was performed using Oleson Microwave Lab (OML) 220–325-GHz VNA extenders (V03VNA2-T/R-A) with a Keysight PNA-X (N5245A). *S*-parameter calibration was performed using on-wafer multiline through-reflect-line (TRL) calibration standards with RF pads that matched the tested PA.

For on-wafer power testing, a Virginia diode (VDI) WR-04 active multiplier chain (WR-04 AMC) was used for the input source, and a VDI Erickson PM-5 power meter was used for output power measurements. Both *S*-parameter and power measurements utilized GGB Industries WR-03 Picoprobes for

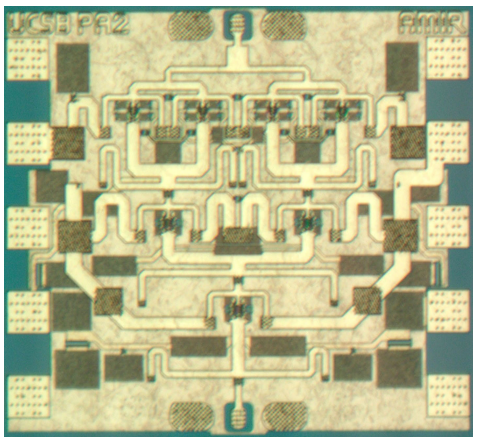

Fig. 16. Die photograph of the implemented PA in the 250-nm InP HBT process from Teledyne Scientific. Chip dimensions are 0.75 mm × 0.82 mm.

on-wafer probing. For power testing, WR-04-to-WR-03 and WR-03-to-WR-10 waveguide transitions were used on the input and output to connect the probes to the source and power meter, respectively.

The scalar power measurements were calibrated as follows: 1) the VDI source was connected to the PM-5 power meter, and the source power was calibrated versus multiplier control voltage at selected frequencies; 2) on-wafer through-line measurements were taken at a fixed input power for each frequency; 3) the on-wafer through-line loss extracted from the *S*-parameter TRL calibration was de-embedded from the loss measurements to establish the total combined loss of the two probes at each frequency; 4) an amplifier design was tested and driven into deep saturation such that maximum output power of the amplifier was reached at each frequency; 5) the input and output probes in the setup were then swapped and the amplifier was again driven into deep saturation such that the maximum output power was reached; and 6) the difference in maximum saturated output power with the two

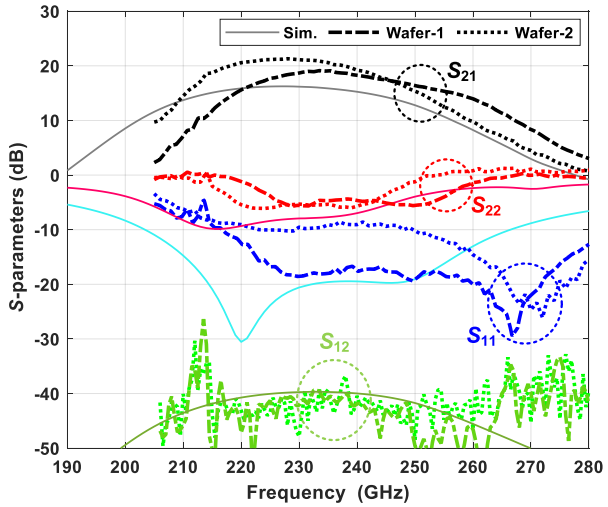

Fig. 17. Simulated and measured S-parameters of the PA from two different wafers for $V_{CC1} = 2.0$ V, $V_{CC2} = 3.0$ V, $I_{CC1} = 44$ mA, and $I_{CC2} = 86$ mA.

probe configurations was used along with the total probe loss to establish the loss of each probe.

For research and development purposes, PAs from two wafers with slightly different collector doping profiles were characterized. The measured and simulated S-parameters of the PA are shown in Fig. 17. Overall, there is a close resemblance between the simulated and measured S-parameters. The measured results are slightly shifted toward the higher frequencies, and the measured S_{21} from both wafers is greater compared to the simulated one. The gain increase in measurements compared to the simulations was observed for all other amplifiers on the reticle that used RBP transistors, and thus it is related to the modeling of these transistors. The measured S_{22} of the PA from Wafer-2 becomes positive above 250 GHz, which is merely a calibration artifact since S_{12} in this region is below -30 dB and there is no abnormal behavior in S_{21} or S_{11}. The abrupt change of S-parameters around 214 GHz is design independent and is due to poor calibration, since it is present exactly at the same frequency for both PAs with different frequency responses.

Fig. 18(a) illustrates the simulated and measured peak PAE of the PA versus frequency. The associated P_{out} and gain of the PA at the peak PAE point are featured in Fig. 18(b) and (c). While the PA was designed and optimized for $V_{CC1} = V_{CC2} = 2.5$ V, $I_{CC1} = 58$ mA, and $I_{CC2} = 80$ mA, in measurements, we adjusted the bias voltages to maximize the PAE. The optimum bias point is $V_{CC1} = 2.0$ V, $V_{CC2} = 3.0$ V, $I_{CC1} = 44$ mA, and $I_{CC2} = 86$ mA, for which the simulation and measurement results are presented in Figs. 17 and 18.

While the measured P_{out}, PAE, and gain curves of the PA from Wafer-1 are close to the simulated counterparts, those from Wafer-2 experienced a downward frequency shift. This can be explained by the lower center frequency of the S_{21} of the PA from Wafer-2 compared to the one from Wafer-1. Taking into account this shift, the measured PAE is close to that measured. The measured P_{out} is approximately 0.7 dB less than its measured counterpart on average. This may be due to inaccuracies in EM simulations and transistor modeling. The measured gain at the maximum PAE point is higher than the

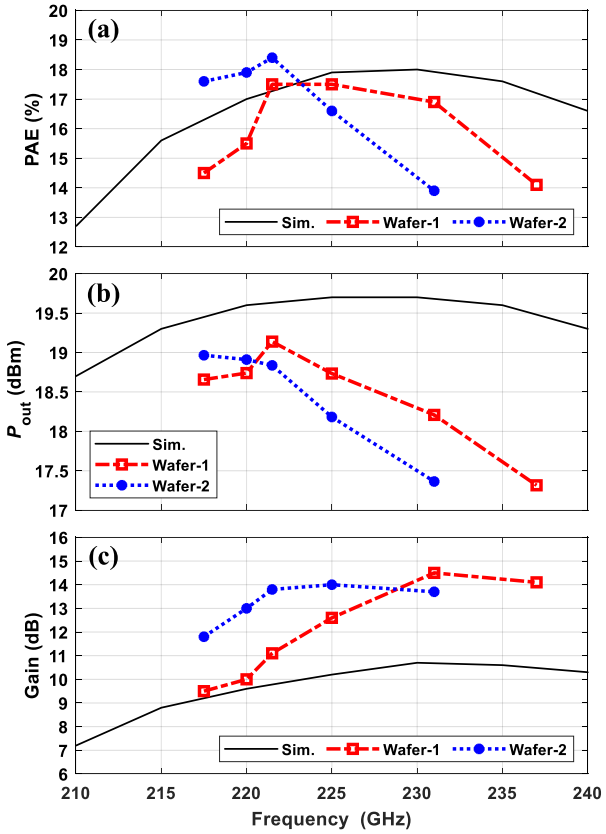

Fig. 18. Simulated and measured (a) peak PAE, (b) P_{out}, and (c) gain of the PA versus frequency. Values are reported for the input power at which peak PAE occurs. ($V_{CC1} = 2.0$ V, $V_{CC2} = 3.0$ V, $I_{CC1} = 44$ mA, and $I_{CC2} = 86$ mA.)

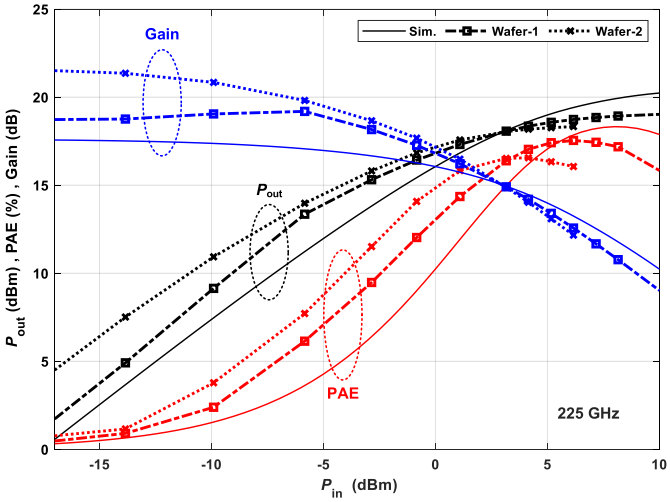

Fig. 19. Simulated and measured P_{out}, PAE, and gain of the PA from two different wafers at 225 GHz versus the input power. (Bias conditions: $V_{CC1} = 2.0$ V, $V_{CC2} = 3.0$ V, $I_{CC1} = 44$ mA, and $I_{CC2} = 86$ mA.)

simulated counterpart since the simulated S_{21} is also higher than the measured S_{21}.

The measured and simulated P_{out}, PAE, and the gain of the PA at 225 GHz are shown in Fig. 19 versus the input power. The peak PAE is achieved at 5–6-dB gain compression. A higher P_{out} can be obtained at the cost of slight degradation in PAE. For instance, at 225 GHz, the PA from Wafer-1 delivers $P_{out} = 19$ dBm with 15.6% PAE for $P_{in} = 10$ dBm. Beyond this point, the source power is limiting and insufficient

TABLE I
SUMMARY OF THE STATE-OF-THE-ART INTEGRATED PAS OPERATING AROUND 220 GHZ WITH $P_{OUT} \geq 10$ MW

Reference$^{\diamond}$	Process	Node (nm)	Topology*	V_{Sup} (V)	P_{out} (dBm)	PAE (%)	Gain† (dB)	Freq. (GHz)	A (mm^2)	$P^{\ddagger}_{den}$ (W/mm^2)
CSICS 2011 [13]	InP HEMT	sub-50	4-stg. CS, 4-way comb.	2.2	17.8–18.6	3.7	9.4–11	205–225	1.84	33–41
IMS 2013 [14]	InP HBT	250	3-stg. cascode, 4-way comb.	2.75	17.7	1.68	14.7	220	1.59	37
IMS 2014 [15]	InP HBT	250	3-stg. cascode, 4-way comb.	2.2	16.7–18.9	4–6	19–22	190–245	1.54	31–51
IMS 2017 [8]	InP HBT	250	3-stg. cascode, 16-way comb.	2.2	20–23.9	1.2–4.1	12.2–17	185–255	3.38	30–73
EuMC 2018 [16]	InP HBT	130	2-stg. 2-stacked, 2-way comb.	5.9	18	4.8	16.5	204	0.91	62
IMS 2020 [17]	GaN HEMT	70	10-stage CS	11	14–15	4–6	9–11	190–215	1.12	22–28
IMS 2021 [7]	InP HBT	250	4-stg. degenerated CB, 4-way comb.	2.4	17.7–18.5	6.9–8.5	13.4–16.8	190–210	1.14	52-62
JMW 2023 [9]	InP HBT	250	3-stg. neutr. CB, 4-way comb.	2.5	17.8–19.7 16.7–17.8	6.5–13 3.2–9.1	12.5 dB at 200-GHz	185–200 200–215	0.29	208–322 161–208
This Work	InP HBT	250	3-stg. degenerated CB, 4-way comb.	3	17.2–19	14.1–18.4	11.8–14	217–231	0.61	86–130

$^{\diamond}$ Spec values for other works were extracted from their text or otherwise estimated from the plots.
* Stg.: stage, CS: common-source, comb.: combiner, neutr.: neutralized.
† Gain at power saturation. ‡Power density.

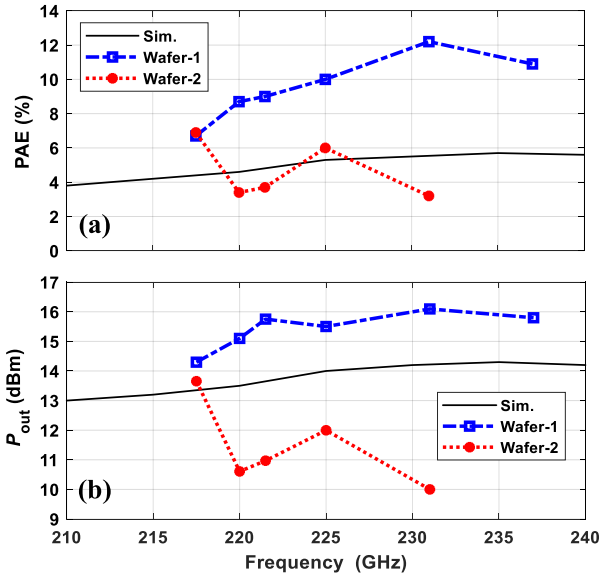

Fig. 20. Simulated and measured. (a) PAE at output 1-dB compression level. (b) $P_{out\text{-}1dB}$ versus the frequency. ($V_{CC1} = 2.0$ V, $V_{CC2} = 3.0$ V, $I_{CC1} = 44$ mA, and $I_{CC2} = 86$ mA.)

to compress the PA. Also, PA from wafer-1 features slight gain expansion (≈ 0.4 dB) at 225 GHz (Fig. 19) and ≤ 0.8-dB gain expansion at all other measured frequencies. This results in a higher PAE and output power at 1-dB compression level of the PA from Wafer-1 compared to those of the PA from Wafer-2 (Fig. 20). The PA from Wafer-1 features $\geq$ 15-dBm output power at its 1-dB compression point ($P_{out\text{-}1dB}$) and $\geq$ 8% corresponding PAE at 220-237 GHz. These values are comparable to (or better than) the saturated PAE and output power of the PAs reported in the literature that operate over a similar frequency range (Table I).

The performance of PAs operating around 220 GHz and having an output power greater than 10 mW is summarized in Table I, where the presented three-stage PA achieves the highest PAE [7], [8], [9], [13], [14], [15], [16], [17]. It is worth mentioning that during the review of our work, a new PA with a higher PAE (23.8%) but a lower saturated output power (17.9 dBm) and much lower gain (6.5 dB) was accepted for publication [18].

VI. SUMMARY

A 212–238-GHz PA with 75-mW output power and peak 17.5% PAE is presented in a 250-nm InP HBT technology with f_{max} of 750 GHz. The PA uses a transistor layout that employs ballast resistors to improve the safe operating region of multifinger transistors, allowing a higher supply voltage and bias current per transistor finger. The PA has three stages, each using a $4 \times 5\,\mu$m four-finger transistor that operates in the common-base topology with capacitive base degeneration. It is shown that while the values of the ballast resistor and the base capacitor do not change the PAE at power saturation, they determine the compression level at which peak PAE takes place. The PA also uses a four-way power combiner to further increase the output power. Using automatic layout scripting, four different circuit topologies have been characterized for the four-way power combiner, showing that the insertion loss can be as low as 1 dB in the 200–240-GHz frequency range.

REFERENCES

[1] D.-W. Park, D. R. Utomo, B. H. Lam, S.-G. Lee, and J.-P. Hong, "A 230–260-GHz wideband and high-gain amplifier in 65-nm CMOS based on dual-peak G_{max}-core," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1613–1623, Jun. 2019.
[2] H. Bameri and O. Momeni, "A 200-GHz power amplifier with a wideband balanced slot power combiner and 9.4-dBm P_{sat} in 65-nm CMOS: Embedded power amplification," *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3318–3330, Nov. 2021.
[3] Z. Wang, P. Chiang, P. Nazari, C. Wang, Z. Chen, and P. Heydari, "A CMOS 210-GHz fundamental transceiver with OOK modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564–580, Mar. 2014.

[4] N. Sarmah, K. Aufinger, R. Lachner, and U. R. Pfeiffer, "A 200–225 GHz SiGe power amplifier with peak P_{sat} of 9.6 dBm using wideband power combination," in *Proc. Europ. Solid-State Circuits Conf. (ESSCIRC)*, Lausanne, Switzerland, Sep. 2016, pp. 193–196.

[5] M. H. Eissa and D. Kissinger, "A 13.5-dBm fully integrated 200-to-255-GHz power amplifier with a 4-way power combiner in SiGe: C BiCMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, 1 Feb. 2019, pp. 82–84.

[6] J. Yu et al., "A 211-to-263-GHz dual-LC-tank-based broadband power amplifier with 14.7-dBm P_{SAT} and 16.4-dB peak gain in 130-nm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 58, no. 2, pp. 332–344, Feb. 2023.

[7] A. S. H. Ahmed, U. Soylu, M. Seo, M. Urteaga, J. F. Buckwalter, and M. J. W. Rodwell, "A 190–210 GHz power amplifier with 17.7–18.5 dBm output power and 6.9–8.5% PAE," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Atlanta, GA, USA, Jun. 2021, pp. 787–790.

[8] Z. Griffith, M. Urteaga, and P. Rowell, "180–265 GHz, 17–24 dBm output power broadband, high-gain power amplifiers in InP HBT," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Honolulu, HI, USA, Jun. 2017, pp. 973–976.

[9] J. S. Chien, W. Lee, and J. F. Buckwalter, "High-efficiency 200-GHz neutralized common-base power amplifiers in 250-nm InP HBT," *IEEE J. Microw.*, vol. 3, no. 2, pp. 715–725, Apr. 2023.

[10] M. Urteaga, Z. Griffith, M. Seo, J. Hacker, and M. J. W. Rodwell, "InP HBT technologies for THz integrated circuits," in *Proc. IEEE*, vol. 105, no. 6, pp. 1051–1067, Jun. 2017.

[11] W. Liu, H.-F. Chau, and E. Beam, "Thermal properties and thermal instabilities of InP-based heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 43, no. 3, pp. 388–395, Mar. 1996.

[12] Y. Wei, S. Lee, P. K. Sundararajan, M. Dahlstrom, M. Urteaga, and M. Rodwell, "High current (100 mA) InP/InGaAs/InP DHBTs with 330 GHz f/sub max," in *Proc. Conf. Indium Phosph. Rel. Mater. Conf.*, Stockholm, Sweden, 2002, pp. 47–50.

[13] V. Radisic et al., "A 75 mW 210 GHz power amplifier module," in *Proc. IEEE Comp. Semicond. Integr. Circuit Symp. (CSICS)*, Waikoloa, HI, USA, Oct. 2011, pp. 1–4.

[14] Z. Griffith, T. Reed, M. Rodwell, and M. Field, "A 220 GHz solid-state power amplifier MMIC with 26.8 dB S21 gain, and 55.5 mW pout at 17.0 dB compressed gain," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Seattle, WA, USA, Jun. 2013, pp. 1–3.

[15] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "A 50–80mW SSPA from 190.8–244 GHz at 0.5mW P_{in}," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Tampa, FL, USA, Jun. 2014, pp. 1–4.

[16] A. S. H. Ahmed, A. A. Farid, M. Urteaga, and M. J. W. Rodwell, "204 GHz stacked-power amplifiers designed by a novel two-port technique," in *Proc. 13th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Madrid, Spain, Sep. 2018, pp. 29–32.

[17] M. Cwiklinski et al., "First demonstration of G-band broadband GaN power amplifier MMICs operating beyond 200 GHz," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Los Angeles, CA, USA, Aug. 2020, pp. 1117–1120.

[18] Z. Griffith, M. Urteaga, and P. Rowell, "A 220-GHz power amplifier with 60-mW P_{out} and 23.5% PAE in 130-nm InP HBT," *IEEE Microw. Wireless Technol. Lett.*, pp. 1–4, 2024. [Online]. Available: https://ieeexplore.ieee.org/document/10438361

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