A Low Loss Die-Embedded Glass Substrate for 140 GHz InP Power Amplifier Integration

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2024 IEEE/MTT-S International Microwave Symposium - IMS 2024 | 979-8-3503-7504-6/24/$31.00 ©2024 IEEE | DOI: 10.1109/IMS40175.2024.10600201

***Abstract*— We present a novel packaging solution for 140 GHz InP power amplifier (PA) integration using an advanced die-embedded glass substrate. This marks the first functional demonstration of a die-embedded glass package for D-band (110 - 170 GHz) applications, effectively tackling both electrical and thermal challenges at high frequencies. We embed the 140 GHz InP PA die into the glass substrate and employ micro-vias for die-to-package interconnects, thereby eliminating assembly. The interconnects using micro-vias introduce less than 1.04 dB loss per interconnect from 110 - 170 GHz. Additionally, thermal management has been effectively addressed by directly electroplating a copper sheet onto the backside of the die, ensuring optimal heat dissipation and maintaining the integrity of the PA under high heat density conditions. With the electrical, thermal, and fabrication benefits, the die-embedded glass package shows immense potential in the development of wireless modules in D-band or higher frequencies.**

***Keywords*— D-band, Glass substrate, Heterogeneous integration, Interconnect, mmWave Packaging, Power amplifier.**

I. Introduction

D-band (110 GHz - 170 GHz) is increasingly seen as one of the prime candidates for next-generation wireless communications (6G), due to its expansive spectrum [1]. For the effective development of communication systems at these high frequencies, researchers are exploring various technologies to boost system performance such as integrating III-V compound semiconductors to enhance output power and efficiency in high-frequency applications [2]. This necessitates seamless integration of diverse technologies, marking a significant challenge and a crucial factor in the evolution of next-generation wireless systems, particularly in heterogeneous integration.

However, the interconnects between the chip and off-chip/on-package components (antenna or other ICs) tend to exhibit significant electrical loss beyond 100 GHz. Conventional integration methods, such as wire-bonding and flip-chip, derived from lower-frequency applications, offer limited benefits as the frequency goes higher. Their electrical losses and assembly challenges are increasingly problematic. Specifically, wire-bonding, while convenient for attaching the chip's backside to heat spreaders, faces significant electrical parasitics due to large bonding pads and less controlled wire shapes [3]. Flip-chip technology, while suffering less loss, is limited by backside heat spreader integration challenges in high-power power amplifier (PA) packaging [4]. These issues underscore the importance of developing new packaging technologies for high-frequency wireless modules, addressing electrical loss, thermal management, and antenna integration.

In the pursuit of advanced packaging technology, the focus is on both integration methods and the selection of appropriate materials. Embedding the die into the substrate dramatically reduces interconnect length, leading to significantly lower loss [5]. This approach also allows for better thermal management by fully exposing the chip's backside for heat spreader integration [6]. Regarding packaging materials, glass substrates have emerged as a promising option, offering thermal expansion compatibility for mechanical reliability, a smooth surface for fine feature fabrication, and availability in large panels for cost-effective manufacturing [7].

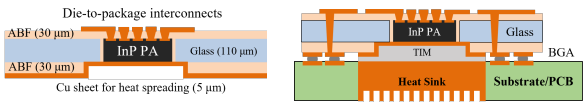
This paper showcases the first functional demonstration of a die-embedded glass package for integrating a 140 GHz InP PA which addresses both electrical and thermal challenges. We discuss the package design, process flow, interconnect modeling, and on-package measurement results. This demonstration shows that die-embedded glass packaging could be a viable solution for overcoming the challenges associated with chip-to-package interconnects and thermal management for developing wireless modules in D-band.

II. Package Design and Fabrication

This section details the structure and fabrication of our proposed package, including a stack-up overview, process flow, and fabrication results. The fabrication benefits of the package are also discussed.

A. Package Stack-up Description

Our package embeds the InP PA within a glass substrate (AGC EN-A1), integrating interconnects in the top dielectric



(a) (b)

Fig. 1. Schematic cross-section of (a) glass substrate for PA integration, and (b) further integration of package to the substrate or PCB

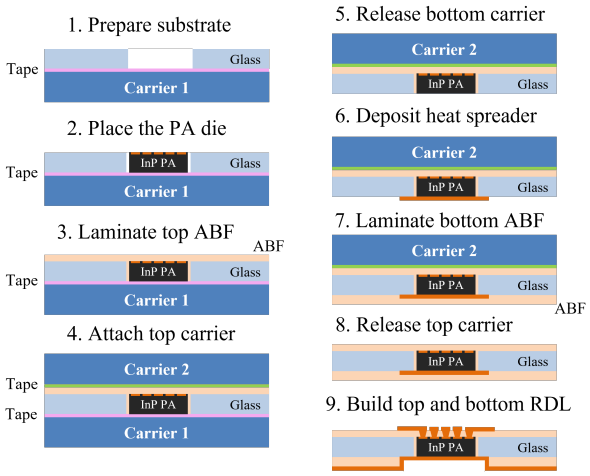


Fig. 2. The fabrication process flow of the PA-embedded glass substrate

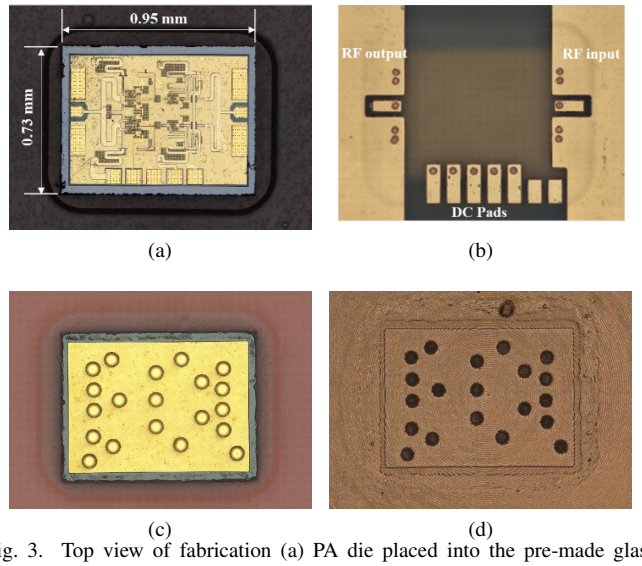


Fig. 3. Top view of fabrication (a) PA die placed into the pre-made glass cavities, (b) interconnects on the top metal layer on the substrate, (c) backside of the embedded PA die being exposed, and (d) backside of the embedded PA die with electroplated Cu heat spreading layer

layer and an electrolytic-plated heat spreader at the bottom. The schematic cross-section of the package is illustrated in Fig. 1a. The embedded InP PA, using Teledyne's 250 nm InP HBT technology is 0.95 mm × 0.73 mm, with a thickness varying from 85 - 95 µm due to surface structure. The PA has a similar design to previous research work of [8]. We chose a glass thickness of 110 µm, aligning with the die thickness and thickness availability from the glass vendor. The top and bottom dielectric layers are composed of Ajinomoto Build-up Film (ABF) GL102, with a dielectric constant (Dk) of 3.3 and a dissipation factor (Df) of 0.0044 at 5.8 GHz, each layer being 30 µm thick. The electrical characterization of similar substrates at 140 GHz has been done in [9]. This dual-layer design is crucial for maintaining the coefficient of thermal expansion (CTE) balance within the stack-up. Micro-vias are laser drilled into the top dielectric layer for die-to-package interconnects, while the bottom layer features an opening to expose the die's backside, enhancing heat spreader integration. Such a package can be further integrated onboard using the ball grid array (BGA) and thermal interface material (TIM) for electrical and thermal interfaces as shown in Fig. 1b.

B. Fabrication Process Flow

The process for embedding the PA into a glass substrate is depicted in Fig. 2. Initially, the glass substrate is prepared with cavities created via laser drilling. This substrate is then temporarily adhered to a carrier using thermal release tapes. Subsequently, the PA die is placed within the cavity and held by the tape. Following this, an ABF dielectric sheet is laminated over the top to encapsulate the PA die. After the ABF cures, an additional carrier is attached to the top, and the bottom carrier is removed to reveal the die's backside for copper (Cu) heat spreader deposition, carried out through a standard semi-additive process (SAP) [10]. Another layer of ABF is then laminated on the bottom to ensure the package's coefficient of thermal expansion (CTE) is balanced, allowing for the release of the top carrier.

With the die now embedded and the heat-spreading layer integrated at the bottom, we employ laser drilling to create vias and windows on the top and bottom layers for electrical and thermal access, respectively. The Cu interconnects and the heat-spreading layer are also built using the SAP method.

C. Fabrication Results

This sub-section highlights the fabrication results of our designed package. Fig. 3a illustrates the placement of the PA die within the glass cavity. Fig. 3b captures the top metal layer with ground-signal-ground (GSG) pads for RF input/output and DC pads for bias. Fig. 3c displays the exposed backside of the die, while Fig. 3d reveals the electroplated heat-spreading layer on the backside.

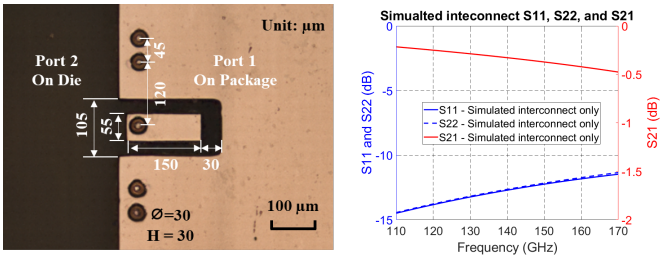
The images collectively demonstrate the advantages of this die-embedded packaging approach. The utilization of precisely drilled vias facilitates the integration of high-density on-die pads, significantly reducing parasitic effects. Moreover, these vias offer more precise shape control (less than 5 µm variance between design and fabrication) compared to other assembly methods, enhancing the overall reliability of the package.

III. Modeling and Measurement

This section outlines the design, simulation, and measurement for the package and the packaged PA. We used Ansys HFSS [11] for pre-fabrication modeling to optimize impedance matching and reduce loss. After fabricating the packaged PA, its performance was measured and compared with the bare PA, enabling us to evaluate our initial simulations against the actual hardware results.

A. Package Modeling

Fig. 4a displays the detailed dimension of the die-to-package interconnects, featuring a single metal



(a) (b)

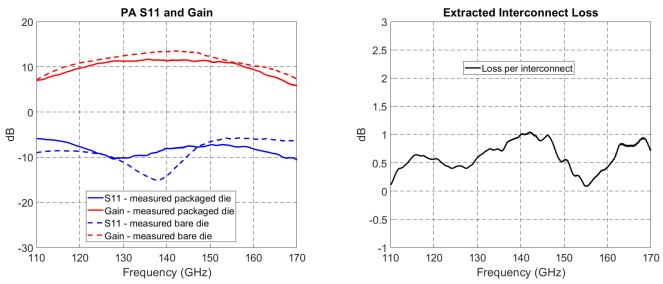
Fig. 4. (a) Detailed dimension of the die-to-package transition, and (b) EM simulation results of the die-to-package transition

layer designed for fan-out from the PA die pads. This layer includes RF GSG pads and DC pads. The interconnects between the InP PA and the glass package are realized through vias in the dielectric, each with a depth and diameter of 30 µm, maintaining a 1:1 aspect ratio. Each on-die signal pad is connected by one signal via. For efficient parasitic inductance minimization in the ground-return path, each on-die ground pad is connected by two ground vias to the on-package ground plane. Both the input and output of the PA are 50 Ω matched. Key parameters (signal pad size, pad spacing, and via pitches) are finely tuned in Ansys HFSS. The simulation of the PA-to-package transition indicates a 0.3 dB loss at 140 GHz and an S11/S22 of less than -10 dB across the D-band, as shown in Fig. 4b.

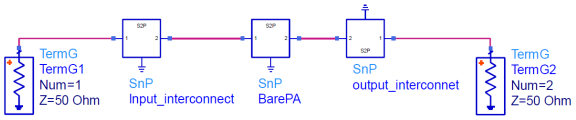
B. Measurement and Analysis

We performed small signal gain measurements to evaluate the loss and matching performance of the die-embedded package, using an Agilent Vector Network Analyzer (VNA) E8361C and D-band frequency extenders (V06VNA2). For RF probing, we used 75 µm pitch Cascade Infinity probes 170-S-GSG-75-BT, and for DC, GGB Multi-Contact Wedge probes were employed. Thermal management was maintained during measurements by vacuum-securing the substrate to the metal stage, ensuring good contact for heat dissipation between the backside heat-spreading layer and the metal stage. The tests were conducted on both a bare PA die and an embedded PA die with the same DC bias condition, to provide a comparative analysis of their performance.

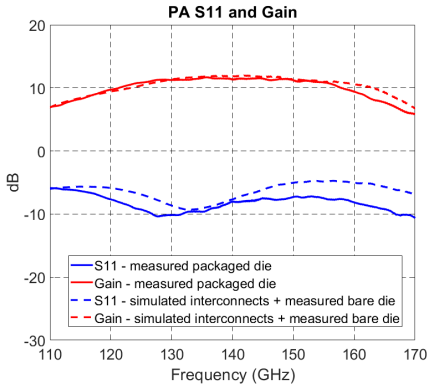
The small signal gain and S11 measurements for both the bare and packaged PAs are presented in Fig. 5a. At 140 GHz, the bare PA exhibits a small signal gain of 13.4 dB, while the packaged PA shows a gain of 11.4 dB, which



(a) (b)



(c)



(d)

Fig. 5. (a) Measurement results of packaged PA and bare PA, (b) extracted loss per interconnect, (c) the schematic of the cascaded circuit for correlation, and (d) comparison between measured S-parameter of packaged PA and bare PA with simulated interconnects

results in around 1 dB loss from each interconnect (input and output). The die-embedded package using micro-vias shows an ultra-wideband response which introduces less than 1.04 dB loss per interconnect from 110 - 170 GHz as shown in Fig. 5b. The performance of this packaging technology at 140 GHz, compared to other methods, is detailed in table 1.

To verify the correlation between measurement and simulation, we cascaded the simulated S-parameters of the die-to-package interconnect (Fig. 4b) with the input and output

Table 1. Comparison among Packaged D-band Modules

	[3]	[4]	**This work**
Package Technology	LTCC	Radio on Glass	Die embedding in glass substrate
Assembly Type	Wire-bonding	Flip-chip	No assembly (Micro-via)
Package Loss at 140 GHz	2.6 dB	1 dB	1 dB
Package Bandwidth	8 GHz 1-dB bandwidth	40 GHz bandwidth for 1-dB package loss	60 GHz bandwidth for 1.04 dB loss
Method to Extract Loss	Interconnect simulation	Psat comparison	Small signal gain comparison
Thermal Management	Attached to on-package pads and thermal vias	Not shown	Backside integrated heat spreading layer

S-parameters of the bare PA (Fig. 5a) as shown in Fig. 5c. The comparative results, shown in Fig. 5d, reveal a discrepancy of less than 0.5 dB in gain between the simulation and the measurement at 140 GHz, which indicates that the interconnect simulation correlates well with the measured package performance.

Encapsulating the embedded die with the ABF layer introduces negligible impact while protecting the ICs to maximize reliability. This is evident from the S11 results, showing only a small notch shift at 140 GHz after packaging. This shift can be attributed to the altered effective dielectric constant in the on-die microstrip structures. Such variations can be accounted for in the design of on-die structures during the design of the PA prior to embedding.

IV. Conclusion

In this paper, we first demonstrated the low-loss die-embedded glass package for 140 GHz InP PA integration. This approach eliminates assembly, provides protection of the PA using dielectric polymer, and enables heat removal from the bottom side, thereby simplifying the fabrication process. We have realized D-band interconnects with less than 1.04 dB loss per interconnect from 110 - 170 GHz, and a bottom heat spreading layer for the thermal management of the PA. This prototype shows that the die-embedded glass package can be a promising solution for high-frequency heterogeneous integration, which also shows a huge potential for further development of large-scale beamforming arrays. Future work can include antenna array integration and chip-package co-design method development.

Acknowledgment

This work was supported in part by the Semiconductor Research Corporation (SRC) and DARPA through the JUMP 1.0 (ASCENT and ComSenter) and the JUMP 2.0 (CHIMES and CUbiC) Programs. This work was also supported in part by the Industry Consortium at the Georgia Tech 3D Systems Packaging Research Center. Authors thank AGC for glass panels, Ajinomoto for dielectric films, Hitachi Chemicals for dry-film photoresist, Nitto Denko Corporation, and Mitsui Chemicals Tohcello, Inc. for thermal release tapes.

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