WSQ-4

ICs and Transceivers for 100–300 GHz Wireless

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With acknowledgements to

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[4]Now with Cairo University
[5]Now with Intel
[6]Teledyne Scientific
[7]Sungkyunkwan University

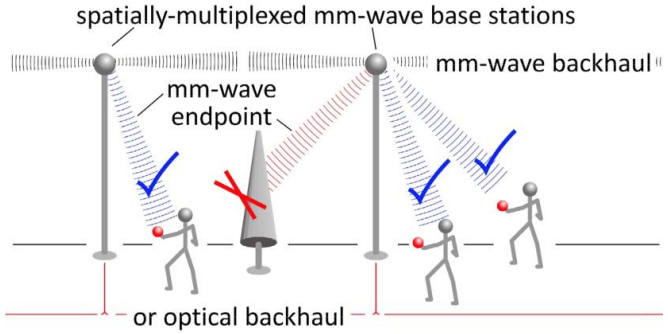
100-300 GHz Wireless

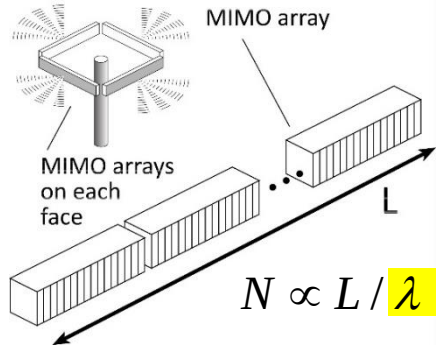
High capacity:
- potentially wide available bandwidth
- massive spatial multiplexing even with compact arrays

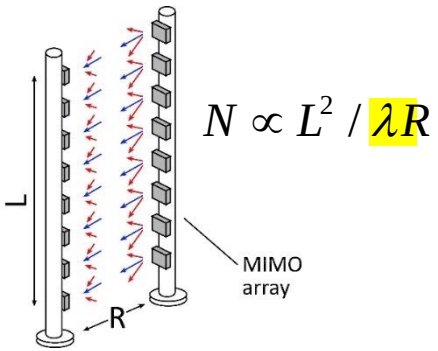
Limited range:
- high λ^2/R^2 path losses
- high worst-case atmospheric attenuation

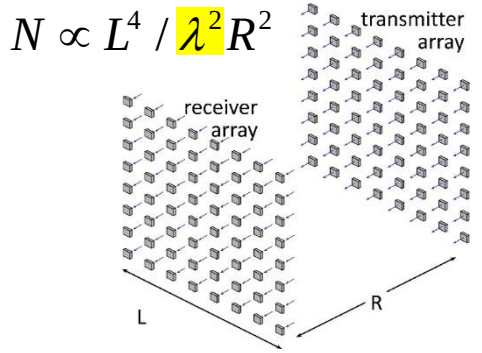
Need:
- arrays with elements
- low receiver noise figure
- compact, efficient, medium-power amplifiers

Nomenclature:
- 30-300 GHz = 10 mm to 1 mm wavelengths
- *** millimeter-waves ***









Atmospheric Attenuation

Fair-weather:

$\alpha < 5$ dB/km DC-300 GHz

Rain at 50-100 mm/hr. (10^{-4} to 10^{-5} probability):

$$\alpha \approx \begin{cases} \propto f^4 & < 50 \text{ GHz} \\ 20-30 \text{ dB/km} & > 50 \text{ GHz} \end{cases}$$

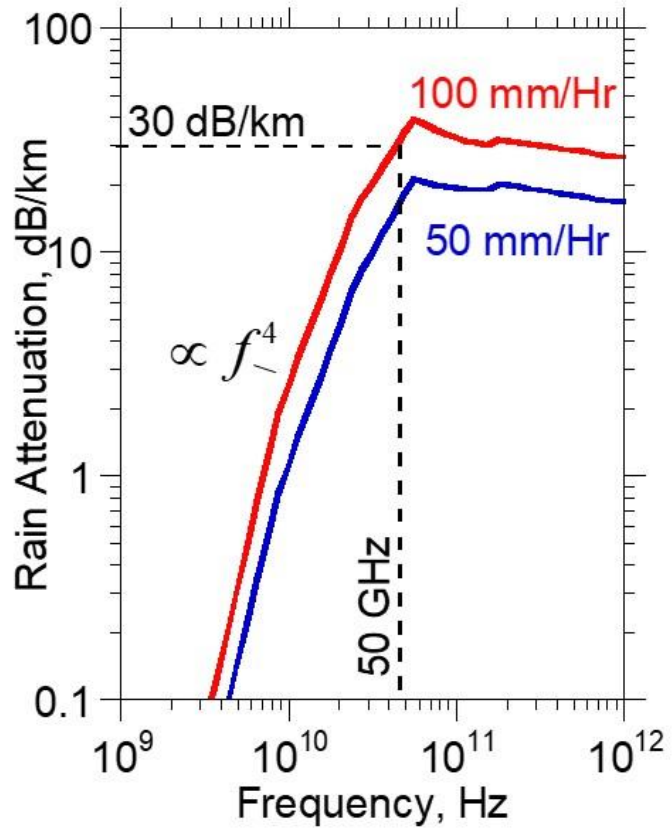
90% Humidity (35 C, 95 F):

$$\alpha \approx \begin{cases} 15 \text{ dB/km} & 200 \text{ GHz} \\ 30 \text{ dB/km} & 300 \text{ GHz} \\ > 100 \text{ dB/km} & 360 \text{ GHz-10 THz} \end{cases}$$

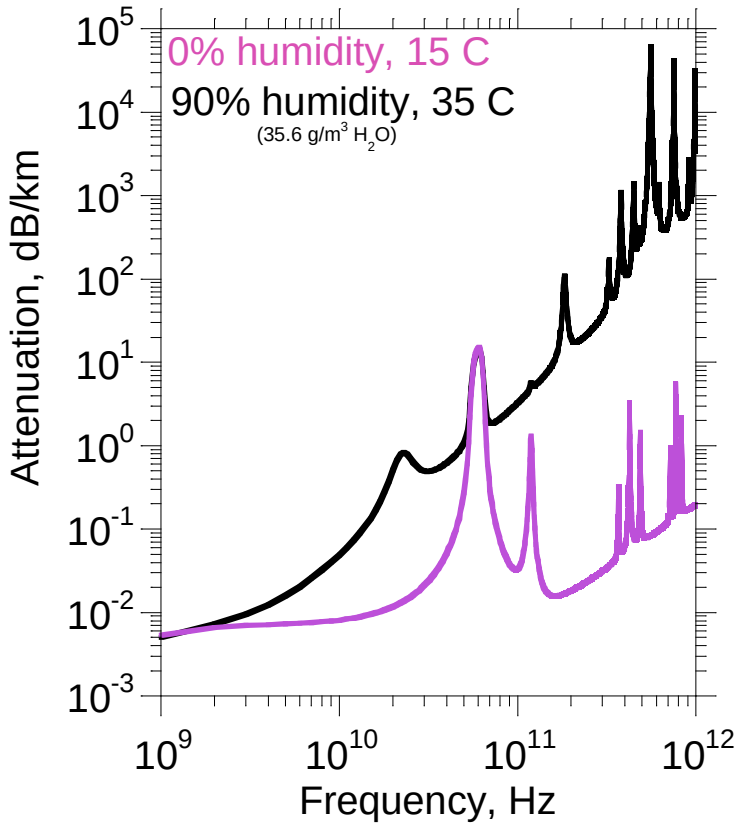
Overall worst-case (10^{-4} to 10^{-5} probability):

$$\alpha \approx \begin{cases} \propto f^4 & < 50 \text{ GHz} \\ 20-30 \text{ dB/km} & 50-300 \text{ GHz} \\ > 100 \text{ dB/km} & 360 \text{ GHz-10 THz} \end{cases}$$

Rain



Humidity

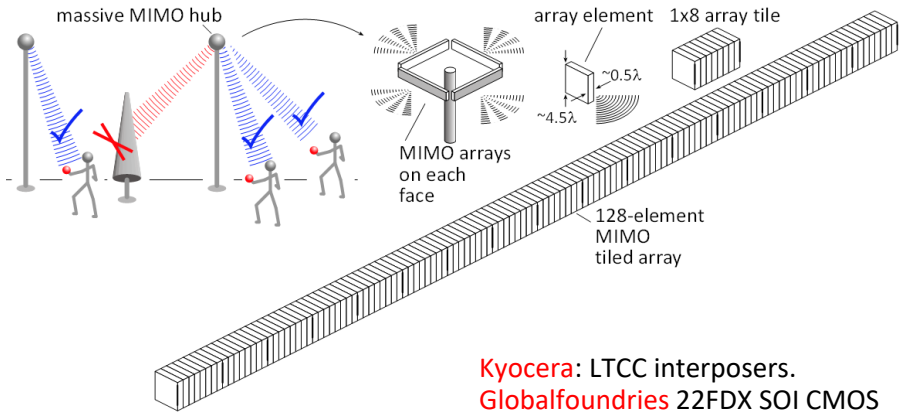


sources: see list of references

Concept: 640 Gb/s, 140 GHz MIMO hub

Concept

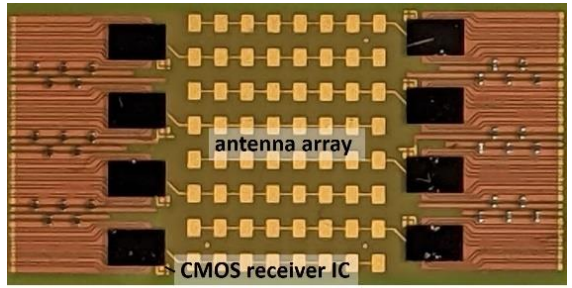
- 64 beams at 10 Gb/s/beam
- 128 antennas, each (9λ x λ/2)
- 70 meters range in 50 mm/hr. rain
- 17 dB margins: (obstruction, operating, aging, packaging)
- LNAs: 8 dB noise figure
- PAs : 100 mW =P_{1dB} (per element)

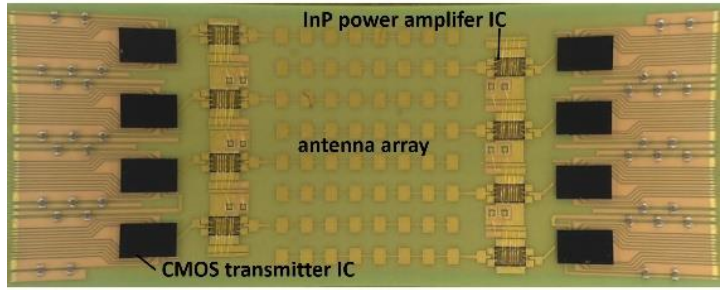


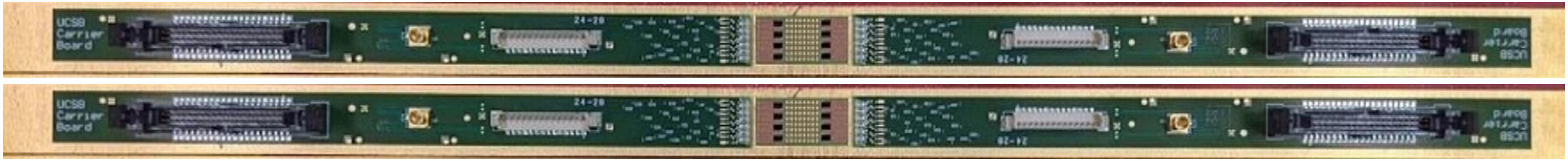
Kyocera: LTCC interposers.
Globalfoundries 22FDX SOI CMOS
Teledyne 250 nm InP HBT

Actual demos (with Samsung, Pi-Radio)

8-element arrays







70 m, 64 × 10 Gb/s hub: 140, 70, 35 GHz

Frequency		140 GHz	70 GHz		35 GHz	
Handset	size	9 mm x 9 mm	9 mm x 9 mm		9 mm x 9 mm	
	# elements	8 x 8	4 x 4		2 x 2	
Hub	size	13 cm x 1.0 cm	26 cm x 2.0 cm		52 cm x 4.0 cm	
	# elements	128 x 1	128 x 1		128 x 1	
Modulation		QPSK	QPSK	16QAM	~~QPSK~~	64QAM
Channel Bandwidth		5 GHz	5 GHz	2.5 GHz	~~5 GHz~~	1.7 GHz
Transmit P_{1dB} /element		20.1 dBm	20.1 dBm	24.2 dBm	~~19.5 dBm~~	27.8 dBm

$$(\#\ \text{elements}) \propto f_{\text{carrier}}^{2}$$

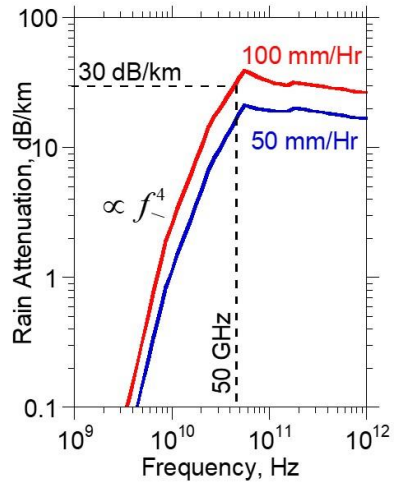
$$\text{Area} \propto f_{\text{carrier}}^{0}$$

$$(\#\ \text{elements}) \propto f_{\text{carrier}}^{0}$$

$$\text{Area} \propto f_{\text{carrier}}^{2}$$

	high capacity	moderate capacity
long range	-----	moderate frequency
short range	high frequency	moderate frequency

$$P_{TX} \propto \frac{1}{N_{TX} N_{RX}} \left(\frac{R^2}{\lambda^2} \right) e^{\alpha(f)R} \cdot \frac{2^{\text{bits/sec/Hz}}}{\text{bits/sec/Hz}}$$



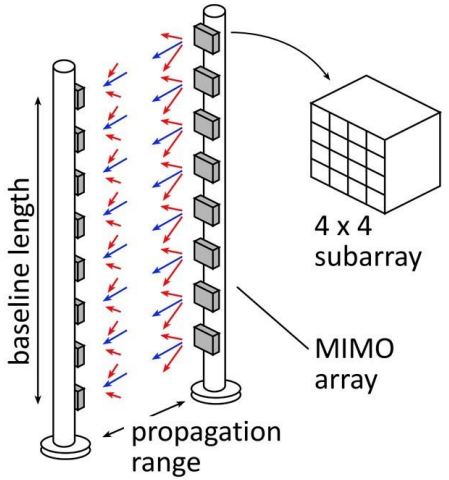
High frequencies are advantageous if $\alpha R < 1$.

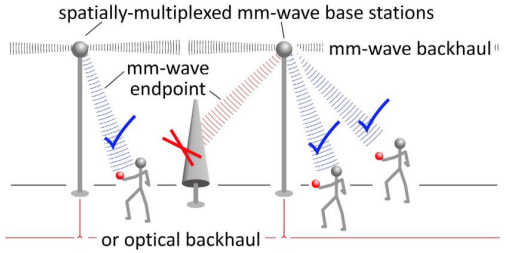
Assumptions: Hub to handset downlink. Link parameters as per previous slide. Same range, noise figure, rain rate, margins.

Concept: 640 Gb/s, 210 GHz MIMO backhaul

Concept

- 8x 80 Gb/s MIMO with 2.1 m baseline
- 16-element subarrays (7λ x 7λ antennas)
- 500 meters range in 50 mm/hr. rain
- 14 dB margins: (obstruction, operating, aging, packaging)
- LNAs: 8 dB noise figure
- PAs: 50 mW =P_{1dB}



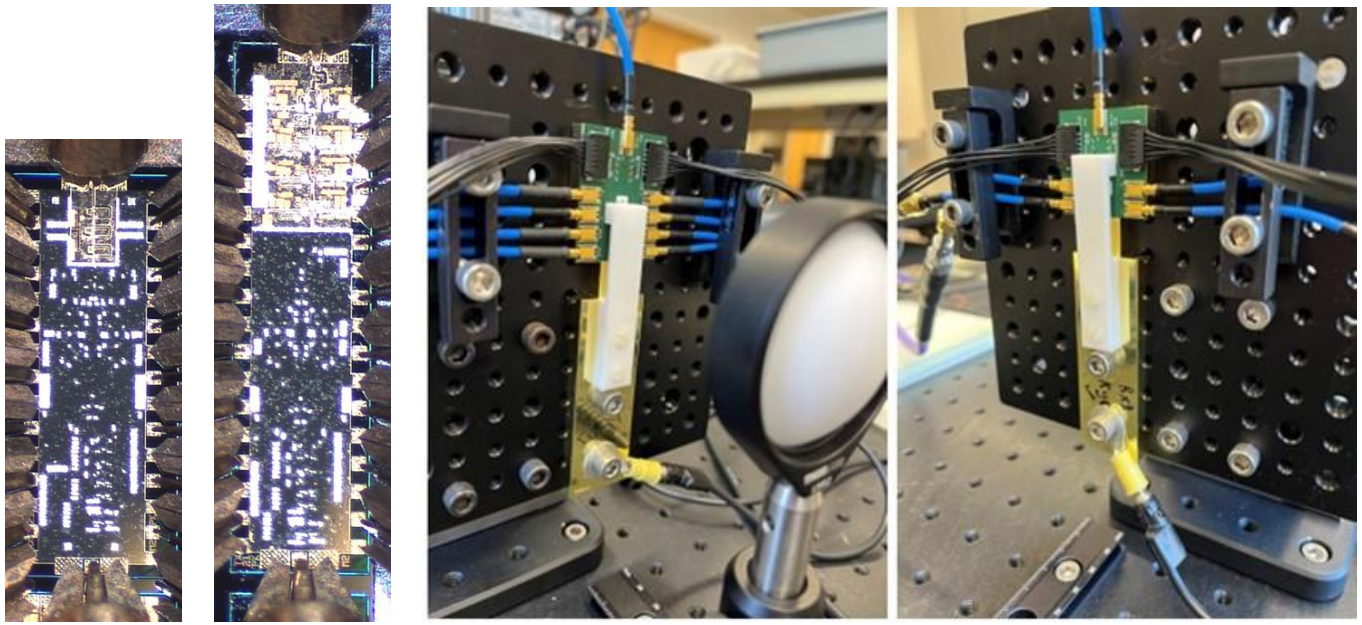


Demonstrated to date:

no subarrays, 1 channel

Ongoing demonstration efforts:

no subarrays, 4 x 4 MIMO

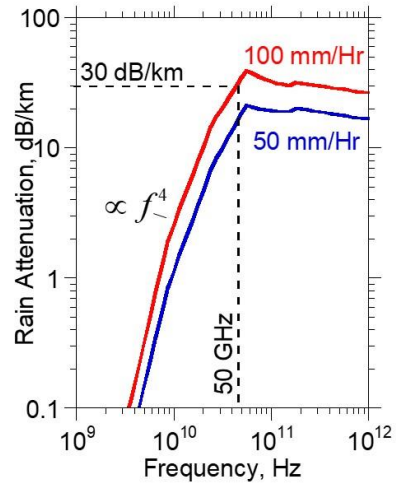


500 m, 640 Gb/s backhaul: 280, 140, 90, 35 GHz

Frequency	280 GHz	140 GHz	90 GHz		35 GHz	
1 x 8 MIMO array length, *L*	1.8 m	2.6 m	3.2 m		5.1 m	
subarrays size	3.1 x 3.1 cm^2	6.2 x 6.2 cm^2	9.5 x 9.5 cm^2		25 x 25 cm^2	
# elements	4 x 4	4 x 4	4 x 4		4 x 4	
Modulation	QPSK	16QAM	~~16QAM~~	64QAM	~~64QAM~~	4096QAM
Channel Bandwidth	40 GHz	20 GHz	~~20 GHz~~	13 GHz	~~13 GHz~~	6.7 GHz
Transmit P_{1dB}/element	19.7 dBm	16.1 dBm	~~12.3 dBm~~	16.5 dBm	~~4.1 dBm~~	19.2 dBm

	high capacity	moderate capacity
long range	-----	moderate frequency
short range	high frequency	moderate frequency

$$P_{TX} \propto \frac{1}{N_{TX} N_{RX}} \left(\frac{R^2}{\lambda^2}\right) e^{\alpha(f)R} \cdot \frac{2^{\text{bits/sec/Hz}}}{\text{bits/sec/Hz}}$$



High frequencies are advantageous if $\alpha R < 1$.

Assumptions: Link parameters as per previous slide. All carrier frequencies analyzed with same range, transmit power/element, noise figure, rain rate, margins.

Radio link design: Implications

$$\frac{P_{RX}}{P_{TX}} = \frac{N_{TX} N_{RX}}{\Omega_{scan,TX} \Omega_{scan,RX}} \left(\frac{\lambda^2}{R^2} \right) e^{-\alpha R}$$

Worst-case atmospheric losses similar at 50 GHz & 200 GHz

Same link budgets, if

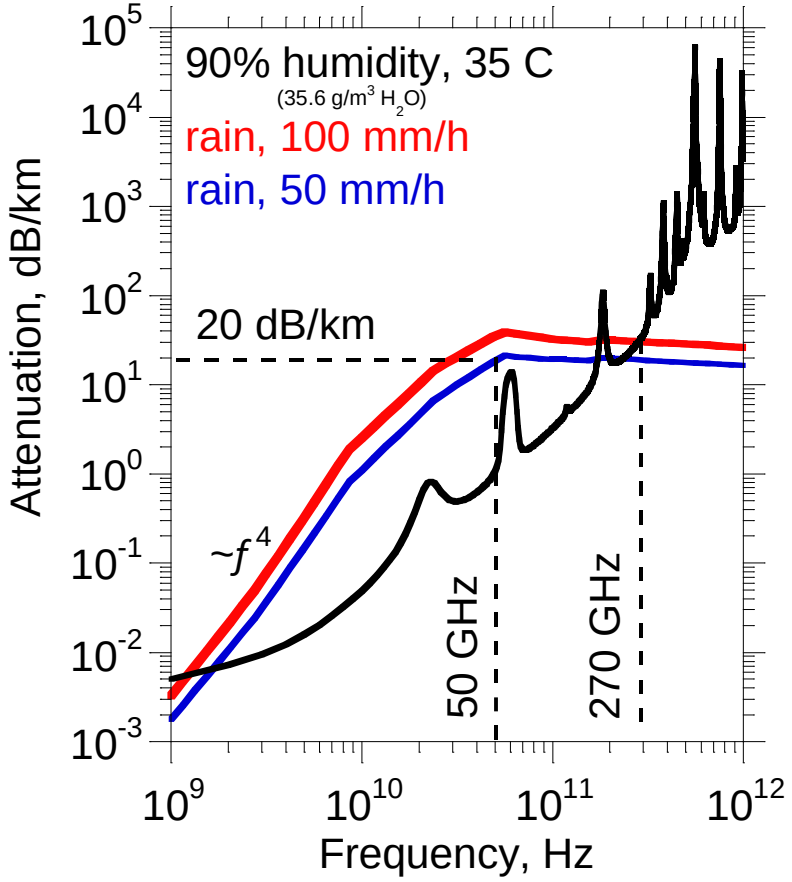
array elements are moderately increased @ 200 GHz

If comparable PA and LNA performance can be obtained.

→ work on LNAs, PAs,

work on realizing much larger arrays

But, any terrestrial > 50 GHz system will be short-range.



100-300 GHz Wireless ?? Even 39 GHz is hard !

Viable 100-300 GHz wireless systems need:

acceptable range, useful capacity, low DC power, low hardware & deployment costs

issues: λ^2/R^2 (beam diffraction) and atmospheric losses, beam blockage

Low communications density (Gb/s/km^2) ? → widely spaced hubs

Lower deployment costs

Long distances, high propagation losses

Lower frequencies are much better.

High communications density (Gb/s/km^2) ? → densely packed hubs

Less Gb/s/hub

Short distances, smaller propagation losses

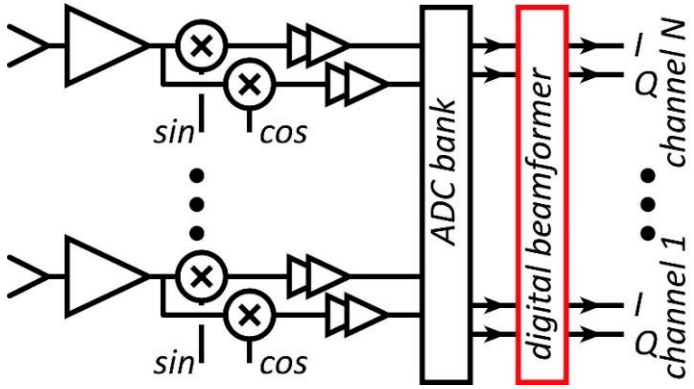
Higher frequencies can work well, can provide very high capacity

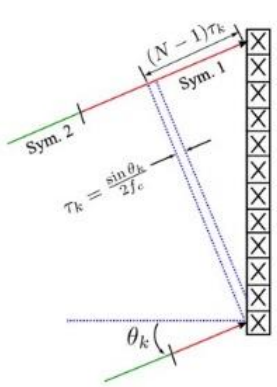
Research for future high-capacity communications:

(1) demonstrate high data rates

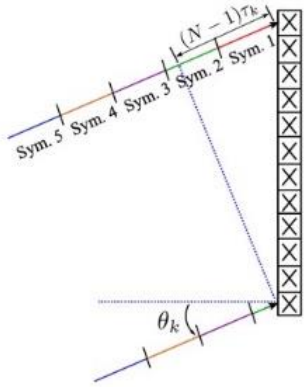
(2) reduce cost, reduce DC power, increase range and operating margins.

Systems

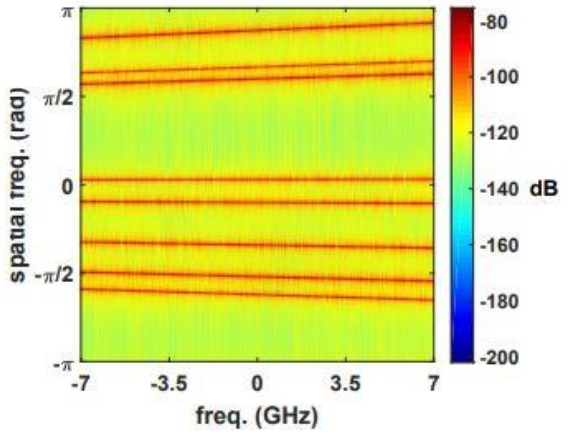




(a) Narrowband scenario.



(b) Wideband scenario.



MIMO System Design

Beamspace algorithm, Dynamic range: Madhow, UCSB
Beamformer ICs: Christoph Studer, ETHZ

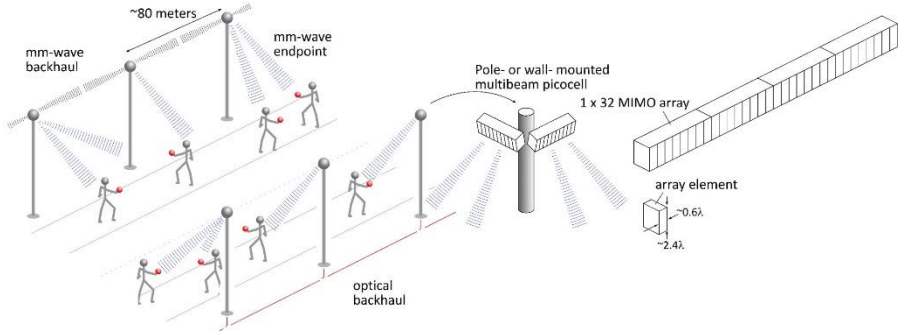
More antennas than signal beams: spatial oversampling (averaging).

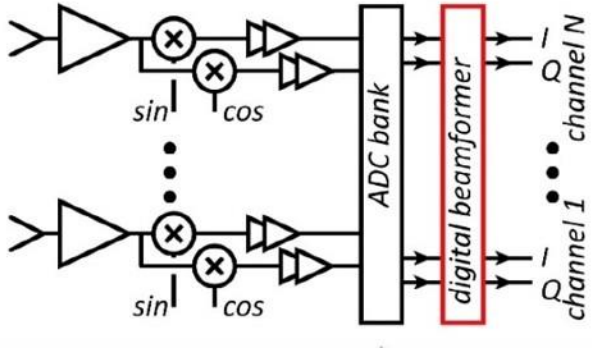
Given QPSK, 2:1 spatial oversampling:

ADCs/DACs only need 3-4 bits
RF/IF/baseband chain needs P_{1dB} only 4 dB above average power

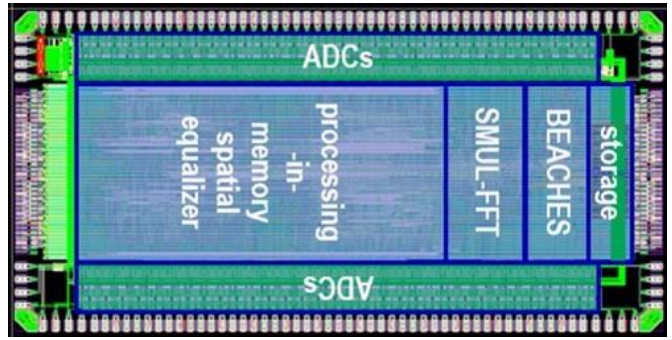
Phase noise requirements similar to single beam system

Efficient digital beamforming using beamspace
First compute (low-resolution) spatial FFT.
Then cancel crosstalk between closely-spaced users
Wideband MIMO arrays: use spatial & temporal FFTs
"true time delay"

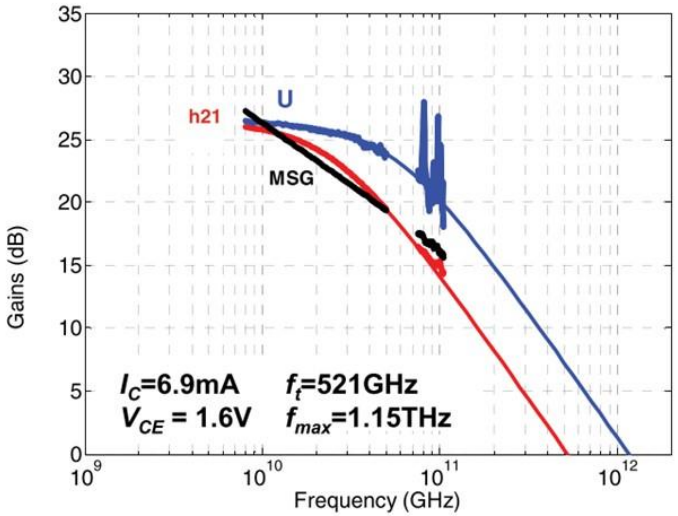


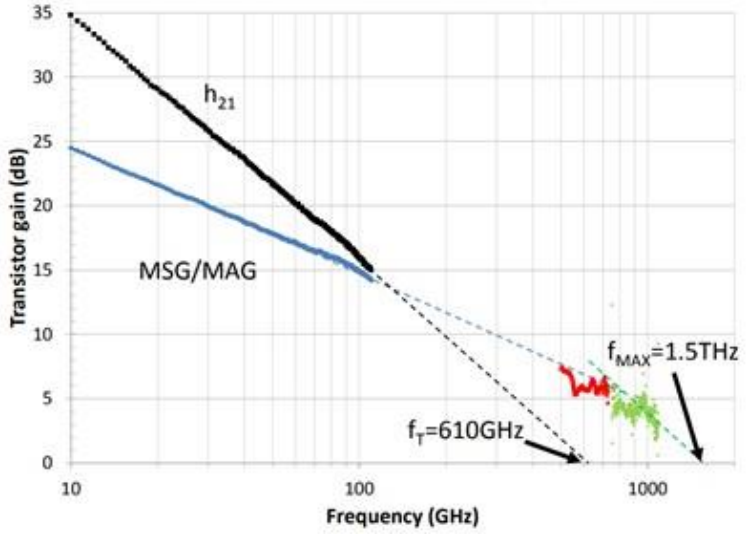


M. Abdelghany et al, IEEE Trans. Wireless Comm, Sept. 2021
M. E. Rasekh et al, IEEE Trans. Wireless Comm, Oct. 2021
A. Puglielli et al, 2016 IEEE ICC
M. Abdelghany, et. al, , 2019 IEEE SPAWC
S. H. Mirfarshbafan et al, IEEE Trans CAS 1, 2020
O Castañeda Fernández et. al, 2021 ESSCIRC
M. Abdelghany et al 2019 IEEE GLOBECOM



Transistors

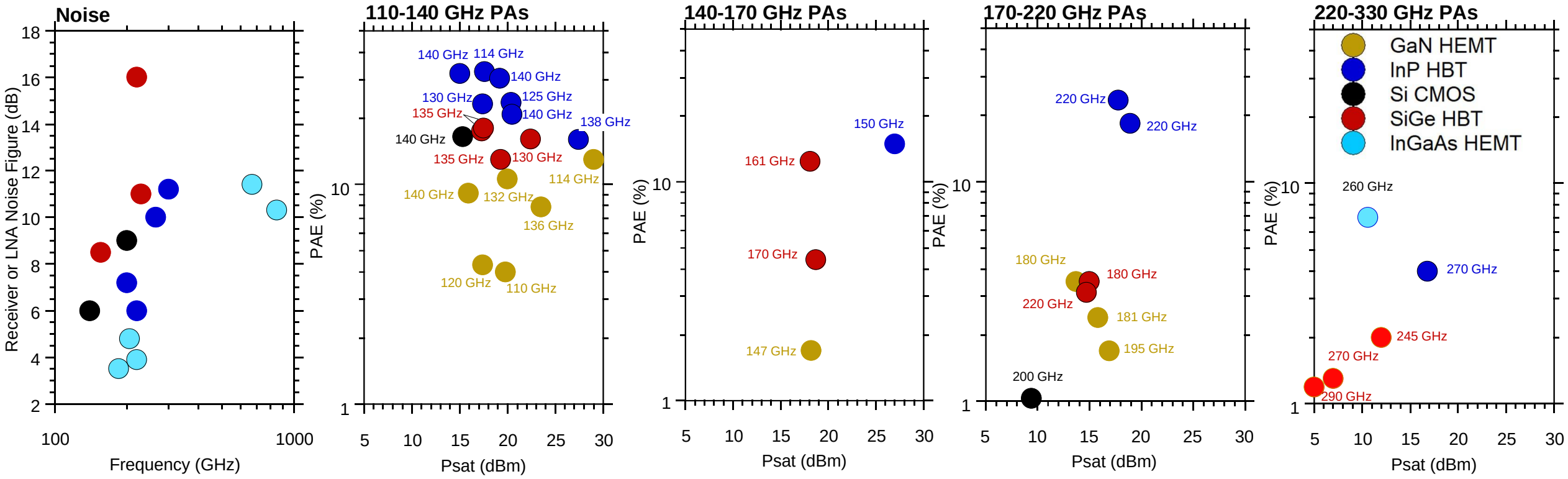




Transistors for 100-300 GHz

CMOS: good power & noise up to ~150GHz. Not much beyond. Best published mmwave results at 65-16 nm nodes.
InP HBT: record 100-300 GHz PAs, record integrated transceivers
SiGe HBT: power better than CMOS, worse than InP HBT
GaN HEMT: record power below 100GHz. Bandwidth improving
InGaAs HEMT: world's best low-noise amplifiers

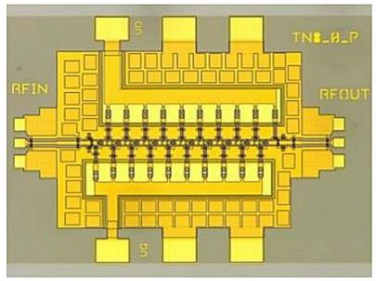
Results compiled 8/16/2023

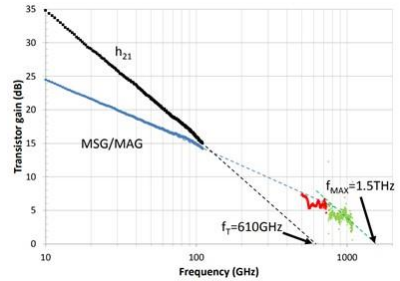


InP Transistors and ICs

30 nm InP HEMTs: 1.5THz f_{max}, 1.0THz amplifiers

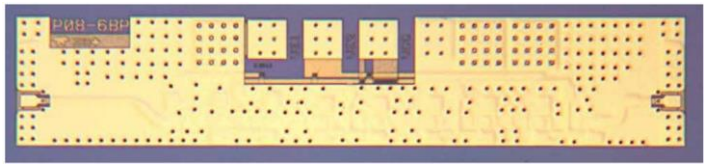
W. Deal et al., 2016 IEDM (Northrop-Grumman)

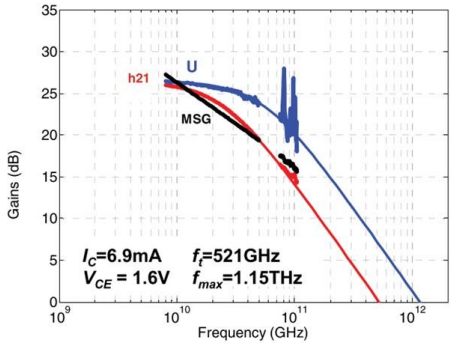


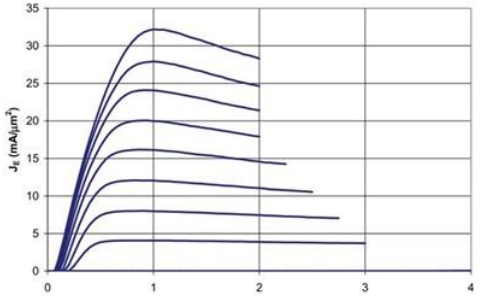


130nm InP HBTs: 1.1THz f_{max}, 3.5V. 670 GHz amplifiers

M. Urteaga, et al., IEEE Device Research Conference, 2011.
M. Urteaga, et al., IEEE Proceedings, 2017 (Teledyne, UCSB)



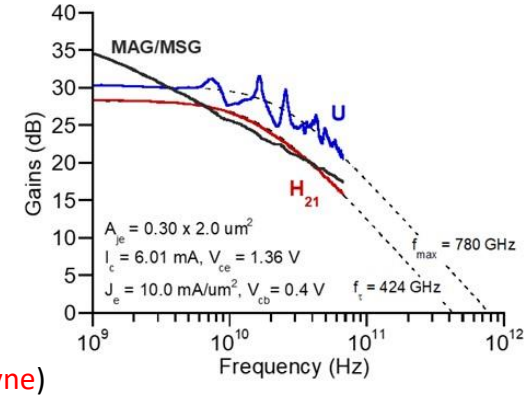


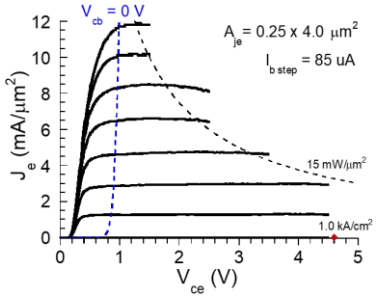


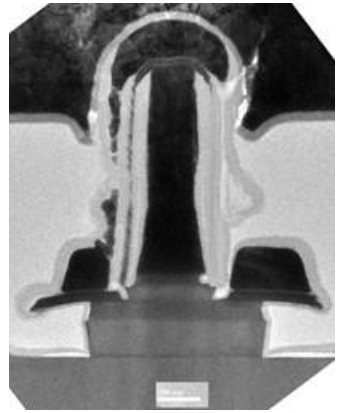
250nm InP HBTs: 650GHz f_{max}, 4.5V.

Z. Griffith et al., 2007 IPRM conference (UCSB)

M. Urteaga, et al., IEEE Proceedings, 2017 (Teledyne)







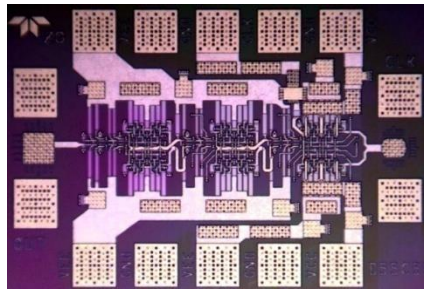
THz HBT Scaling Laws

Rodwell, et al., IEEE Proceedings June 2008 (UCSB, Teledyne)
Contacts: Baraskar et al., Journal of Applied Physics 2013 (UCSB)

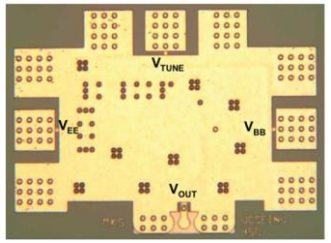
InP HBT ICs: 60-670 GHz

M. Urteaga, et al., IEEE Proceedings, 2017 (Teledyne)
Z. Griffith et al., IEEE CSICS, 2010 (Teledyne)
M. Seo et al., IEICE Electronics Express, 2015 (Teledyne)

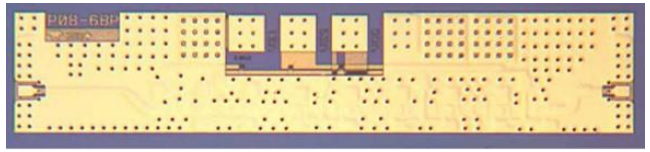
208 GHz master-slave latch



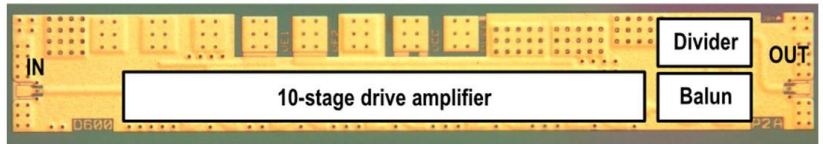
688 GHz fundamental oscillator



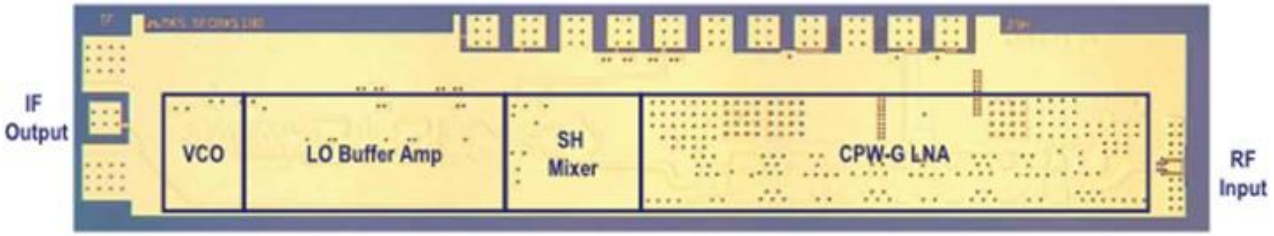
670 GHz amplifier



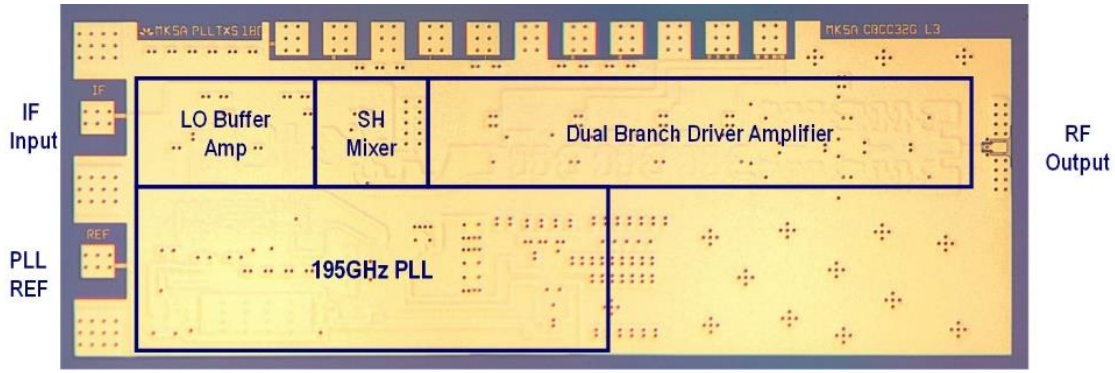
529 GHz dynamic divider



570 GHz receiver



600 GHz transmitter



Bipolar Transistor Design

$$\tau_b \approx T_b^2 / 2D_n$$

$$\tau_c = T_c / 2v_{sat}$$

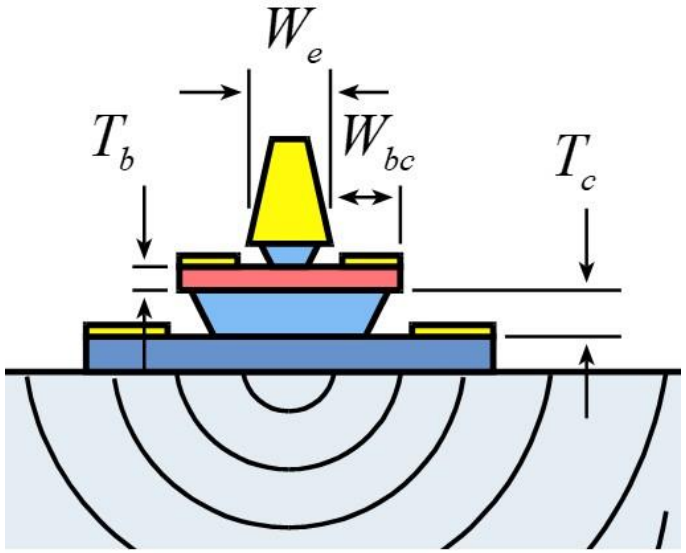
$$C_{cb} = \varepsilon A_c / T_c$$

$$I_{c,\max} \propto v_{electron} A_e (V_{\text{ce,operating}} + V_{\text{ce,punch-through}}) / T_c^2$$

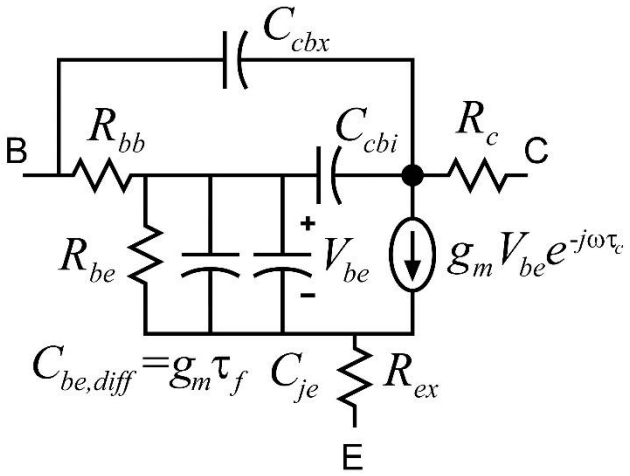
$$\Delta T \propto \frac{P}{L_E}\left[1 + \ln\left(\frac{L_e}{W_e}\right)\right]$$

$$R_{ex} = \rho_{\text{contact}} / A_e$$

$$R_{bb} = \rho_{\text{sheet}}\left(\frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e}\right) + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}}$$



(emitter length L_E)



Bipolar Transistor Design: Scaling

$$\tau_b \approx T_b^2 / 2D_n$$

$$\tau_c = T_c / 2v_{sat}$$

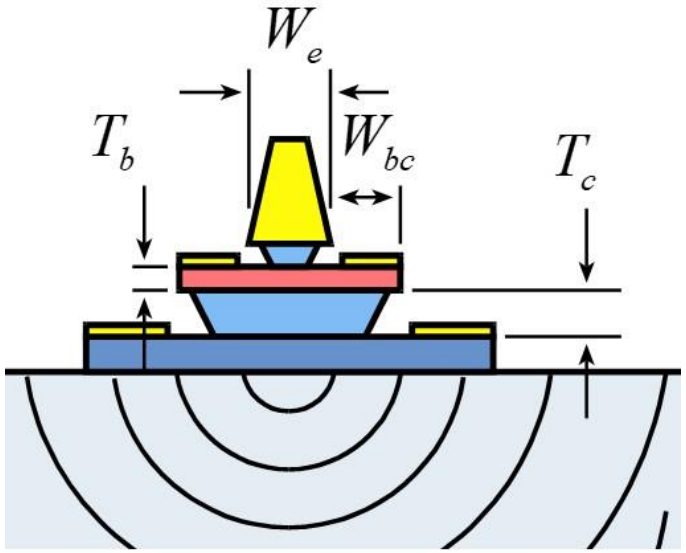
$$C_{cb} = \varepsilon A_c / T_c$$

$$I_{c,\max} \propto v_{electron} A_e (V_{\text{ce,operating}} + V_{\text{ce,punch-through}}) / T_c^2$$

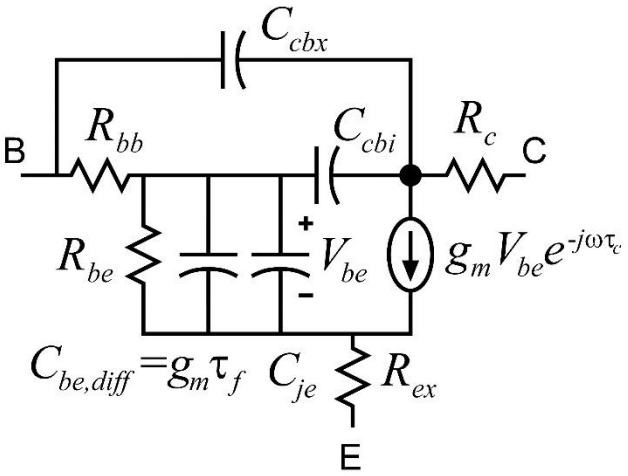
$$\Delta T \propto \frac{P}{L_E}\left[1 + \ln\left(\frac{L_e}{W_e}\right)\right]$$

$$R_{ex} = \rho_{\text{contact}} / A_e$$

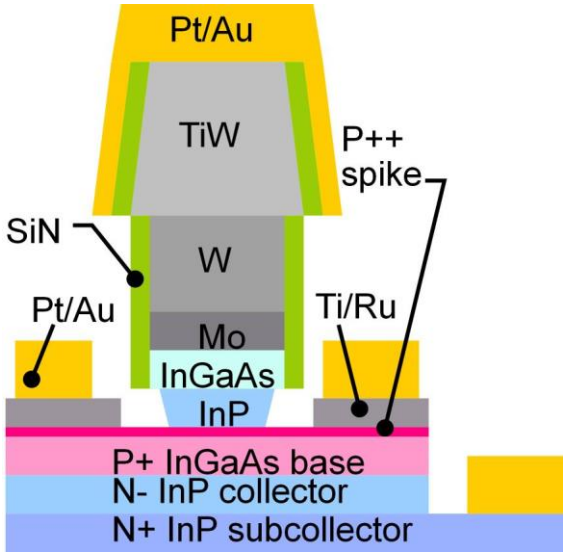
$$R_{bb} = \rho_{\text{sheet}}\left(\frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e}\right) + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}}$$



(emitter length L_E)



Bipolar Transistor Scaling Laws



to double the bandwidth:	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm^2)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1

Narrow junctions.

Thin layers

High current density

Ultra low resistivity contacts

Ultra low resistivity refractory contacts for THz HBTs

Ohmic contact resistivity:
the key challenge for THz HBTs.

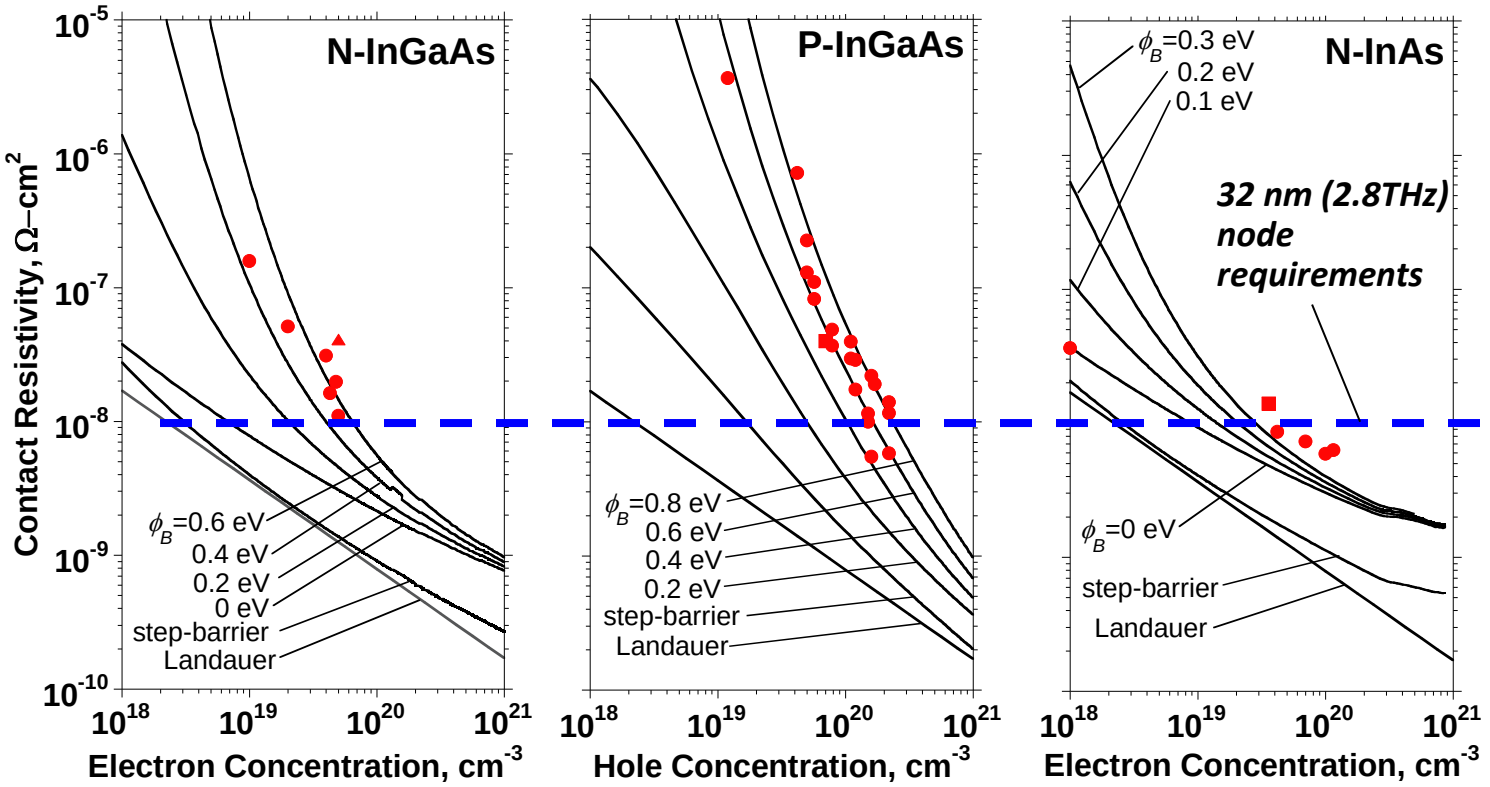
Refractory contacts:
robust under high-current operation

Low penetration depth: ~ 1 nm

Performance sufficient for 32 nm /2.8 THz node.

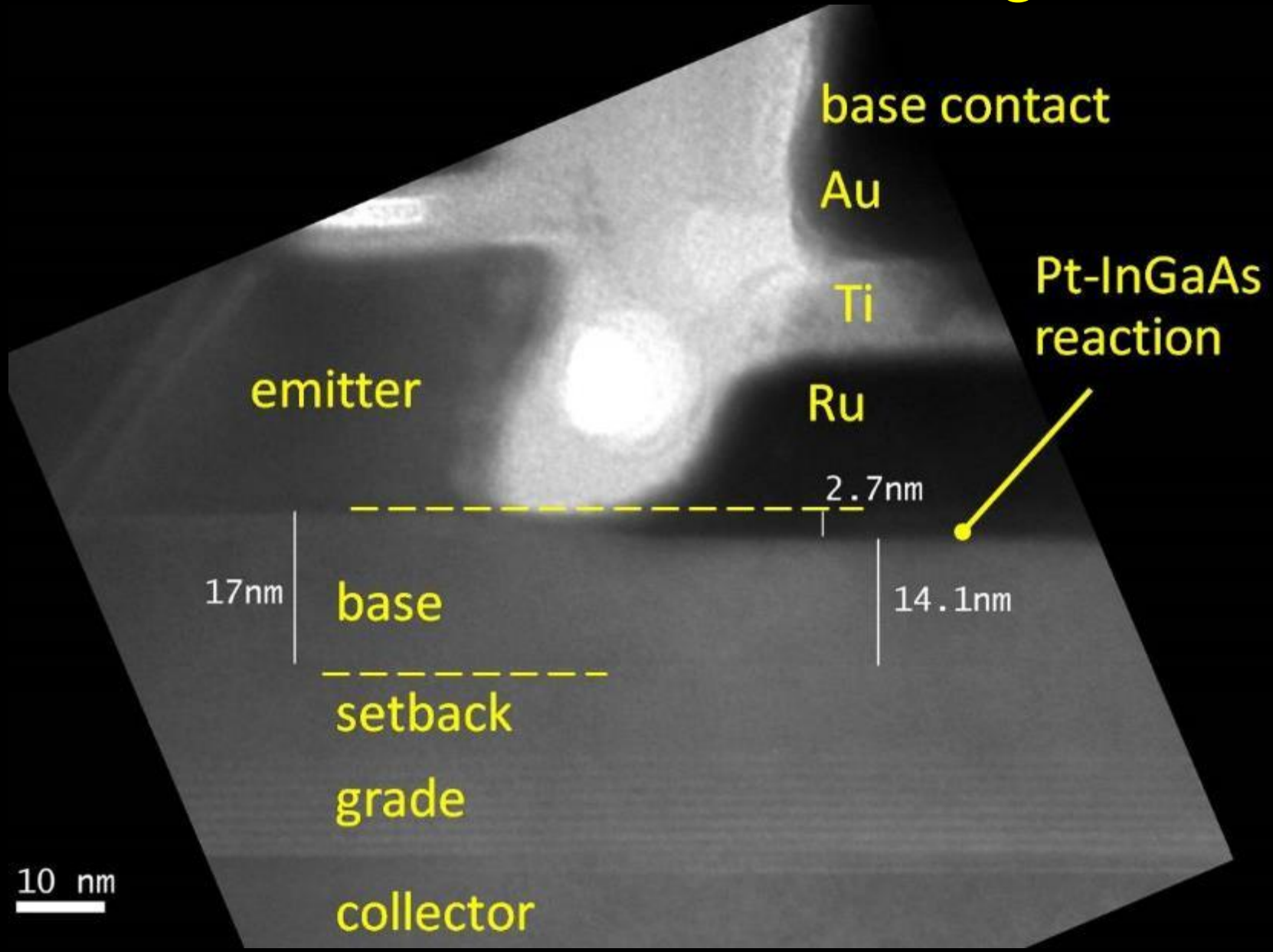
Why no ~2 THz HBTs today ?
Can't reproduce such base contacts in full HBT process flow.

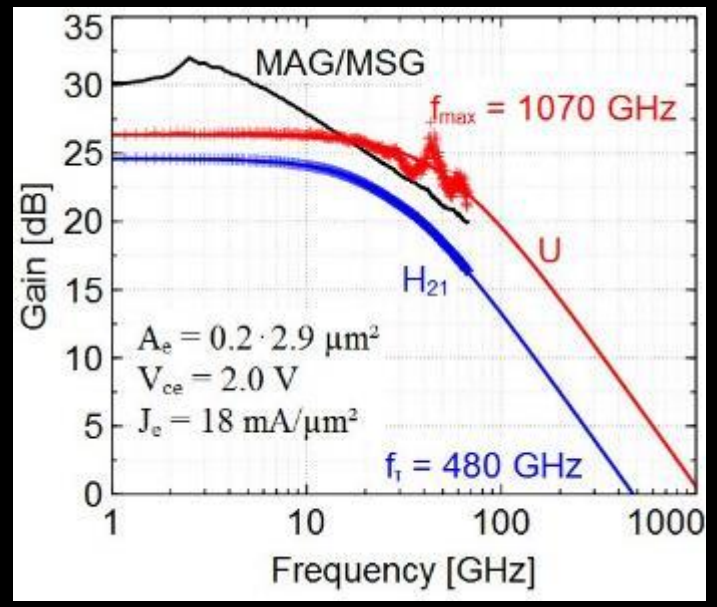
Baraskar *et al*, Journal of Applied Physics, 2013 (UCSB)

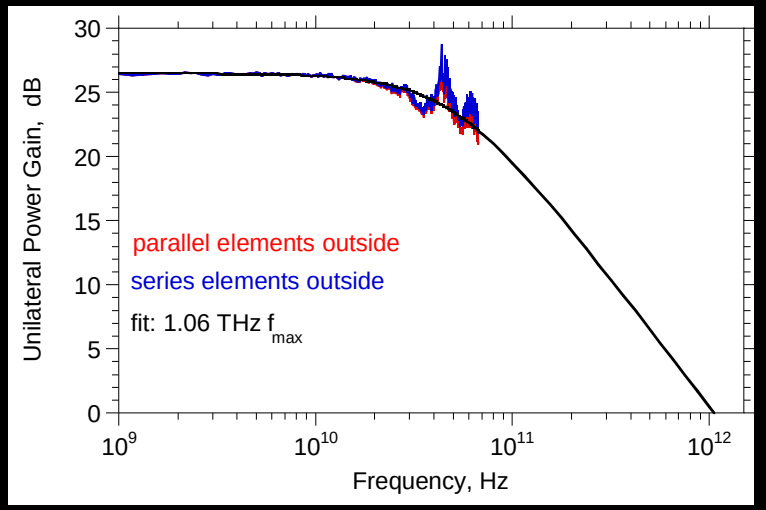


InP HBTs: 1.07 THz @ W_e= 200 nm

Rode et al., IEEE TED, Aug. 2015 (UCSB)





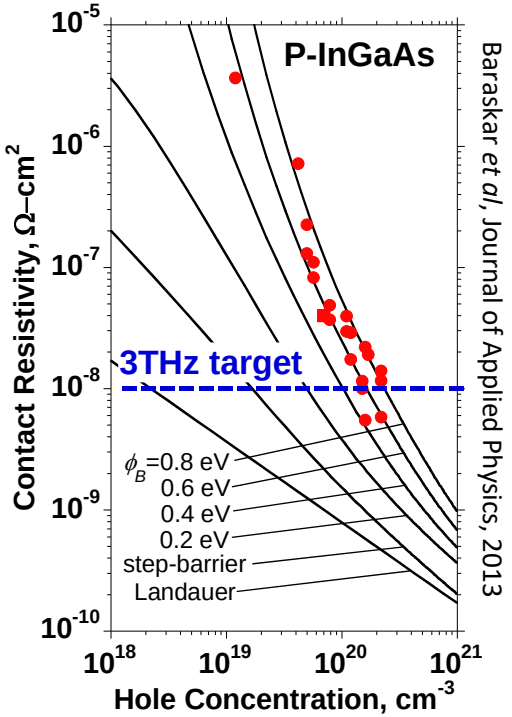


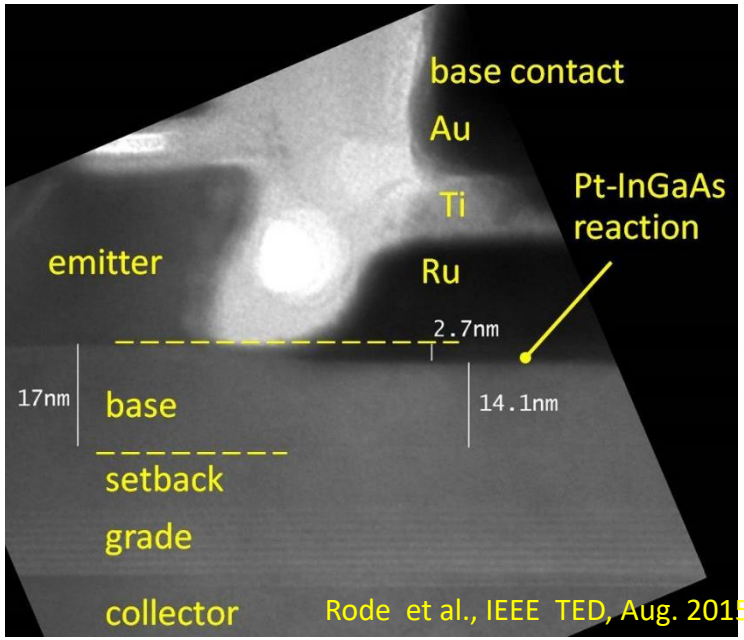
Challenges at the 64nm/2THz & 32nm/3THz Nodes

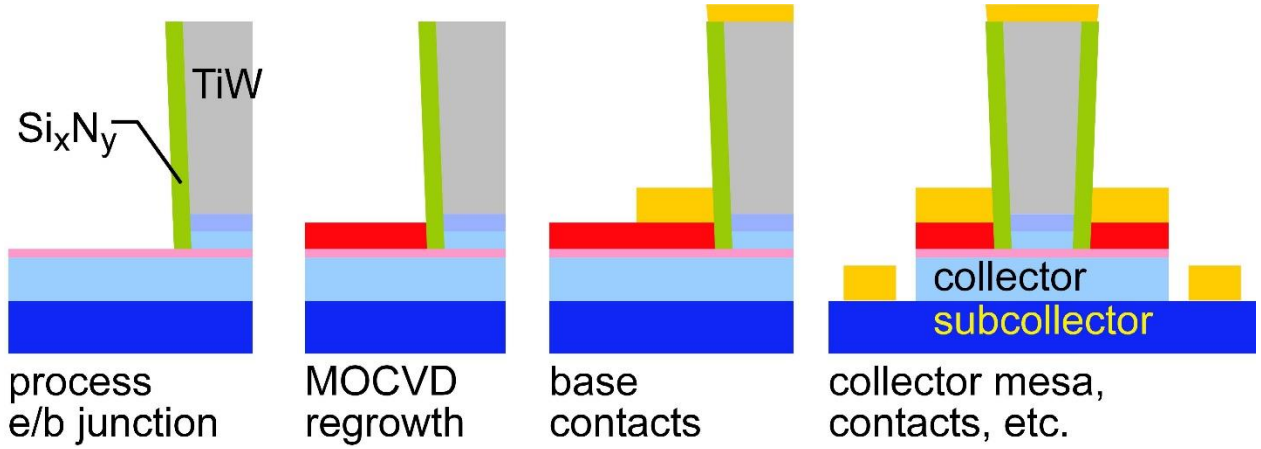
Need high base contact doping
>10^{20}/cm^3 for good contacts
high Auger recombination
very low β.

Need moderate contact penetration
Pd or Pt contacts
react with 3++ nm of base
penetrate surface contaminants
too deep for thin base

Solution: base regrowth:
thin, moderately-doped intrinsic base
InGaAs or GaAsSb @ 10^{19}-10^{20}/cm^3
thick, heavily-doped extrinsic base
P-GaAs, ~10^{21}/cm^3







Regrown-Base InP HBTs: status at end of effort.

Good DC data: even given regrowth

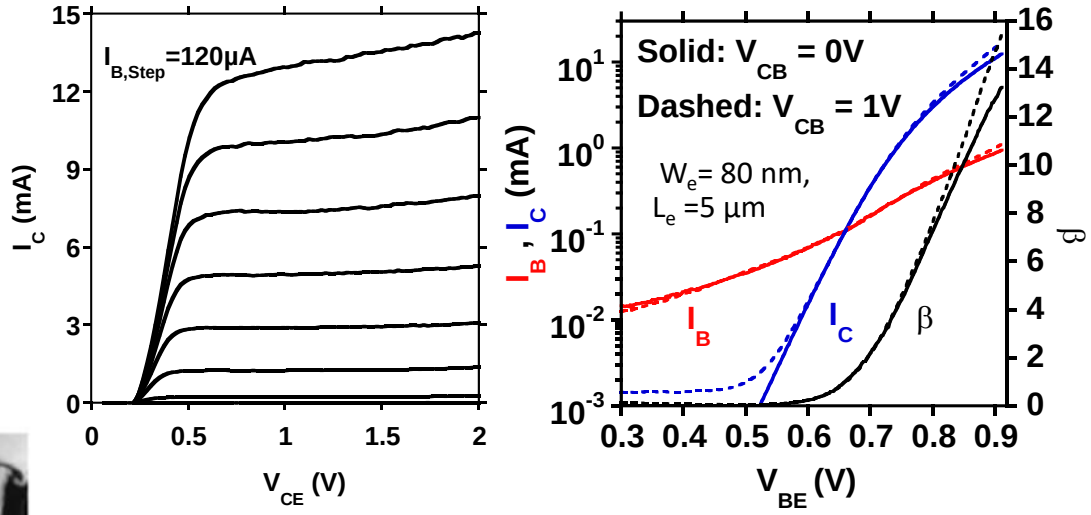
refractory Mo/W/TiW emitter contact maintains low ρ_c.

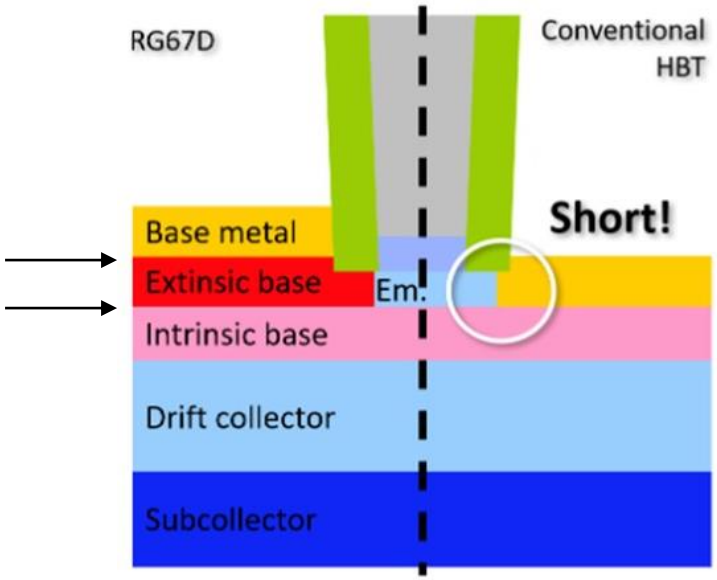
Excellent base contacts; but hydrogen base passivation

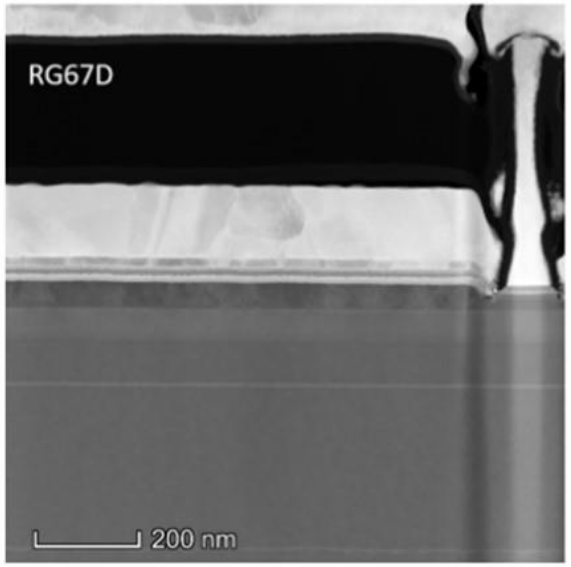
- 0.4 Ω–μm² resistivity for GaAs/metal contact ✓
- 290 Ω sheet resistivity for regrown base ✓
- 0.60Ω–μm² resistivity for InGaAs/GaAs contact ✗
- 1940Ω/ sheet resistivity for intrinsic base ✗

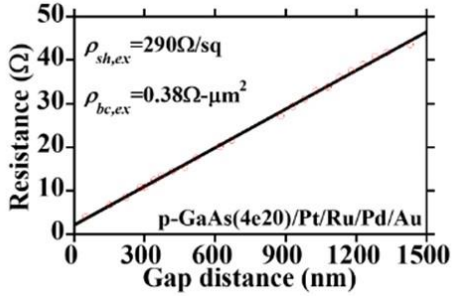
(hydrogen anneal needed further adjustment)

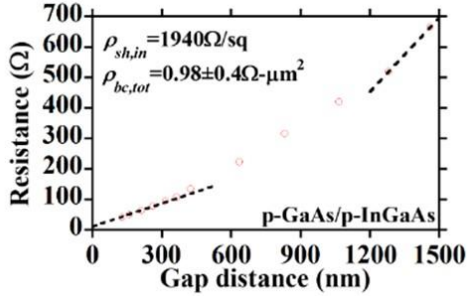
Y. Fang et al, 2019 IEEE DRC (UCSB)











Making faster field-effect transistors

Scaling laws: Rodwell, IEEE DRC 2010
1.5 THz HEMTs: Deal, 2016 IEDM
1 THz MOS-HEMT: Whitaker, IEEE DRC 2023

III-V FET scaling laws to double bandwidth →

FET parameter	change
gate length	decrease 2:1
transport mass	constant
2DEG electron density	increase 2:1
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel state density	increase 2:1
contact resistivities	decrease 4:1

Needs:

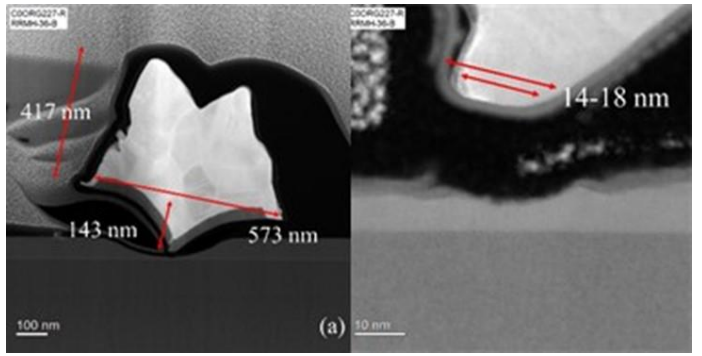
shorter gates
thinner channels
less resistive contacts
thinner (equivalent) gate dielectric
greater channel charge

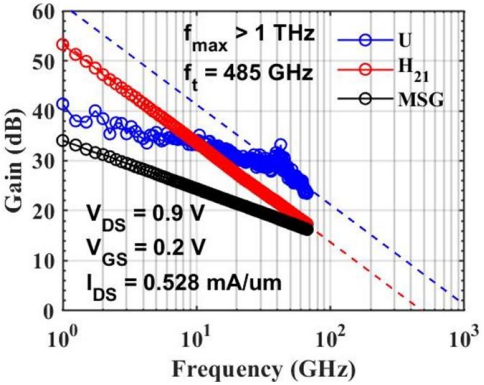
State of art: 32 nm gate length HEMT

1.5 THz f_{max} (Northrop-Grumman)
semiconductor gate dielectric limits further scaling

Further scaling may be feasible

target ~2 THz f_{max}
lower F_{min} @ 100-300 GHz
high-K ZrO_2 gate dielectric
increased charge: InP channel ?



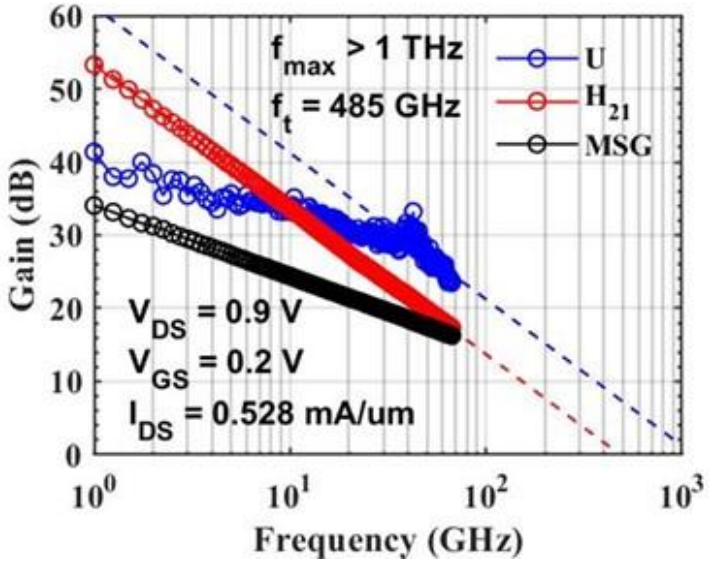


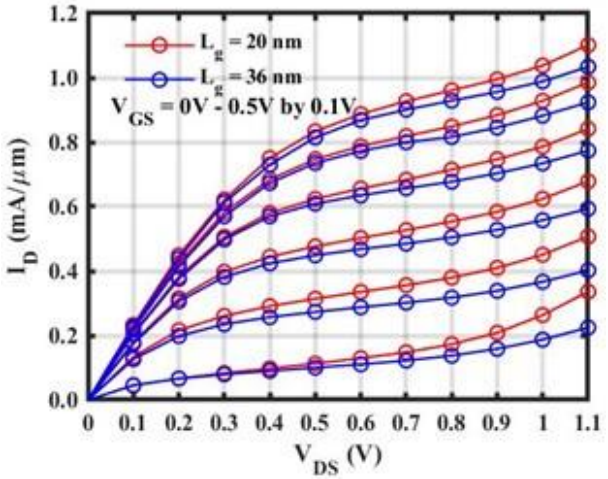
THz InGaAs-channel MOS-HEMT

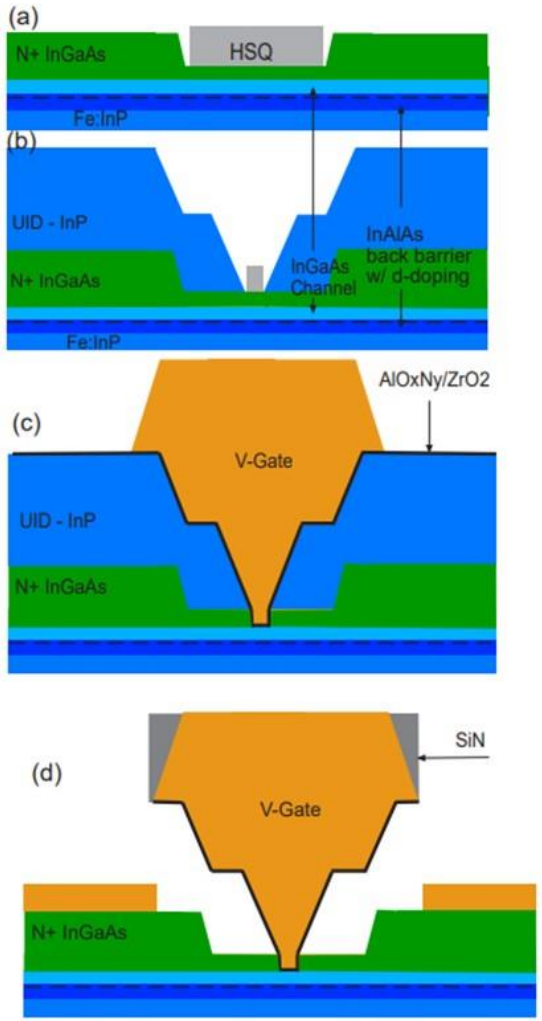
L. Whitaker et al, 2023 IEEE DRC (UCSB)

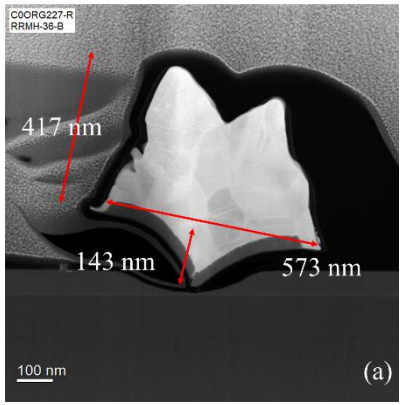
Gate dielectric:
0.83 nm $Al_xO_yN_z$ / 1.7 nm ZrO_2
improved electrostatics vs. ~6 nm InAlAs.
potential for improved (f_τ, f_{max}) with scaling

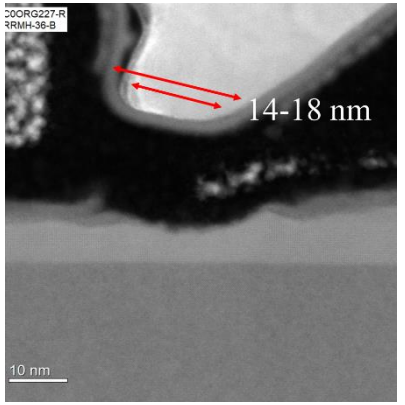
Remaining scaling barrier:
Limited (low) state density of InGaAs channel
Barrier to necessary g_m/W_g increase with scaling
Theory (right/wrong ?) suggests using InP channel

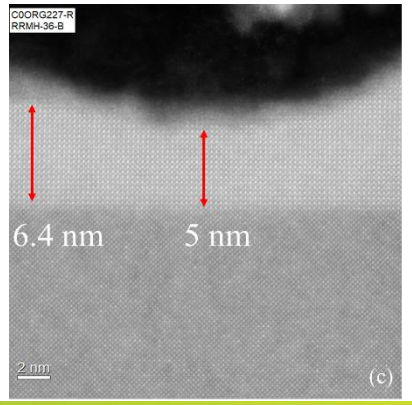












Transistor layouts: *I*, *V*, *Z*, and *P*.

R_L below 25 Ω or above 75 Ω is hard to realize.

$$I_{\max} = \frac{\Delta V}{R_L} = J_{\max} \cdot (\text{number fingers})(\text{finger length});$$

$$\rightarrow (\text{number fingers})(\text{finger length}) = \frac{\Delta V}{J_{\max} R_L}$$

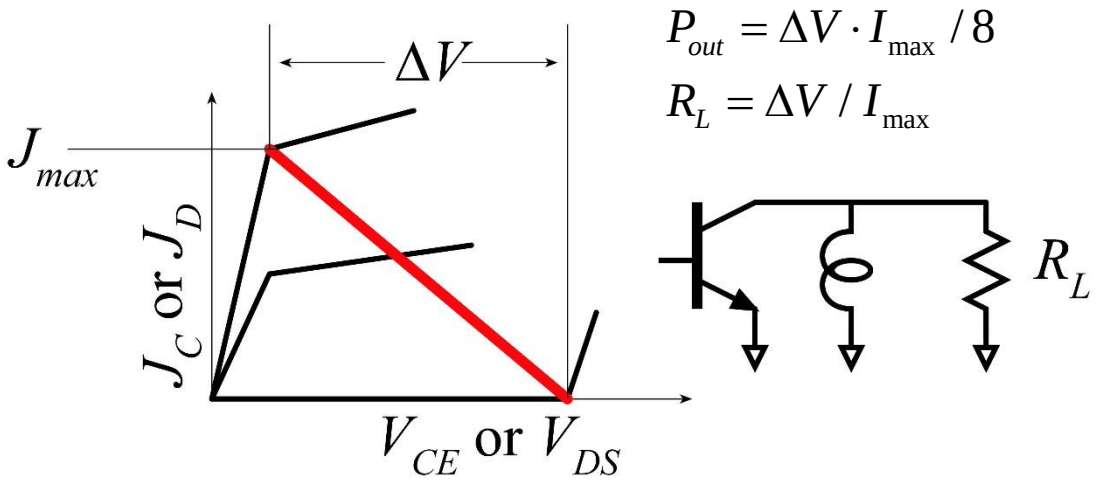
Large ΔV, small $J_{\max}$, or small R_L:

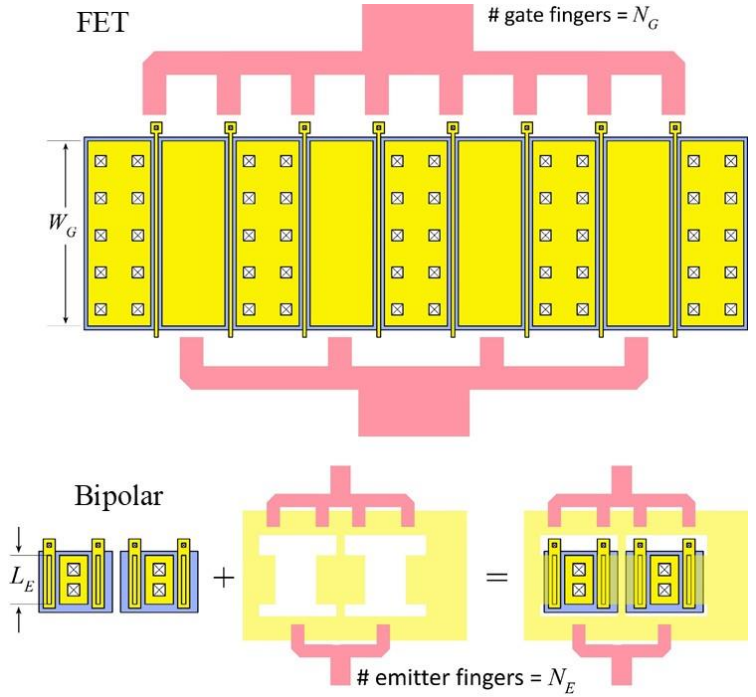
long fingers or many fingers → layout parasitics → lower $f_{\max}$.

Higher frequencies need smaller layout parasitics

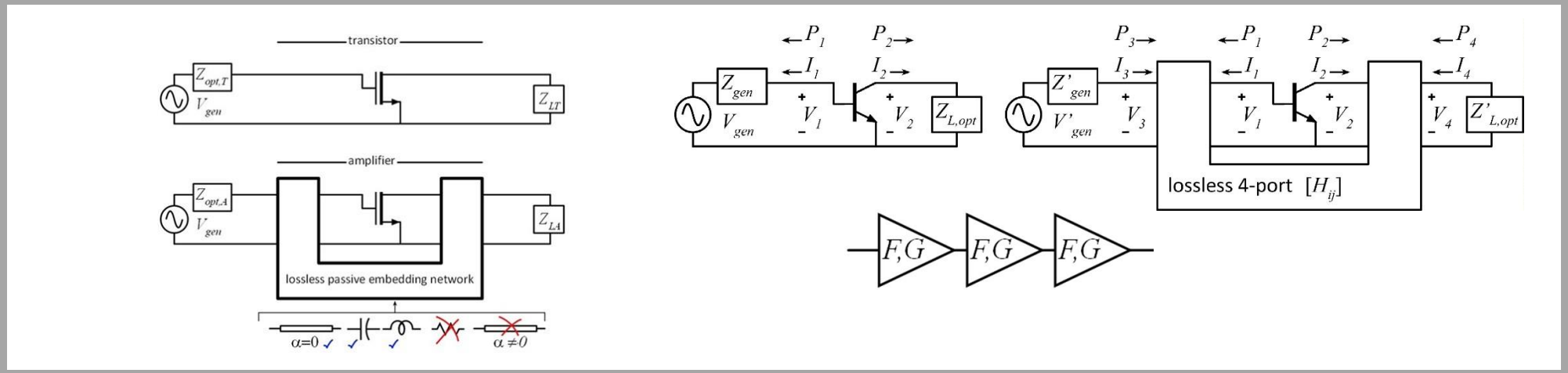
→ shorter fingers (length$_{\max} \propto f^{-1/2}$), fewer fingers (#$_{\max} \propto f^{-1}$)

Technologies with high ΔV and low $J_{\max}$ are problematic.





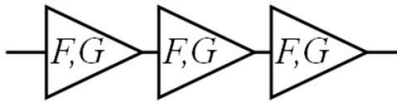
IC Design Basics



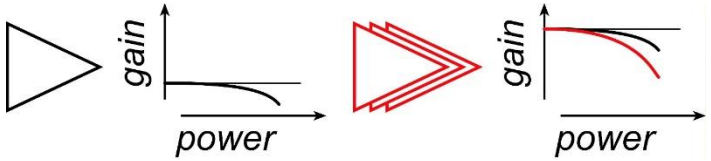
100-300 GHz: transistor requirements, IC design

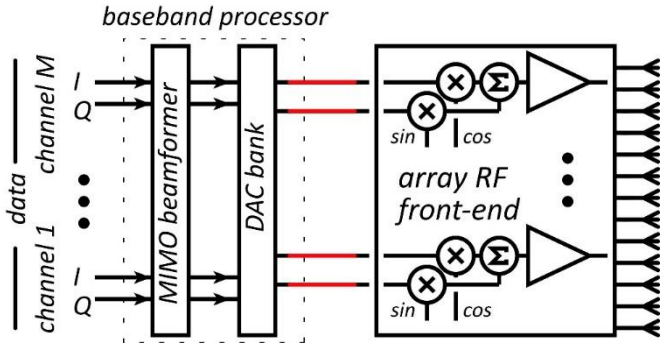
Transmitters need:
high power-added efficiency $PAE = (P_{out} - P_{in})/P_{DC}$
high added power density (P_{out}-P_{in})/(gate width, emitter length)

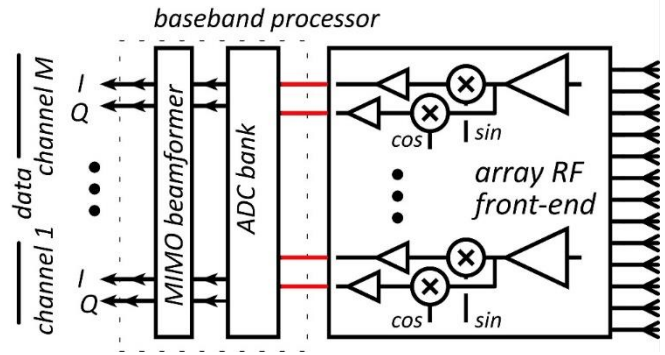
Receivers need:
low cascaded noise $F_{casc} = F + (F-1)/G + (F-1)/G^2 + \cdots$



Need reasonable gain/stage.
die area, power,
accumulated gain compression







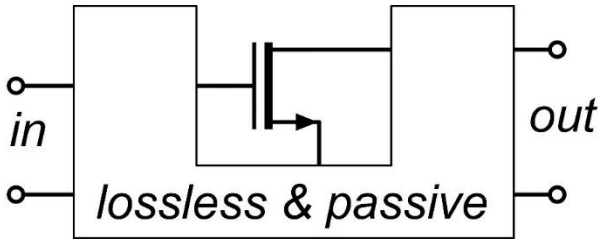
At 100-300 GHz, transistor performance is marginal…
…how do we design PAs, LNAs, for performance close to transistor limits ?

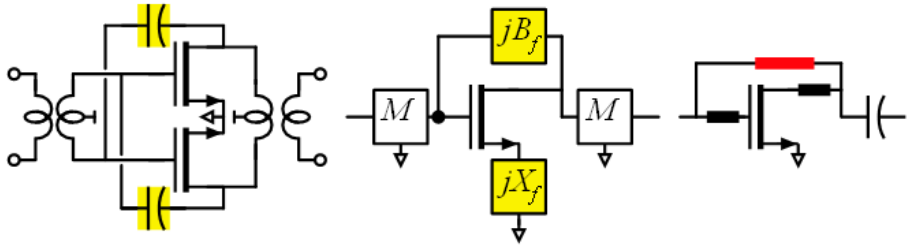
Where the IC designer can't help

mm-wave transistor gain is low: gain-boosting is common

Common-source vs. common-gate.

Capacitive neutralization. Unconditionally stable positive feedback (Singhakowinta, Int. J. Electronics, 1966)

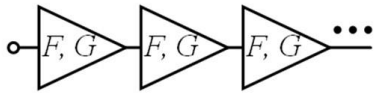




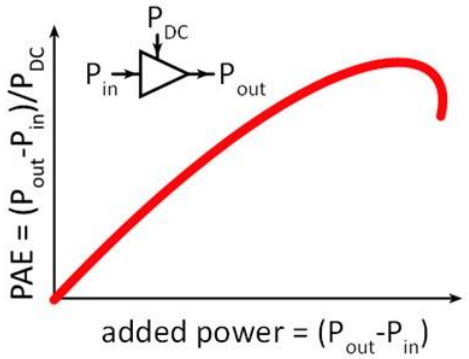
Such circuits don't improve the parameters that matter the most.

The circuit* doesn't change the transistor minimum cascaded noise figure. (Haus, Adler, Proc. IRE, 1958)

The circuit* doesn't change the transistor maximum efficiency vs. added power curve.



$$F_{casc} = 1 + M = F + (F-1)/G + (F-1)/G^2 + \cdots$$

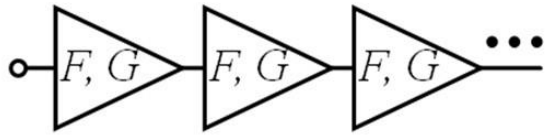


*If lossless, and given the correct source and load impedances.

Noise Measure Invariance

Cascaded noise figure F_C , noise measure M.

$$F_c = M + 1 = F + (F-1)/G_A + (F-1)/G_A^2 + \ldots$$



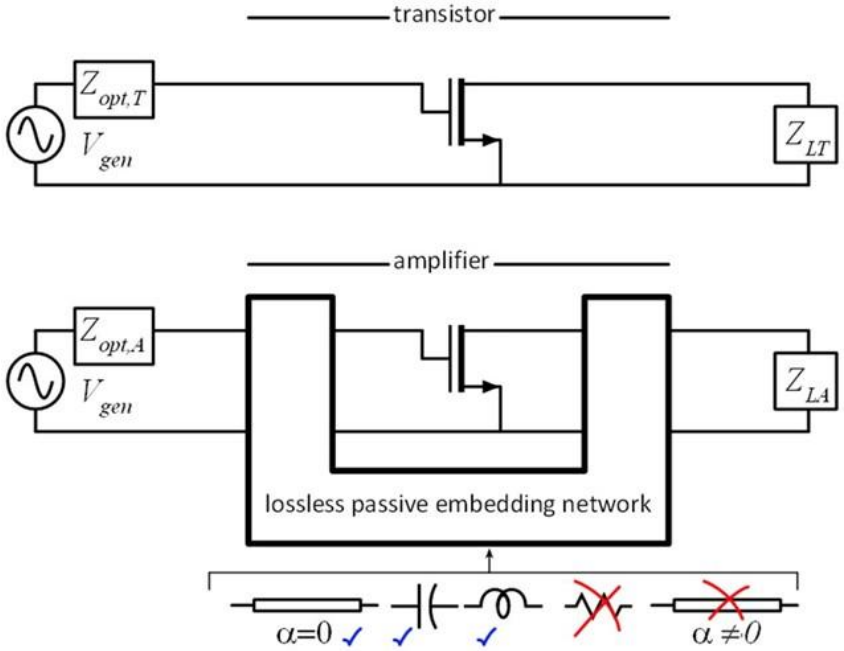
Minimum cascaded noise figure $F_{C,\min}$, optimum noise measure M_{opt}:

...minimum values obtained with optimum source impedance.

M_{opt} (and hence $F_{C,\min}$) are invariant with respect to lossless embedding.

In any lossless LNA topology, $M_{\min,\mathrm{LNA}} = M_{\min,\mathrm{transistor}}$, $F_{C,\min,\mathrm{LNA}} = F_{C,\min,\mathrm{transistor}}$.

$F_{C,\min.\mathrm{transistor}}$ defines the lowest acheivable LNA cascaded noise figure.



H. A. Haus and R. B. Adler, "Optimum Noise Performance of Linear Amplifiers," in Proceedings of the IRE, vol. 46, no. 8, pp. 1517-1533, **Aug. 1958**.

N. Baniasadi and A. M. Niknejad, "Noise Measure Revisited for Design of Amplifiers Close to Activity Limits," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 69, no. 6, pp. 2276-2283, June 2022.

Noise Measure Invariance: Implications

All lossless circuits using the same transistor have the same $M_{\min}$.

Common source/emitter has the same $M_{\min}$ as common gate/base.

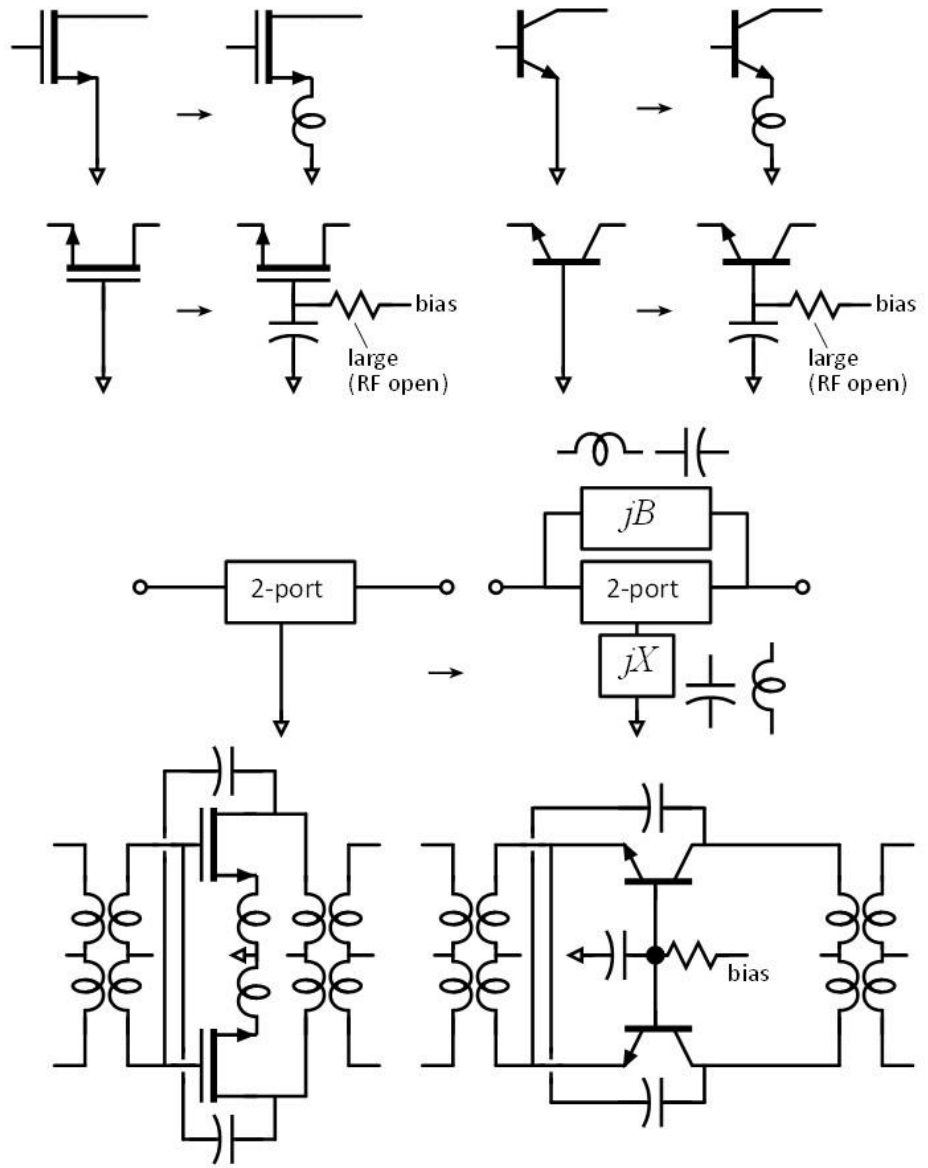
Reactive feedback for simultaneous noise and gain tuning does not change $M_{\min}$.

Capacitive neutralization for gain-peaking does not change $M_{\min}$.

Singhakowinta's feedback does not change $M_{\min}$.

... in all cases *given that the appropriate Z_{source} is used*.
and *given that the embedding circuit is lossless*

For lowest LNA noise, pick topology with smallest tuning losses.



Cascode LNAs and noise measure invariance

Simple cascode:

Sub-optimum Z_{source} for common-base stage

$\rightarrow$ Cascode stage $F_{C,cascode} > F_{C,transistor}$.

Cascode with internal noise-match

Optimum Z_{source} for common-base stage

$\rightarrow$ Cascode stage $F_{C,cascode} = F_{C,transistor}$.

Cascaded common-emitter stages

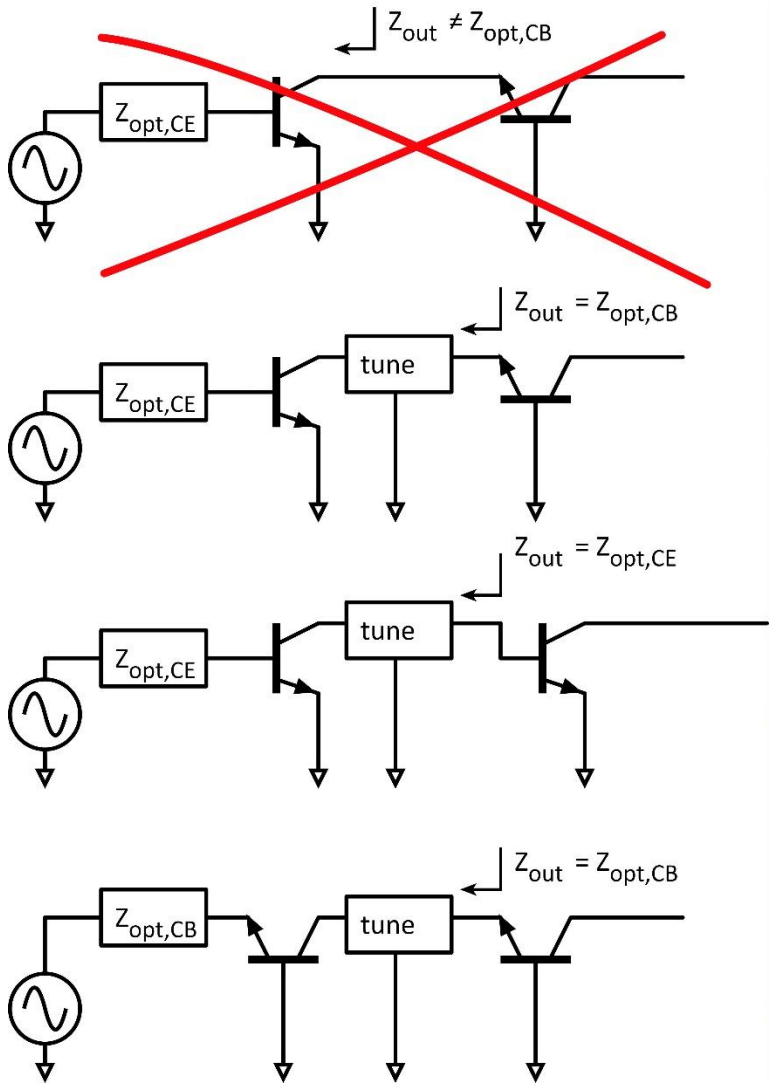
Optimum Z_{source} for each stage

$F_{C,multi-stage} = F_{C,transistor}$

Cascaded common-base stages

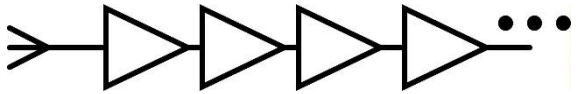
Optimum Z_{source} for each stage

$F_{C,multi-stage} = F_{C,transistor}$



LNA design for noise close to transistor limit

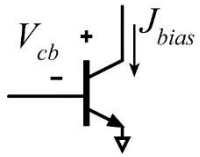
1) Goal: low noise measure, not noise figure

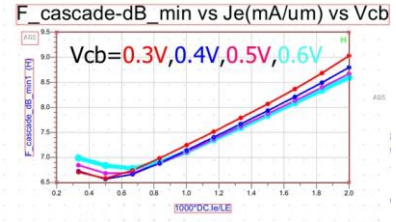


$$F_{\text{cascade}} = M + 1 = F + \frac{F-1}{G} + \frac{F-1}{G^2} + \ldots = \frac{F - 1/G}{1 - 1/G}$$

F = noise figure, M = noise measure

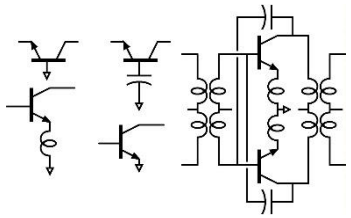
2) Find bias (*J*,*V*) for lowest noise measure





@210GHz,
$F_{\text{cascade,min}}$= 6.57 dB
given:
J_e=0.5 mA/um,
V_{cb}=0.3V

3) Minimum M is independent of circuit configuration*; pick for high bandwidth or high gain/stage (= low P_{DC})

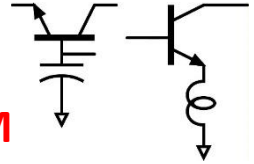


<-- all give the same minimum M…

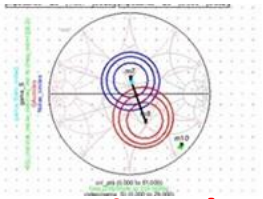
…but common-base gives highest gain (InP HBT @210GHz).

*HA Haus, RB Adler, Proceedings of the IRE, 1958

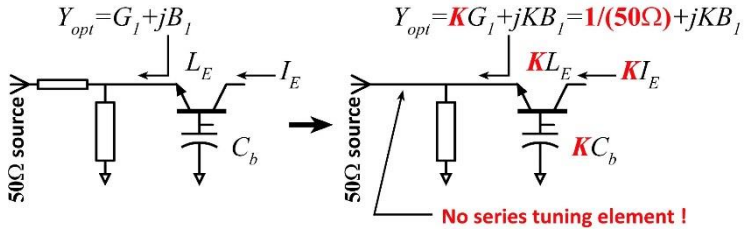
4) Capacitance in common-base; just like inductance in common-emitter, allows simultaneous tuning for zero reflection coefficient and minimum M



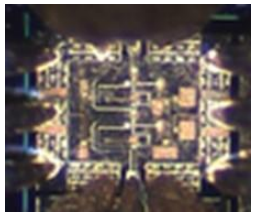
5) Write ADS Python code to display source impedance for minimum M.

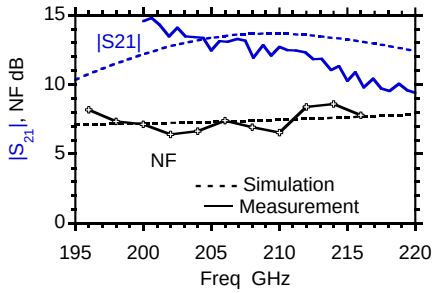


6) Scale transistor size to eliminate series tuning element. Less input tuning→ less noise from passive element loss.



7) Result: $F_{C,LNA}$= 7.4 dB (F=7.2 dB, G=13 dB) given $F_{C,transistor}$= 6.6 dB

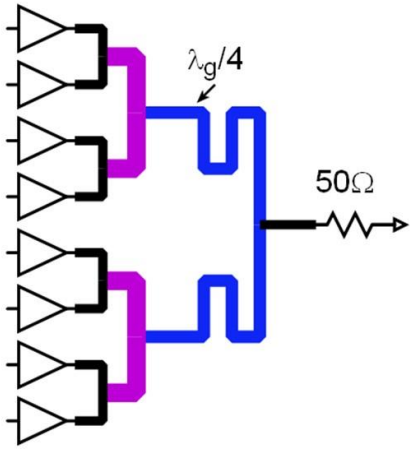




U. Solyu et. al, 2021 EuMIC

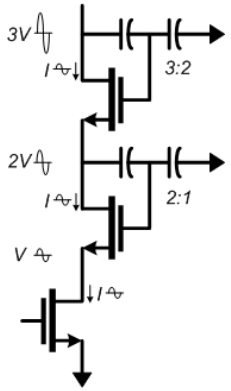
100-300 GHz Power combining: what is best ?

Corporate T-line



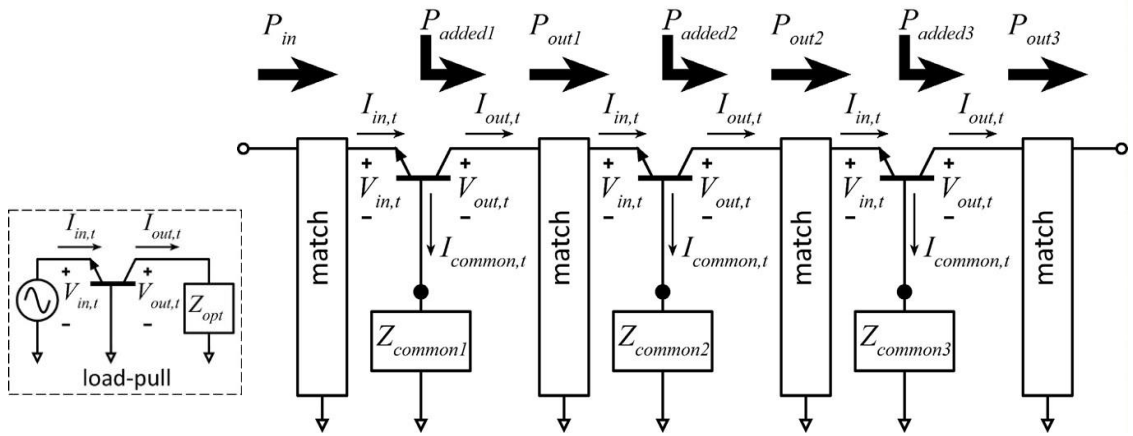
Direct series-connected

M. Shifrin: 1992 IEEE μWave/mmWave Monolithic Circuits Symp. **(Raytheon)**



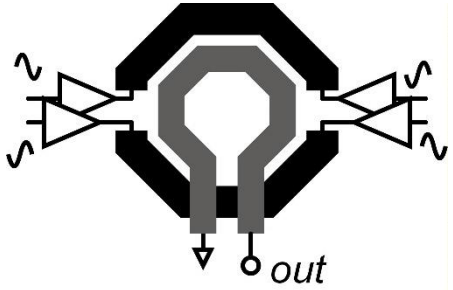
Cascaded combining

A. Ahmed 2018 EuMIC, 2021 RFIC **(UCSB)**



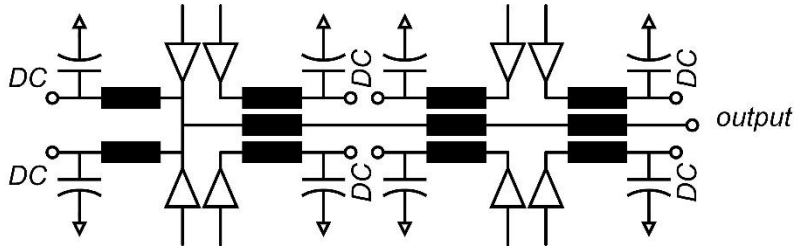
Distributed Active Transformer

I. Aoki, IEEE Trans MTT, Jan. 2002 **(CalTech)**



Balun series-connected

λ/4 baluns: Y. Yoshihara, 2008 IEEE Asian Solid-State Circuits Conference **(Toshiba)**
sub-λ/4 baluns: H. Park, et al., IEEE JSSC, Oct. 2014 **(UCSB)**



On-Wafer Interconnect Losses

Interconnects in packages and on PCBs:

$H \propto 1/\text{frequency}$ (to control radiation loss)

$\text{loss (dB/mm)} \propto (\text{frequency})^{3/2}$

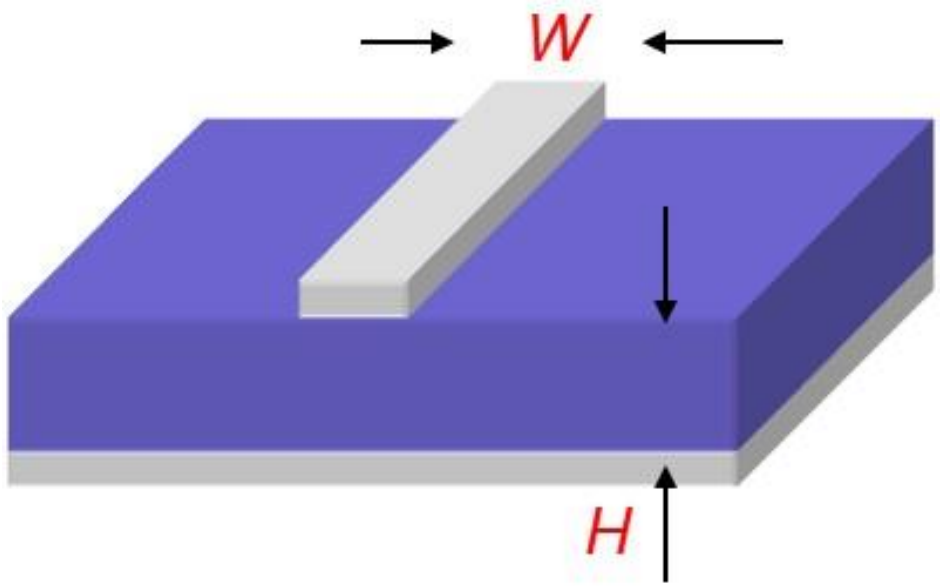
$\text{loss (dB/wavelength)} \propto \sqrt{\text{frequency}}$

Interconnects in ICs:

H is independent of frequency

$\text{loss (dB/mm)} \propto \sqrt{\text{frequency}}$

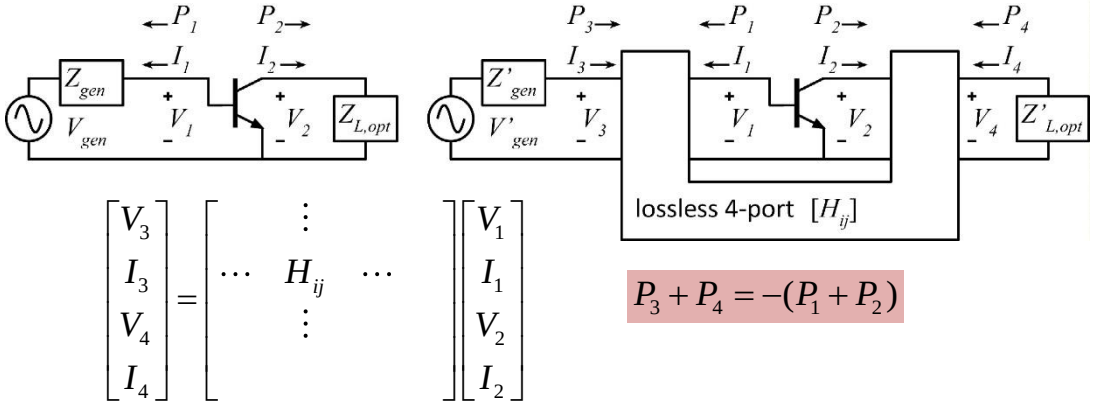
$\text{loss (dB/wavelength)} \propto 1/\sqrt{\text{frequency}}$



Invariance of PAE vs. added power

Given the correct source and load impedances,
all (lossless) power amplifier circuits have the same maximum efficiency vs. added power curve.

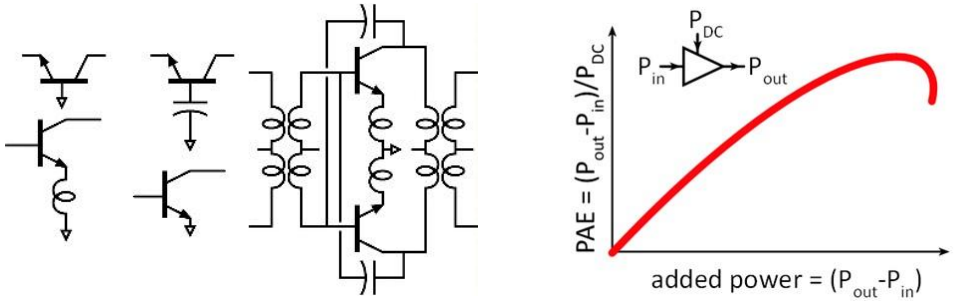
…which is that of the transistor itself.



$(V_1, V_2, I_1, I_2, H_{ij}) \rightarrow (V_3, V_4, I_3, I_4, Z'_{L,opt}, P_{in}, Z_{in})$

Things that don't change PAE:

- Source/emitter inductance in common-source/emitter
- Base/gate capacitance in common base/gate.
- Capacitive neutralization
- Singhakowinta's unconditionally stable positive feedback.

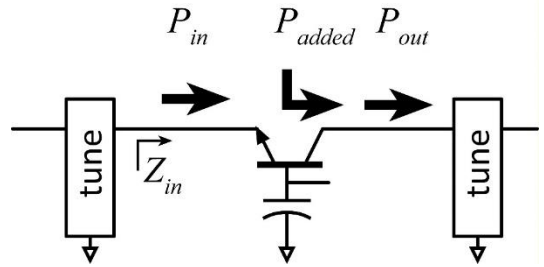


Design for highest PAE:

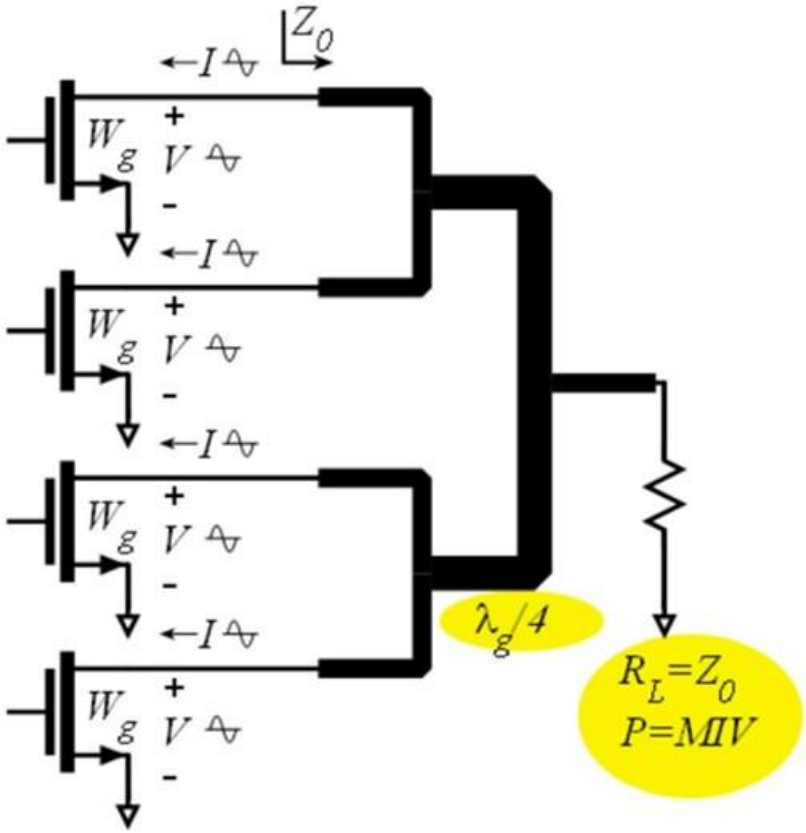
- Pick topology with smallest tuning loss.

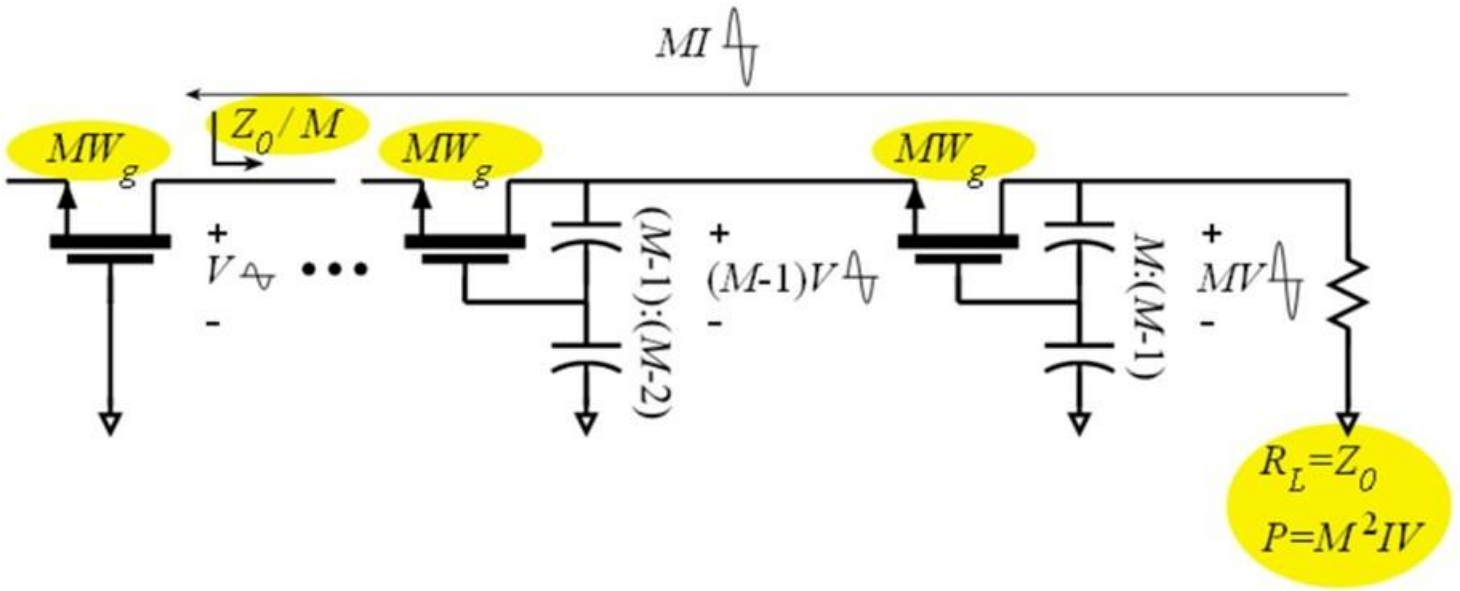
Real PAE design:

- PAE, accumulated gain compression, bandwidth, IM3, …



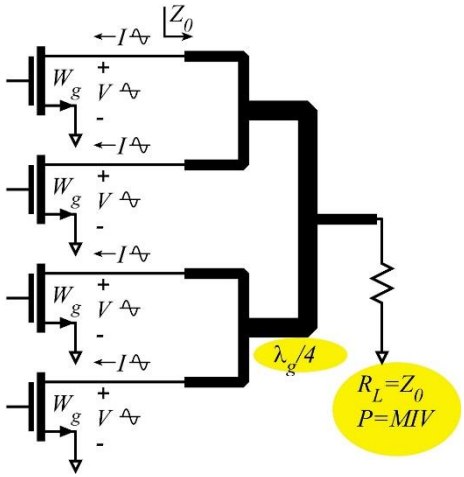
Transistor stacking. Why ? Why not ?

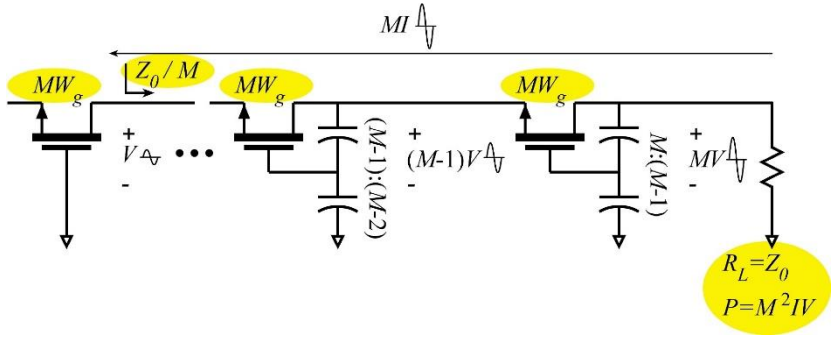


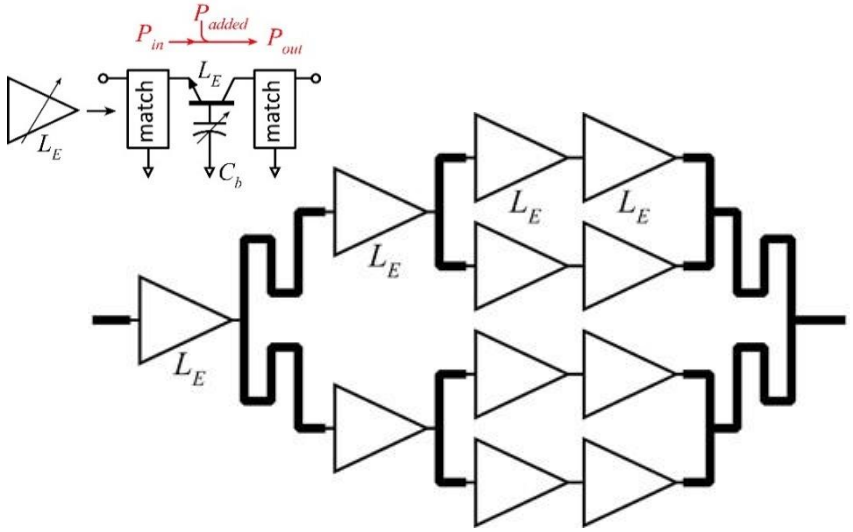


	Lower frequencies	Higher frequencies
Corporate combining	length $\propto 1/f \rightarrow$ large die area ✗ dB loss $\propto 1/\sqrt{f} \rightarrow$ high loss ✗	length $\propto 1/f \rightarrow$ small die area ✓ dB loss $\propto 1/\sqrt{f} \rightarrow$ low loss ✓
Series-connected	more transistor fingers per cell → ok ✓	more transistor fingers per cell→ parasitics ✗

Cascade Combining: Why ? Why not ?

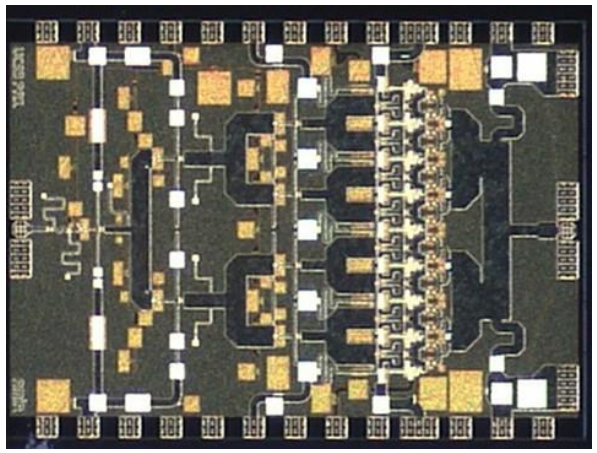


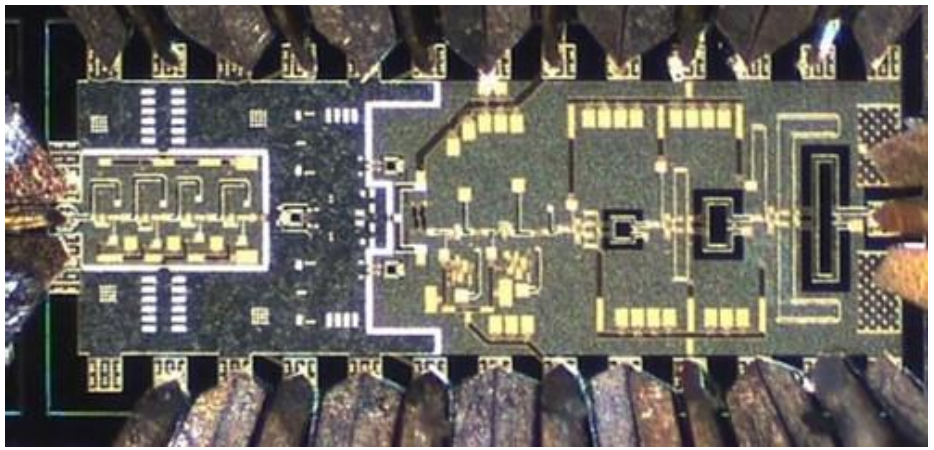


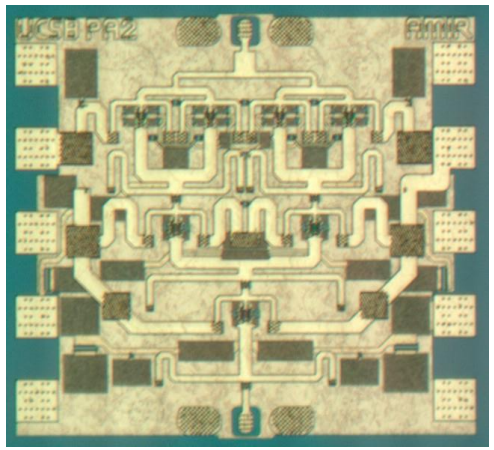


	Lower frequencies	Higher frequencies
Corporate combining	length $\propto 1/f \rightarrow$ large die area ✗ dB loss $\propto 1/\sqrt{f} \rightarrow$ high loss ✗	length $\propto 1/f \rightarrow$ small die area ✓ dB loss $\propto 1/\sqrt{f} \rightarrow$ low loss ✓
Series-connected	more transistor fingers per cell → ok ✓	more transistor fingers per cell→ parasitics ✗
Cascade combining	large interstage matching networks ✗	small interstage matching networks ✓ small # transistor fingers per cell → ok ✓ cascade cell pass-though losses ✗

100-300 GHz ICs

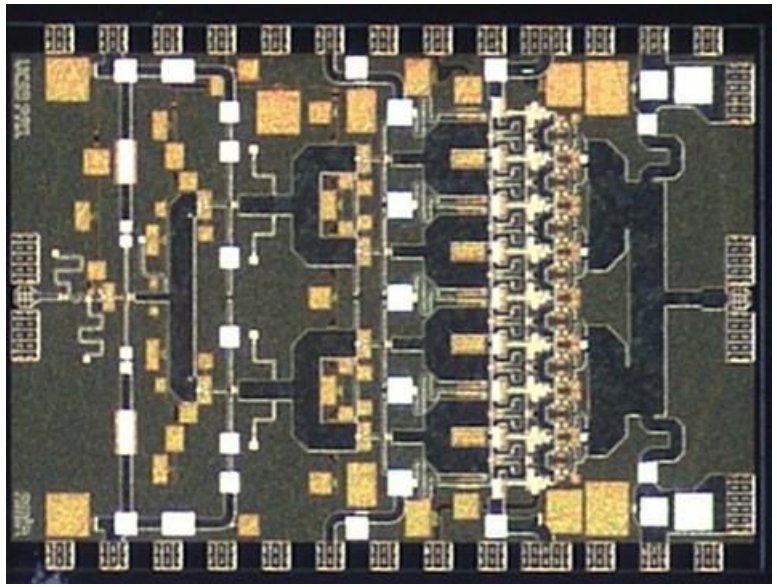




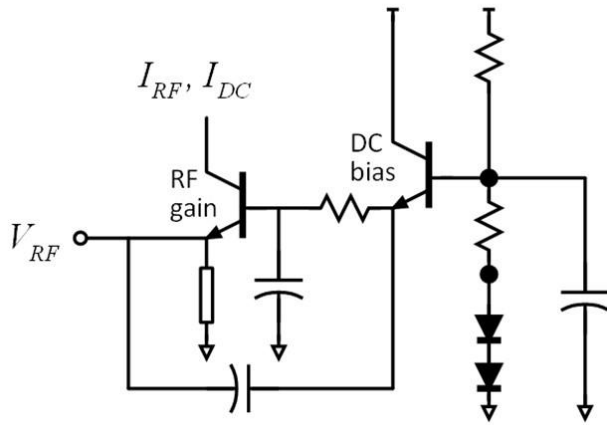


InP HBT Amplifier: 500 mW, 14.9% PAE, 150 GHz

Teledyne 250 nm InP HBT; 2 mm x 1.5 mm

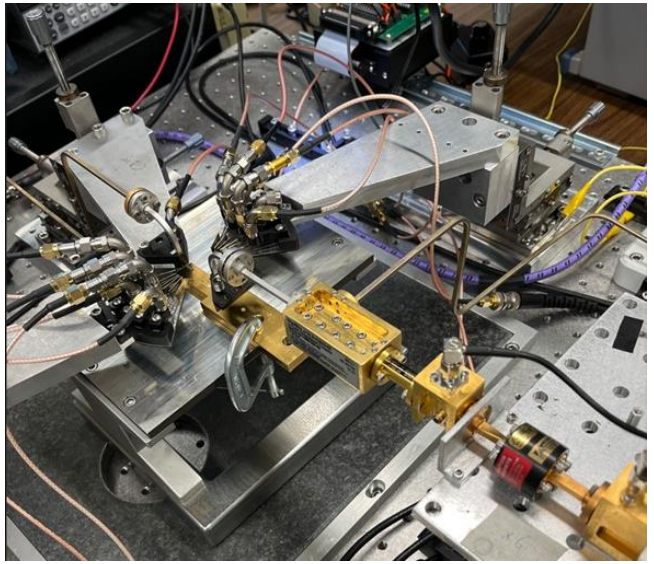


adaptive class-AB bias

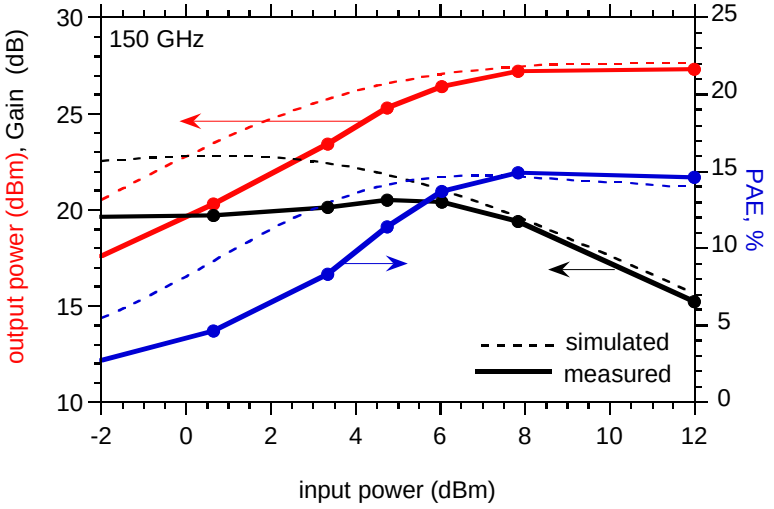


combination of corporate and cascade power-combining

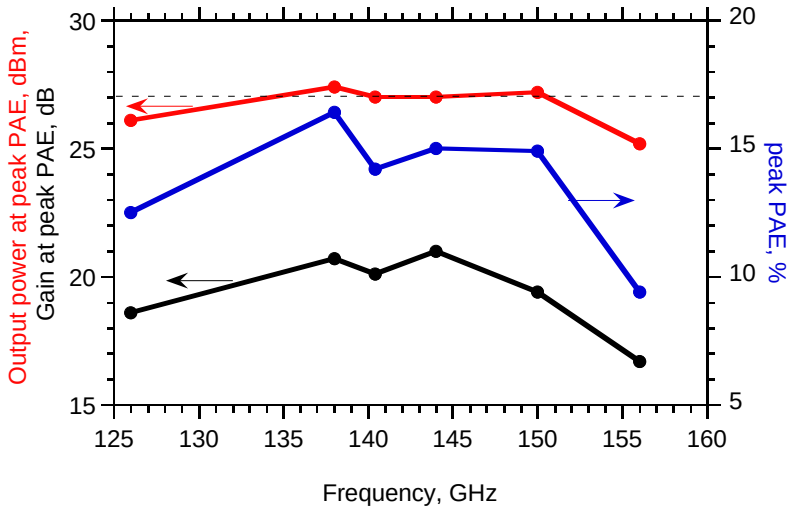
Alizadeh 2023 IEEE BCICTS



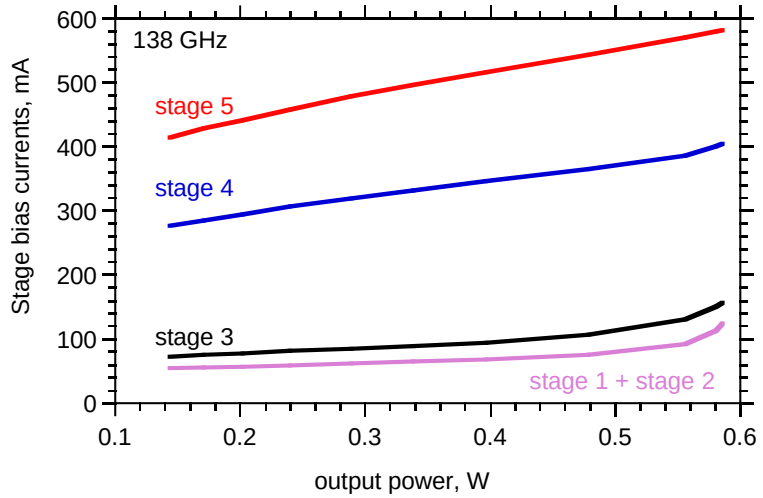
Output power, PAE, and Gain



Peak PAE with associated output power & gain vs. frequency



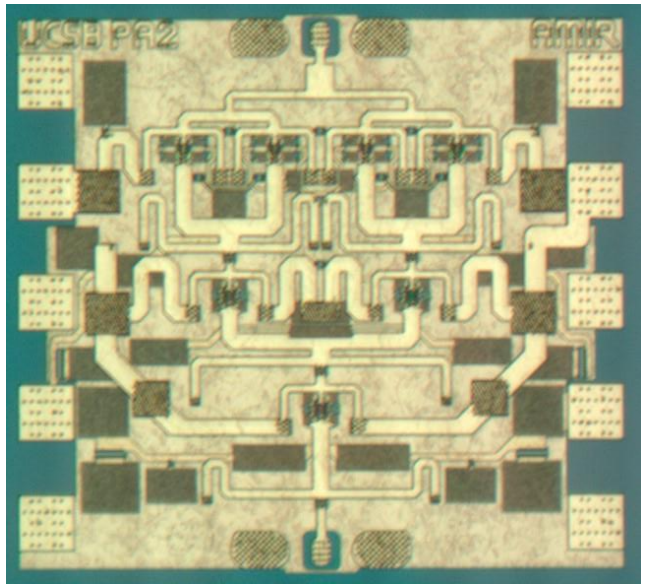
Adaptive class-AB bias currents vs. output power



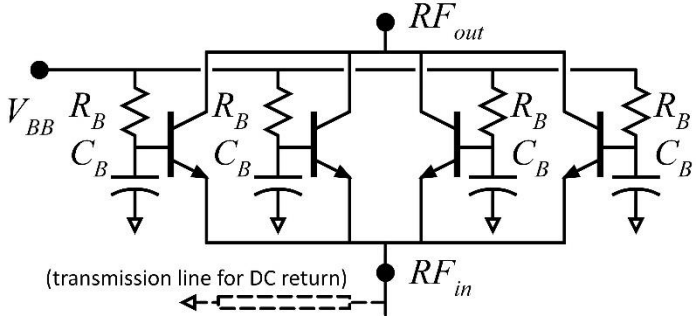
InP HBT Amplifier: 78 mW, 18.4% PAE, 220 GHz

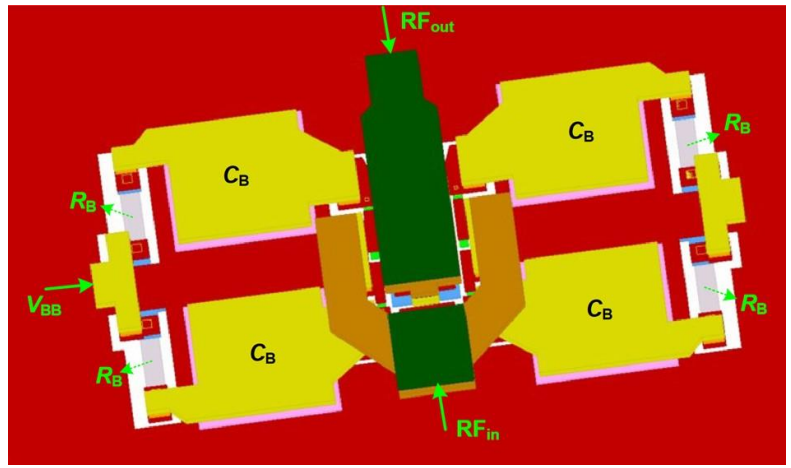
Alizadeh 2024 IEEE MTT Trans. ; to be published

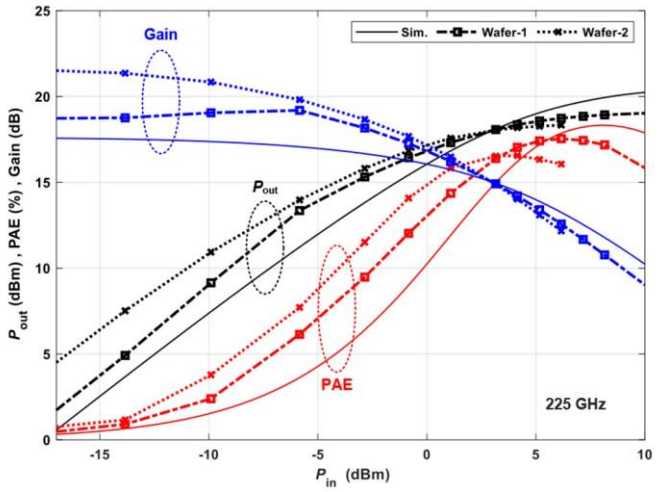
Teledyne 250 nm InP HBT (reduced base post)

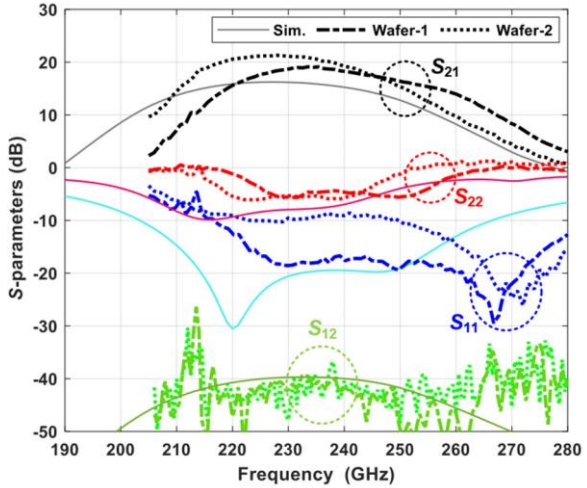


Thermally ballasted 4-finger common-base cell: increases maximum V_{ce}.

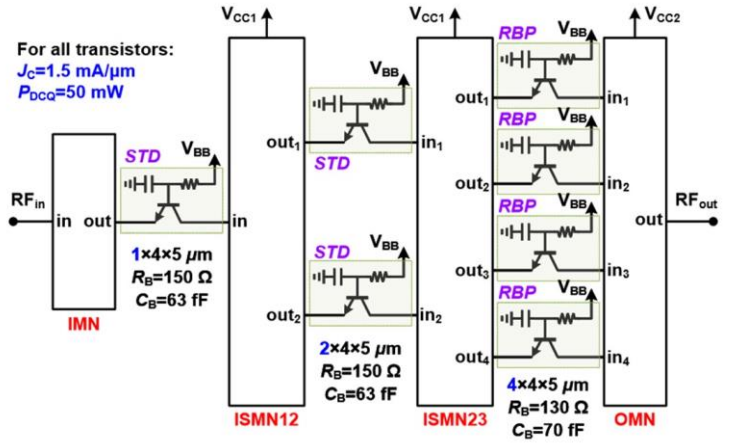








combination of corporate and cascade power-combining



InP HBT Amplifier: 16.8 dBm, 4.0% PAE, 266 GHz

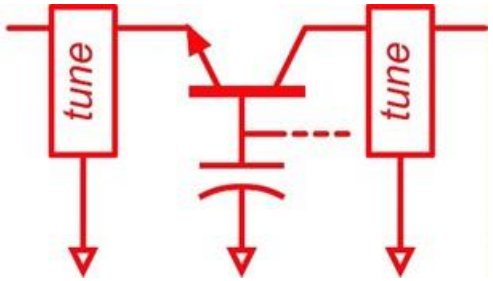
Ahmed et al, 2021 RFIC

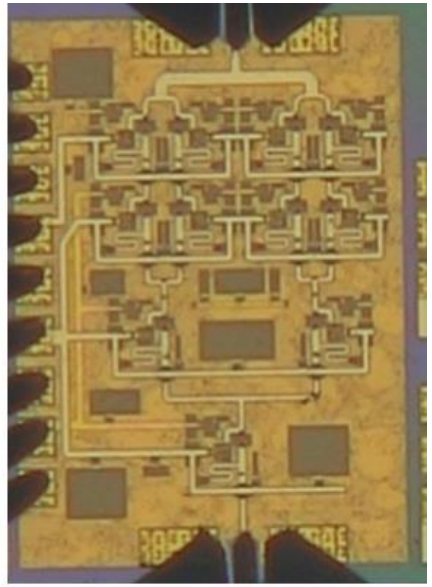
Teledyne 250 nm InP HBT

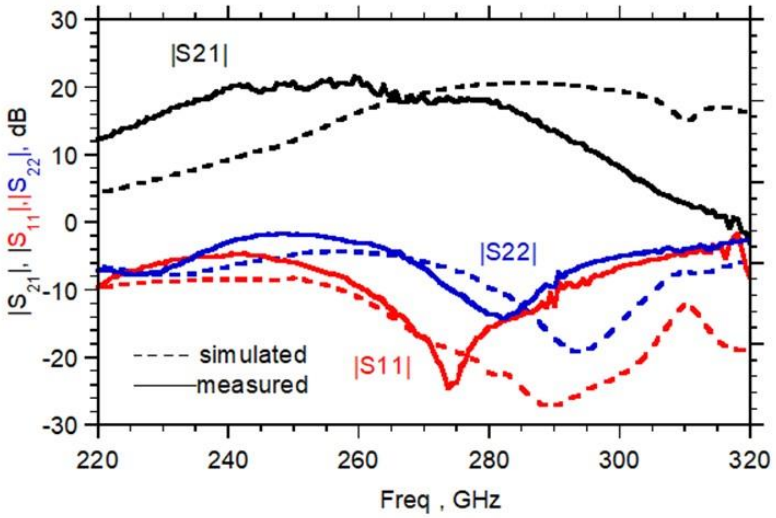
4-stage capacitively degenerated common-base

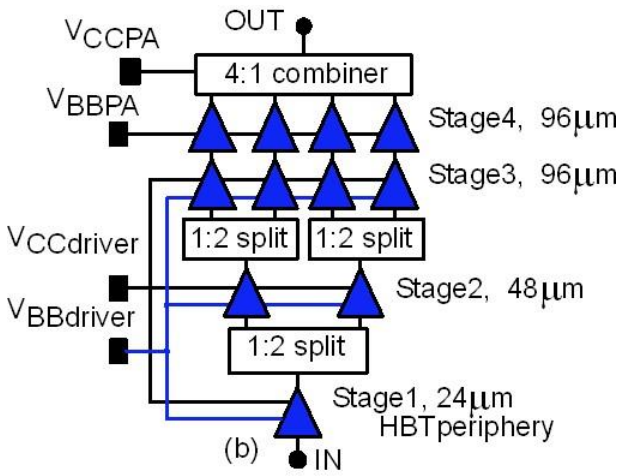
Cascade combining:
- ~40% of Pout from output stage
- ~40% from driver
- ~20% from pre-driver.

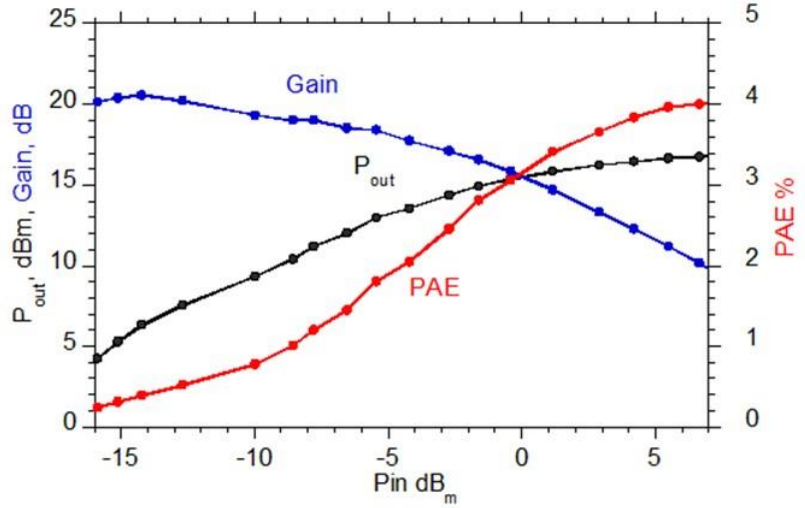
Improved PAE feasible with re-design, or using 130 nm node











Record PAE @ 220 GHz

IEEE MICROWAVE AND WIRELESS TECHNOLOGY LETTERS, VOL. 34, NO. 4, APRIL 2024 431

A 220-GHz Power Amplifier With 60-mW P_{out} and 23.5% PAE in 130-nm InP HBT

Zach Griffith, *Senior Member, IEEE*, Miguel Urteaga, *Fellow, IEEE*, and Petra Rowell

Key finding: RF breakdown > DC breakdown (thermal effects)

200 GHz Low-Noise Amplifier: 130 nm InP HBT

Unpublished data: do not distribute outside this workshop.

5-stage common-emitter design.

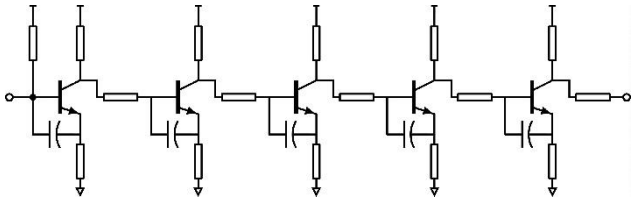
F = 6.3-5.5 dB over 180-217 GHz; record for bipolar transistor

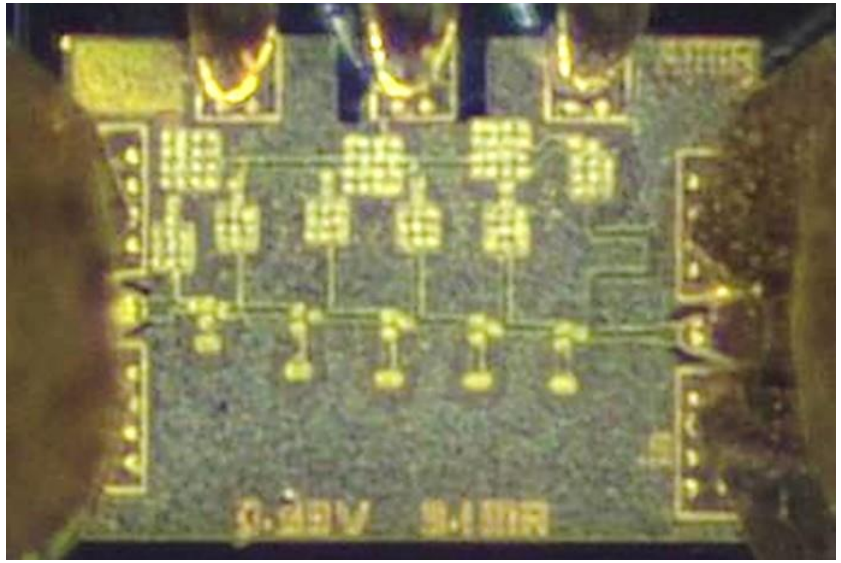
-22 dBm IP1dB at 210 GHz.

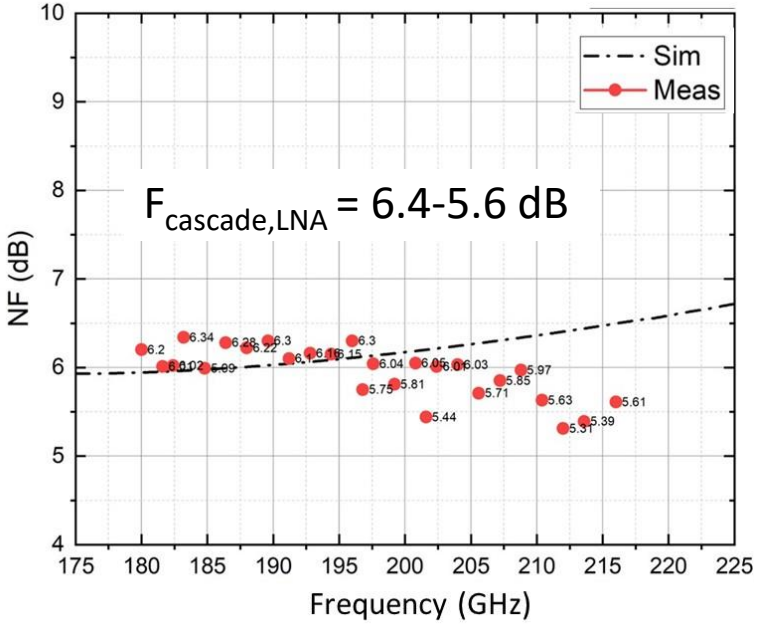
12-16 dB gain over 170-220 GHz

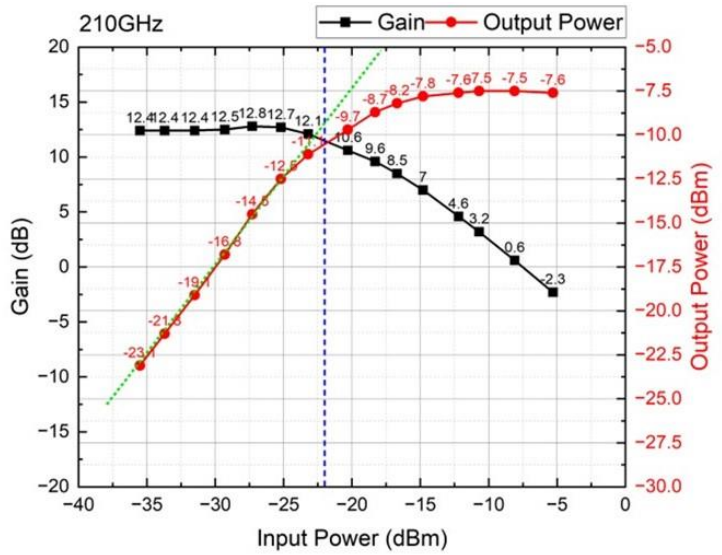
7 mW DC power dissipation.

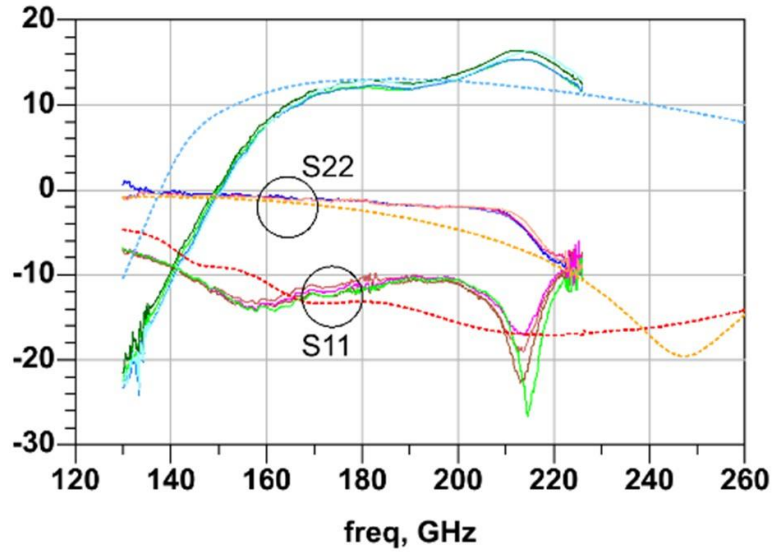
Alizadeh, Park, Urteaga, Rowell, Rodwell, to be submitted





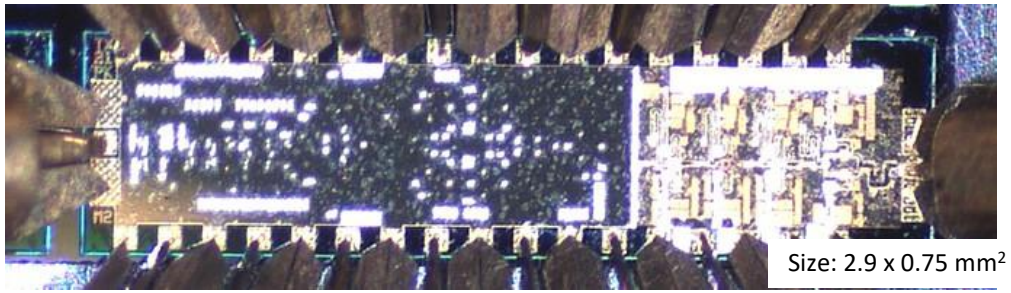


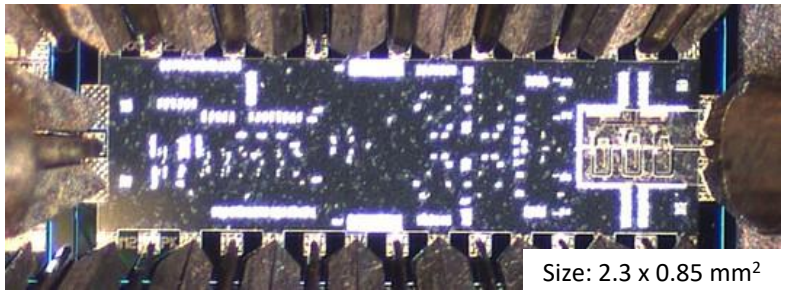


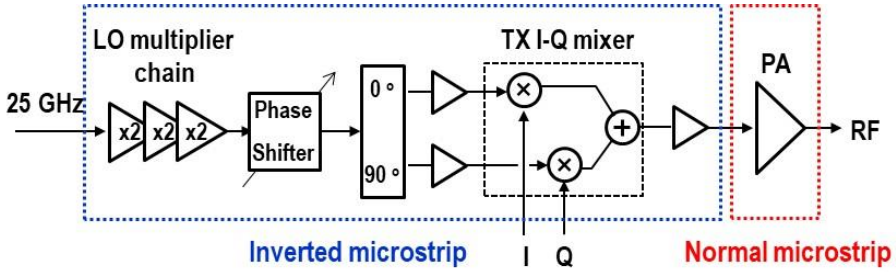


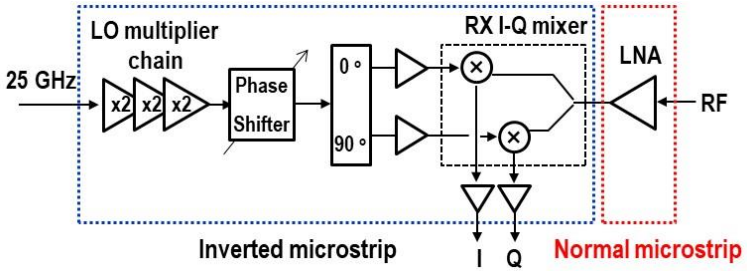
210 GHz Transmitter and Receiver ICs

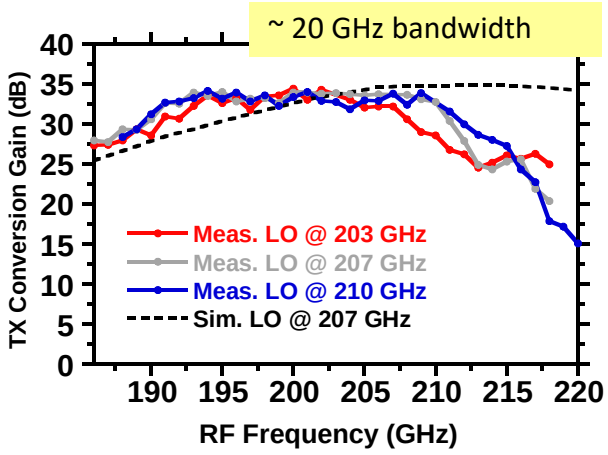
Teledyne 250nm InP HBT

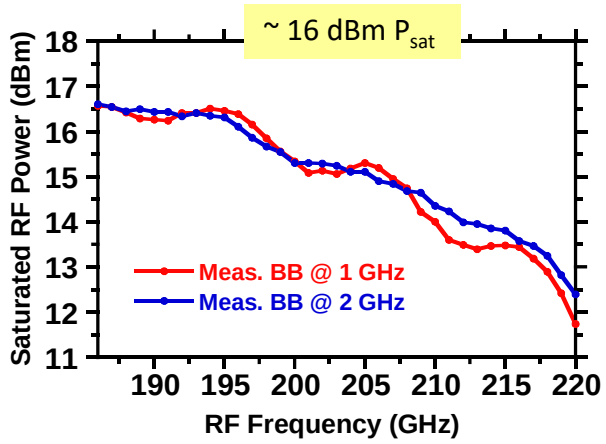


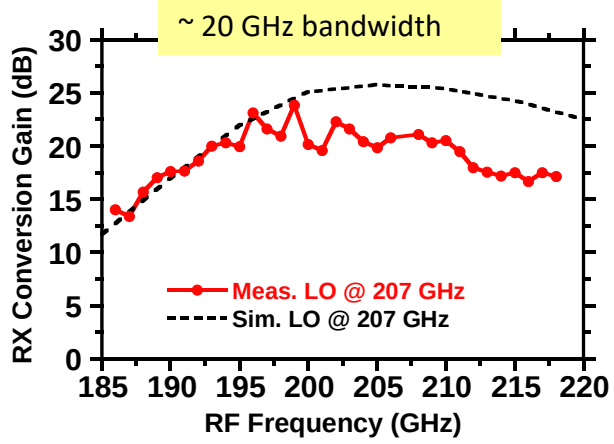


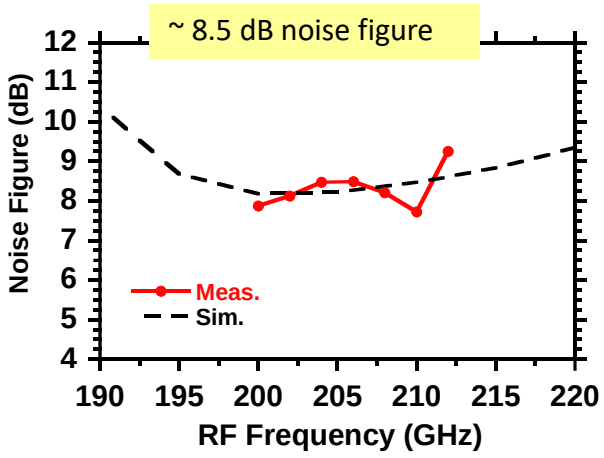








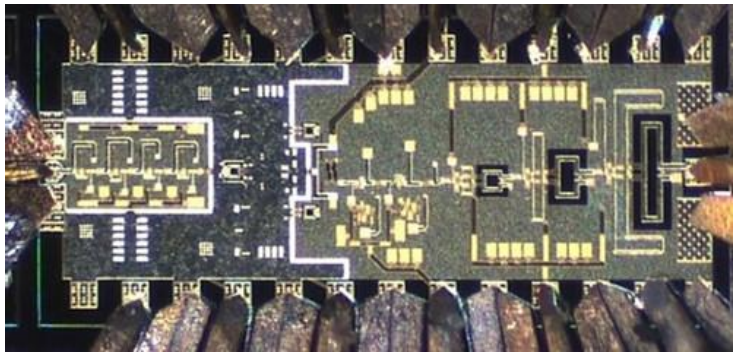


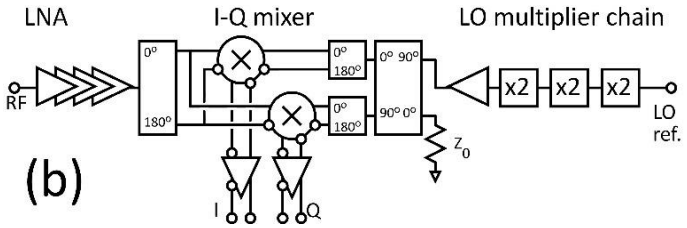


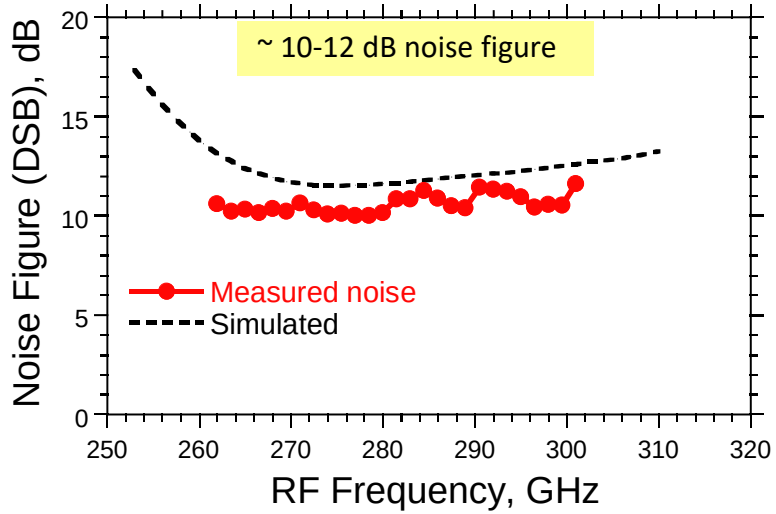
280 GHz Transmitter and Receiver ICs

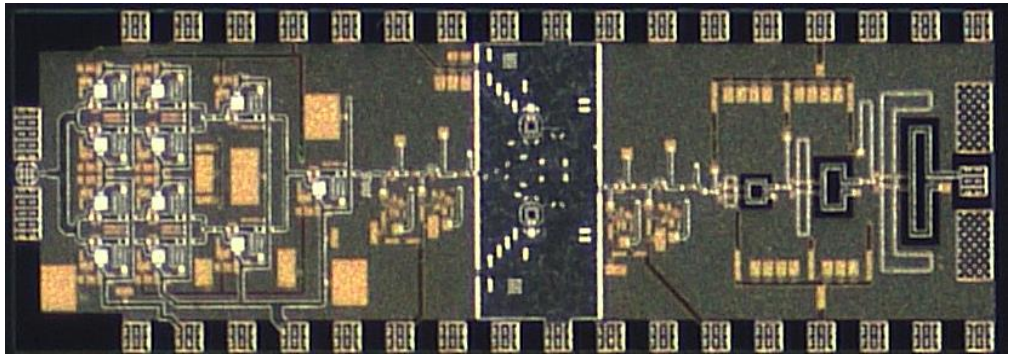
Soylu;
2023 RFIC,
2023 EuMIC

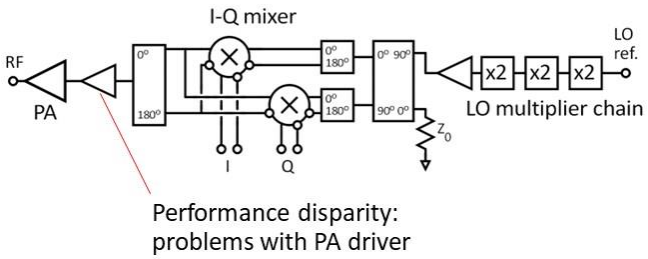
Teledyne 250nm InP HBT



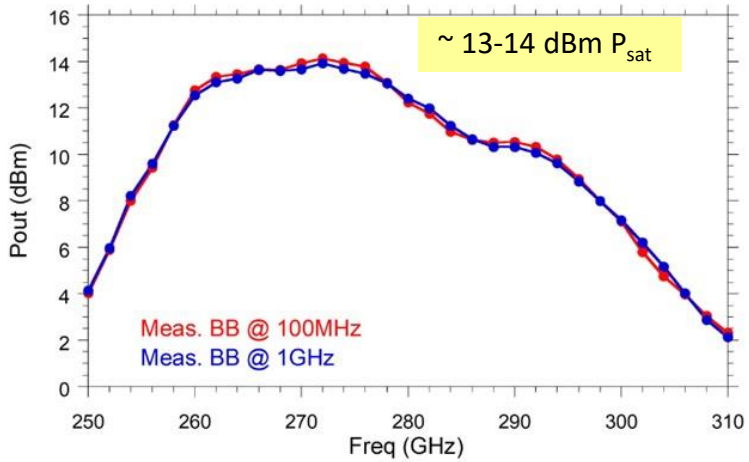




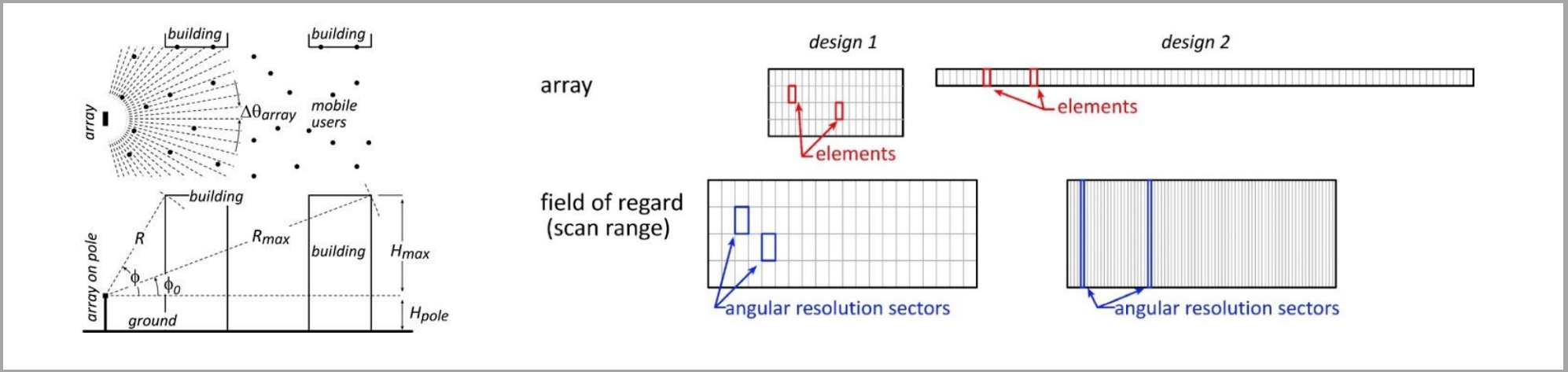




Performance disparity:
problems with PA driver

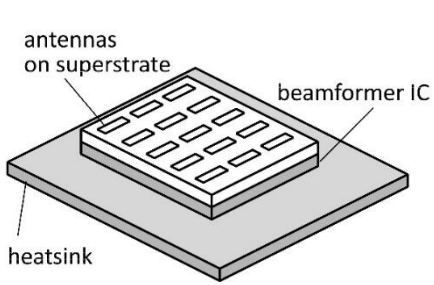


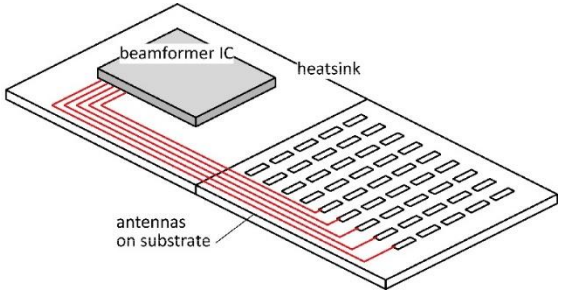
1D and 2D Array Design



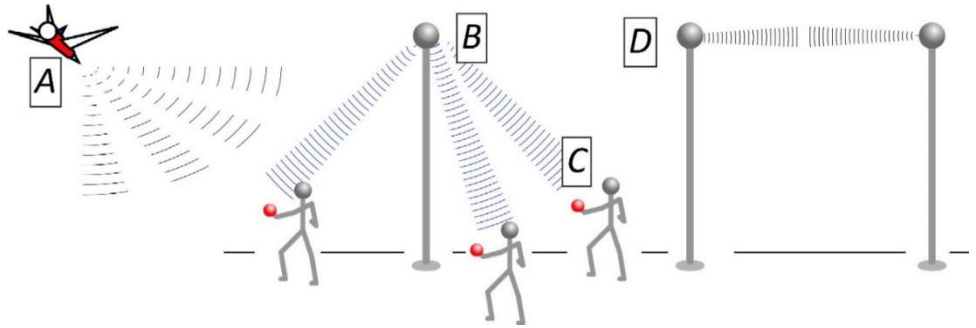
The mm-wave module design problem

How to make the IC electronics fit ?
How to avoid catastrophic signal losses ?
How to remove the heat ?

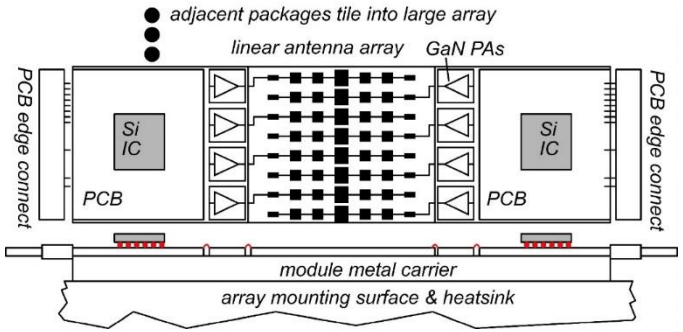


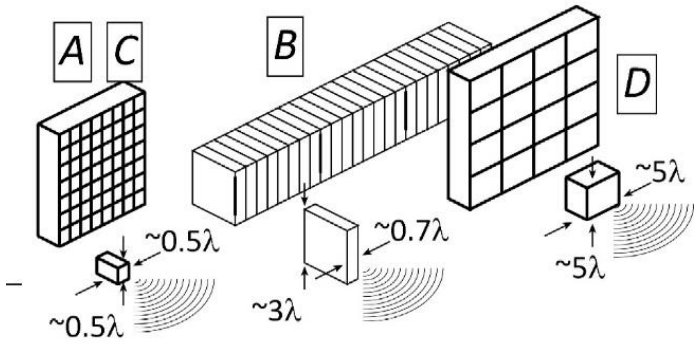


Not all systems steer in two planes...
...some steer in only one.



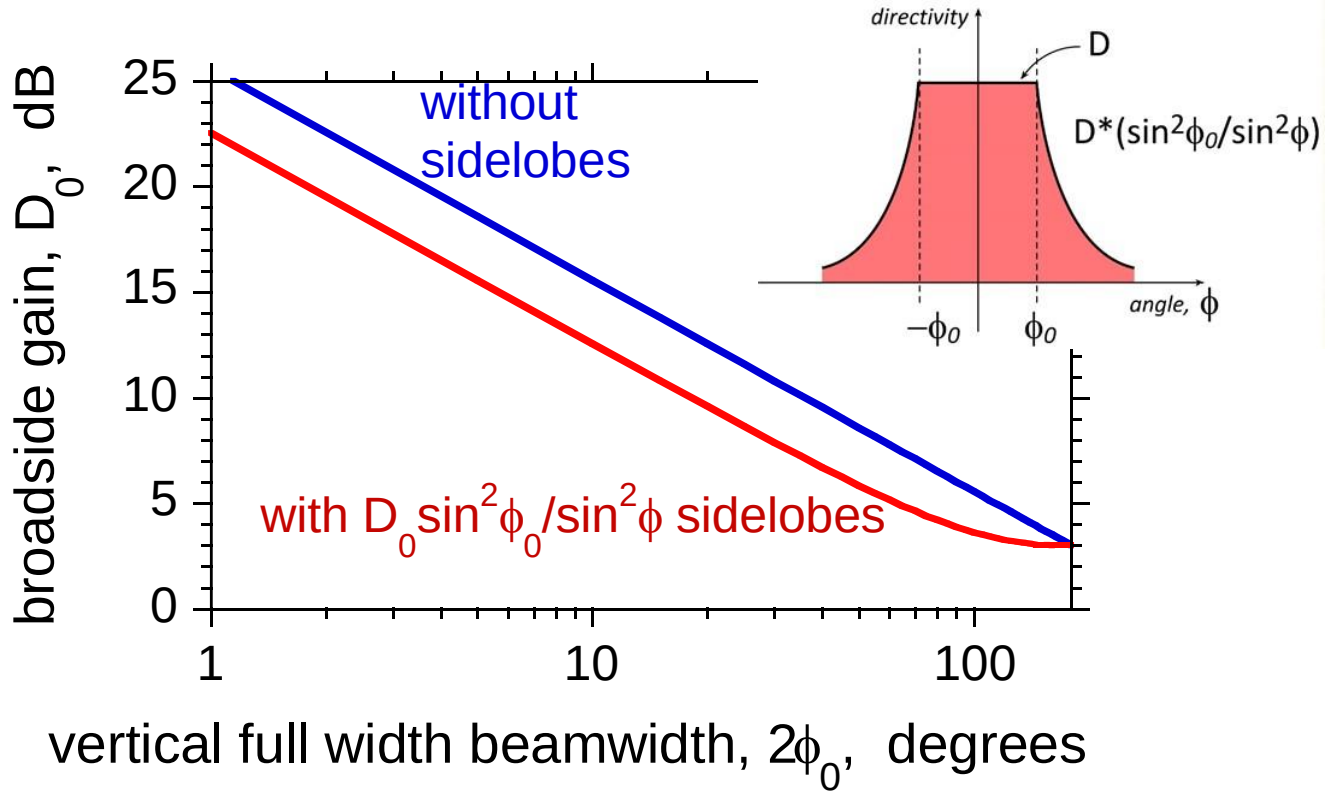
Not all systems steer over 180 degrees...
...some steer a smaller angular range

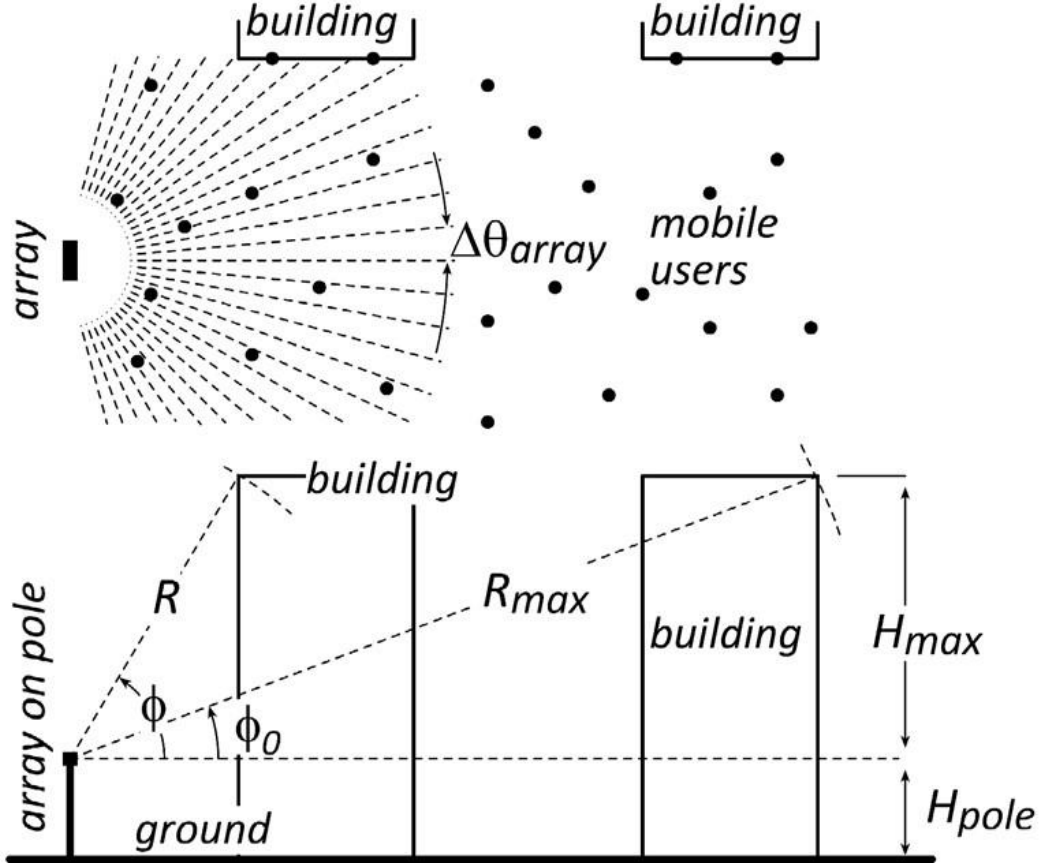




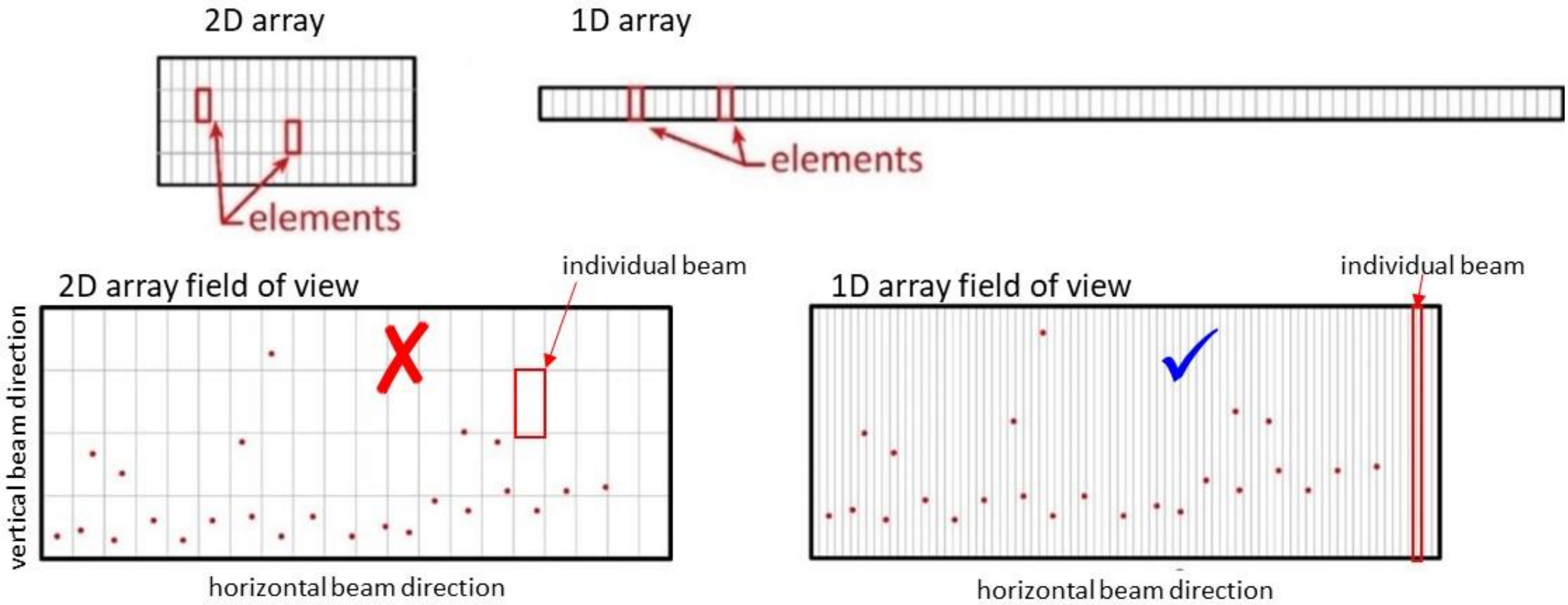
Do we need 2D arrays ? 1D steering might be fine.

1/sin²ϕ sidelobes provide strong signals to tall buildings.
Providing sidelobes reduces broadside gain by less than 3dB.
→ Don't need 2D arrays to serve tall buildings



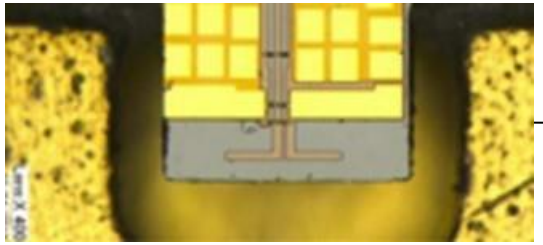


2D vs. 1D: Don't aim beams in useless directions

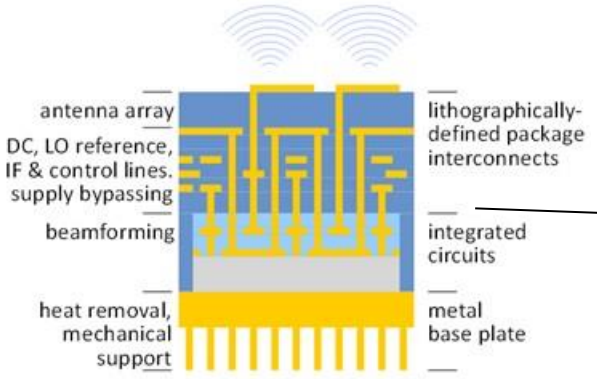


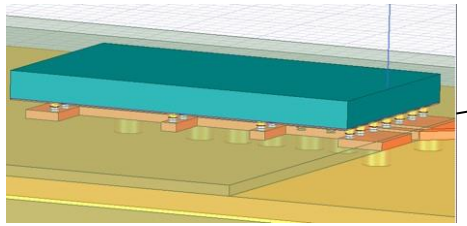
With most users on the ground, 2D array wastes spatial degrees of freedom on unoccupied directions.
Need some 2D beamsteering to avoid ground reflections.

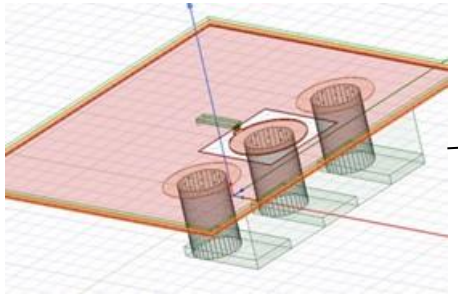
100-300 GHz IC-package connections

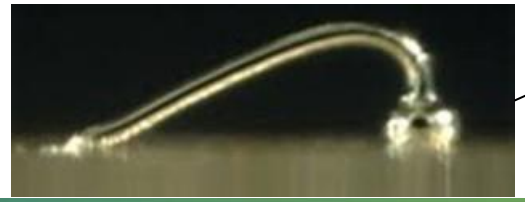


Deal, IEEE Trans THz, Sept 2011



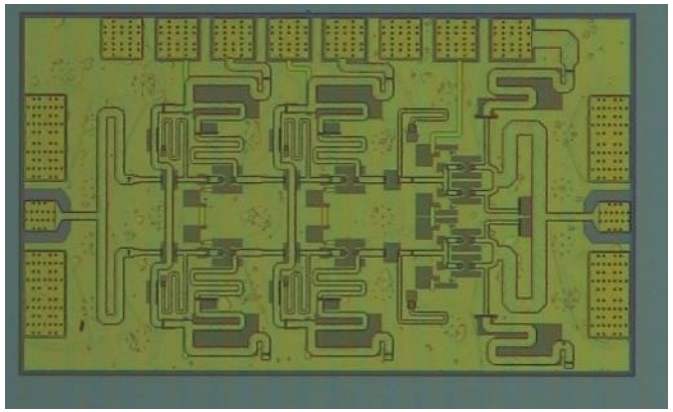


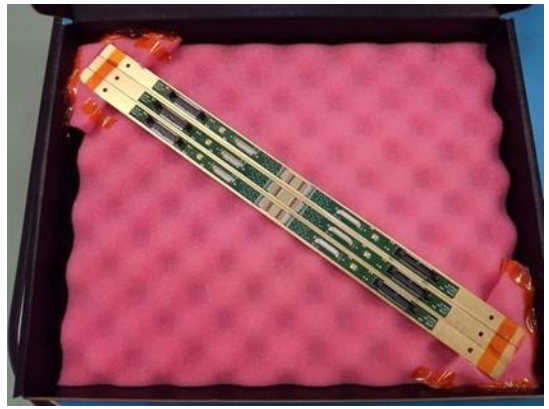


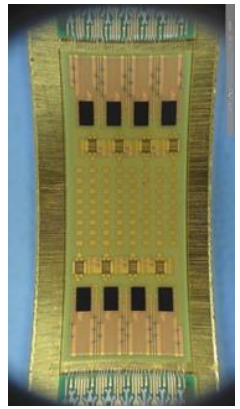


type	Frequency	technology	cost	heatsinking
micromachined waveguide interface	1000 GHz	Research. Cheap one day ?	high ✗	good
ribbon, mesh bond	200 GHz	Handcrafted.	high ✗	good
wafer-scale fan-out package	>200 GHz	Industry standard	low	good
Cu stud flip-chip	>200 GHz	Industry standard	low	ok, marginal for PA ✗
hot vias	200 GHz	Development	low ?	good
(ball) wirebonds	100 GHz ✗	Industry standard	low	good

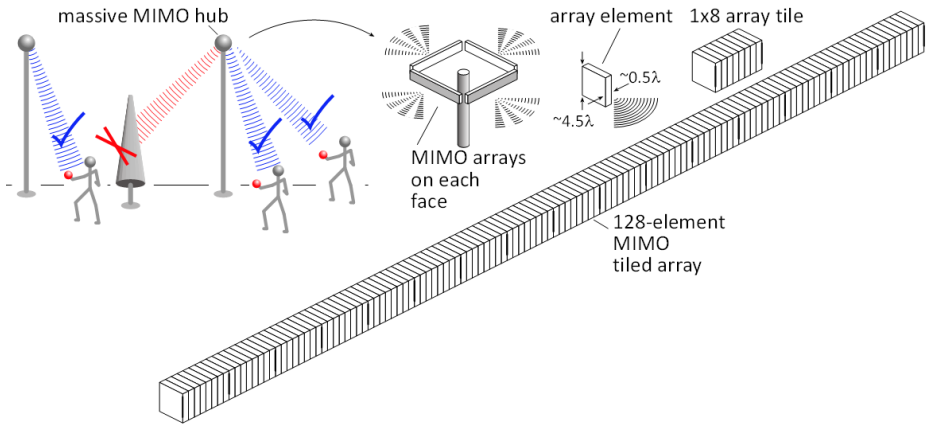
140 GHz





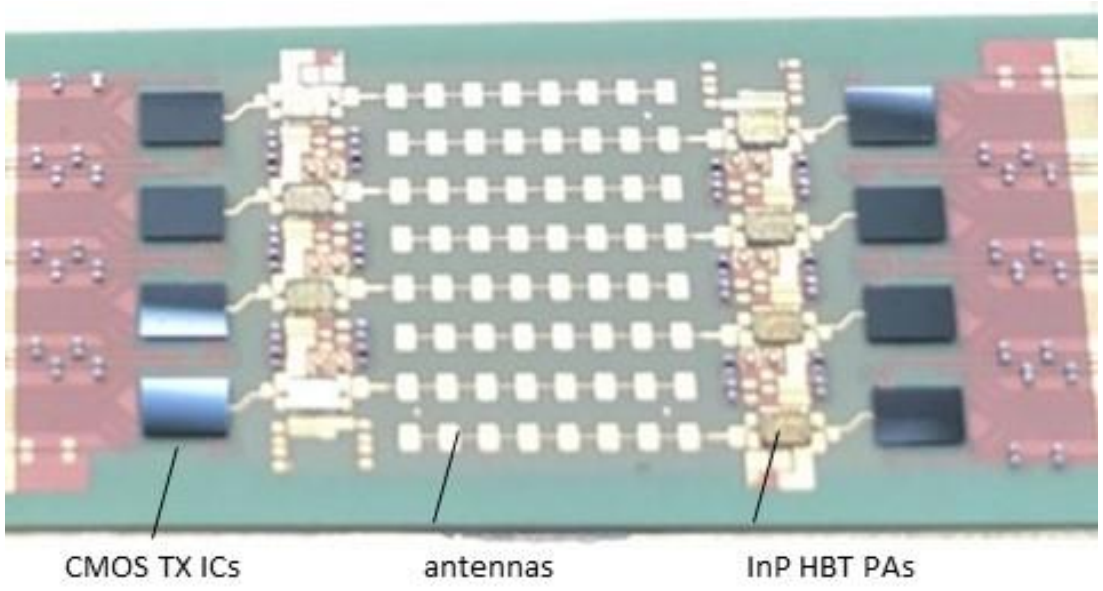


140 GHz Hub Demonstration

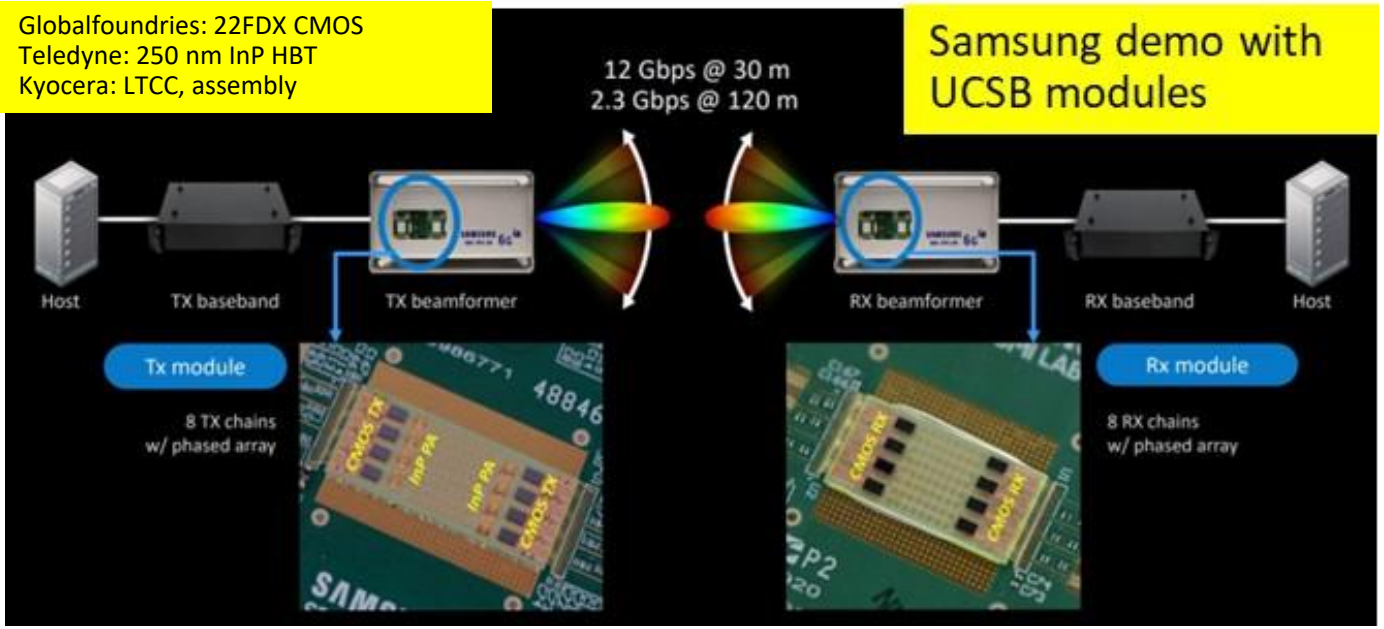


Concept: 128 elements, 64 x 10 Gb/s/user, 70 meters.

Demonstration (Samsung + UCSB)
8-element receiver*: 22 nm SOI CMOS
8-element transmitter*: 22 nm SOI CMOS + 100 mW InP HBT PAs
2.3 Gb/s @ 120 meters*
PTFE lens used to extend link range

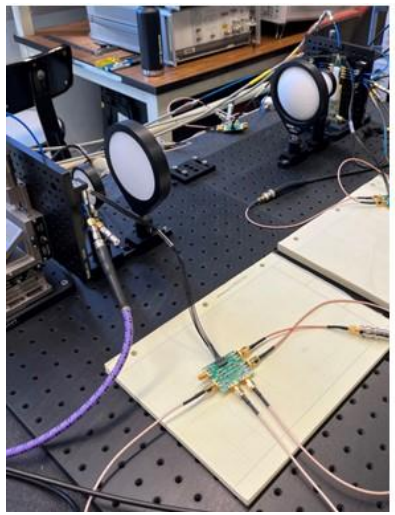


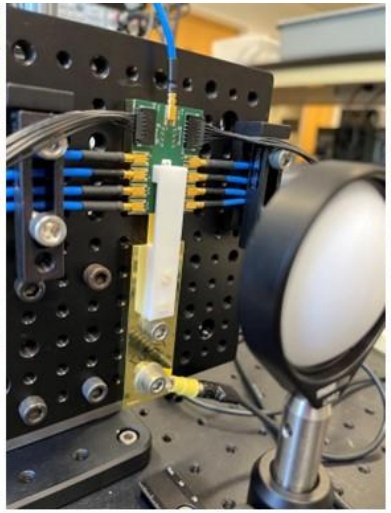
Globalfoundries: 22FDX CMOS
Teledyne: 250 nm InP HBT
Kyocera: LTCC, assembly

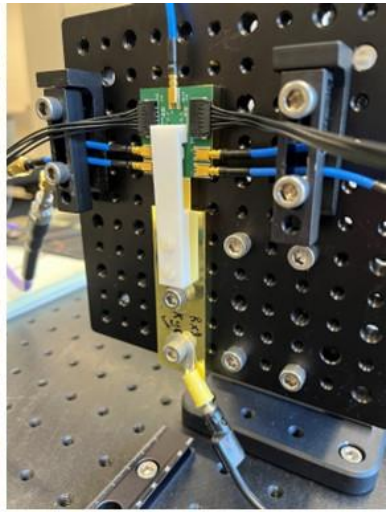


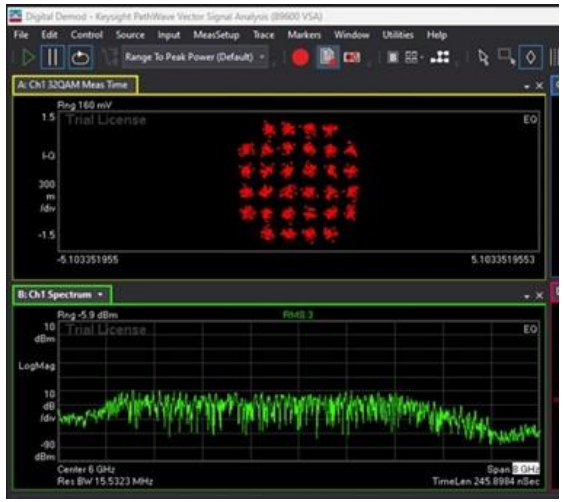
*Modules: Farid et al, IEEE BCICTS 2021, IEEE Trans MTT 2022,
Demo: Abu-Surra et. al. (Samsung) 2022 IEEE International Conference on Communications, 16 -20 May 2022, Seoul, Korea

210 GHz and 280 GHz ICs, Modules, Links





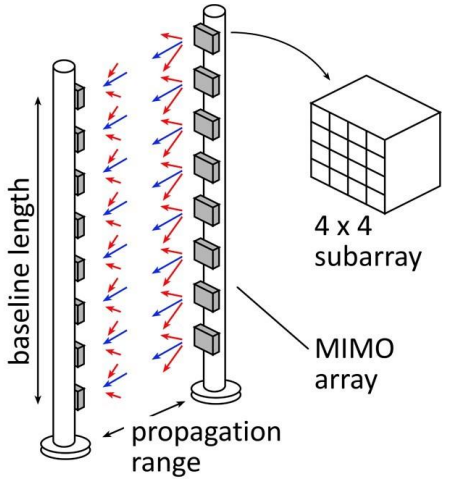


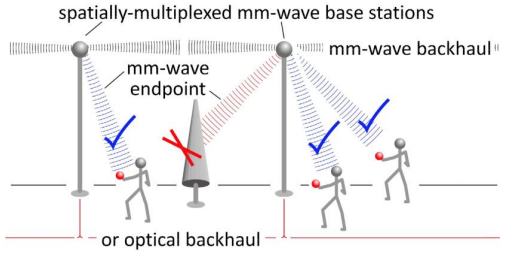


Concept: 640 Gb/s, 210 GHz MIMO backhaul

Concept

- 8 x 80 Gb/s MIMO with 2.1 m baseline
- 16-element subarrays (7λ x 7λ antennas)
- 500 meters range in 50 mm/hr. rain
- 14 dB margins: (obstruction, operating, aging, packaging)
- LNAs: 8 dB noise figure
- PAs: 50 mW =P_{1dB}



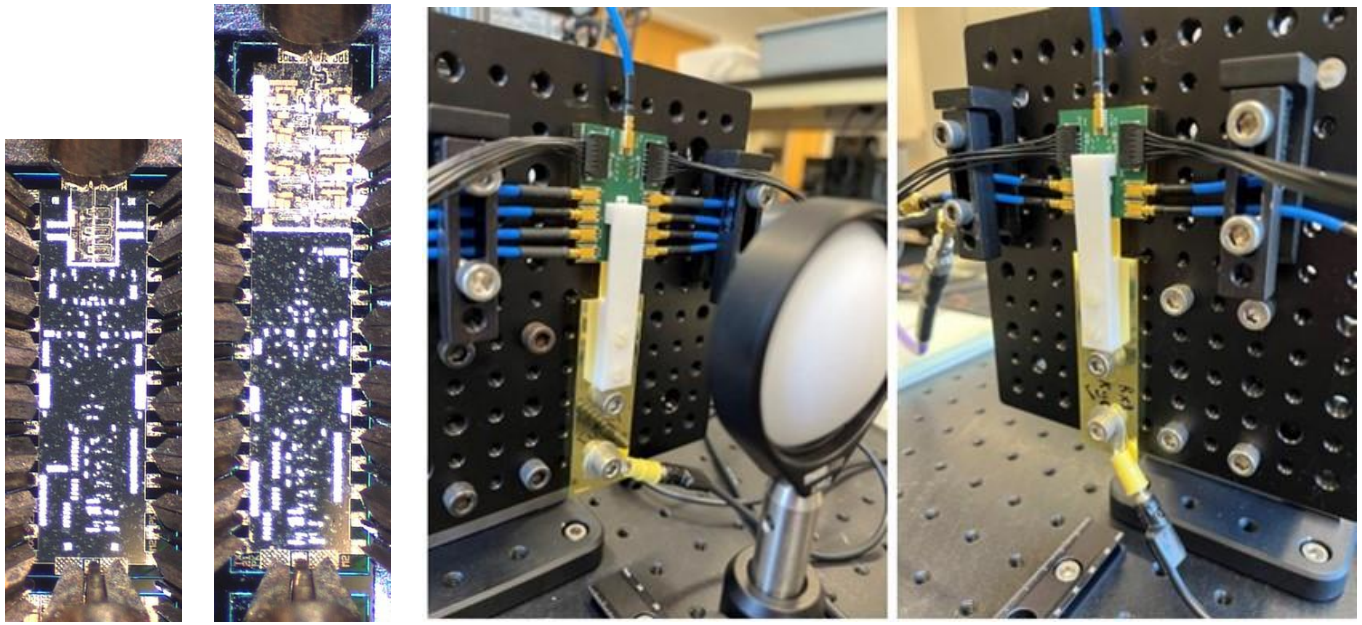


Demonstrated to date:

no subarrays, 1 channel

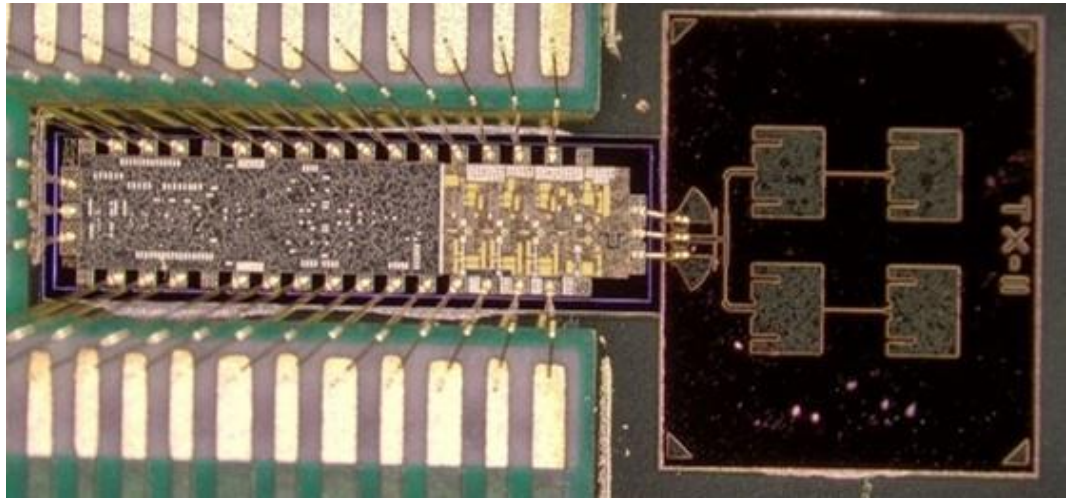
Ongoing demonstration efforts:

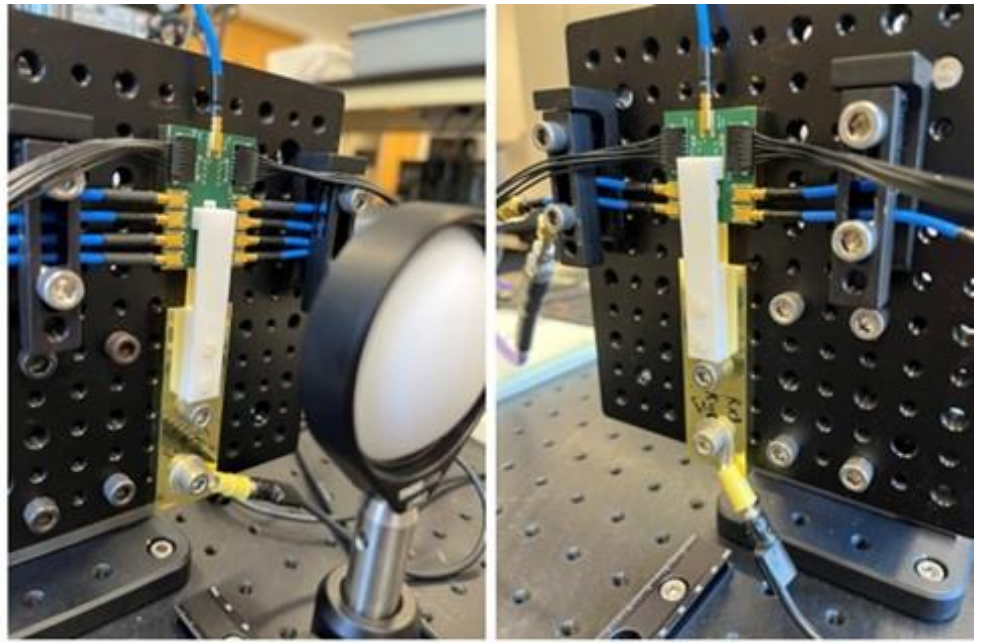
no subarrays, 4 x 4 MIMO

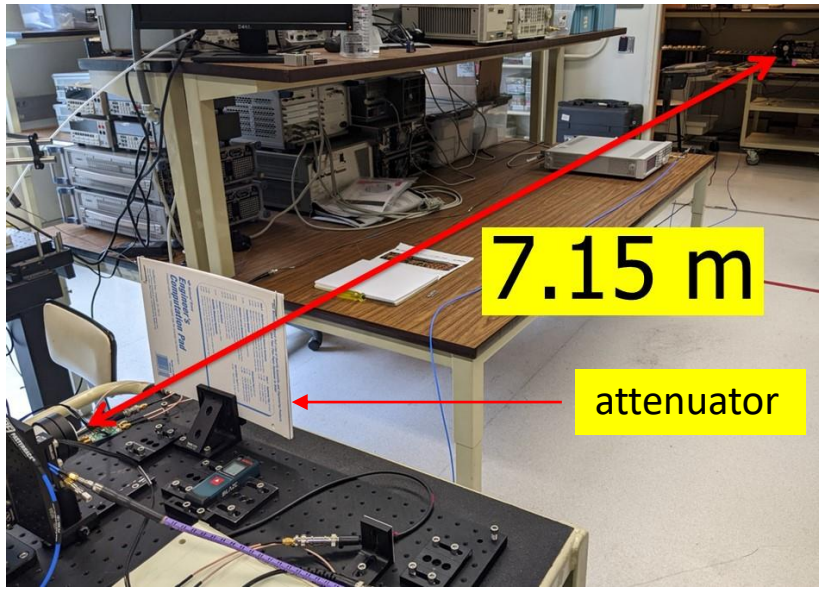


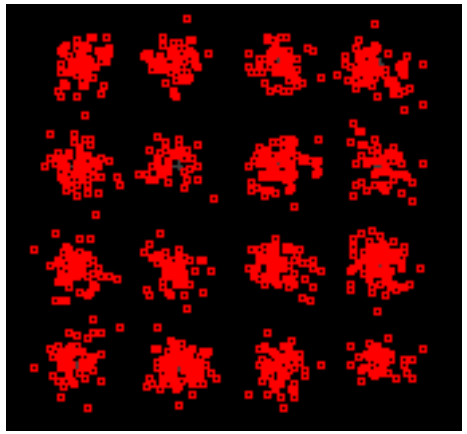
200 GHz link demonstration

Soylu, 2023 IEEE BCICTS (UCSB)
Teledyne 250 nm InP HBT
Kyocera module assembly









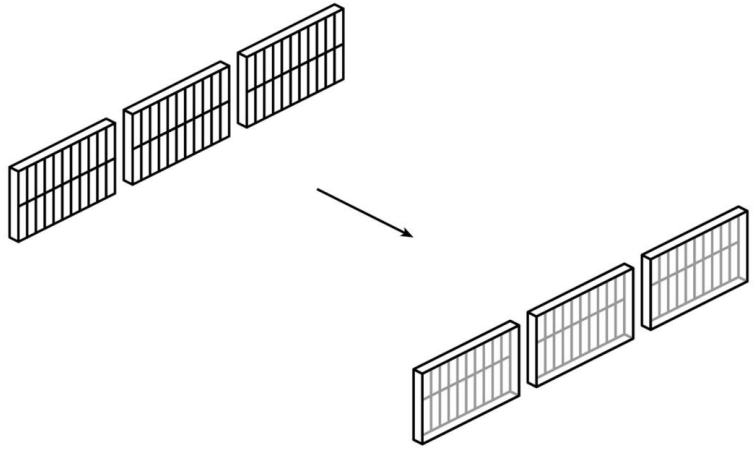
8 Gbaud

32 Gb/s

13.4% error vector magnitude
→ BER < 10^{-3}

Now working towards
4 x 4 MIMO demo.

What's next:
100-300 GHz



$$\frac{P_{RX}}{P_{TX}} = \frac{N_{TX} N_{RX}}{\Omega_{scan,TX} \Omega_{scan,RX}} \left(\frac{\lambda^2}{R^2} \right) e^{-\alpha R}$$

What's Next ? Large Arrays, Dense Arrays

λ/2-pitch 2D arrays at 200-300 GHz

Not all systems need 2D arrays, but many do.

very small spacing: hard to fit in the circuits

Highest-frequency ~ λ/2-pitch 2D arrays: 140 GHz CMOS (Rebeiz group, UCSD)

Target: large-scale λ/2-pitch 220 GHz 2D arrays in InP HBT

Massive inexpensive arrays at 70-140 GHz

Motivation: difficulties even with 5G @ 39 GHz

Goal: greatly increase $P_{received}/P_{transmit.}$

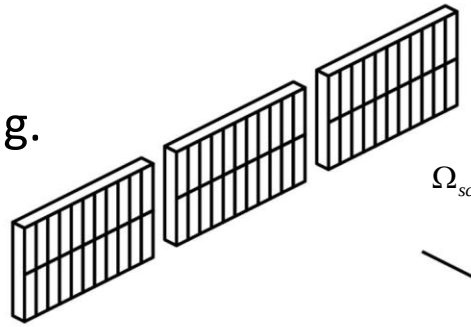
longer range, greater margins against blocking and fading.

Approach: greatly increase # transmit, receive elements.

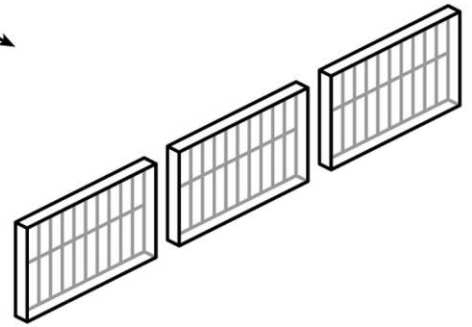
low cost: need very low die area per element

low DC power: need very low DC power per element

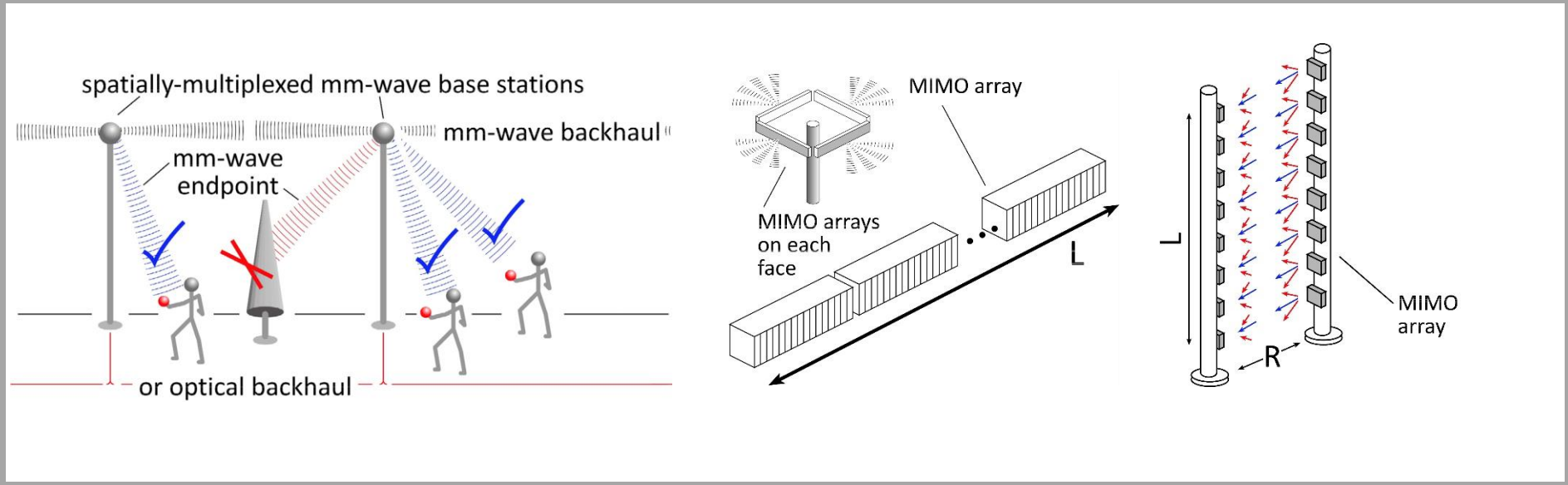
$$\frac{P_{RX}}{P_{TX}} = \frac{N_{TX} N_{RX}}{\Omega_{scan,TX} \Omega_{scan,RX}} \left(\frac{\lambda^2}{R^2} \right) e^{-\alpha R}$$



Ω_{scan} : angular scan field of view; solid angle in steradians



ICs and Transceivers for 100–300 GHz Wireless



100-300 GHz Wireless

Massive (near Tb/s) aggregate capacities: large spectral bandwidths, massive spatial multiplexing .

Limited range: ~100-500 m; atmospheric loss, λ^2/R^2 loss.

Easily-blocked beams: need redundant paths.

IC technologies: CMOS, InP, SiGe (GaN)

Near-term commercial impact:
range is too short, cost is too high
capacity (Gb/s/km^2) is much more than needed

Research (long-term):
demonstrate 100+ Gb/s capacity, reduce cost, reduce power, increase range and operating margins.
(λ/2) pitch arrays at 200+ GHz
massive low-cost arrays