2025 IMS Workshop WSL "Sub-THz Power Amplifiers in CMOS, SiGe, and III-V"

100-300 GHz power amplifiers: transistor limits, circuit topologies

Mark Rodwell
Doluca Family Chair
University of California, Santa Barbara

rodwell@ece.ucsb.edu

Co-authors: **Amirreza Alizadeh** (Keysight/UCSB), **Ahmed Samir Sayed Ahmed** (Cairo University/ Analog Devices / UCSB), **Yuya Nemoto** (UCSB), **Utku Soylu** (UCSB/IBM), **Miguel Urteaga** (Teledyne)

Co-Authors

Dr. Miguel Urteaga
Teledyne Scientific
130 nm & 250 nm
InP HBT technology

Dr. Amirreza Alizadeh
Now with Keysight
140 GHz 0.5 W amplifiers
220 GHz high-efficiency PAs
220 GHz LNAs

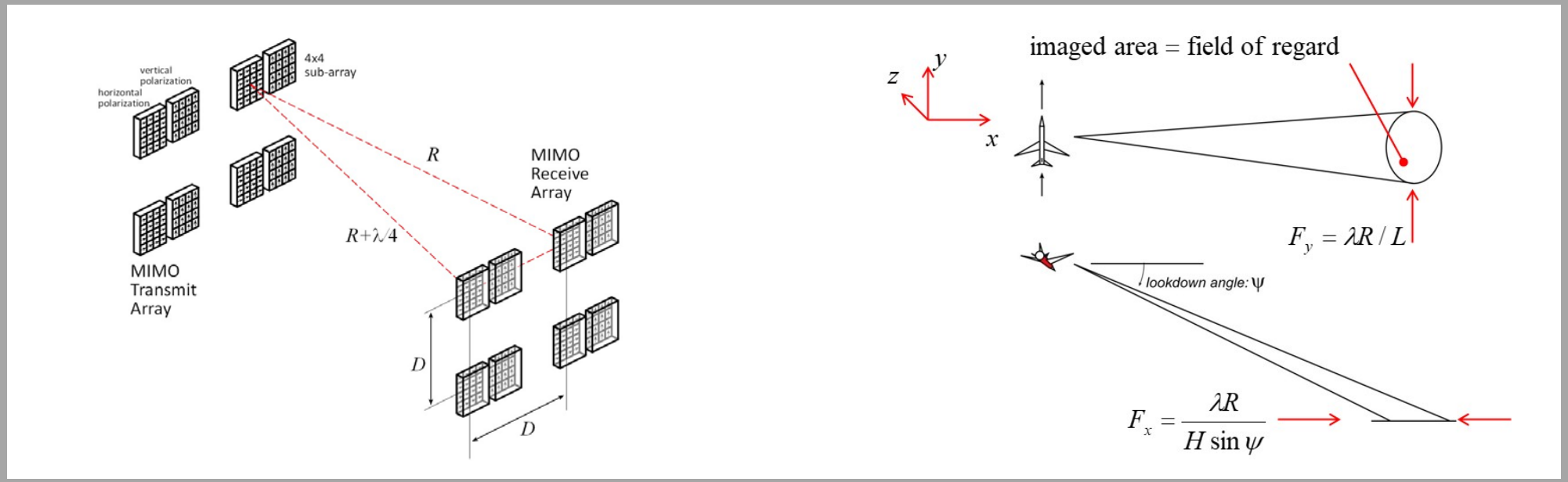
Prof. Ahmed S. S. Ahmed
Now with Cairo Univ. & ADI
140, 200, 270 GHz
power amplifiers
cascade power-combining
capacitively degenerated CB

Dr. Utku Soylu
Now with IBM Yorktown
LNA design principles
220 GHz LNAs

Yuya Nemoto
UCSB

Also acknowledging:
Dr. Zachary Griffith
Teledyne Scientific
100-300 GHz InP PAs
250 nm InP HBT technology

applications

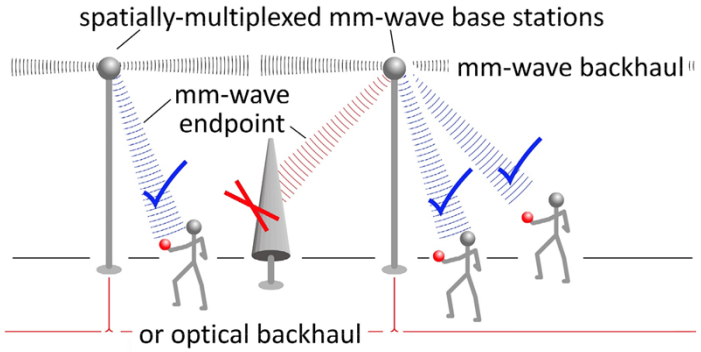


100-300 GHz Wireless

High capacity:

potentially wide available bandwidth

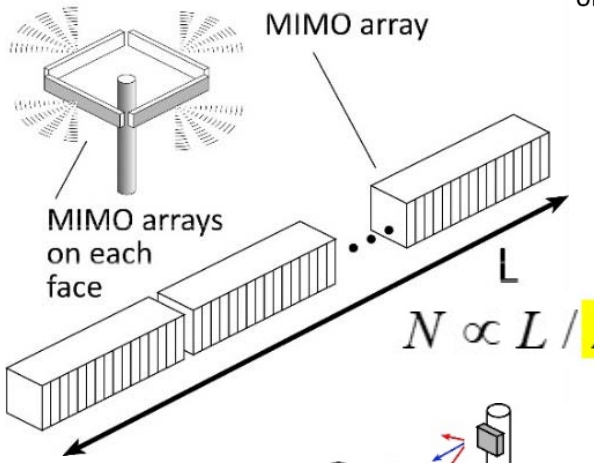
many simultaneous signal beams even with compact arrays

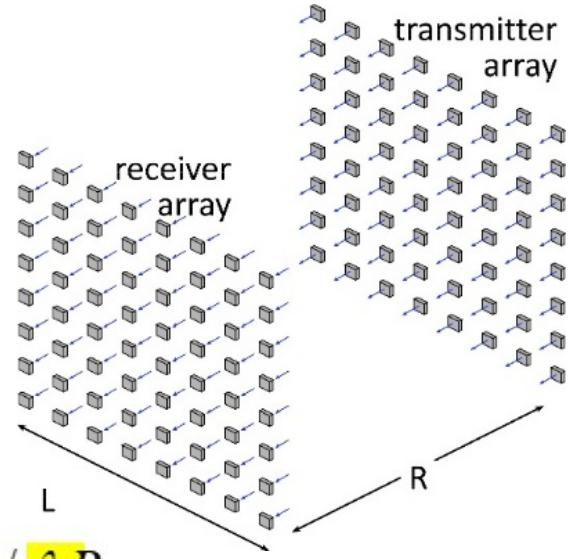


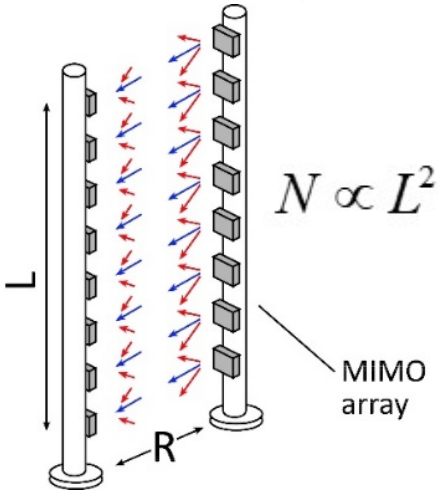
Limited range: (max 500-1000 m)

high λ^2/R^2 Friis (beam diffraction) losses

high worst-case atmospheric attenuation







Need:

arrays with *very* many elements

low receiver noise figure

efficient medium-power amplifiers

Terminology:

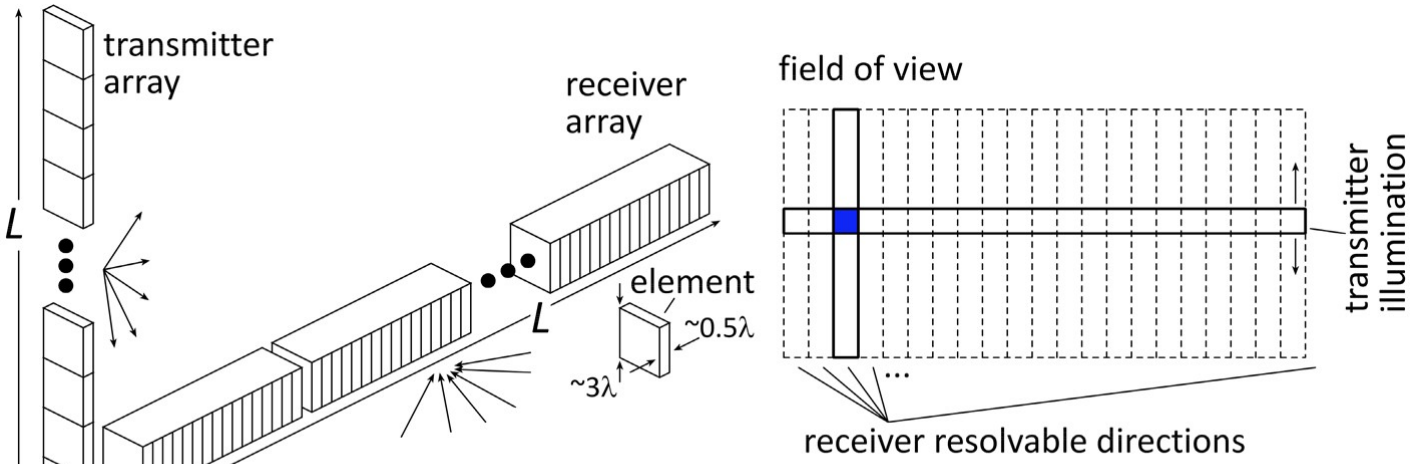
30-300 GHz → λ = 10 to 1 mm→ "millimeter-waves"

220 GHz FMCW crossed-array imaging radar

36 × 1 transmit array, 6" long
1 × 216 receive array, 6" long
36 × 216 image; 10° ×90° field of view
0.3° beamwidth

Sees soccer ball
@ 200 meters range,
in heavy fog.

P_{1dB} = 17 dBm PAs
F = 6 dB LNAs



17 dBm PAs, F=6 dB LNAs , 2 dB TX packaging losses, 2 dB RX packaging losses, 4 dB operating margins, 40 Hz scan, 10 dB SNR, -10 dB target reflectivity, 22 dB/km fog. soccer ball is 22 cm diameter

Video Rate Synthetic Aperture Radar

Video-rate, video-resolution SAR

like infrared: high-resolution, real-time images

better: sees even through fogs/cloud

2012 DARPA VISAR program:

220 GHz, 1km range system

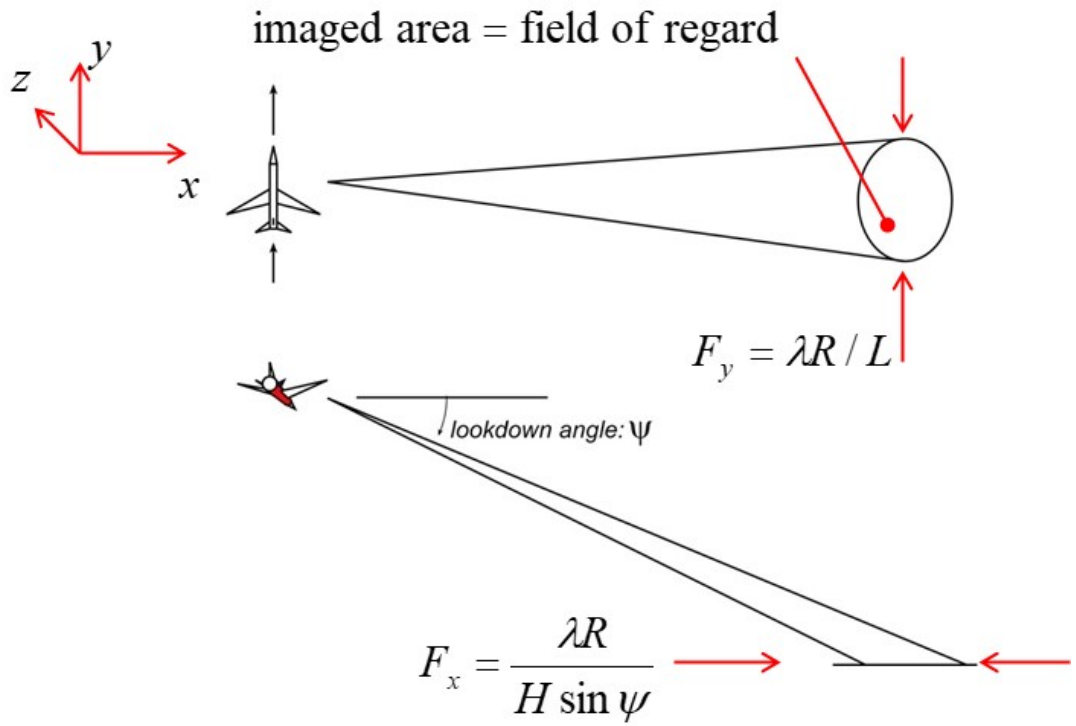
transmitter: 50 W vacuum tube.

Feasible now: InP HBT solid-state-source

2 tiles x (16 x 16 elements) x 100 mW/element

P_{1dB} = 20 dBm PAs

F = 7 dB LNAs



1.6 Tb/s wireless data center links ?

75-165, 195-305 GHz → 200 GHz bandwidth

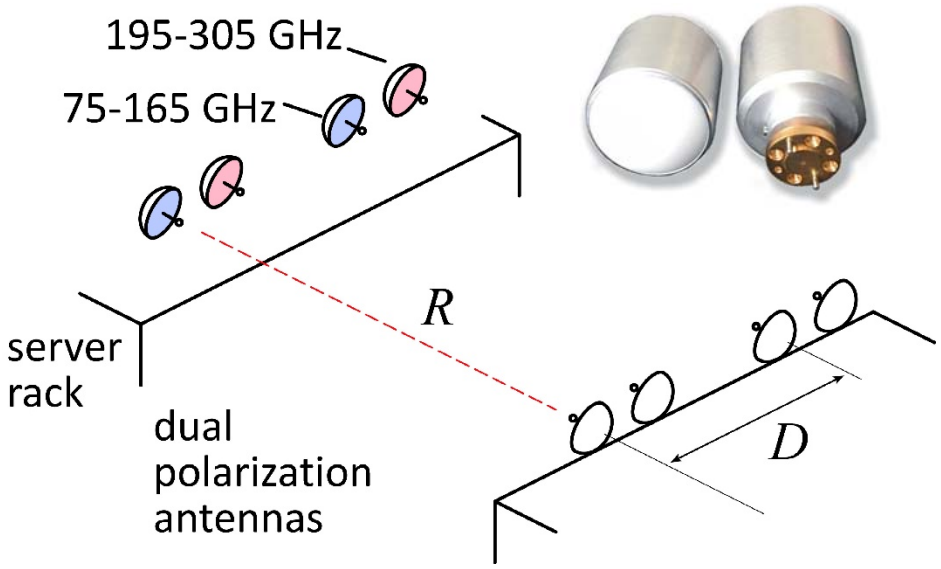
16QAM→ 4 bits/Hz→ 800 Gb/s

2 polarizations→ 1.6 Tb/s

100 m range

pJ/bit = ?

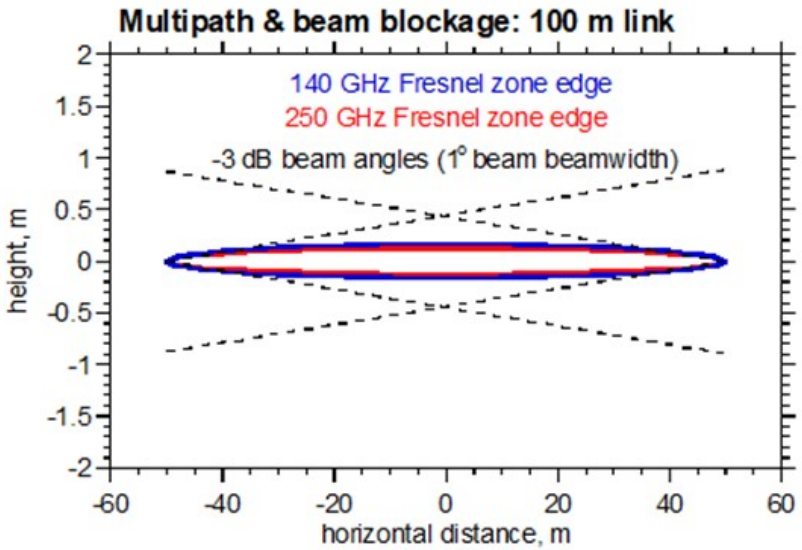
blockage ? crosstalk ?

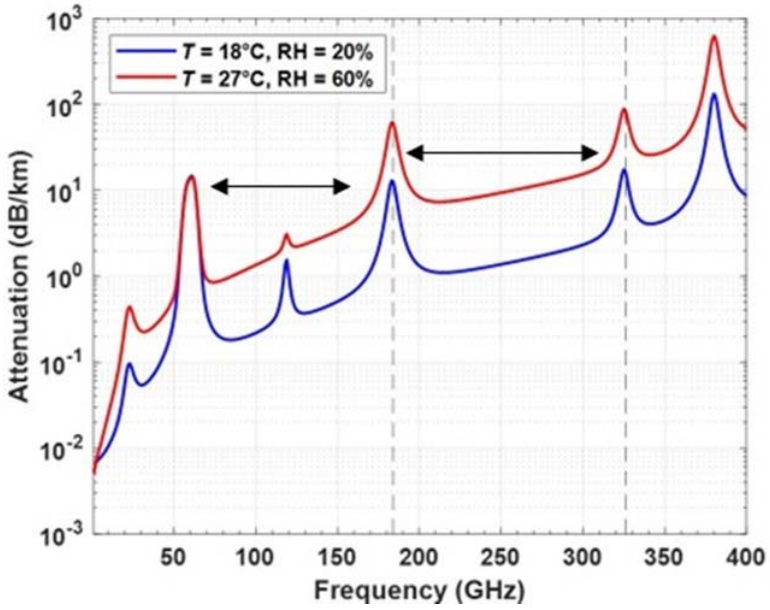


P_{1dB} = 12 dBm PAs

F = 7 dB LNAs

~10 dBm PAs, F=7 dB LNAs , 2 dB TX packaging losses, 2 dB RX packaging losses, 10 dB operating margins, 1^0 beamwidhs, 10^{-3} uncoded BER.
mechanical alignment
P1dB =12 dBm if 5 dB backoff from Ppeak





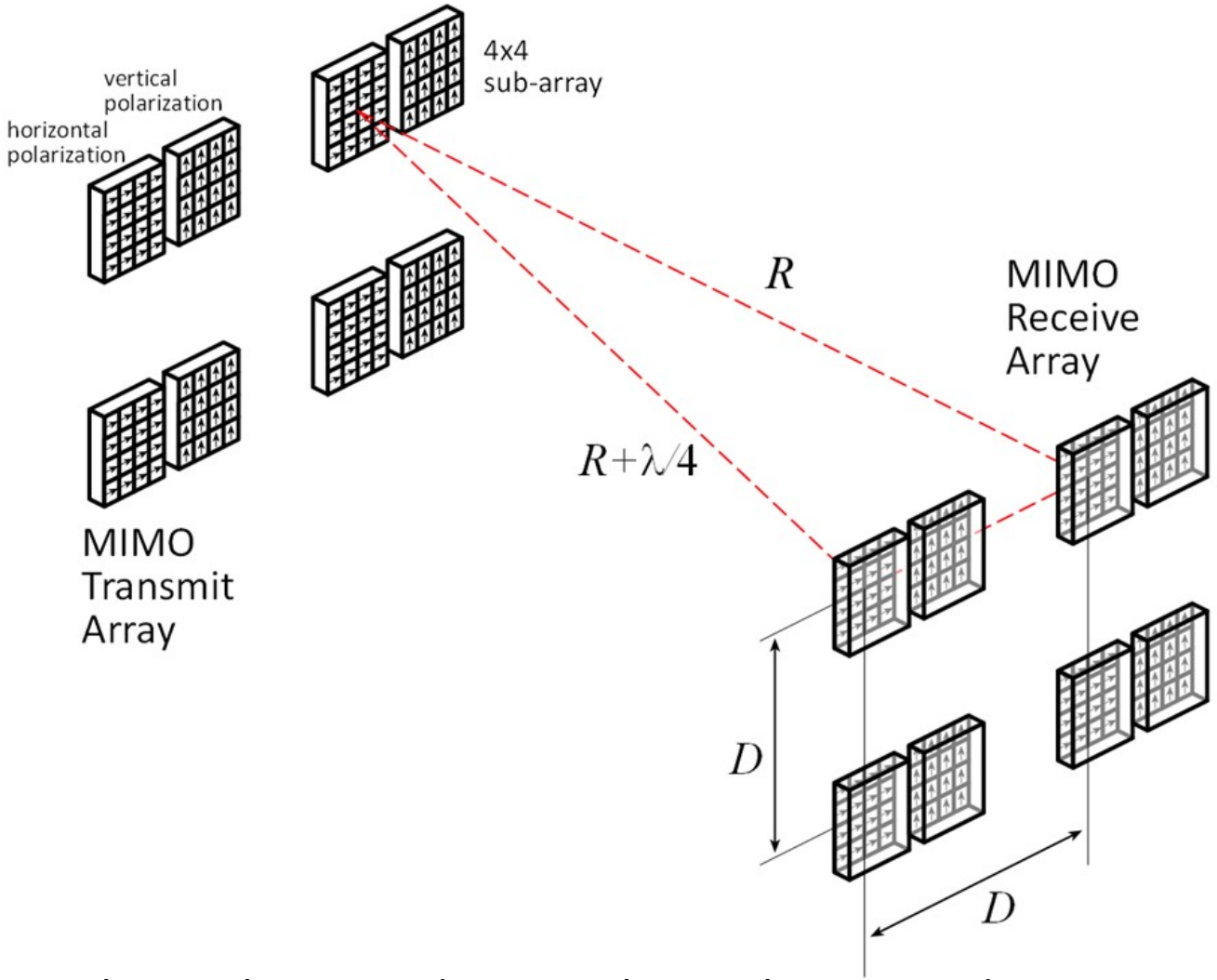
250 GHz, 1.0 Tb/s, 1.5 km MIMO Backhaul

8-element MIMO array

~ 1m baseline

125 Gb/s/subarray; 1.0 Tb/s total

1.5 km range in 50 mm/hour rain



P_{1dB} = 25 dBm PAs

F = 6 dB LNAs

25 dBm P1dB PAs (5 dB backoff), F=6 dB LNAs , 2 dB TX packaging losses, 2 dB RX packaging losses, 10 dB operating margins, 8λ × 8λ sub-array elements → 7 degree beamsteering

500 m, 640 Gb/s backhaul: 220, 90, 35 GHz

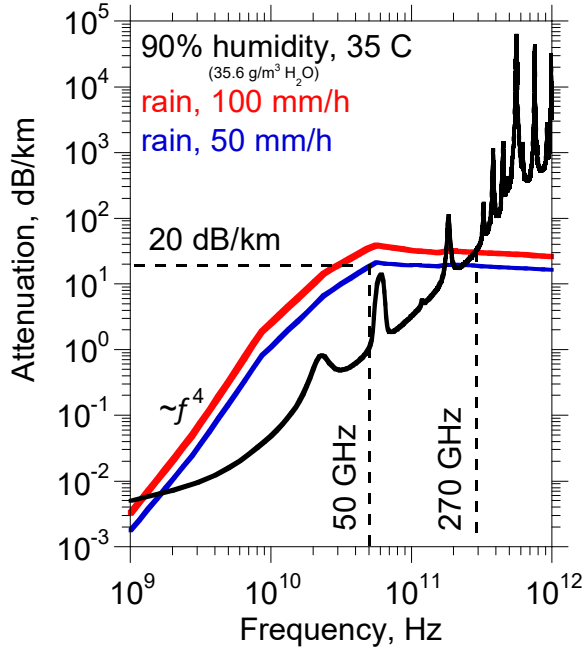
Carrier frequency	220 GHz		90 GHz			35 GHz	
Array baseline	0.58 m		0.91 m			1.5 m	
Atmospheric attenuation	23 dB/km		20 dB/km			11.5 dB/km	
subarrays size	78 × 78 mm^2	39 × 39 mm^2	95 mm × 95 mm			250 mm × 250 mm	
# elements	8 × 8	4 × 4	4 × 4			4 × 4	
Modulation	QPSK	QPSK	QPSK	16QAM	64QAM	256QAM	1024QAM
Channel bandwidth	40 GHz	40 GHz	40 GHz	20 GHz	13 GHz	10 GHz	8 GHz
Fractional bandwidth	18%	18%	44%	22%	15%	29%	23%
Total transmit power*	0.17 W	2.8 W	0.33 W	1.5 W	5.5 W	1.1 W	3.7 W

500 m range, 8 dB noise figure, 50 mm/hr. rain, 10^{-3} uncoded error rate, 2dB (each) transmitter and antenna packaging losses, 10 dB total operating margins, 2 polarizations × 4 channels/polarization × 80 Gb/s/channel, 640 Gb/s total
*Summed over all array elements.

High frequencies competitive if αR < about 5-10 dB

$$\frac{P_{RX}}{P_{TX}} = \frac{N_{TX} N_{RX}}{\Omega_{scan,TX}\,\Omega_{scan,RX}} \left(\frac{\lambda^2}{R^2}\right) e^{-\alpha R}$$

$$\bar{P}_{RX,\min} \simeq \mathrm{SNR} \cdot \left(\frac{kTF}{2}\right) \cdot (\mathrm{bits/sec}) \cdot \frac{2}{\pi} \cdot \frac{2^{\mathrm{bits/sec/Hz}}}{\mathrm{bits/sec/Hz}}$$



Radio link design: Implications

$$\frac{P_{RX}}{P_{TX}} = \frac{N_{TX} N_{RX}}{\Omega_{scan,TX}\,\Omega_{scan,RX}} \left(\frac{\lambda^2}{R^2}\right) e^{-\alpha R}$$

50 GHz or 250 GHz ?

Worst-case losses similar at 50 & 250 GHz

Same link budget at 250 GHz if

- slightly more elements @ 250 GHz
- or less spectrally efficient modulation
- and if we can make good PAs and LNAs.

Any terrestrial > 50 GHz system will be short-range.

$$\bar{P}_{RX,\min} \simeq \mathrm{SNR} \cdot \left(\frac{kTF}{2}\right) \cdot (\mathrm{bits/sec}) \cdot \frac{2}{\pi} \cdot \frac{2^{\mathrm{bits/sec/Hz}}}{\mathrm{bits/sec/Hz}}$$

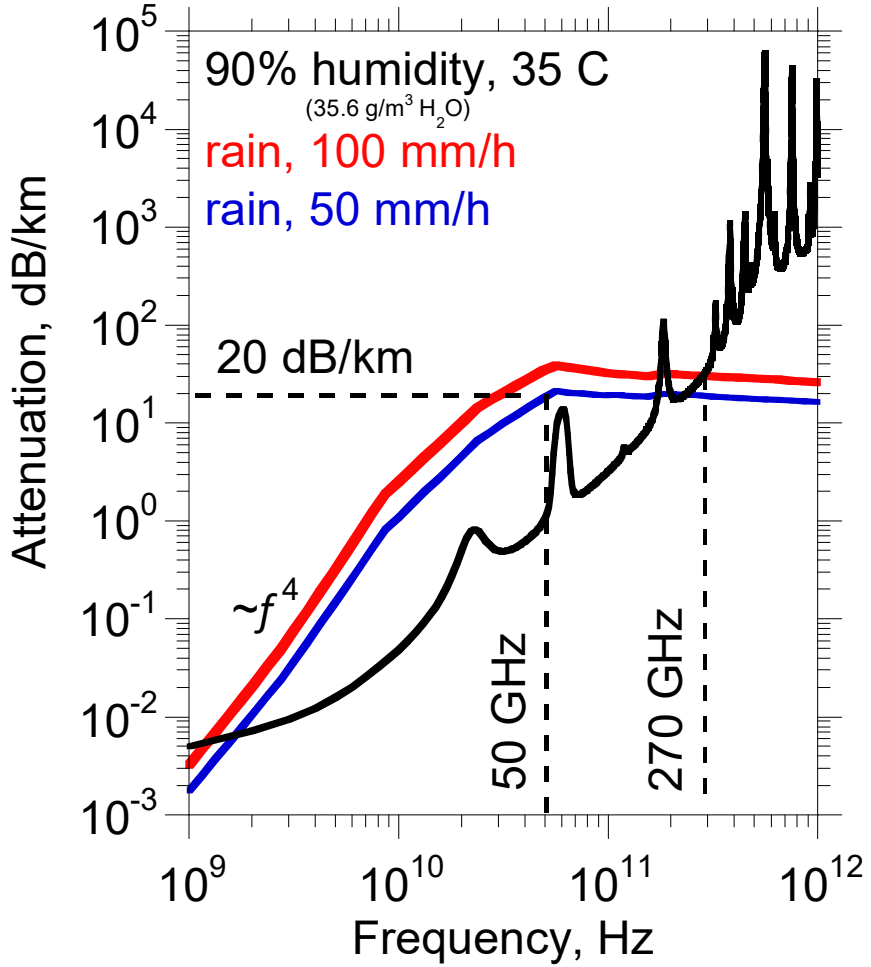
Low frequency (6-12 GHz) or high (28-50, 110-270 GHz)?

Low communications density (Gb/s/km^2) ?

- low deployment costs: widely spaced hubs
- long link distances → use lower frequencies.

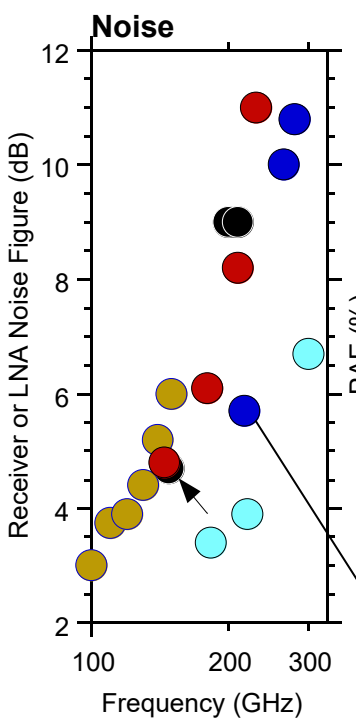
High communications density (Gb/s/km^2) ?

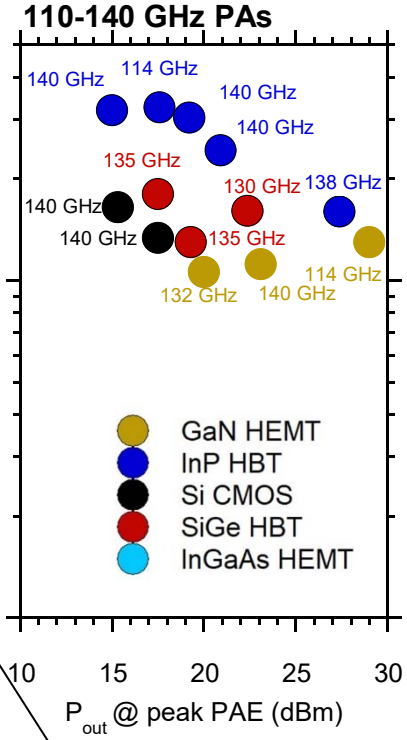
- can afford more closely spaced hubs
- short link distances → can used high frequencies

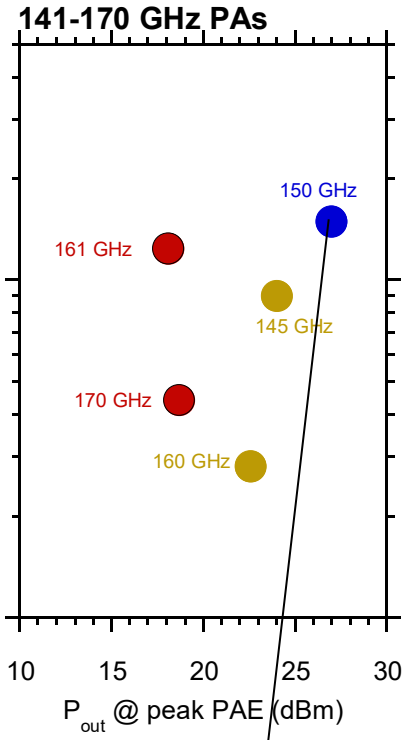


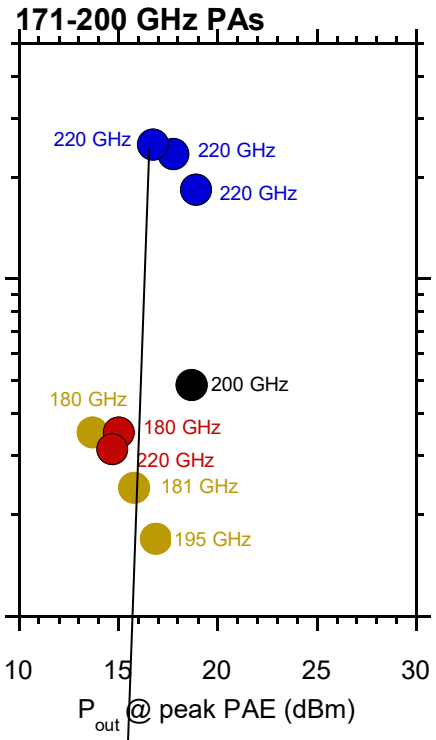
Transistor performance comparison

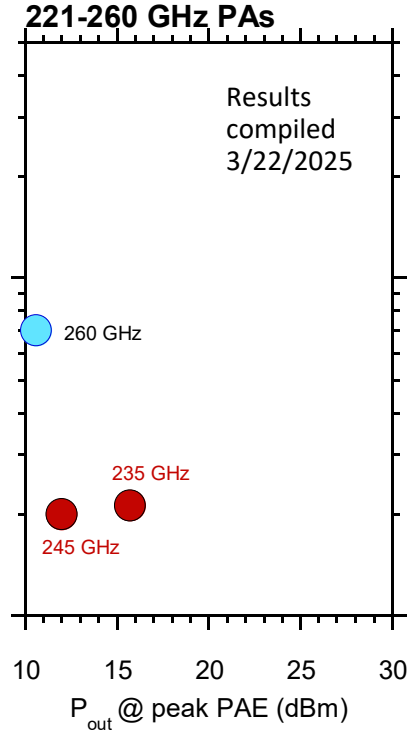
100-300 GHz IC Technologies

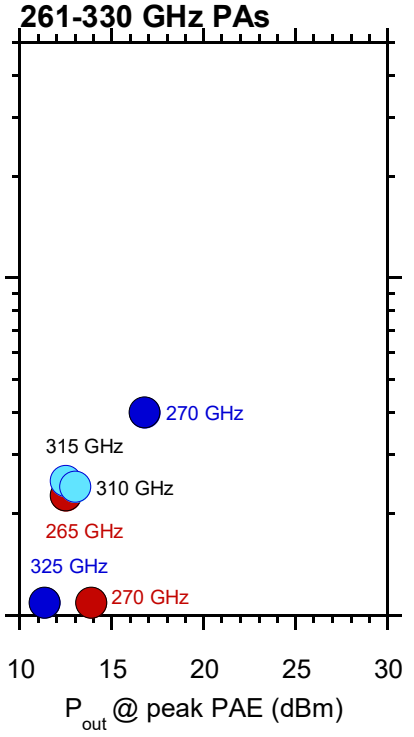




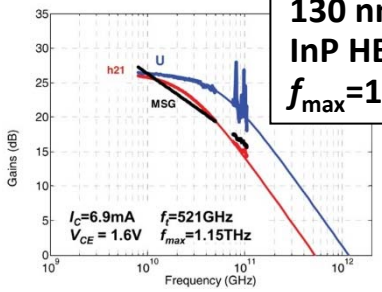






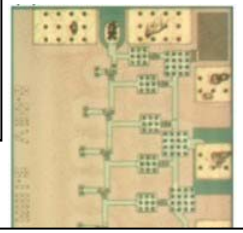


Urteaga, 2011 DRC



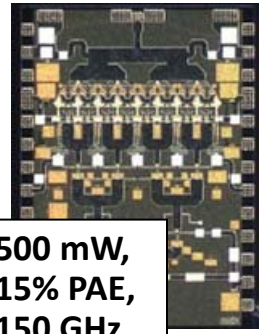
130 nm InP HBT f_{max}=1.15 THz

Alizadeh, 2024 BCICTS



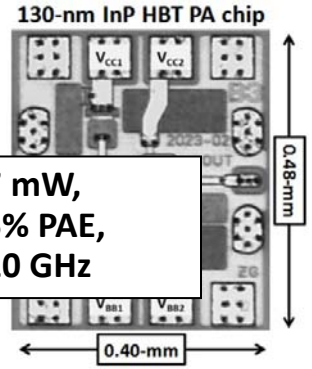
F~5.75 dB, @215 GHz

Alizadeh, 2023 BCICTS



500 mW, 15% PAE, 150 GHz

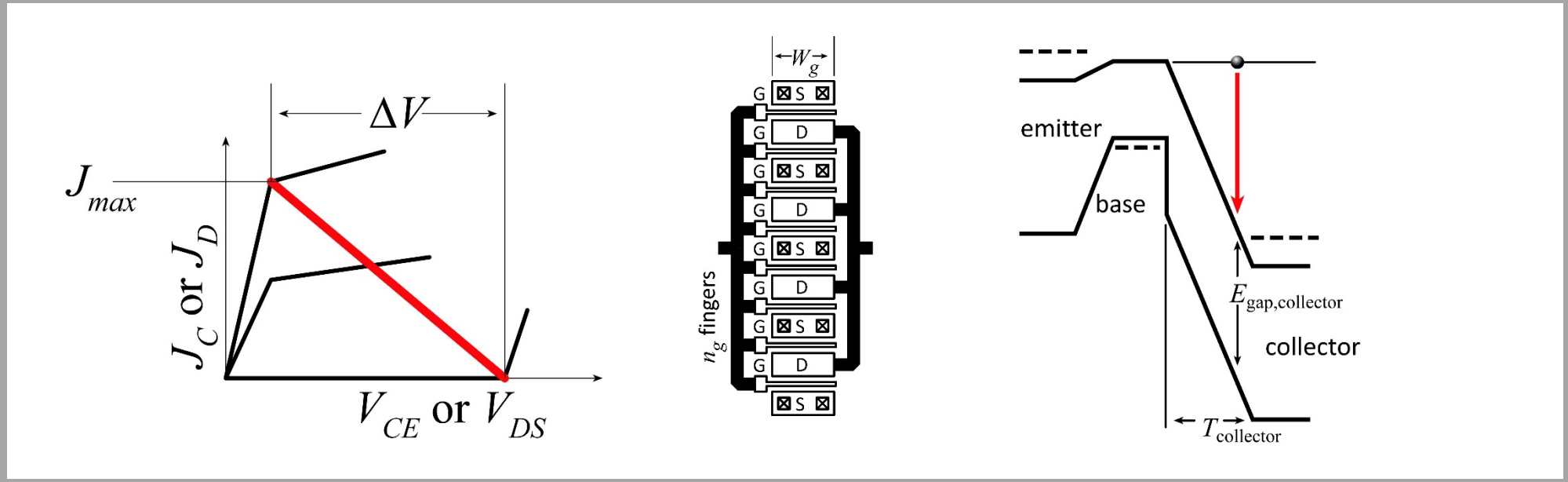
Griffith, 2024 IMS



47 mW, 25% PAE, 220 GHz

What parameters are important for high PAE at 100-300 GHz ?

transistor\circuit co-design



Voltage, current, impedance, power

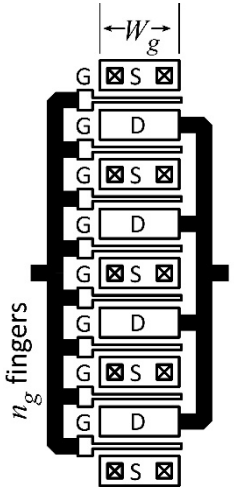
$I_{\max} \propto W_g \cdot (\#\ \text{fingers})$

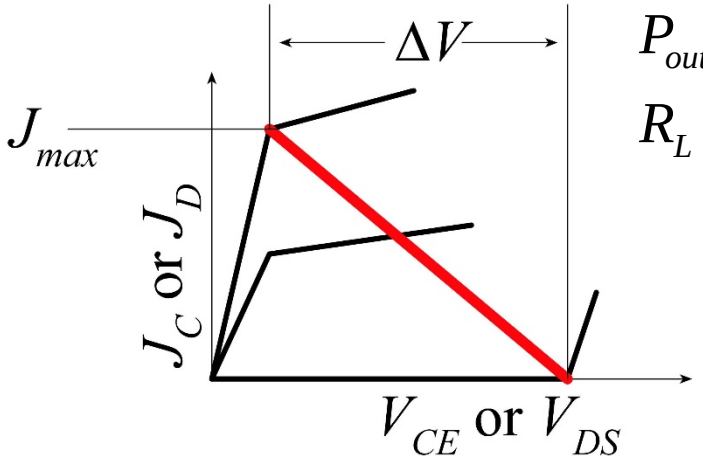
$R_L = \Delta V / I_{\max}$

$P_{out} = \Delta V \cdot I_{\max} / 8 = (\Delta V)^2 / 8R_L$

more fingers $\rightarrow$ more power

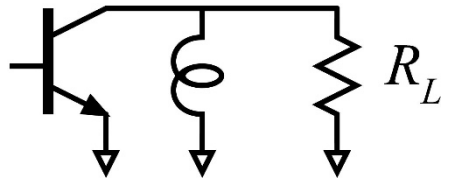
minimum $R_L \rightarrow$ maximum P_{out}





$P_{out} = \Delta V \cdot I_{\max} / 8$

$R_L = \Delta V / I_{\max}$



Transmission lines: minimum $Z_{0,\text{line}}$

lateral modes, junction parasitics

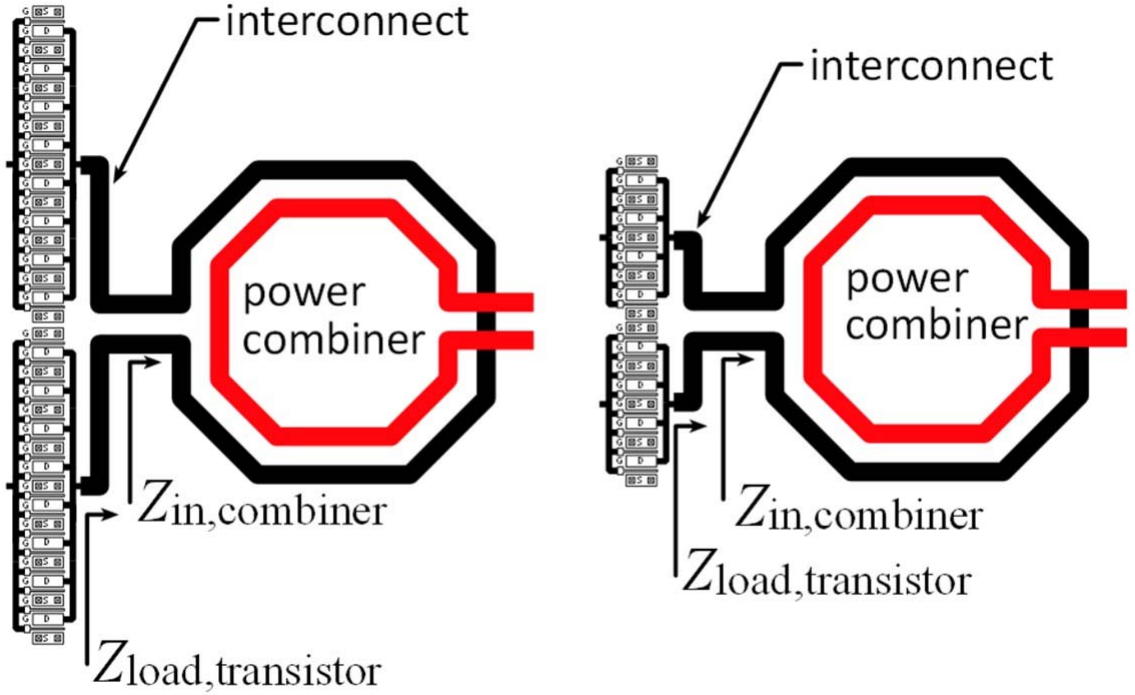
High P_{out} with small ΔV ?

R_L smaller than interconnect $Z_{0,line}$

Substantial impedance shift on interconnect

Desired low R_L cannot be presented to transistor

Large ΔV is necessary for high power

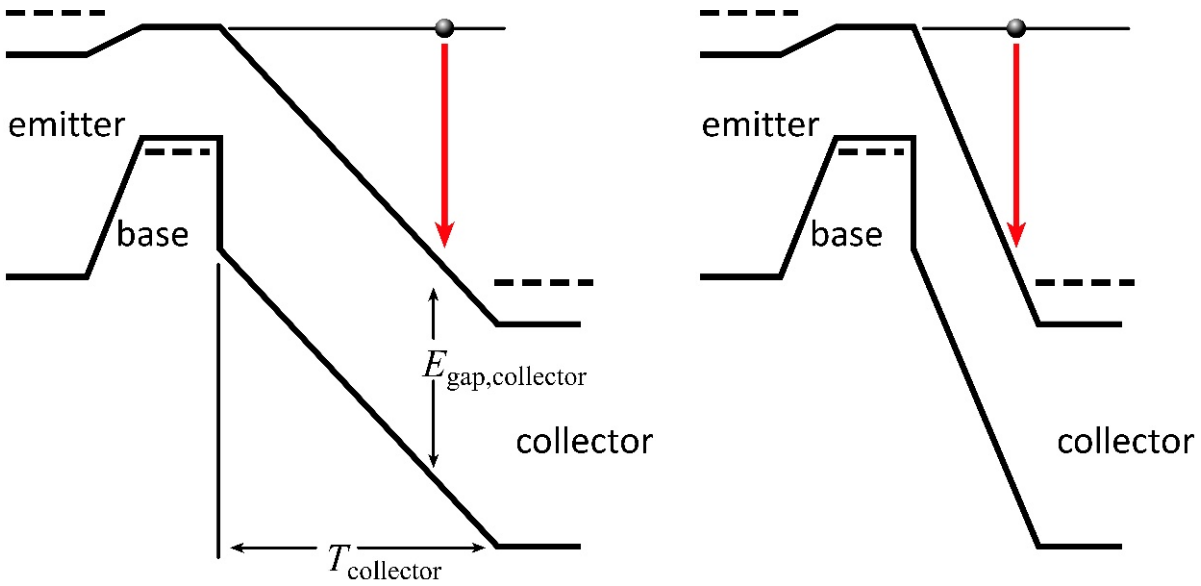


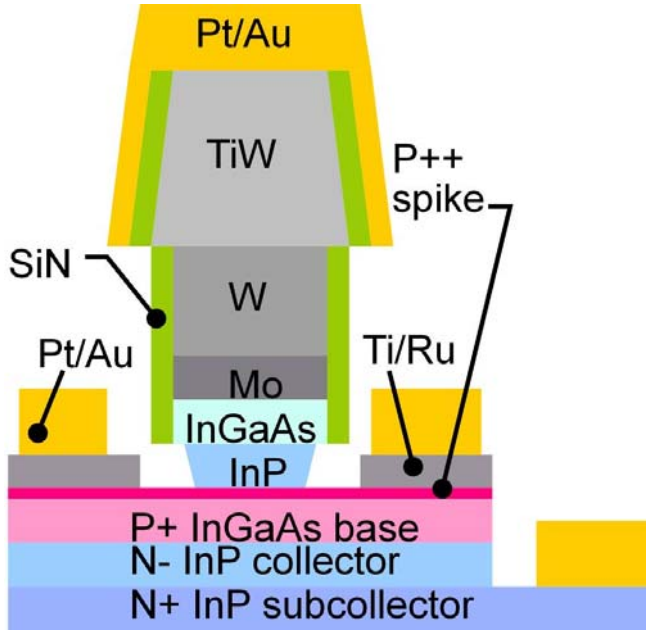
Increasing bipolar transistor bandwidth

Increased transistor bandwidth:

Thinner collector depletion layers

→ reduced breakdown voltage





to double the bandwidth:	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm^2)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1

Johnson figure of merit

Breakdown voltage: $V_{br} \approx \mathcal{E}_{\max} T_C$

Collector transit time: $\tau_c \approx T_C / 2v_{electron}$

Current gain cutoff frequency: $f_\tau = 1/2\pi(\tau_c + \cdots)$

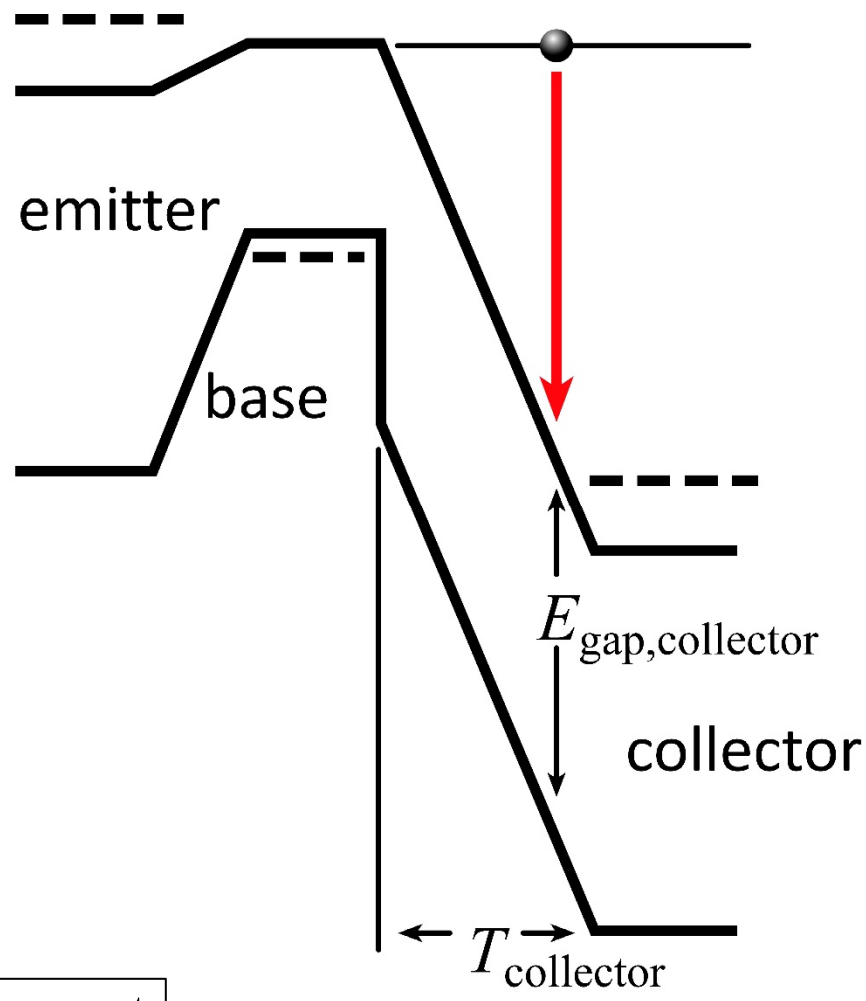
$V_{br}\, f_\tau \le v_{electron} \mathcal{E}_{\max} / \pi \leftarrow$ Johnson figure-of-merit

$P_{out} \propto V_{br}^2 / R_{L,\min} \rightarrow P_{out} \propto \left(v_{electron} \mathcal{E}_{\max} / f\right)^2$

Wide bandgap $E_{gap} \rightarrow$ greater $\mathcal{E}_{\max}$.

InP: moderate $\mathcal{E}_{\max}$, very high $v_{electron}$

GaN: extremely high $\mathcal{E}_{\max}$, moderate $v_{electron}$



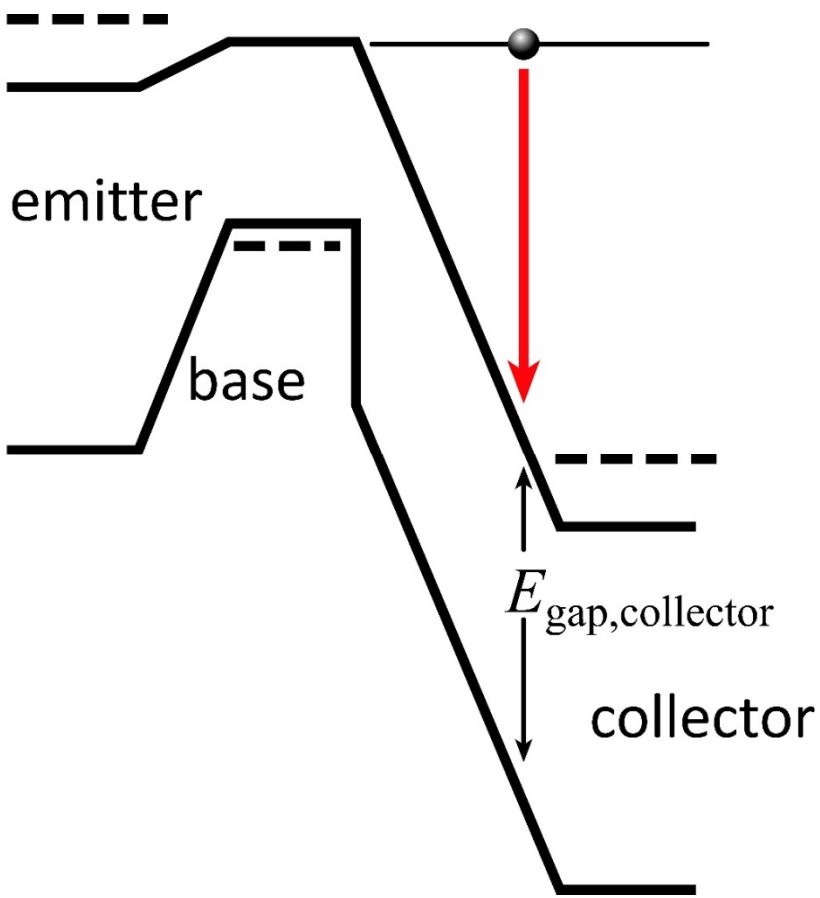
The Johnson F.O.M. has long guided microwave transistor development.

What else matters for 100-300 GHz power amplifiers ?

Breakdown is never less than the bandgap

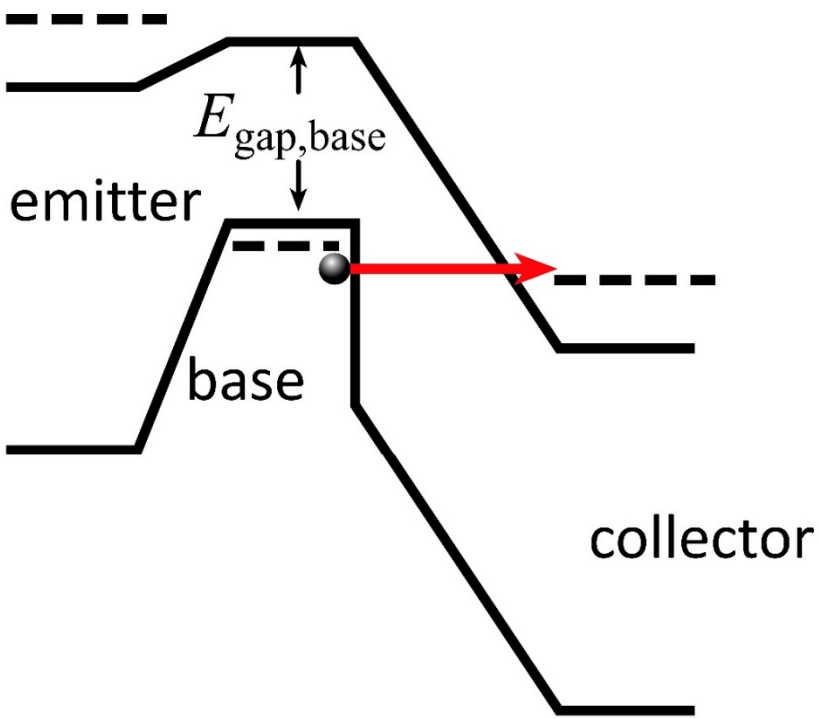
Impact ionization:

$qV_{CE} \geq E_{\text{gap,collector}}$



Band-band tunneling:

$qV_{CE} \geq E_{\text{gap,base}} + \text{base doping degeneracy}$



Impact Ionization vs. Avalanche, BCVEO vs. BVCBO

Impact ionization: electron + hole from energetic carrier

Avalanche: alternating electron and hole ionization

BVCBO: multiplication $m = \infty$; avalanche

BVCEO: multiplication $m = 1/\beta$; avalanche or just ionization.

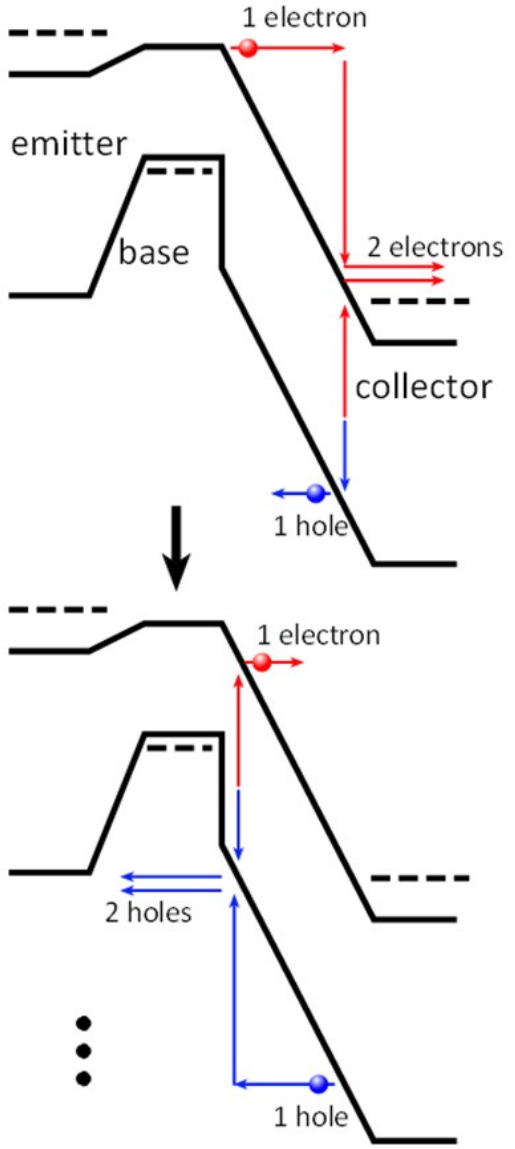
Avalanche is slow:

repeated electron transists, hole transits

InP: $v_{hole} << v_{electron} \rightarrow$ long hole transit time

Silicon: electrons impact ionize more readily than holes

$\rightarrow$ BVCBO significantly larger than BVCEO



BVCBO vs. BVCBO depends on base impedance.

Breakdown varies between

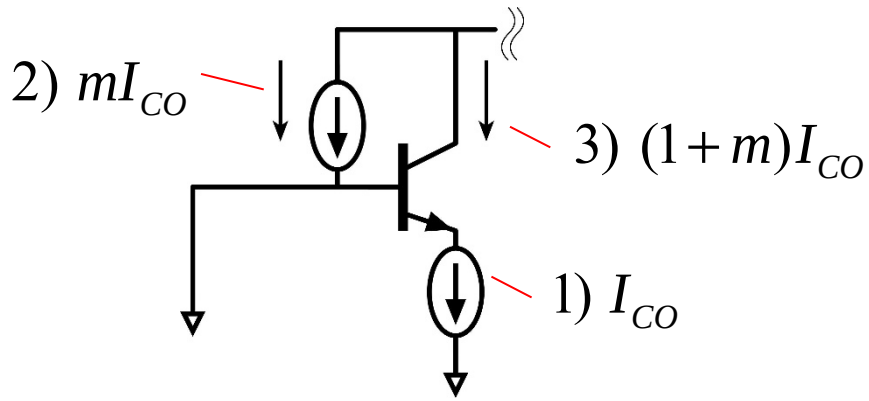
BVCBO and BVCEO

as the impedance

presented to the base

varies from zero to infinity.

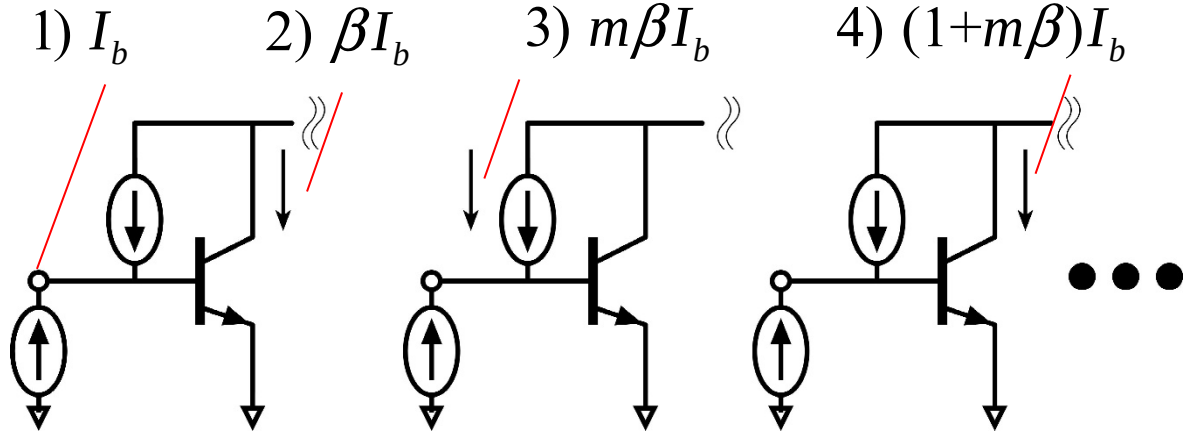
BVCBO



breakdown: $m \to \infty$

BVCEO

breakdown: $m = 1/\beta$



HBT thermal resistance

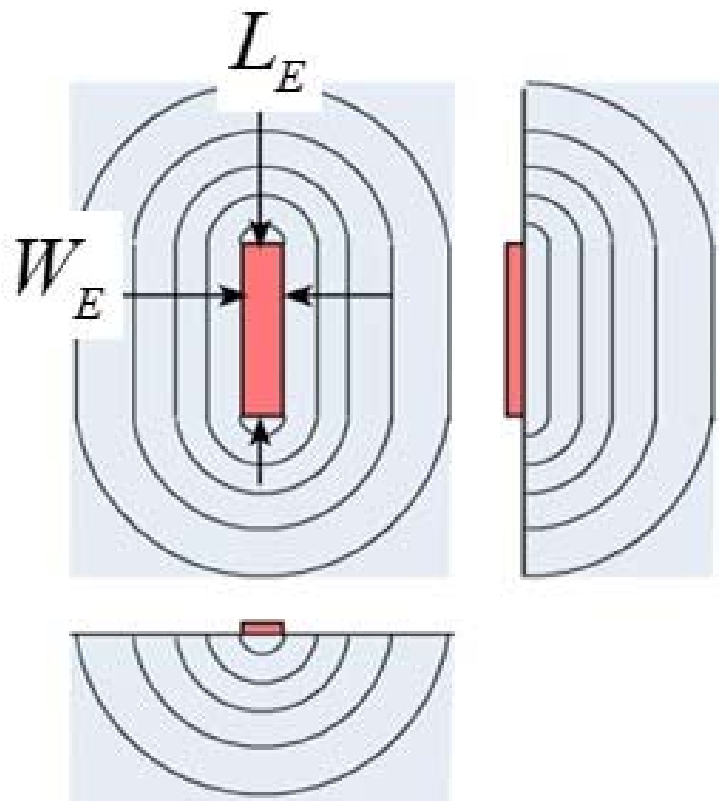
Rodwell, IEEE Proceedings, 2008
Carslaw & Jaeger 1959
W. Liu, IEEE TED, June 1995

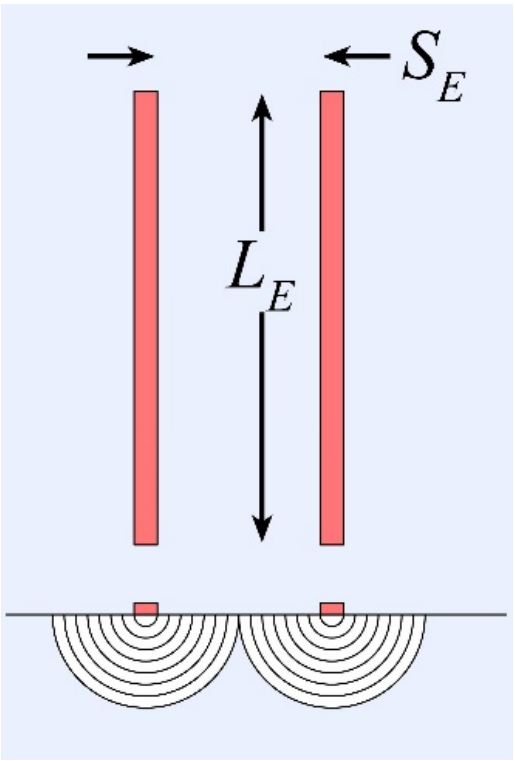
$$\Delta T / P = \frac{1}{\pi K_{th} L_E} \sinh^{-1}\left(\frac{L_E}{W_E}\right) + \frac{1}{\pi K_{th} W_E} \sinh^{-1}\left(\frac{W_E}{L_E}\right)$$

$$\approx \frac{1}{\pi K_{th} L_E} \ln\left(\frac{L_E}{W_E}\right) + \frac{1}{\pi K_{th} L_E}$$

Cylindrical heat flow for $W_E/2 < r < L_E/2$,

Spherical heat flow for $L_E/2 < r$





Near the emitter:

$$T(R) = \frac{P}{\pi K_{th} L_E} \ln\left(\frac{L_E}{2R}\right) + \frac{P}{\pi K_{th} L_E} \; ;$$

Steep temperature gradient

Finger thermal coupling is <<100%.

Bias circuits cannot compensate transistor self-heating

Formula from Carslaw & Jaeger, Conduction of heat in solids, 1959, page 265

HBT electrothermal runaway

Thermally unstable unless

$$K_{\text{th}} = \left.\frac{-\partial V_{be}}{\partial T}\right|_{\text{constant } I_C} \times \frac{V_{CE}\theta_{JA}}{R_{ex} + R_{EE} + R_b/\beta + nkT/qI_E} < 1$$

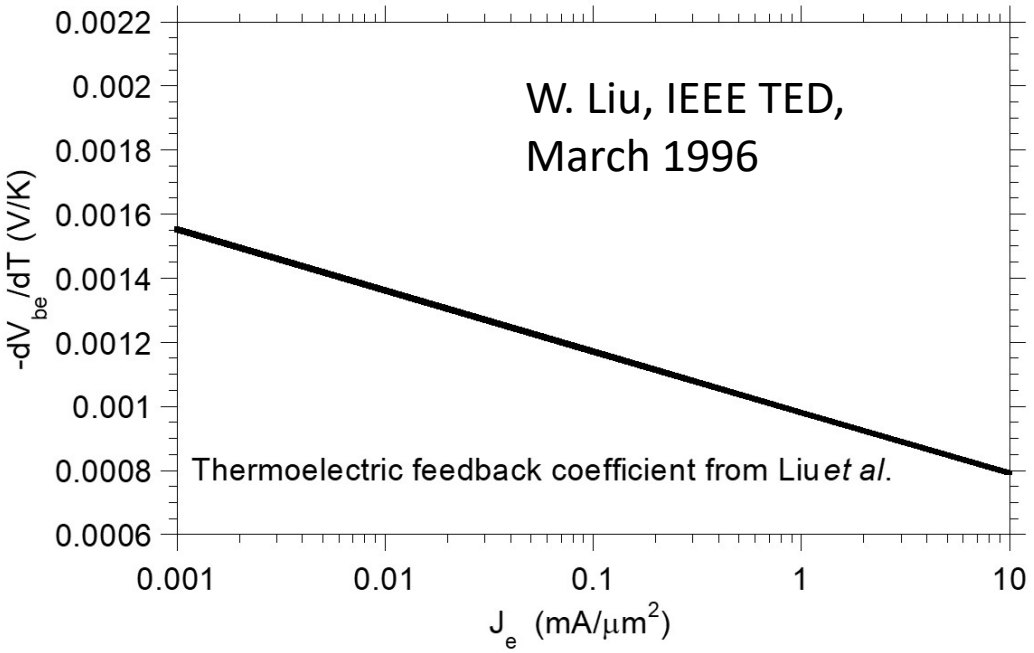
Thermal runaway $\rightarrow$ increasing current $\rightarrow$ destruction

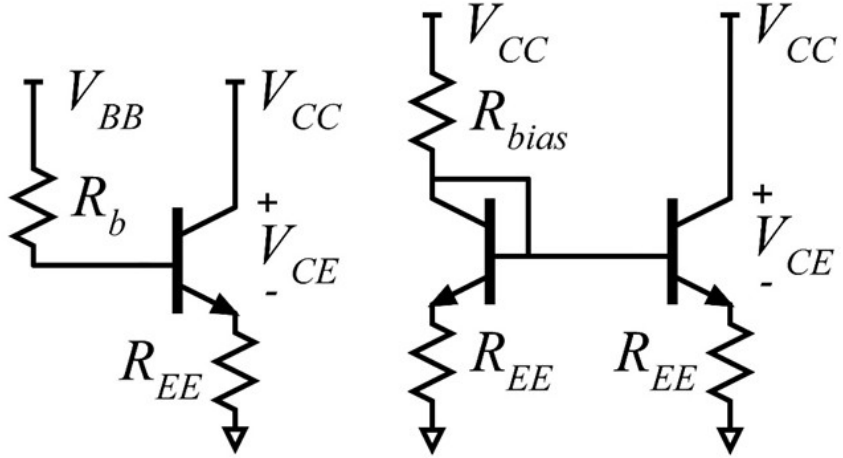
Teledyne 250 nm InP HBT technology:

$$\theta_{JA} \approx 55 \frac{\text{Kelvin}}{\text{mW}} \cdot \frac{1\ \mu\text{m}}{L_E}$$

Griffith, 2007 IEEE IPRM

$$\text{InP HBT @ } J_E \sim 8\ \text{mA}/\mu\text{m}^2 : \frac{\partial V_{be}}{\partial T} \approx -0.8\ \text{mV/Kelvin}$$



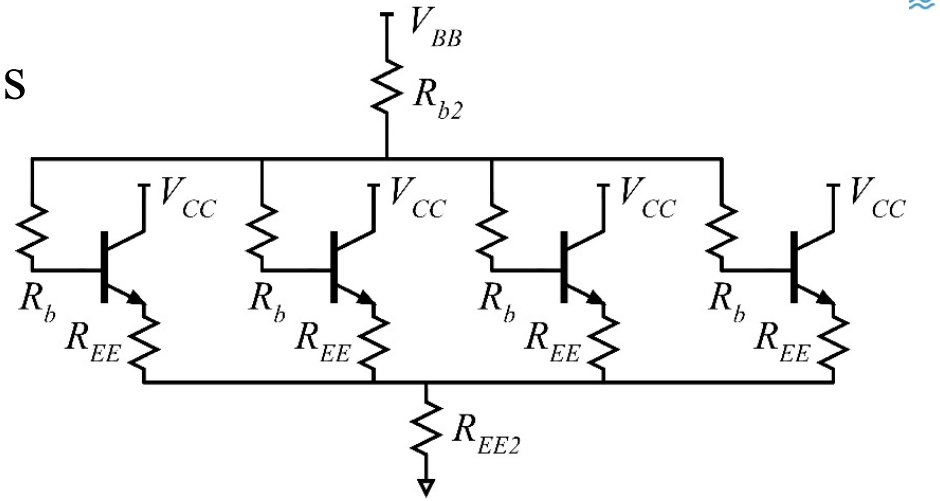


Thermal compensation does not help: weak thermal coupling.

HBT electrothermal runaway

Currents will distribute unequally in a multifinger HBT unless

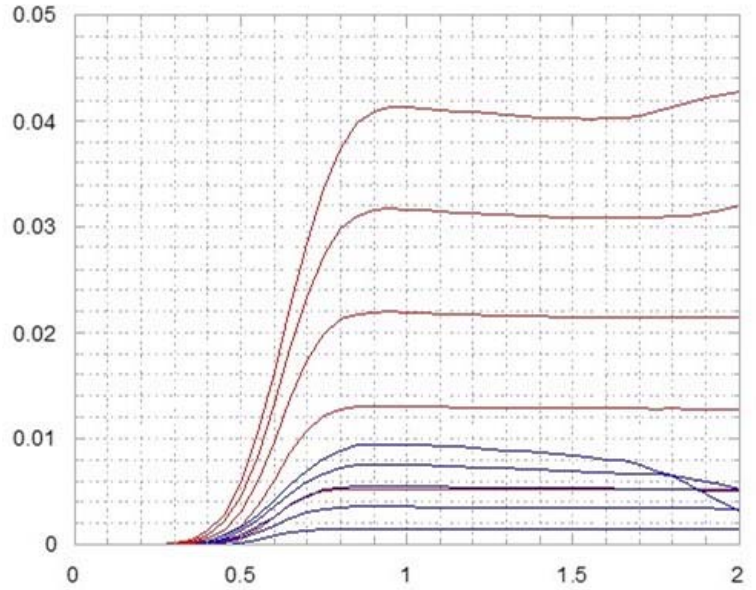
$$K_{\text{thermal stability}} = \left(\frac{-dV_{be}}{dT}\right)\frac{V_{CE}\theta_{JA}}{R_{ex}+R_{EE}+R_b/\beta+nkT/qI_E} < 1$$



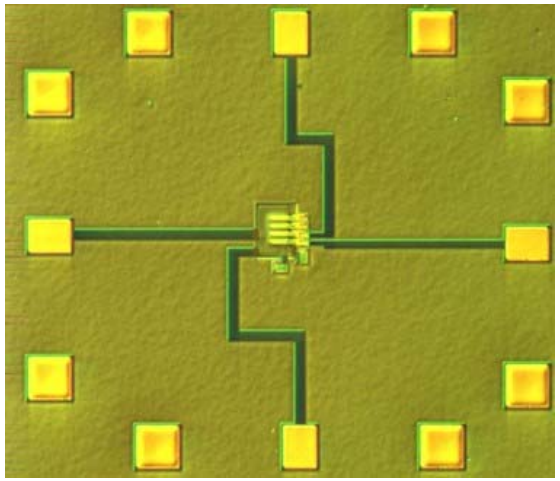
R_{b2} and R_{EE2} do not help.

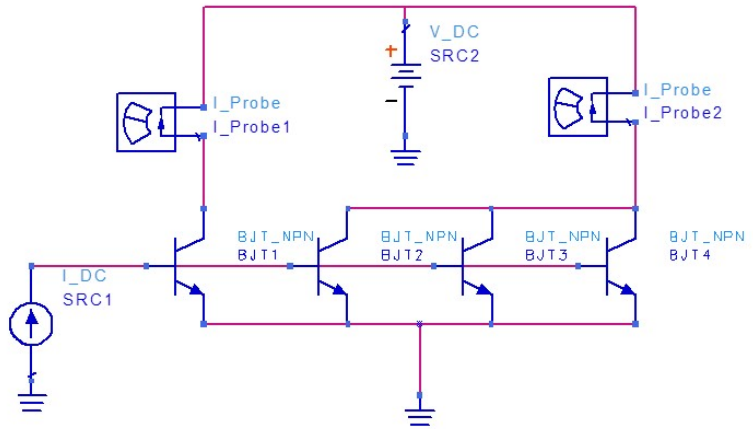
Unequal currents $\rightarrow$ destruction

Finger-finger thermal coupling is too weak to suppress runaway.



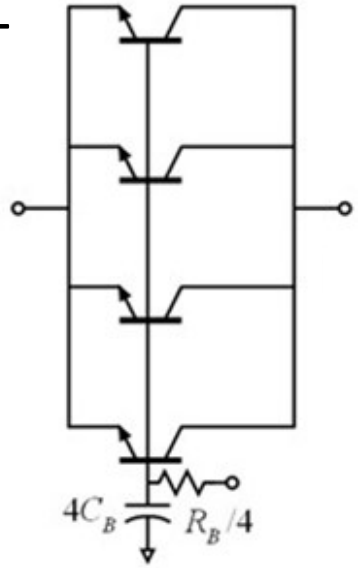
Yun Wei, PhD. thesis, UCSB, 2003

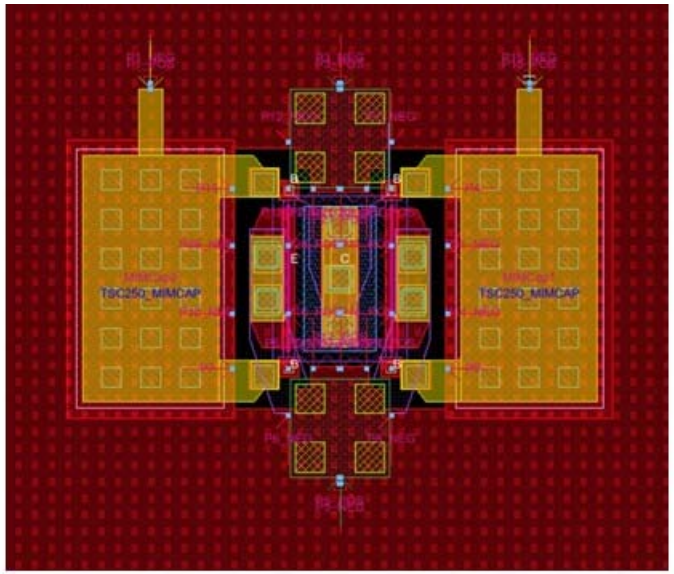




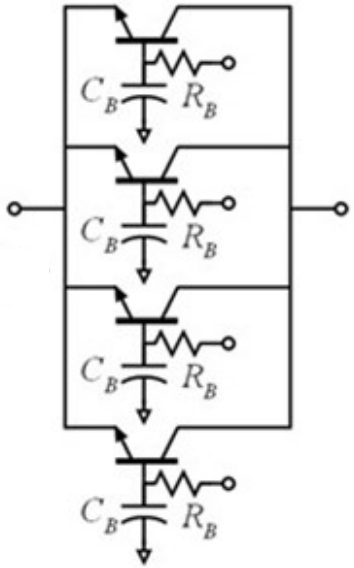
Electrothermally segmented common-base layout

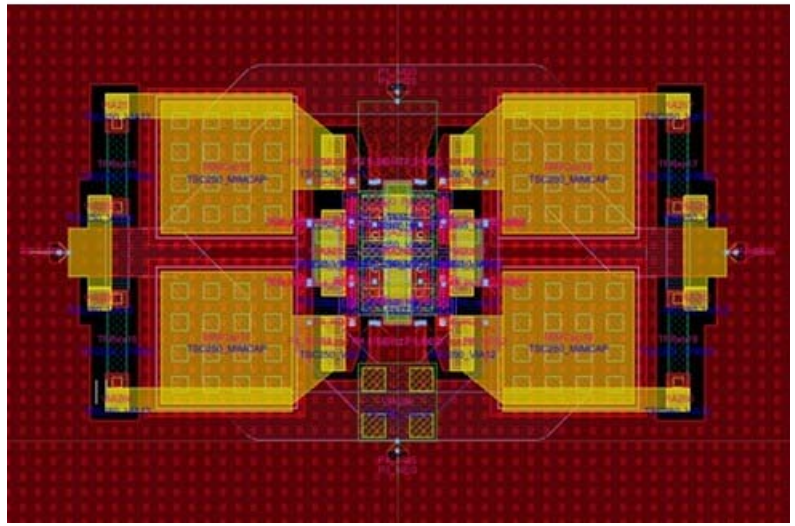
4 finger cell (4 x 0.25 μm x 6 μm); 250 nm InP HBT





Normal cell:
parallel RF connection
parallel DC connection
prone to electro-thermal runaway





Segmented cell:
parallel RF connection
independent DC connection
reduced electro-thermal runaway
no degradation in high-frequency performance.
operates at higher currents at a given Vce.

Amirreza, IEEE Trans MTT 2024

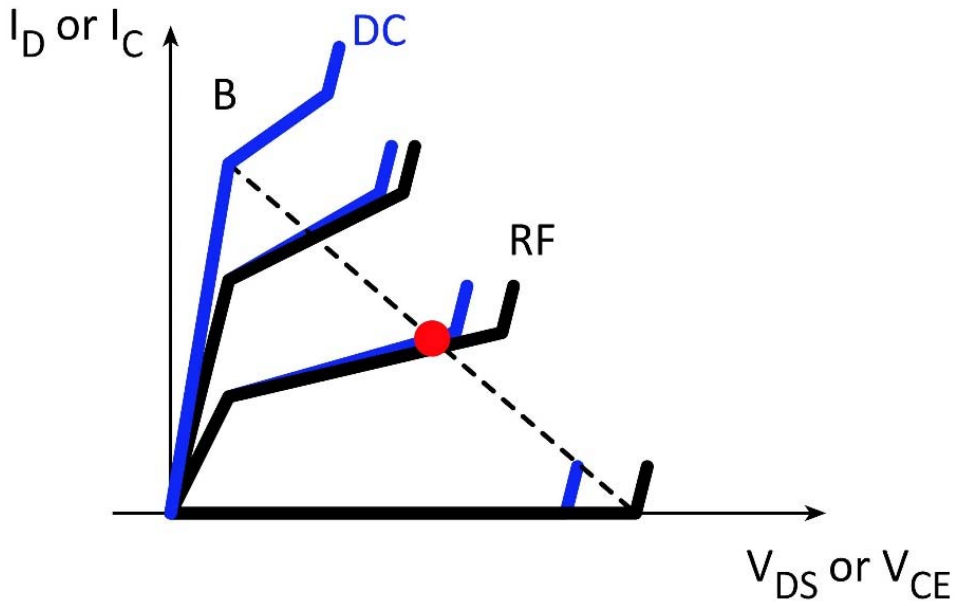
DC and RF breakdown are not the same

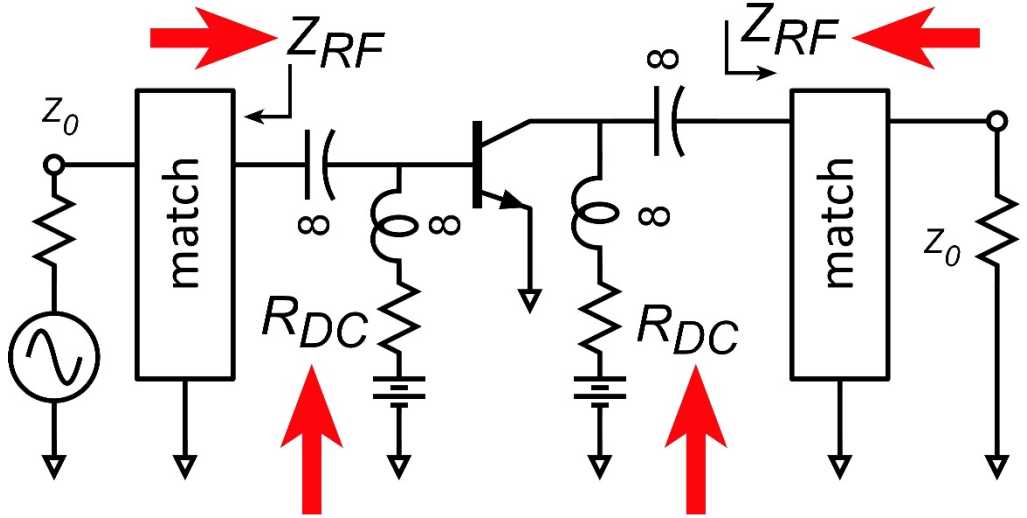
Thermal time-constants
- breakdown depends on temperature
- temperature can't track RF cycle

Electrothermal runaway (thermal positive feedback)
- contributes to breakdown
- temperature can't track RF cycle

Avalanche multiplication
- impact ionization is fast (electron transit time)
- avalanche is slower (hole + electron times)

BVCEO vs. BVCBO
- depends on RF impedances,
- not on DC impedances.





What do 100-300 GHz power transistors need ?

RF/microwave emphasis (DC-30 GHz)

need high V_{br} for high output power

need high V_{br}/V_{sat} for high drain\collector efficiency

need high gain for high PAE (hence high fmax)

These are insufficient at 100-300 GHz.

need high current density for compact transistor layout

transistor cell parasitics, circuit layout parasitics

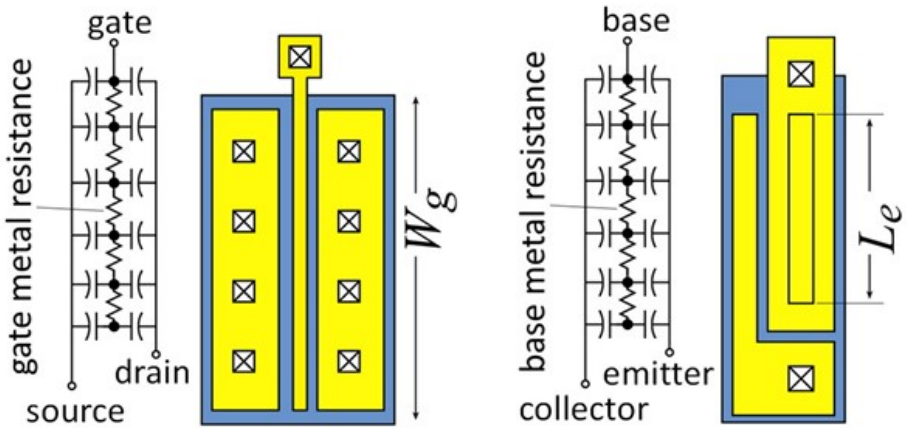
need high current density for adequate large-signal gain

Current density, finger pitch limit cell output power

$$\text{Electrode } RC \text{ charging time} \propto (\text{finger length})^2$$

$$\text{Maximum finger length} \propto 1/\sqrt{\text{frequency}}$$

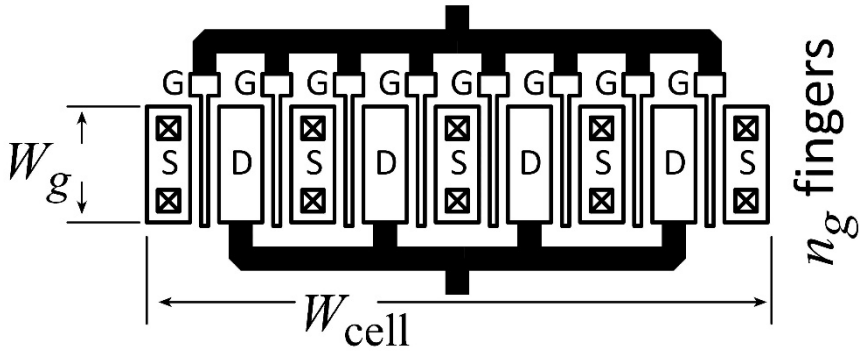
$$\text{Current per finger} \propto 1/\sqrt{\text{frequency}}$$



$$\text{Maximum cell width} \propto 1/\text{frequency}$$

$$\text{Maximum number fingers} \propto 1/\text{frequency}$$

$$\text{Maximum current per cell} \propto 1/\text{frequency}^{3/2}$$



$$\text{Maximum cell power} \propto (\text{maximum load resistance}) \cdot (\text{maximum current})^2 \propto 1/(\text{frequency})^3$$

$$\text{Johnson: maximum power} \propto (\text{maximum voltage})^2/(\text{minimum load resistance}) \propto 1/(\text{frequency})^2$$

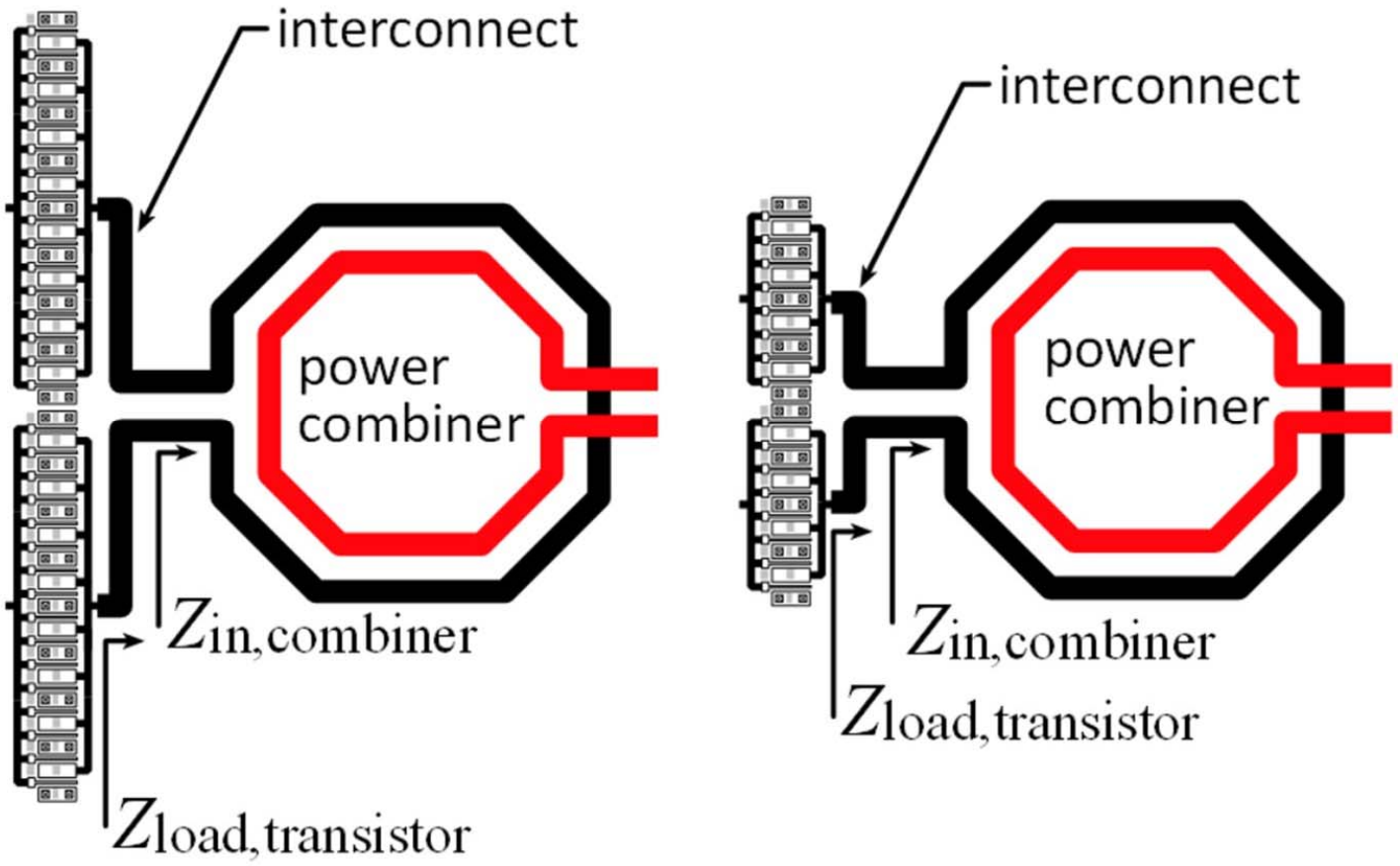
Current density (mA/μm) is a key figure of merit

Low mA/μm→ transistor and circuit layout problems

Low mA/μm → many fingers

Transistor layout:
- large interconnect parasitics
- uncontrolled, unmatched impedances
- degraded f_τ, f_{max}, G, F, P_{sat}, PAE…

IC layout:
- large transistor footprint
- longer interconnects to combiner
- impairs low-Z (high power) design
- reduces feasible P_{out}

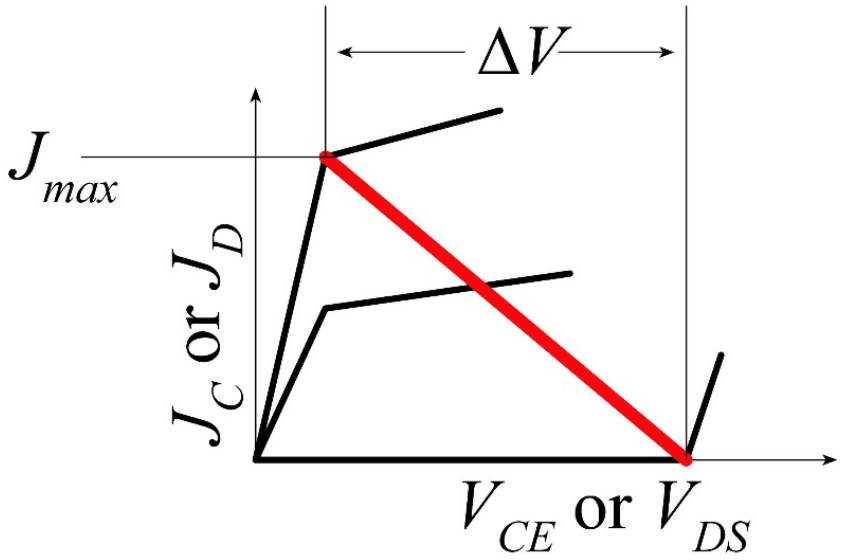


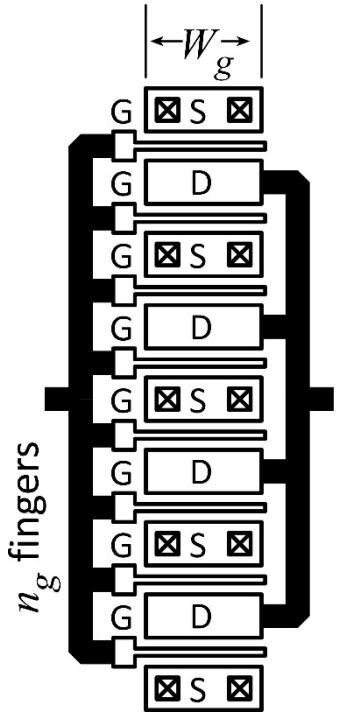
Power-added efficiency

$$\mathrm{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{1}{2}\frac{V_{\max} - V_{\min}}{V_{\max} + V_{\min}} \cdot \left(1 - \frac{1}{G}\right)$$

$$= \eta_{\text{drain/collector}} \cdot \left(1 - \frac{1}{G}\right)$$

$$\text{where} \quad \eta_{\text{drain/collector}} = \frac{P_{out}}{P_{DC}} = \frac{1}{2}\frac{V_{\max} - V_{\min}}{V_{\max} + V_{\min}}$$





$$I_{\max} = J_{\max} n_g W_g$$

What factors determine PAE ?

Can G approach the maximum small-signal gain ?

Invariance of PAE & added power

Alizadeh, IEEE Trans. MTT, 2025

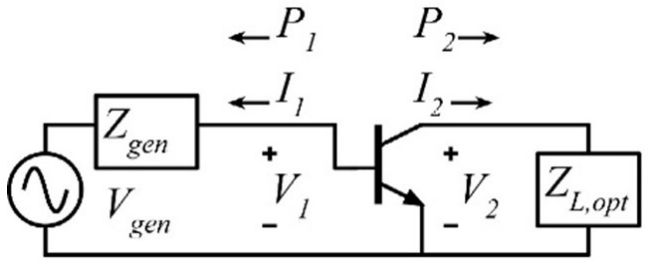
PAE and (P_{out}-P_{in}) are network invariant:
no change given lossless passive embedding.

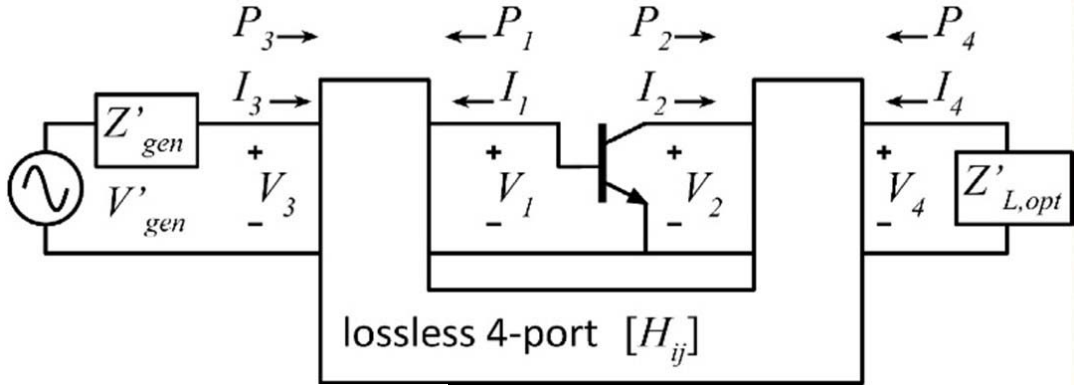
Given correct Z_L,
All (lossless) PAs the same PAE and same (P_{out}-P_{in}).

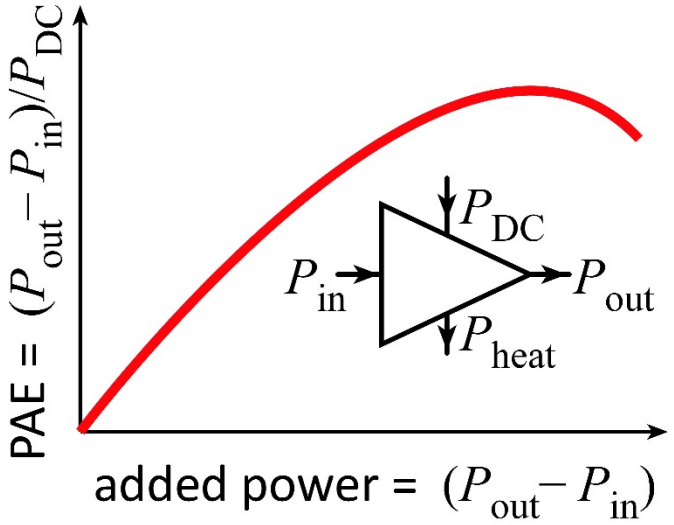
PAE and (P_{out}-P_{in}) are that of the transistor itself.

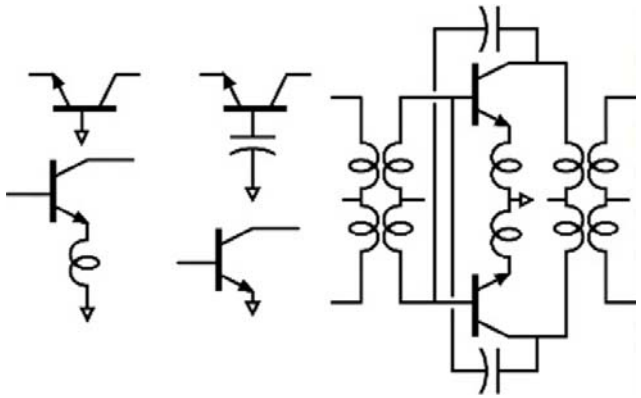
Things that do not change PAE:
CE/CS emitter/source inductance
CB/CG base/gate capacitance
Neutralization
Unconditionally stable positive feedback
(Singhakowinta 1966)

For highest PAE pick circuit with smallest loss.









Maximum transistor PAE

Classic expression: $\mathrm{PAE} = \frac{1}{2}\left(\frac{V_{max} - V_{min}}{V_{min} + V_{min}}\right)\left(1 - \frac{1}{G}\right)$ What is G???????

Can show: $\mathrm{PAE} = \frac{1}{2}\left(\frac{V_{max} - V_{min}}{V_{min} + V_{min}}\right)\left(1 - \frac{f^2}{f_{max}^2}\right)$ *IF* transistor I_{max} is sufficient

...if (BJTs) $I_{max} \geq I_{peak,opt} = 2\pi f_\tau C_{cbi}\left(V_{max} - V_{min}\right)$;

...if (FETs) $I_{max} \geq I_{peak,opt} = 2\pi f_\tau C_{gd}\left(V_{max} - V_{min}\right)$;

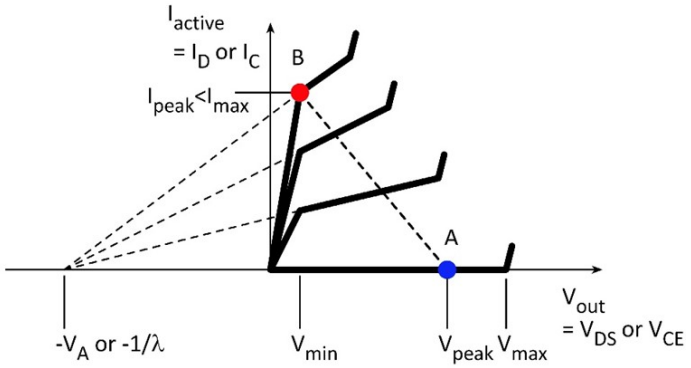
Can show: $\mathrm{PAE} = \frac{1}{2}\left(\frac{V_{max} - V_{min}}{V_{min} + V_{min}}\right)\left(1 - \frac{f^2}{f_{power}^2}\right)$ *IF* I_{max} is insufficient

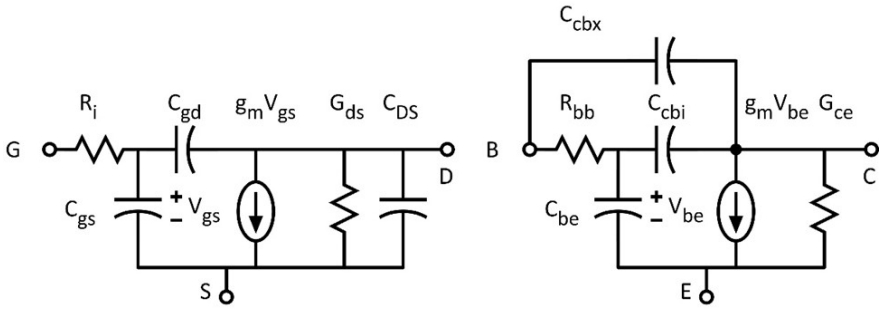
where $f_{power} = \frac{2 f_{max}}{\left(I_{peak} / I_{peak,opt}\right)^{1/2} + \left(I_{peak} / I_{peak,opt}\right)^{-1/2}} \rightarrow f_{max}$ if $I_{peak} = I_{peak,opt}$

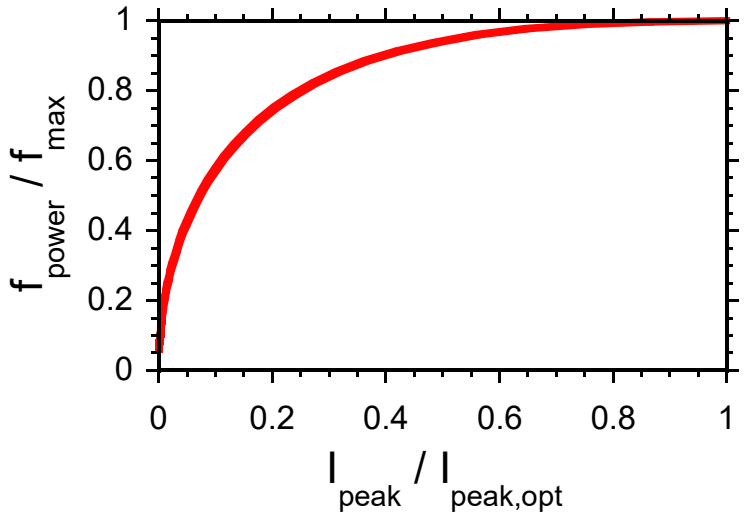
BJT cutoff frequencies: $f_\tau = g_m / 2\pi\left(C_{be} + C_{cbi}\right)$; $f_{max} = \left(f_\tau / 8\pi R_{bb} C_{cbi}\right)^{1/2}$

FET cutoff frequencies $f_\tau = g_m / 2\pi\left(C_{gs} + C_{gd}\right)$; $f_{max} = \left(f_\tau / 8\pi R_g C_{gd}\right)^{1/2}$;

All parameters are large-signal: $g_m \triangleq \Delta I_D / \Delta V_{gs}$ not $\partial I_D / \partial V_{gs}$, etc.







Current Drive capabilities

200 nm InP HBT; Rode 2015 IEEE TED

$f_\tau = 480$ GHz, $f_{max} = 1.07$ THz

$V_{max} = 4$ V, $V_{min} = 0.7$ V

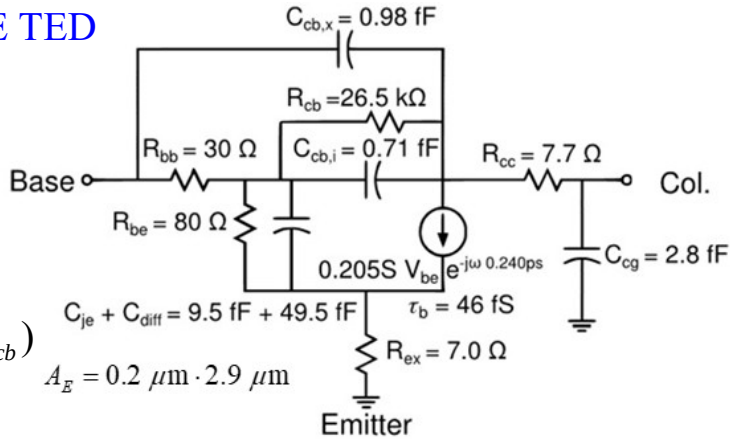
$I_{max} = 3\ \text{mA}/\mu\text{m} \cdot 2.9\mu\text{m} = 8.7$ mA

$I_{opt} = 2\pi f_\tau C_f (V_{max} - V_{min})$

$= (V_{max} - V_{min}) \cdot g_m C_{cbi} / (C_{be} + C_{cb})$

$= 8.0$ mA

$I_{opt} = 8.0$ mA $< I_{max} = 8.7$ mA



48 nm GaN HEMT;

Asko 2023 IEEE Microwave & Wireless Tech. Lett.

$f_\tau = 114$ GHz, $f_{max} = 241$ GHz

$V_{max} = 34$ V, $V_{min} = 6$ V

$I_{max} = 2\ \text{mA}/\mu\text{m} \cdot 100\mu\text{m} = 200$ mA

$I_{opt} = 2\pi f_\tau C_f (V_{max} - V_{min})$

$= (V_{max} - V_{min}) \cdot g_m C_{gd} / (C_{gs} + C_{gd})$

$= 281$ mA

$I_{opt} = 281$ mA $> I_{max} = 200$ mA...but not far off

45 nm GaN HEMT; Shinohara 2011 IEEE EDL

$f_\tau = 257$ GHz, $f_{max} = 396$ GHz

$V_{max} = 13$ V, $V_{min} = 1.5$ V

$I_{max} = 2.3\ \text{mA}/\mu\text{m} \cdot 80\mu\text{m} = 184$ mA

$I_{opt} = 2\pi f_\tau C_f (V_{max} - V_{min})$

$= (V_{max} - V_{min}) \cdot g_m C_{gd} / (C_{gs} + C_{gd})$

$= 161$ mA

$I_{opt} = 161$ mA $< I_{max} = 184$ mA

Model parameters

g_m (mS)	84.9
g_d (mS)	9.4
C_{gs} (fF)	39.9
C_{gd} (fF)	7.9
R_i (Ω)	0.21
R_g (Ω)	5.5
R_s (Ω)	2.6
R_d (Ω)	2.6
$f_{T.model}$ (GHz)	257
$f_{max.model}$ (GHz)	396

$W_g = 2 \times 40\ \mu$m

SMALL SIGNAL MODEL PARAMETERS OF THE 4 × 25 μm DEVICE

g_M (mS)	C_{GS} (fF)	C_{GD} (fF)	C_{DS} (fF)	r_{DS} (ohm)	r_{GS} (ohm)	r_{GD} (ohm)	tau (fsec)
56.9	65.5	14	27	268	2.65	18	311
r_G (ohm)	r_D (ohm)	r_S (ohm)	L_G (pH)	L_D (pH)	L_S (pH)	outer finger	inner finger
1.2	3.2	1.6	15.5	6.1		≈ 0	3.2

Theory vs. simulation...and vs. measurement

Teledyne 250 nm InP HBT, 220 GHz

$V_{max} = 4.2$ V, $V_{min} \simeq 0.8$ V, $f_{max} = 580^*$ GHz

$$\frac{1}{2}\left(\frac{V_{max} - V_{min}}{V_{min} + V_{min}}\right) = 34\%$$

$$\left(1 - f^2 / f_{max}^2\right) = 86\%$$

$PAE_{theory} = 29.1\%$

$PAE_{CAD} = 30\%$ (4-finger, $@P_{sat}$)

$\approx 33\%$ (1-finger, $@P_{sat}$)

*long finger; reduces f_{max}.

Teledyne 130 nm InP HBT, 220 GHz

$V_{max} = 4$ V, $V_{min} \simeq 0.8$ V, $f_{max} = 1.15$ THz

$$\frac{1}{2}\left(\frac{V_{max} - V_{min}}{V_{min} + V_{min}}\right) = 33.3\%$$

$$\left(1 - f^2 / f_{max}^2\right) = 96\%$$

$PAE_{theory} = 32.1\%$

$PAE_{CAD} = 35\%$ (4-finger, $@P_{sat}$)

$\approx 38\%$ (1-finger, $@P_{sat}$)

Teledyne 130 nm InP HBT, 280 GHz

$V_{max} = 4$ V, $V_{min} \simeq 0.8$ V, $f_{max} = 1.15$ THz

$$\frac{1}{2}\left(\frac{V_{max} - V_{min}}{V_{min} + V_{min}}\right) = 33.3\%$$

$$\left(1 - f^2 / f_{max}^2\right) = 94\%$$

$PAE_{theory} = 31.4\%$

$PAE_{CAD} = 32.6\%$ (4-finger, $@P_{sat}$)

$\approx 35\%$ (1-finger, $@P_{sat}$)

Theory works reasonably for InP HBT; less well for Ga-polar GaN. Why ?

Should use large-signal, not small-signal f_{max}. (s.s. is optimistic)
CAD and measurements: heavily saturated; enhances PAE
Harmonic tuning, when feasible, further enhances PAE
4-finger HBTs are ~3% less efficient that 1-finger HBTs
150-300 GHz PAs are ~10% less efficient than 4-finger HBTs (InP)
InP HBT PA measurements are reasonably close to simulation.

UCSB N-polar GaN, 132 GHz

$V_{max} = 34$ V, $V_{min} \simeq 6$ V, $f_{max} = 241$ GHz

$$\frac{1}{2}\left(\frac{V_{max} - V_{min}}{V_{min} + V_{min}}\right) = 35\%$$

$$\left(1 - f^2 / f_{max}^2\right) = 70\%$$

$PAE_{theory} = 24.5\%$

$PAE_{measured} = 25\%$ (load-pull)

Max PAE analysis: Caveats

Model assumes constant values for (g_m, C_{gs}, C_{gd})

Reality: these vary very strongly across loadline

So: use large-signal quantities:

$g_m = \Delta I_D / \Delta V_{GS}, C_{gs} = \Delta Q_{gate} / \Delta V_{GS}, C_{gd} = \Delta Q_{gate} / \Delta V_{GD}$

As these vary over the (I_{out}, V_{out}) plane, there will be further optimization beyond the above analysis

Even given this correction, analysis remains very approximate.

The goal of this analysis is to provide 1st understanding of current drive requirements:

Specifically, what load current is required for the optimum loadline impedance

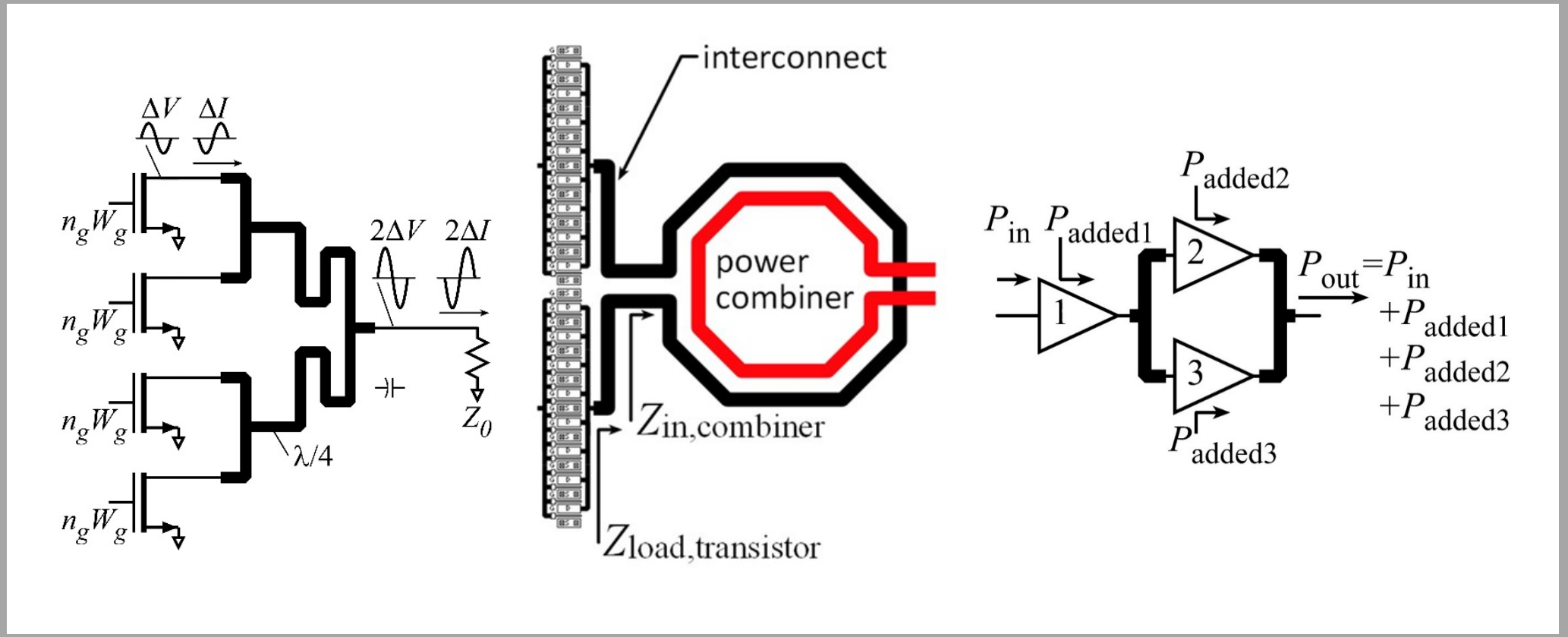
to be the same as the optimum impedance for small-signal gain ?

And, if the transistor cannot deliver this, how much gain is sacrificed ?

For GaN, trapping behavior plays critical role in setting large-signal gain near peak PAE

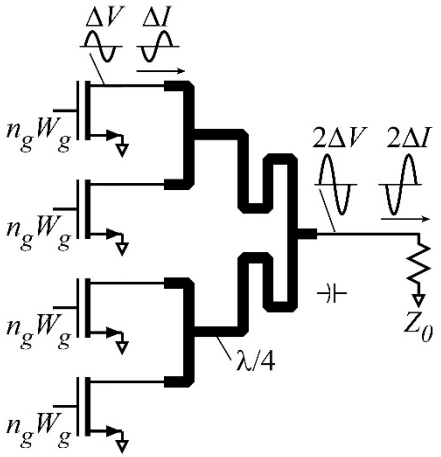
(thanks to Keisuke Shinohara, Teledyne, for this and other guidance)

power amplifier design



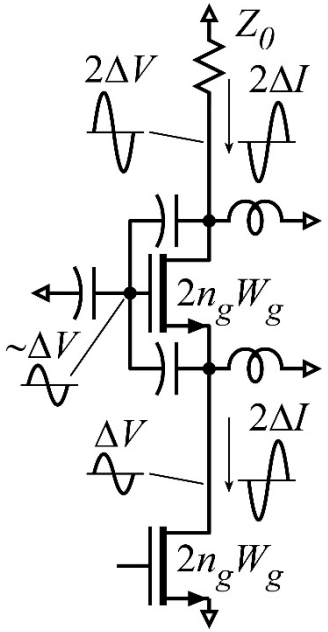
100-300 GHz Power combining: what is best ?

Corporate T-line



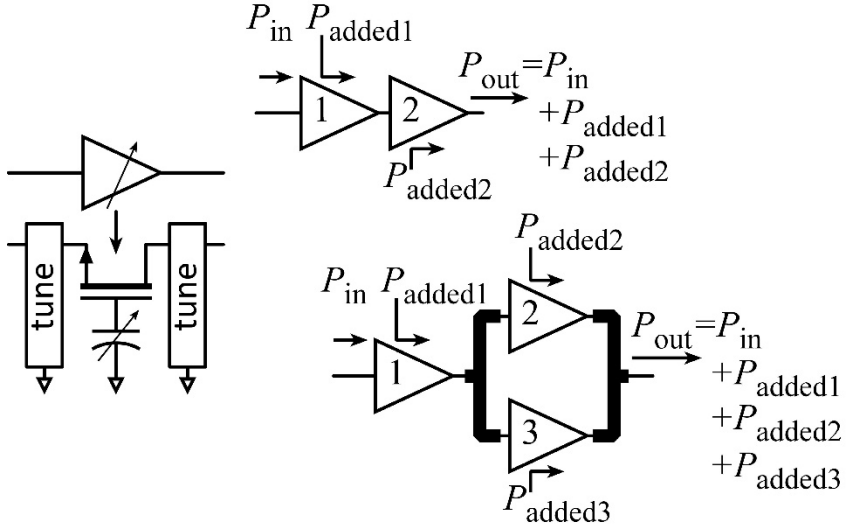
Direct series-connected

M. Shifrin: 1992 IEEE µWave/mmWave Monolithic Circuits Symp. (Raytheon)



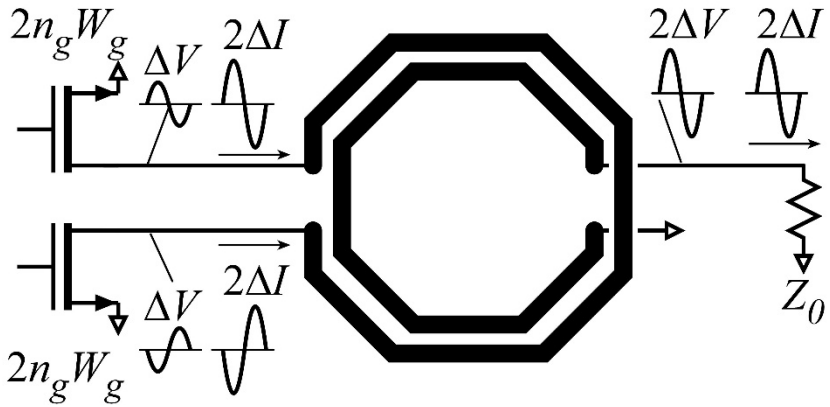
Cascade combining

A. Ahmed 2018 EuMIC, 2021 RFIC (UCSB)



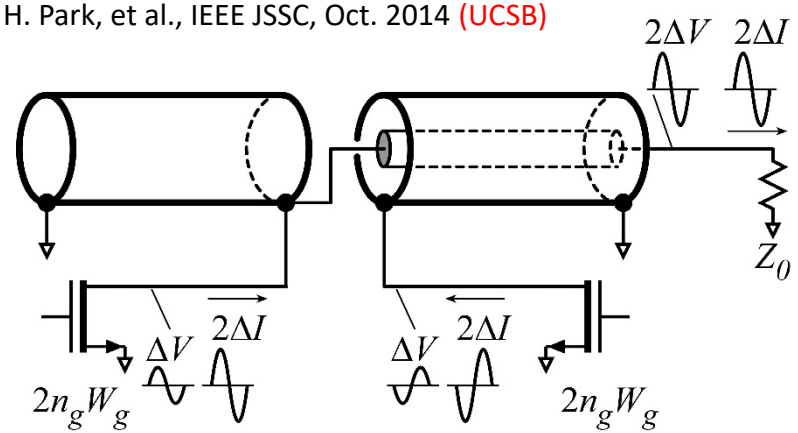
Distributed Active Transformer

I. Aoki, IEEE Trans MTT, Jan. 2002 (CalTech)

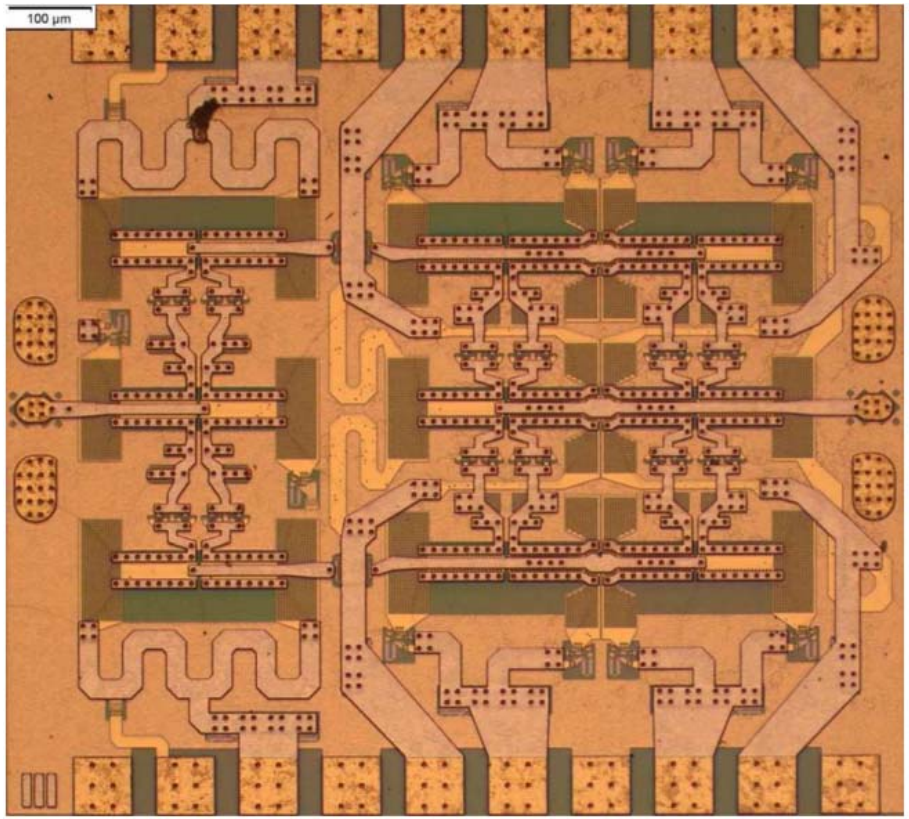


Balun series-connected

λ/4 baluns: Y. Yoshihara, 2008 IEEE Asian Solid-State Circuits Conference (Toshiba)
sub-λ/4 baluns: H. Park, et al., IEEE JSSC, Oct. 2014 (UCSB)

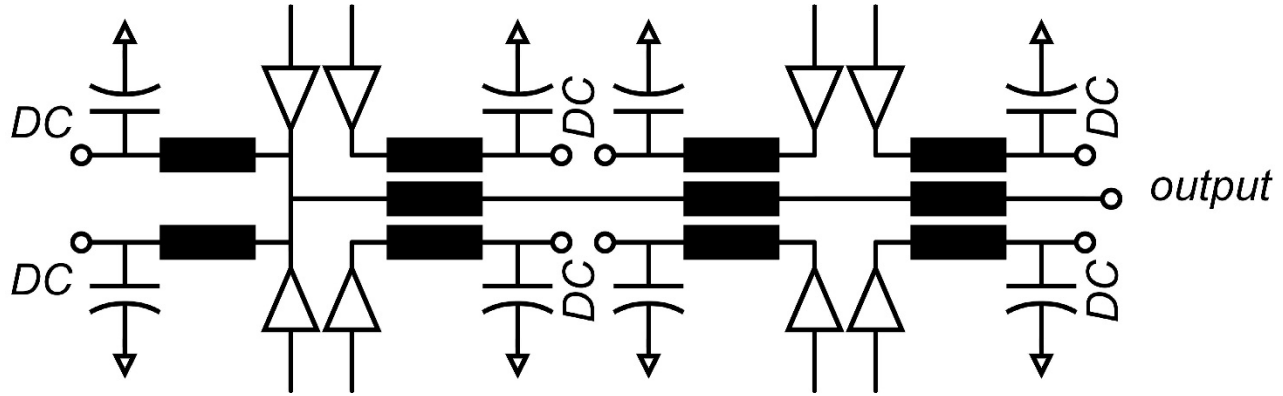


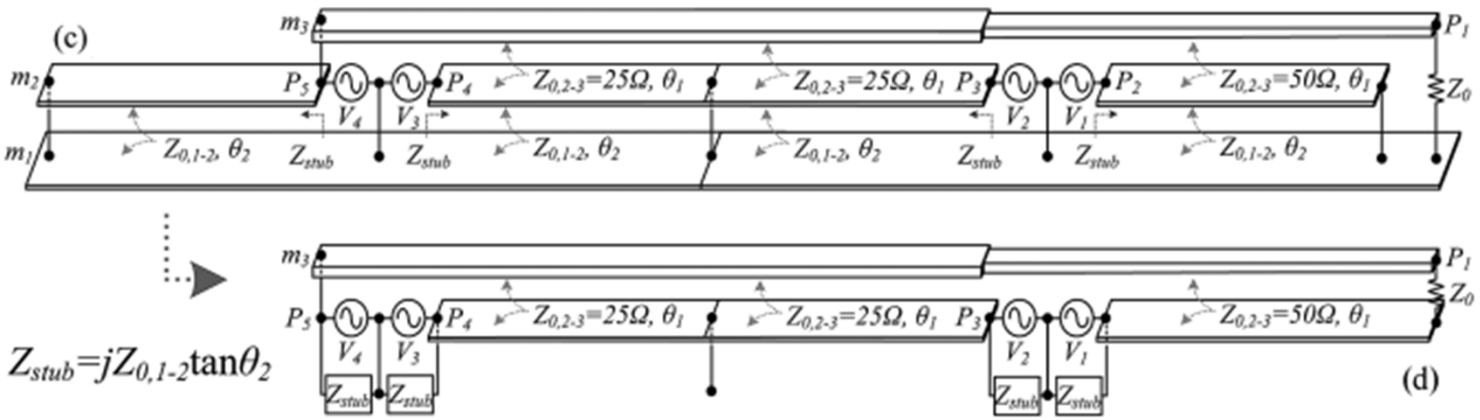
Example: 4:1 Balun Series-Connected @ 81 GHz



81GHz, 17 dB Gain
470 mW P_{sat} , 23% PAE
Teledyne 250 nm InP HBT
2 stages, 1.0 mm^2(incl pads)

λ/4 baluns: Y. Yoshihara, 2008 IEEE Asian Solid-State Circuits Conference (Toshiba)
sub-λ/4 baluns: H. Park, et al, IEEE JSSC, Oct. 2014 (UCSB)





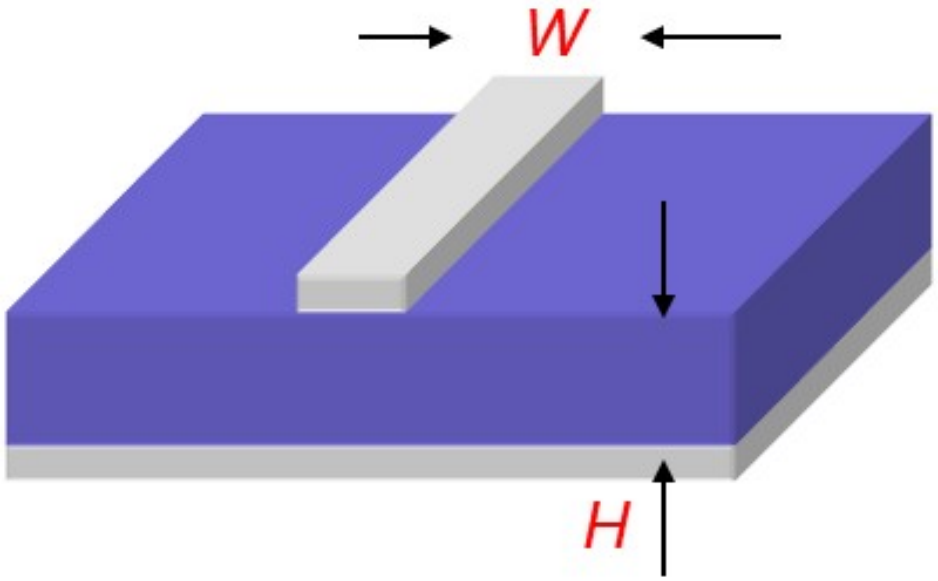
On-Wafer Interconnect Losses

Interconnects in packages and on PCBs:

$H \propto 1/\text{frequency}$ (to control radiation loss)

$\text{loss (dB/mm)} \propto (\text{frequency})^{3/2}$

$\text{loss (dB/wavelength)} \propto \sqrt{\text{frequency}}$



Interconnects in ICs:

H is independent of frequency

$\text{loss (dB/mm)} \propto \sqrt{\text{frequency}}$

$\text{loss (dB/wavelength)} \propto 1/\sqrt{\text{frequency}}$

100-300 GHz: corporate power-combining often best

loss (dB/wavelength) $\propto 1/\sqrt{\text{frequency}}$

length $\propto$ 1/frequency

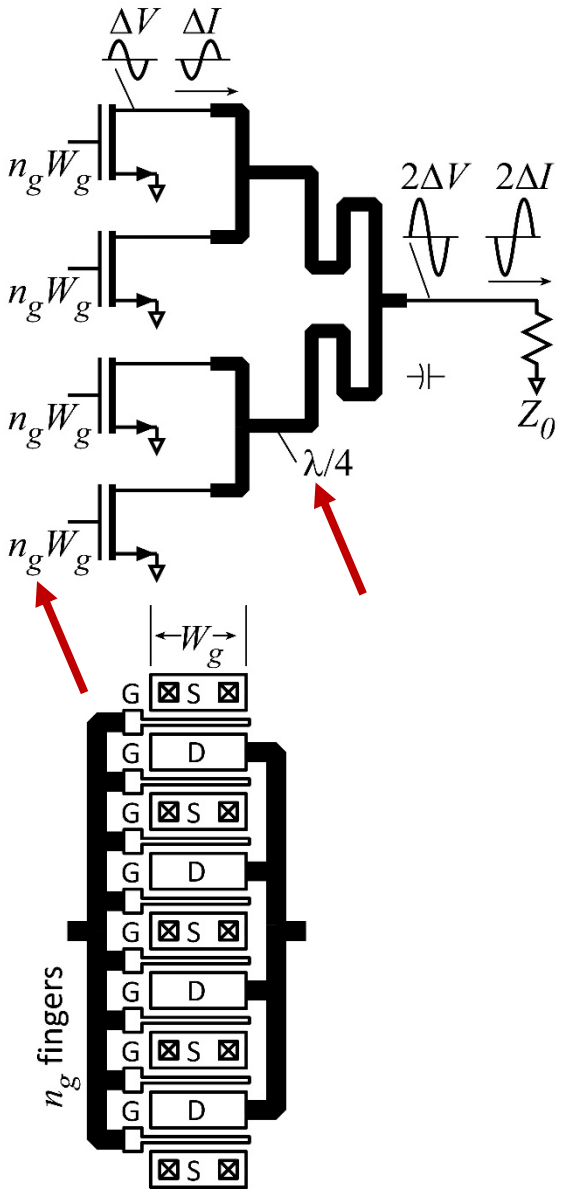
Big problem @ 10-100 GHz

No problem @ 100-300 GHz

Small # transistor fingers per cell

Not an advantage at @ 10-100 GHz

Big advantage at @ 100-300 GHz

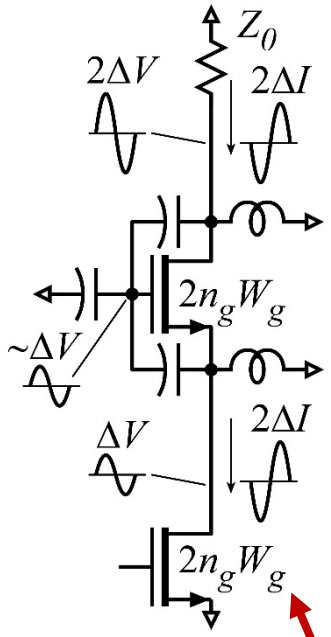


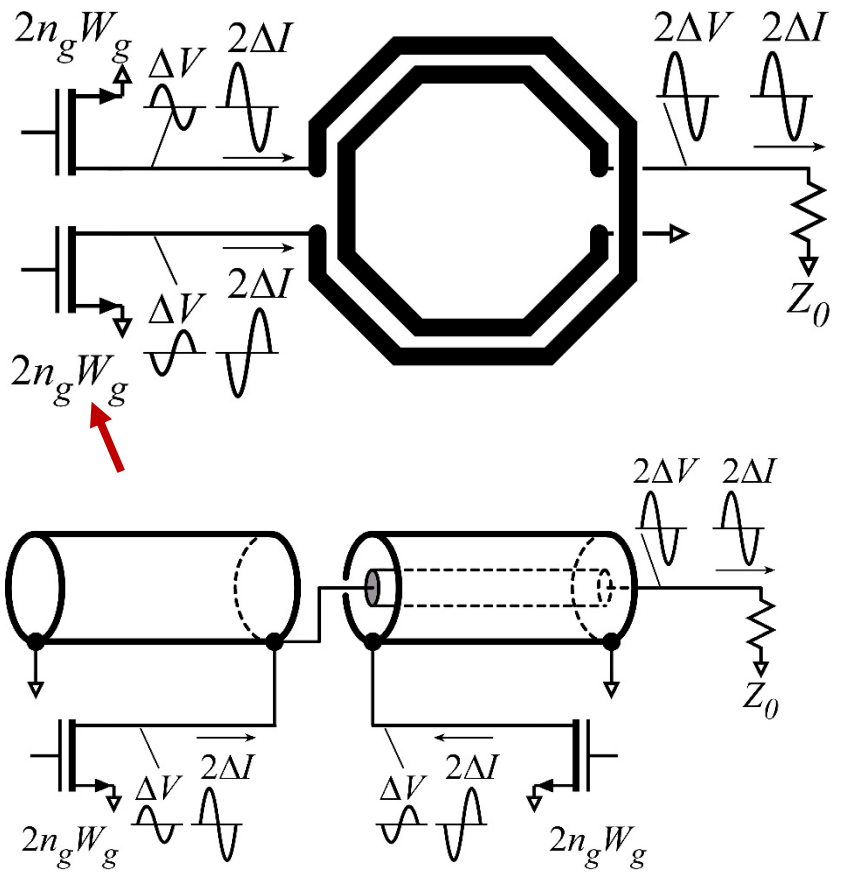
100-300 GHz: series combining often inferior

Compact power-combining networks

Big advantage at @ 10-100 GHz

Limited advantage at @ 100-300 GHz

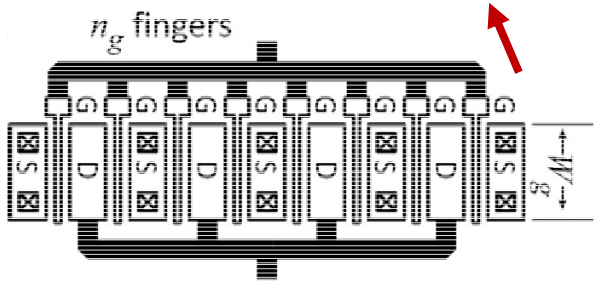




Large # transistor fingers per cell

No problem at @ 10-100 GHz

Significant disadvantage at @ 100-300 GHz



100-300 GHz: series combining often inferior

Transformer shown: same issues with stacking & baluns:

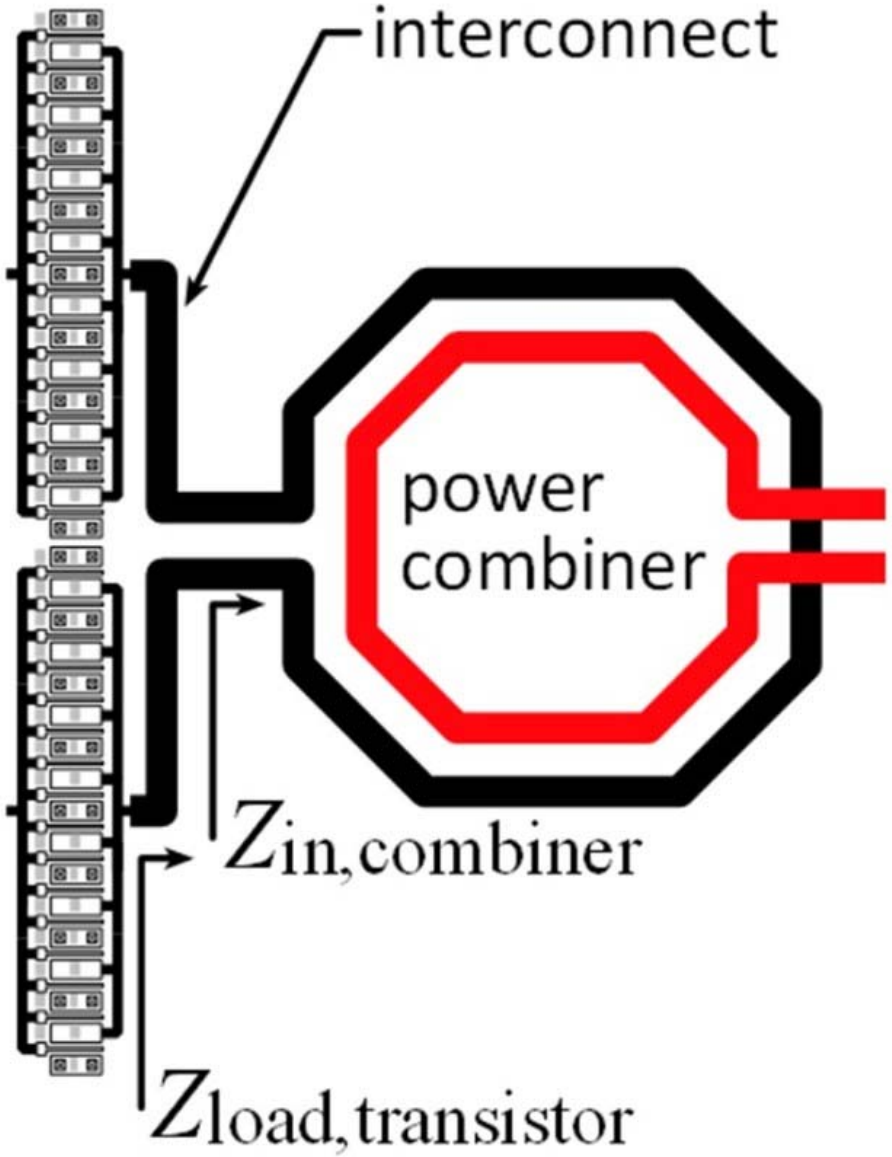
Many fingers per cell: big transistor footprint

Low impedances at combiner port

Impedance shift between transistor and combiner

Gets worse as combining ratio is increased

No problem at 10-100 GHz; big problem at 100-300 GHz



Coupled Lines vs. Transformers

Balun:

ports connected in series

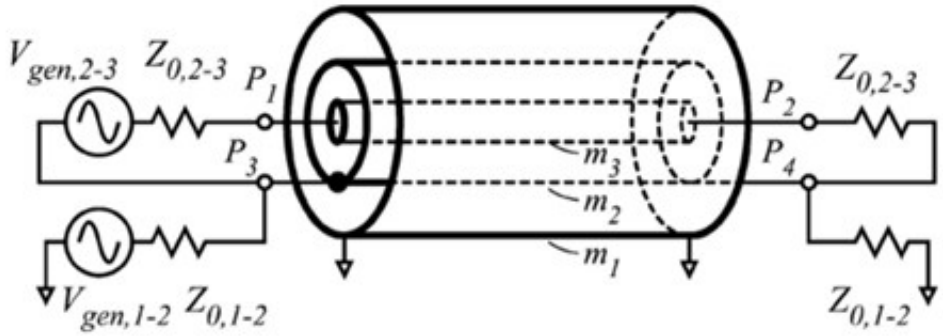
shunt loading by shorted stubs.

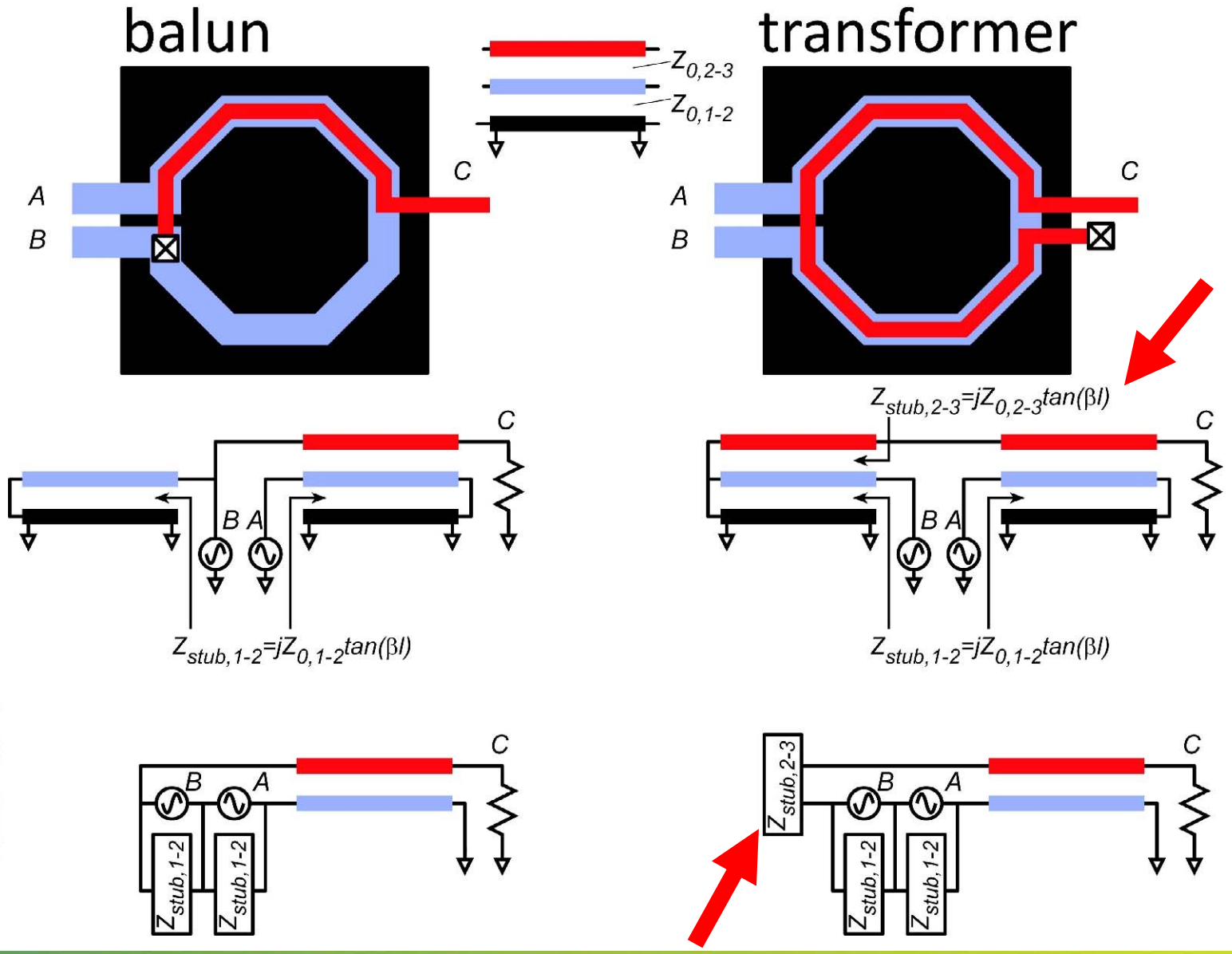
1:1 transformer:

ports connected in series

shunt loading by shorted stubs.

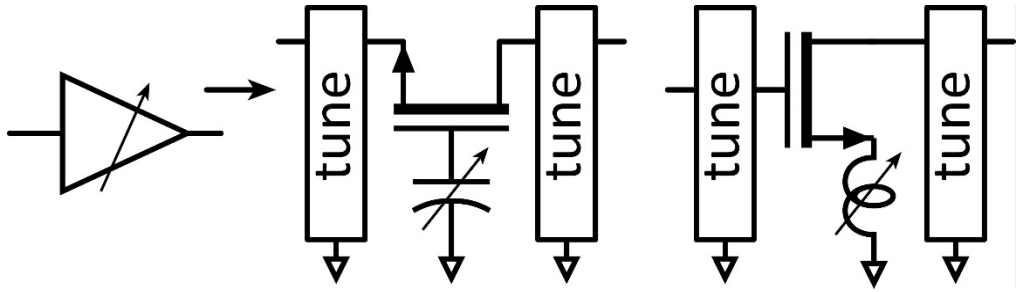
series loading by shorted stub

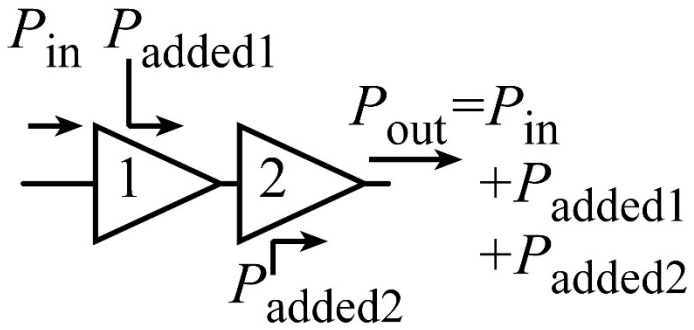




Cascade combining

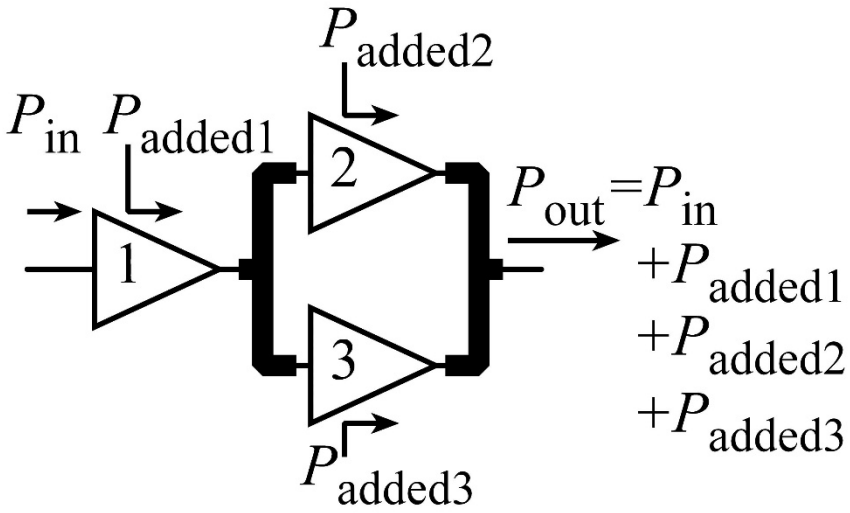
Reduced stage gain
- local negative feedback
- reactive, no loss in PAE
- reduces P_{out}/P_{in}.
- does not change (P_{out}-P_{in})
- → P_{out} increases





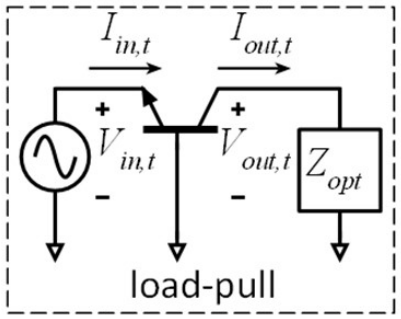
Requires higher-power driver stages

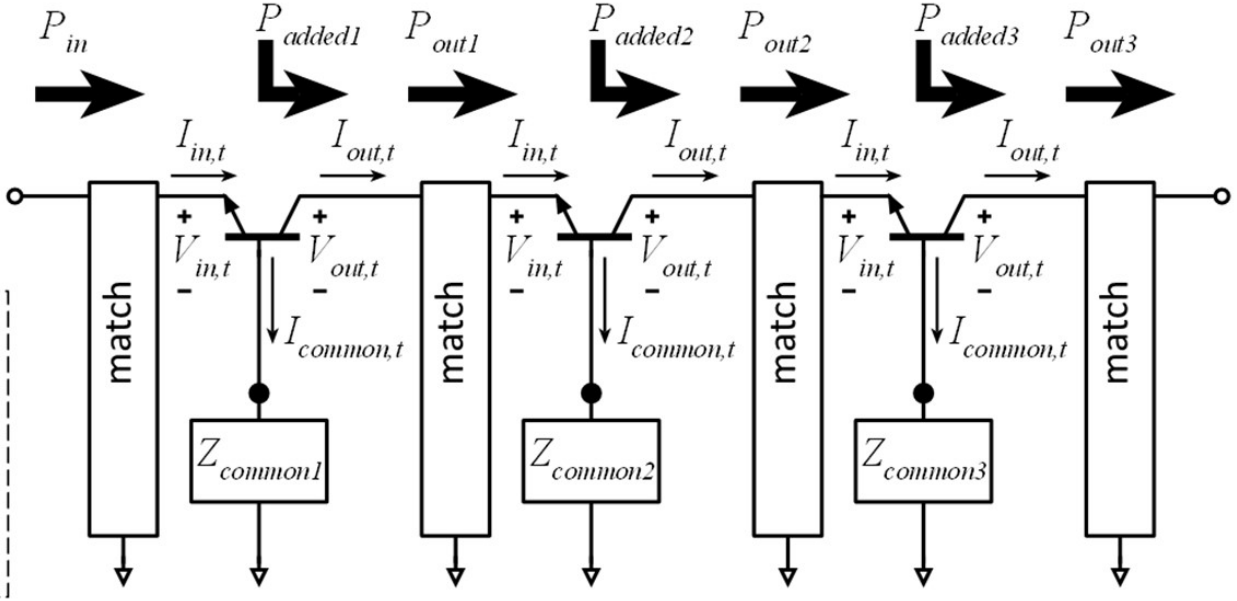
Driver power contributes to output power

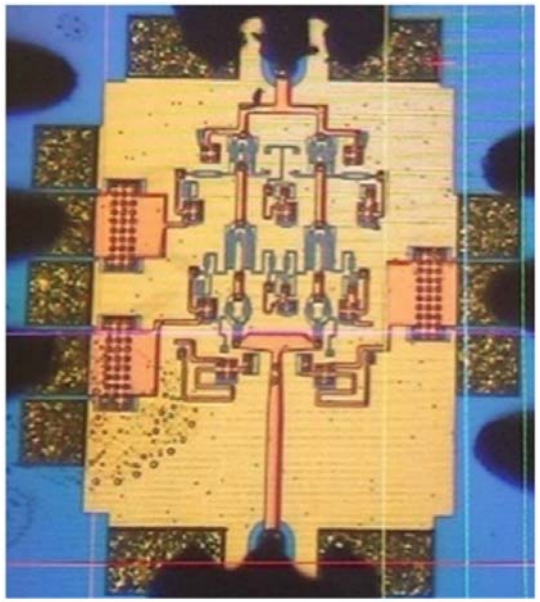


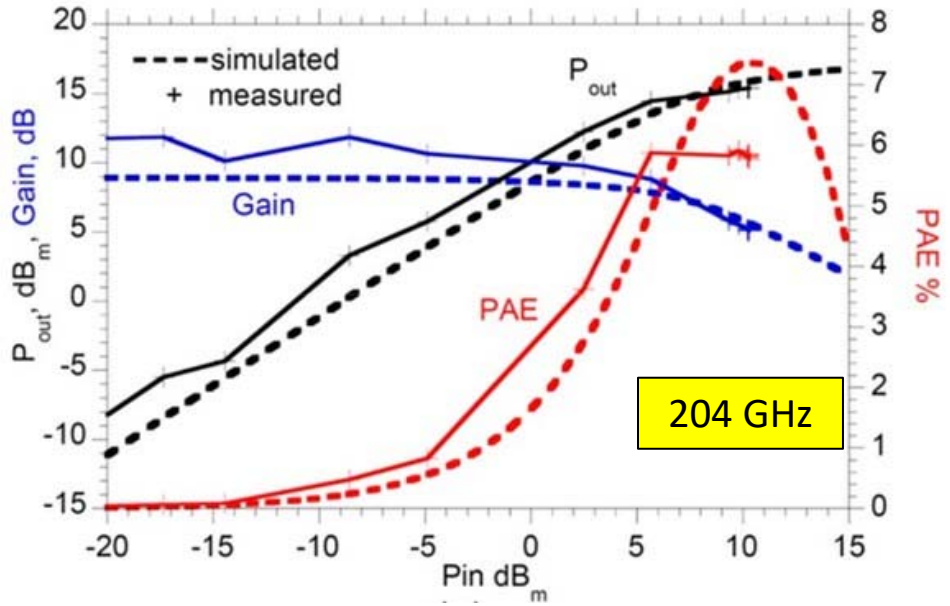
Cascade combining as stacking plus matching

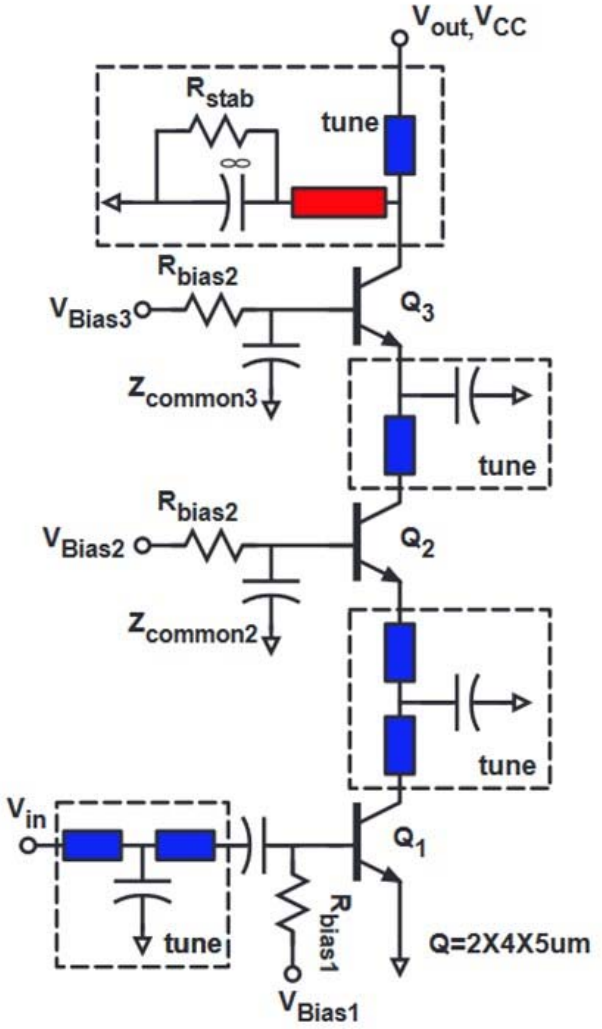
A. S. H. Ahmed et al.,
2018 EuMIC (UCSB)







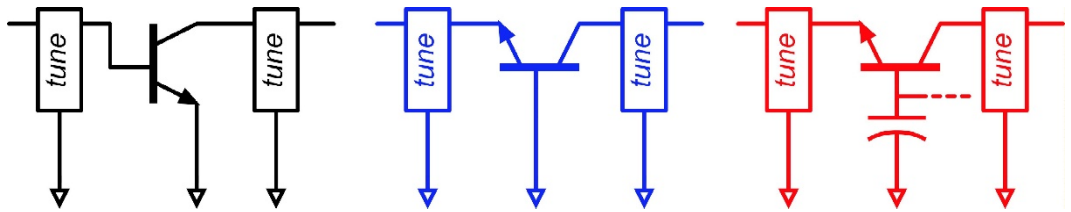


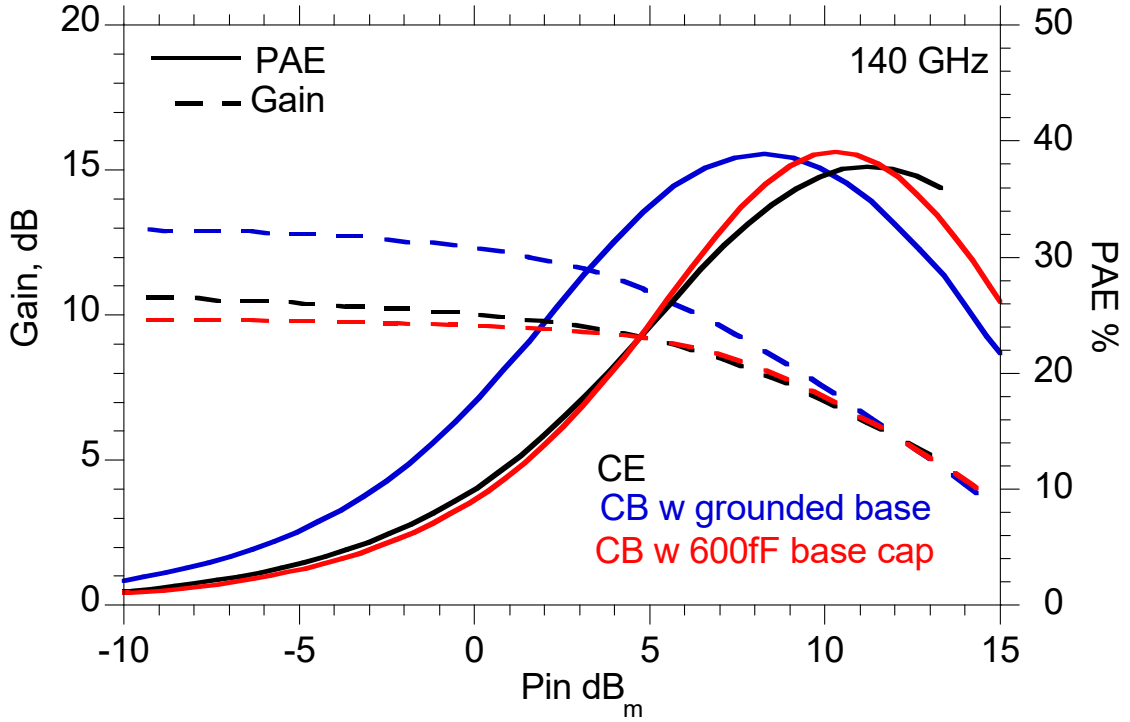


Also: A. S. H. Ahmed, "8.6-13.6 mW Series-Connected Power Amplifiers Designed at **325 GHz** Using 130 nm InP HBT Technology," *2018 IEEE BCICTS*

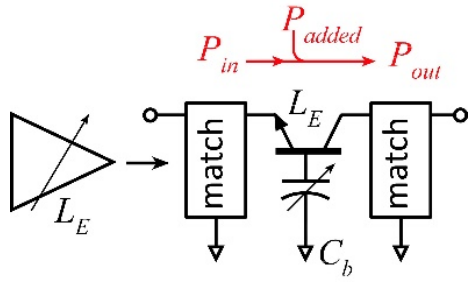
Capacitively degenerated common-base = cascade combining

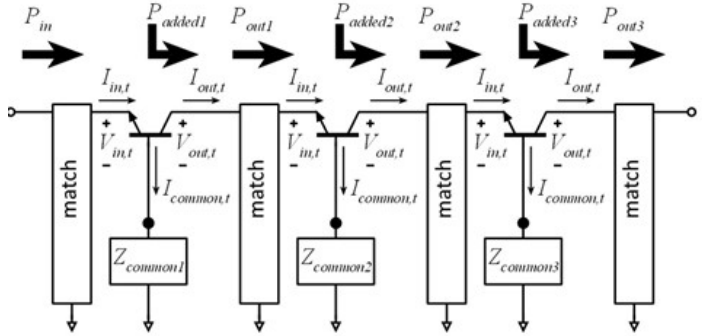
Lower gain, same peak PAE, higher PAE at P_{1dB}.

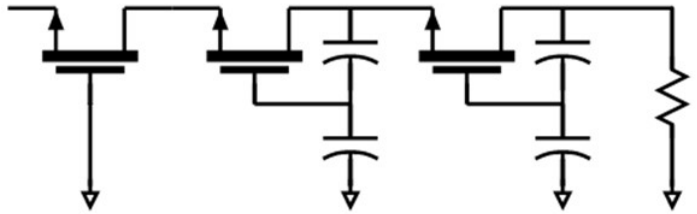


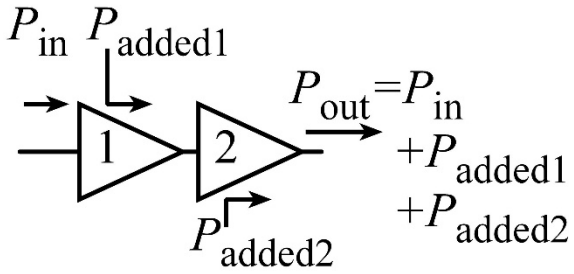


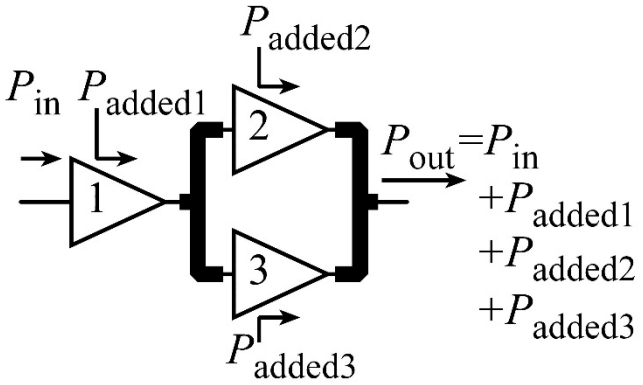
This is the same as a stack with internal matching











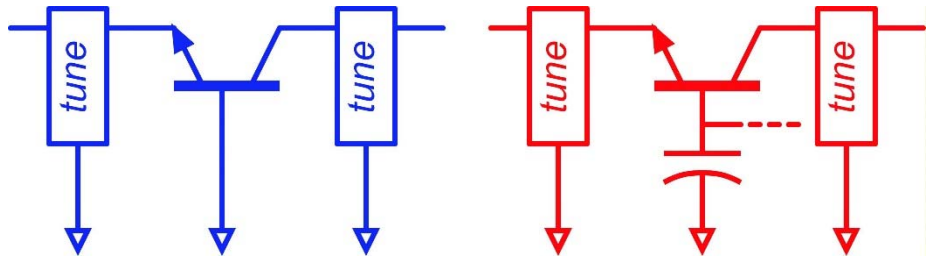
Capacitive degeneration: optimum gain

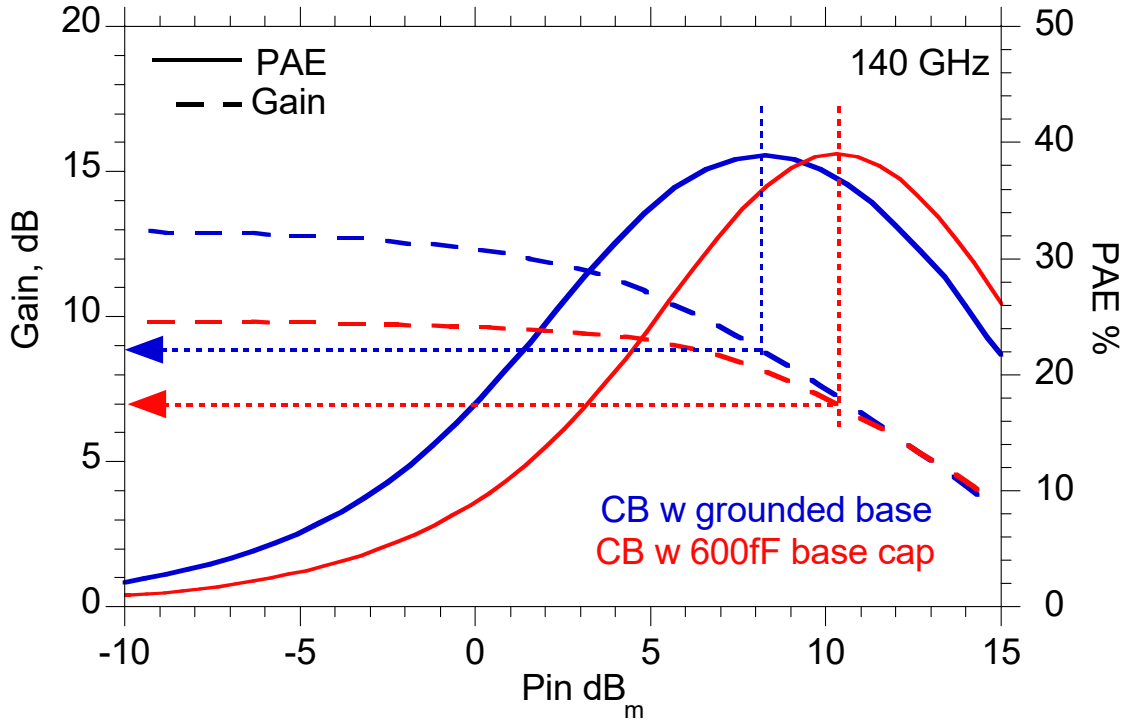
Capacitive degeneration:
no effect on peak PAE

No capacitive degeneration:
more gain compression @ P_{1dB}. ✗
more gain @ P_{1dB} ✓
input matching losses have less effect on PAE ✓

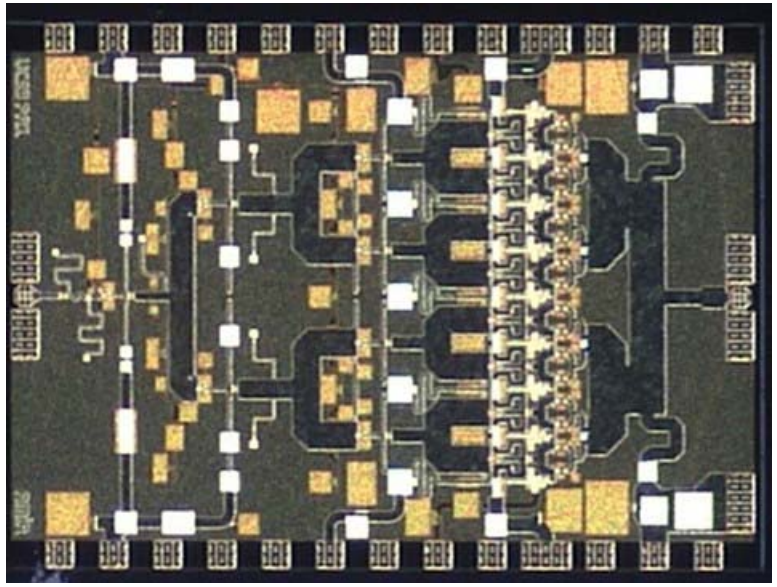
With capacitive degeneration:
less gain compression @ P_{1dB}. ✓
less gain @ P_{1dB} ✗
input matching losses have more effect on PAE ✗

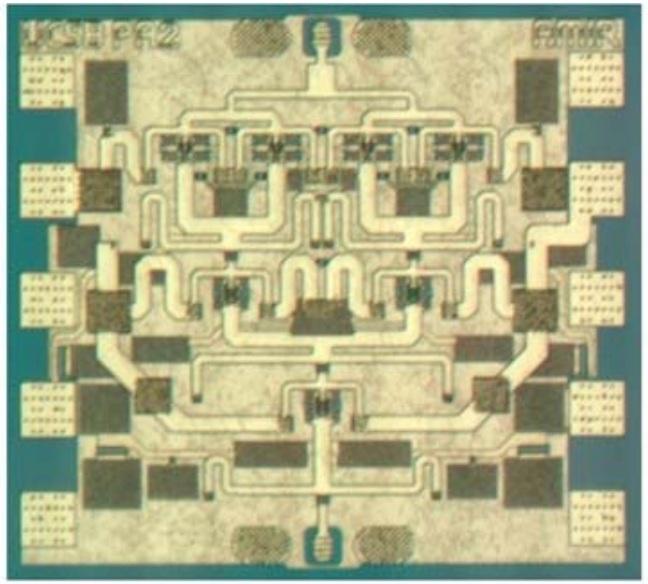
Design for greatest PAE @ P_{1dB}
balances these two considerations.





examples

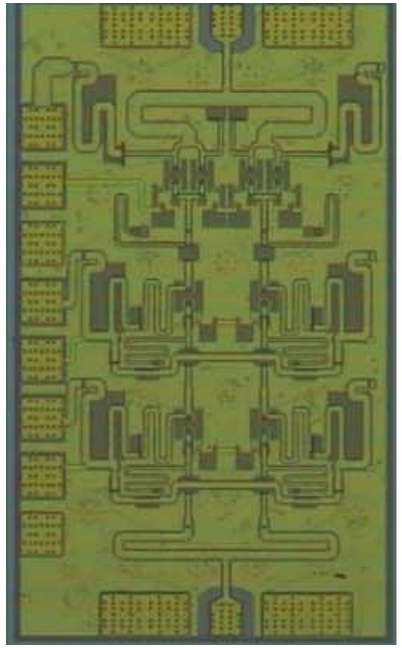


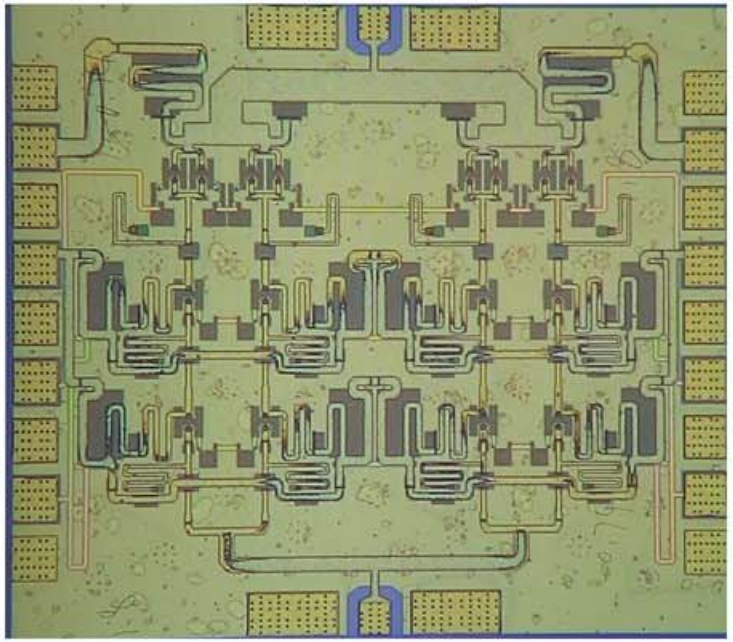


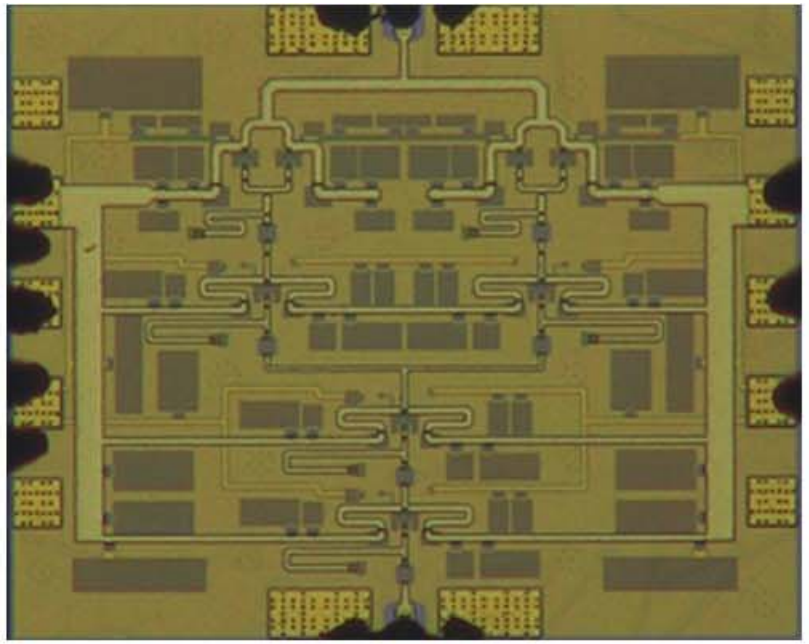
PAs with corporate & cascade combining

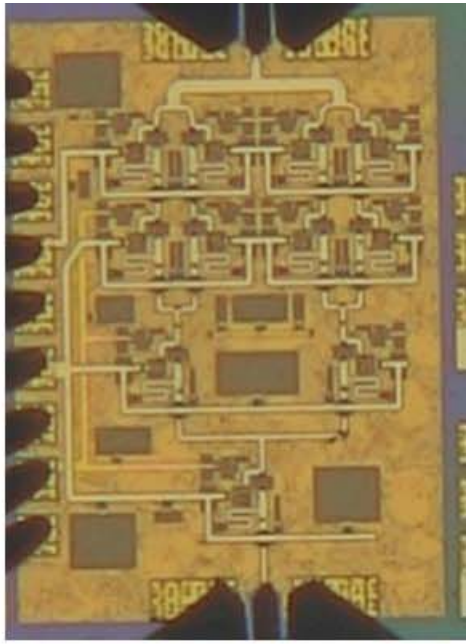
Teledyne 250nm InP HBT technology

Ahmed et al., 2020 IMS, 2020 EuMIC, 2021 IMS, 2021 RFIC

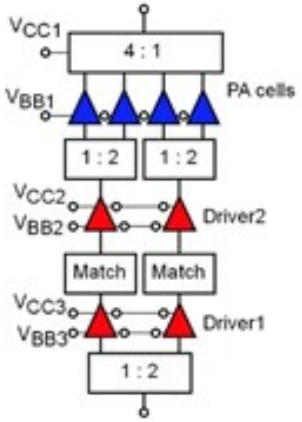




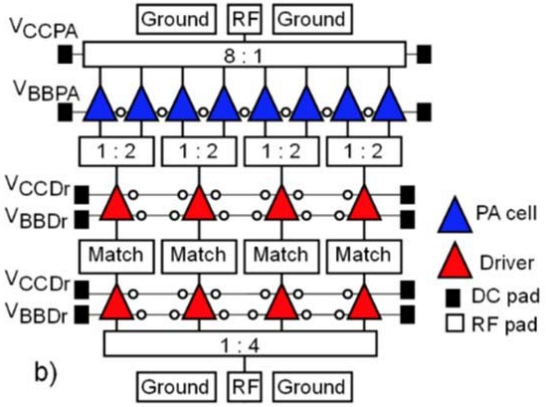




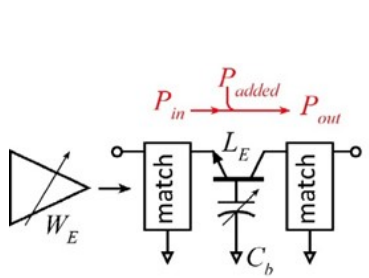
140GHz, 20.5dBm, 20.8% PAE

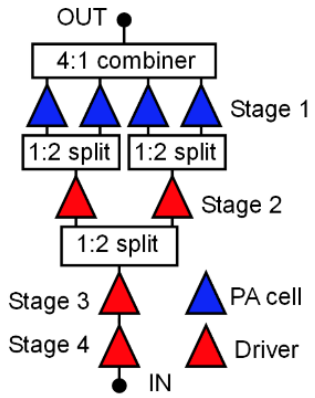


130GHz, 200mW, 17.8% PAE

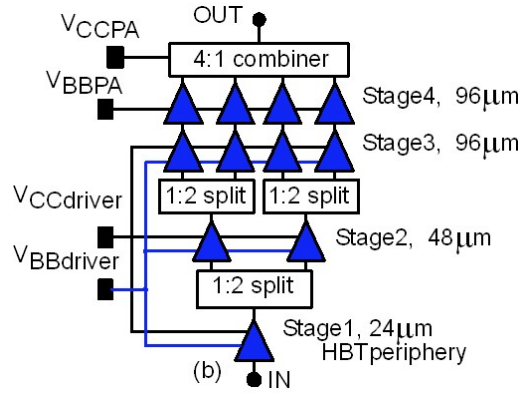


194GHz, 17.4dBm, 8.5% PAE





266GHz, 16.8dBm, 4.0% PAE



Class-B biasing of HBT power amplifiers

Class-B bias: $I_{C,DC} = \frac{I_{RF,peak}}{\pi} \propto \sqrt{P_{out}}$

Constant I_C or I_B bias:

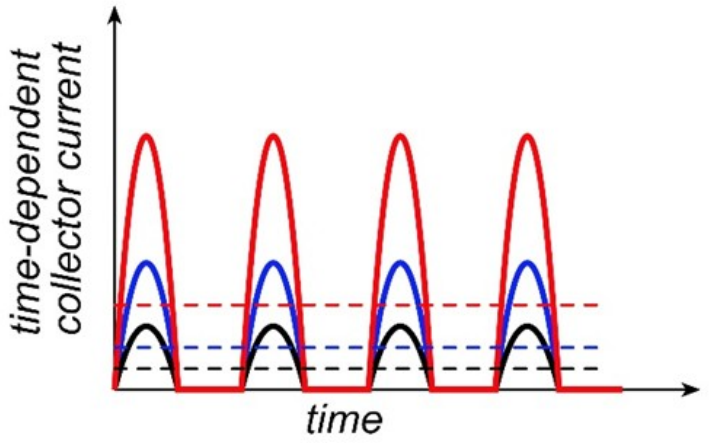
class B only at one RF power level

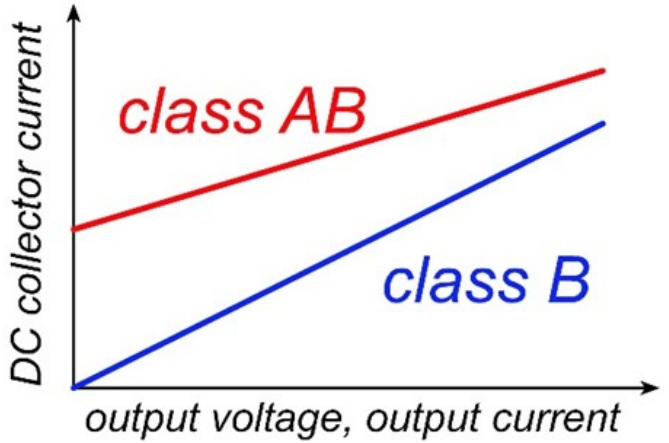
Constant-V_{be} bias:

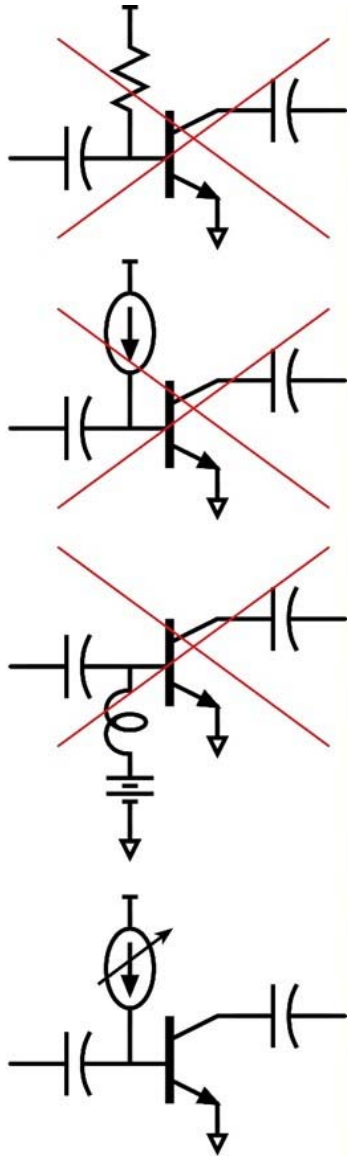
electrothermally unstable → destruction

Need adaptive bias circuit

I_C bias increasing in proportion to $\sqrt{P_{out}}$







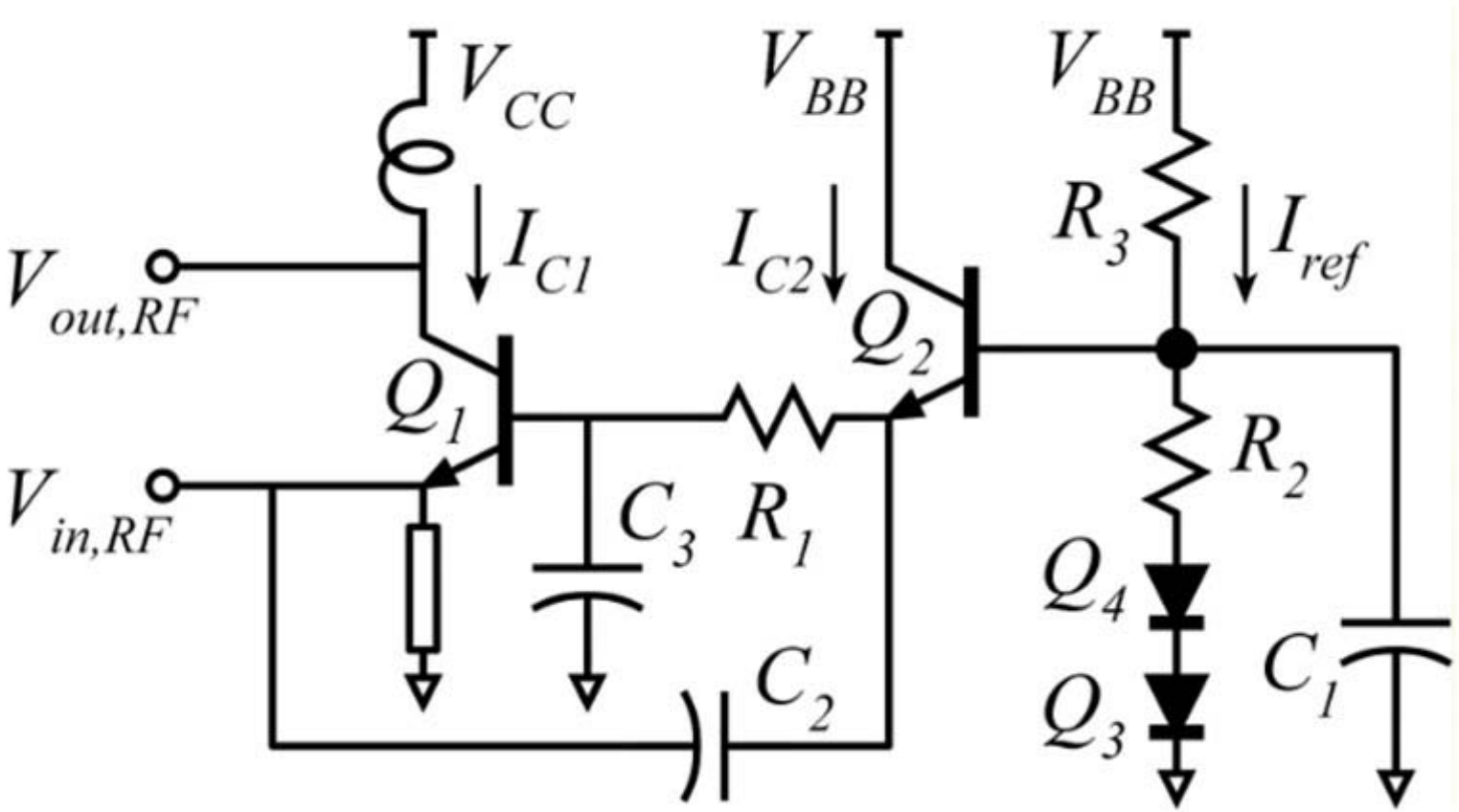
Common-base adaptive bias circuit

Q1: RF gain & adaptive bias
Q2: adaptive bias

Q1-4: current mirror; sets I_{c1}

RF drive:
V_{be1}, V_{be2} decrease
I_{c1} increases

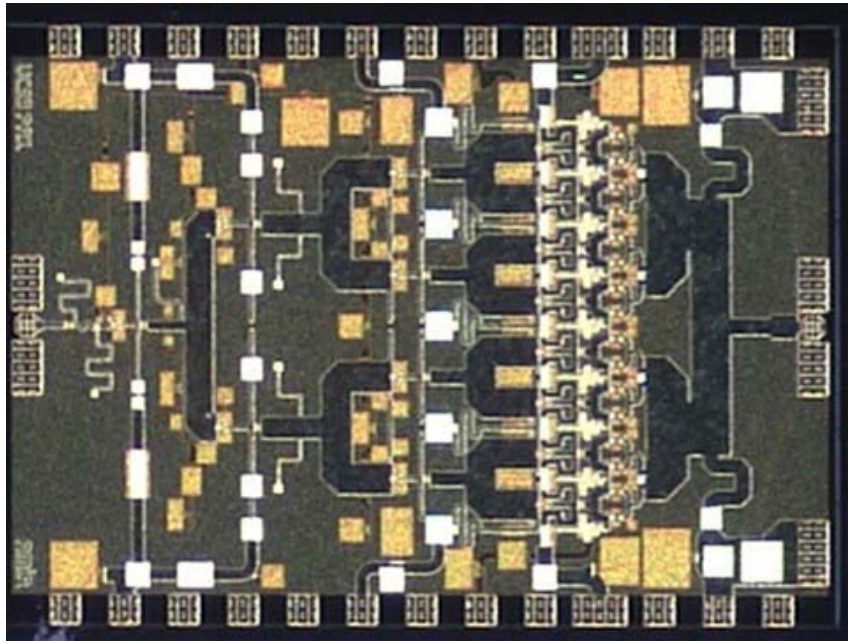
Why use Q2 for adaptive bias ?
More RF→ DC rectification
R_1 can be larger for given dI_{c1}/dP_{RF}
→ greater electrothermal stability

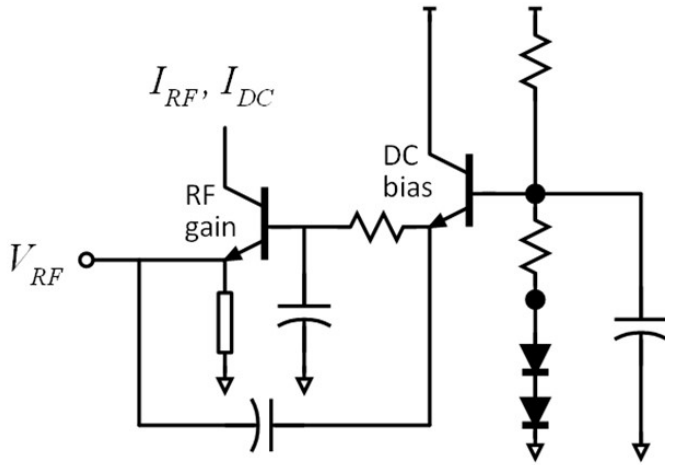


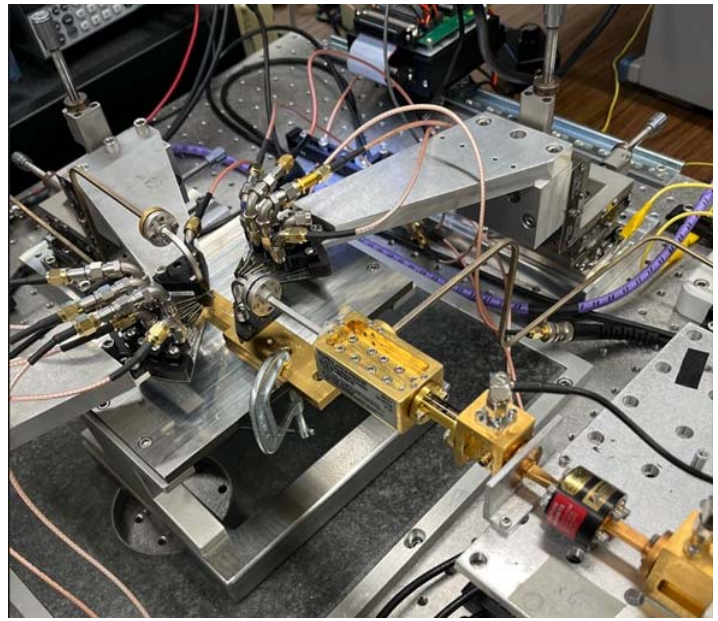
0.5 W, 150 GHz Power Amplifier: 250 nm InP HBT

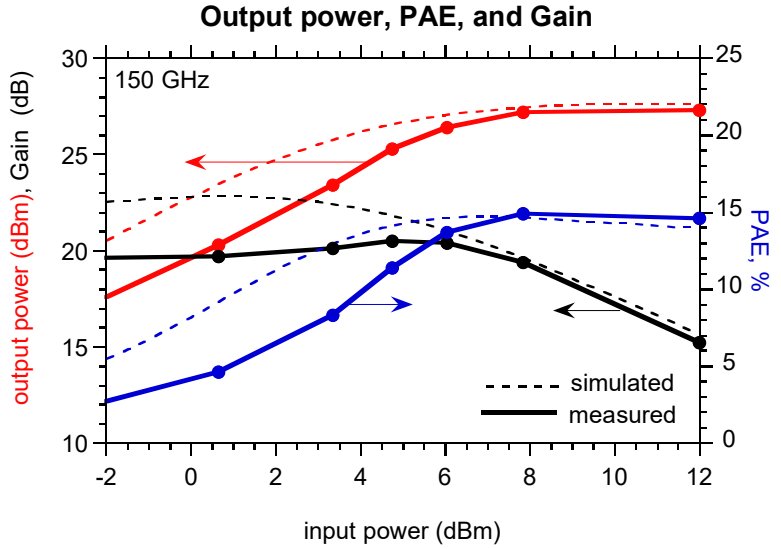
adaptive class-AB bias

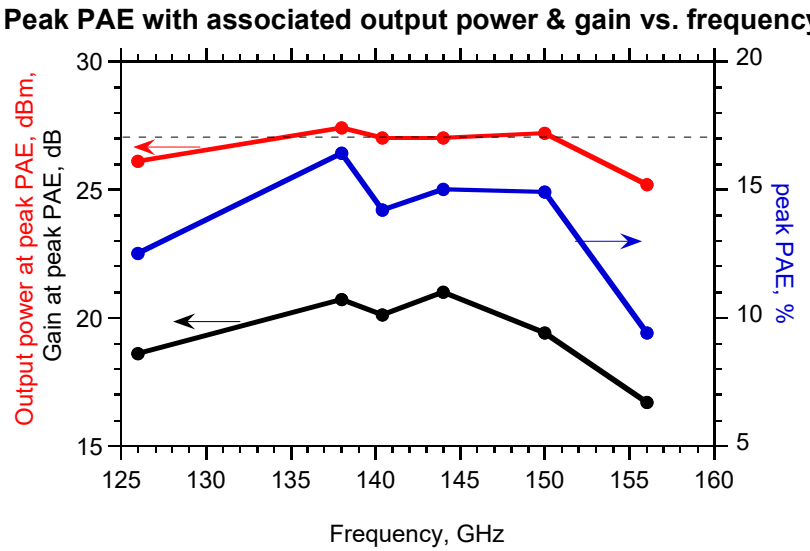
Alizadeh, 2023 IEEE BCICTS

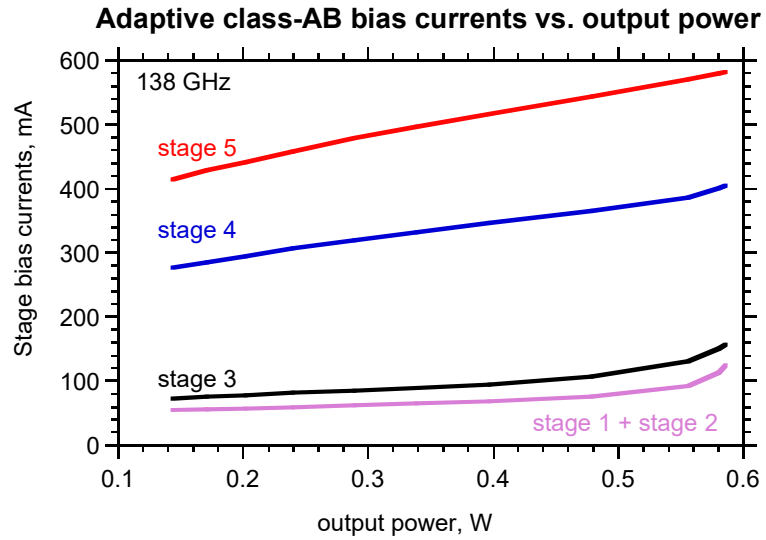








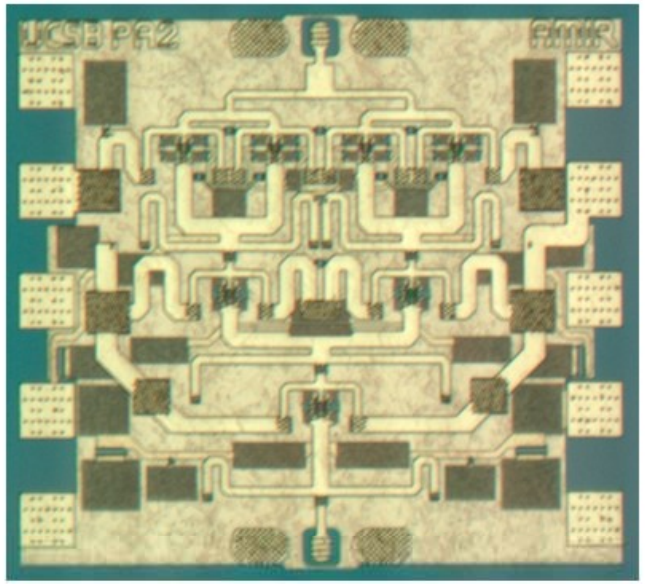




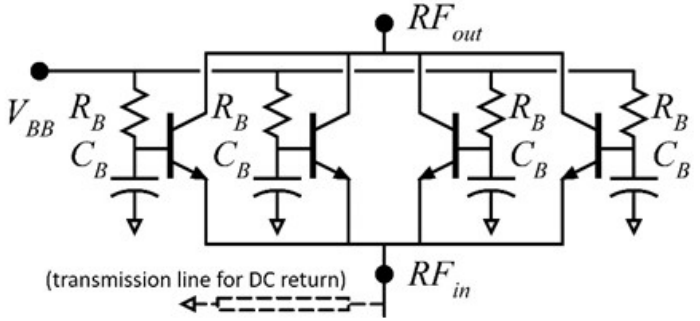
InP HBT Amplifier: 78 mW, 18.4% PAE, 220 GHz

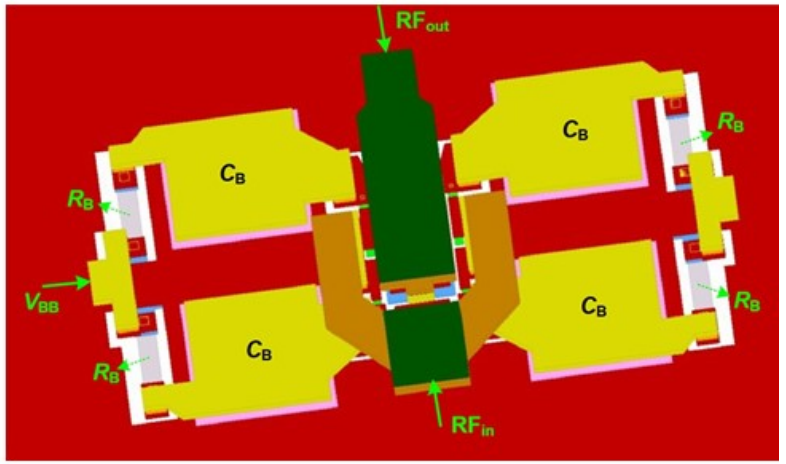
Alizadeh, 2023 IEEE MTT Trans

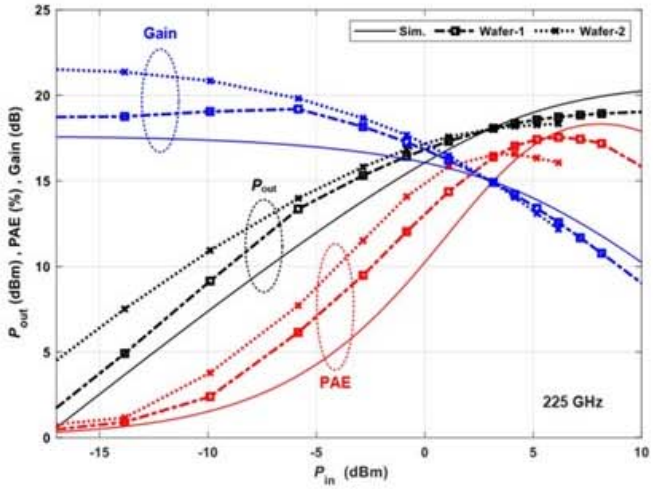
Teledyne 250 nm InP HBT (reduced base post)

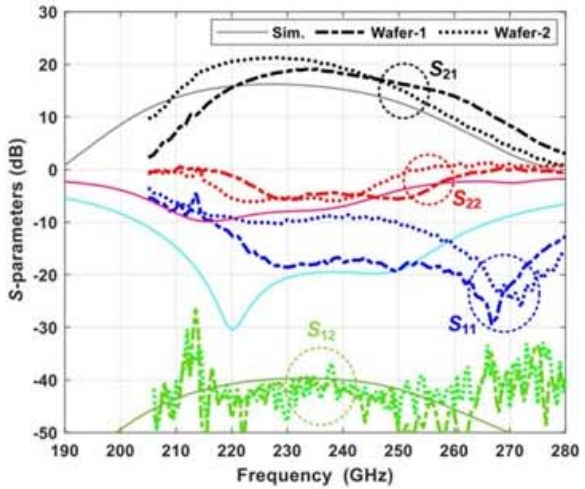


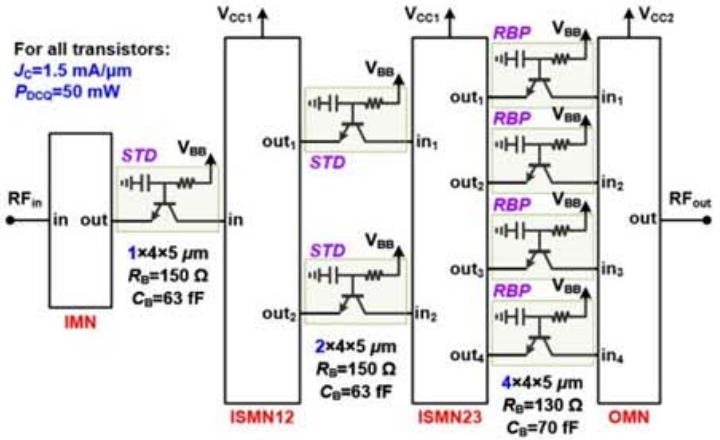
Thermally ballasted 4-finger common-base cell: increases maximum V_{ce}.











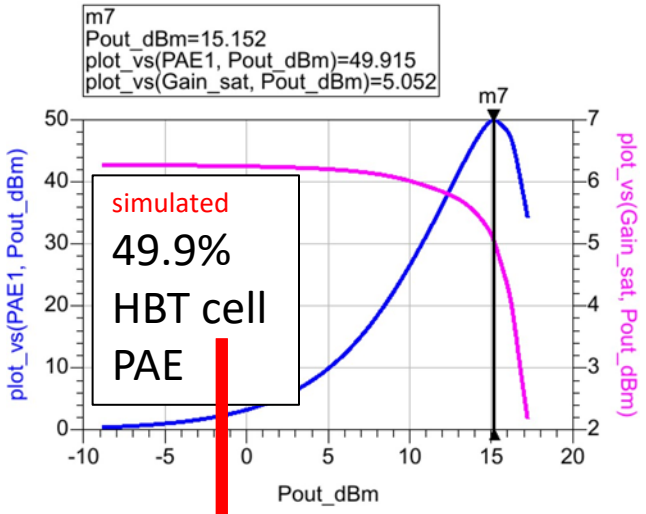
Key record result: Z. Griffith, 2024 IMS: 25% PAE, 16.7 dBm @ 220 GHz, 130 nm InP HBT

37%, 29%, 24% PAE is feasible @ 150, 220, 280 GHz

130 nm InP HBT technology

Design: Amirreza Alizadeh
Transistors, IC technology: Miguel Urteaga

150 GHz

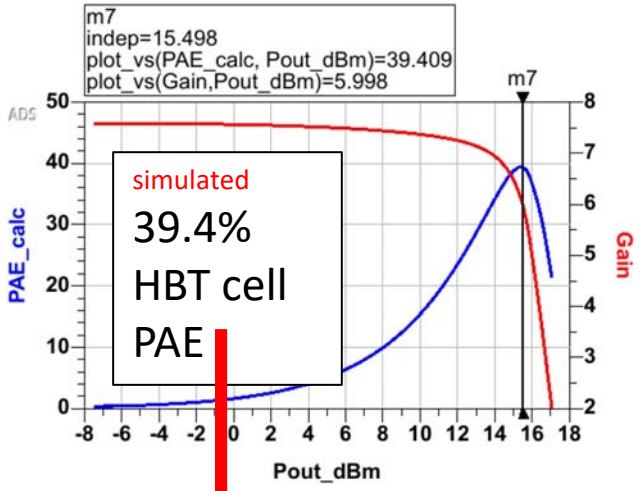


simulated
49.9%
HBT cell
PAE

estimated
Same passive
element losses ?

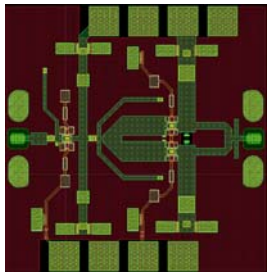
37.5 % amplifier PAE ?
(19 dBm design, estimated)

225 GHz



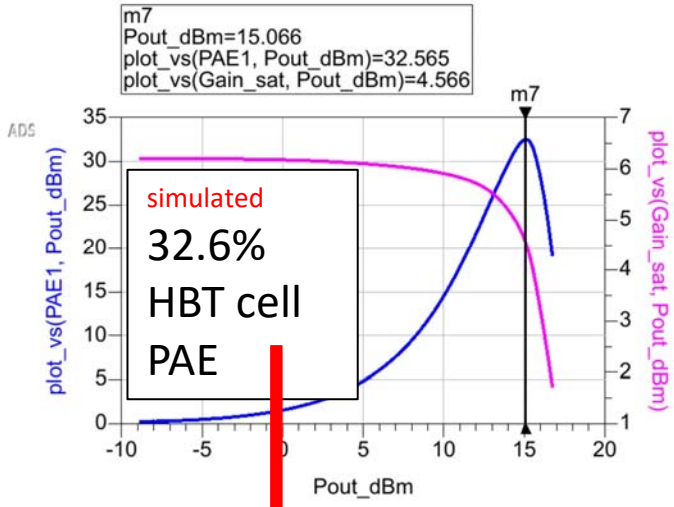
simulated
39.4%
HBT cell
PAE

simulated
9.9% PAE drop
HBT cell→ power amplifier



29.5% amplifier PAE
(19 dBm design, simulated)

280 GHz



simulated
32.6%
HBT cell
PAE

estimated
Same passive
element losses ?

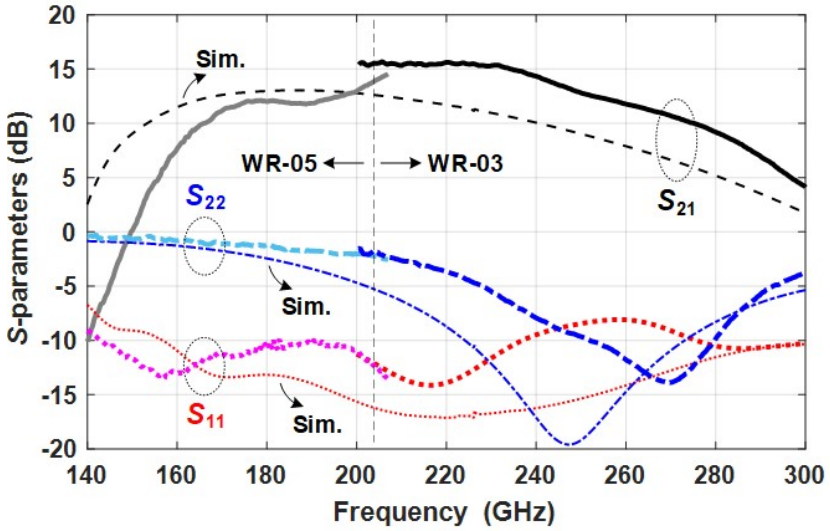
24.5% amplifier PAE ?
(19 dBm design, estimated)

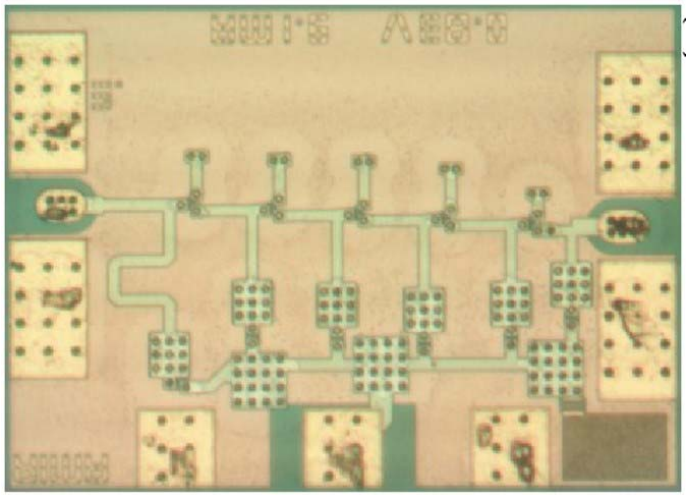
200 GHz LNA:130 nm InP HBT

Alizadeh, 2024 IEEE BCICTS

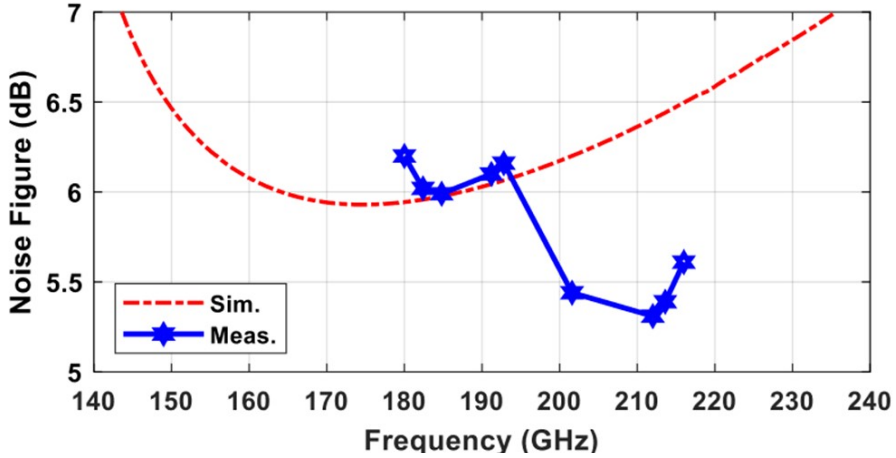
F = 6.3-5.5 dB over 180-217 GHz; record for bipolar transistor

$F_{cascade,LNA}$ = 6.4-5.6 dB, 7 mW DC power .

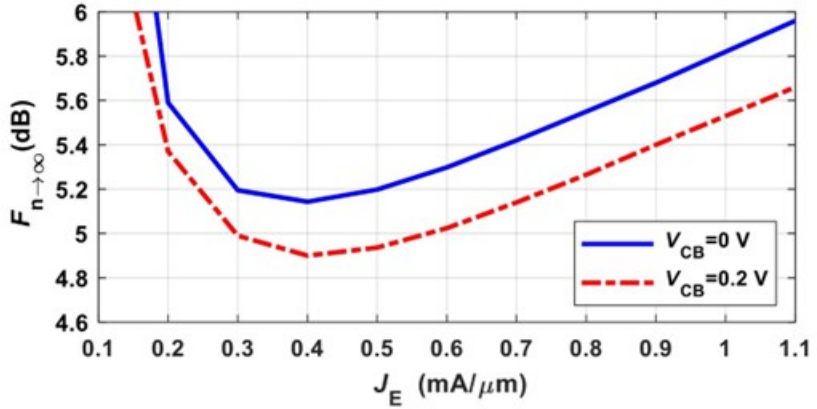


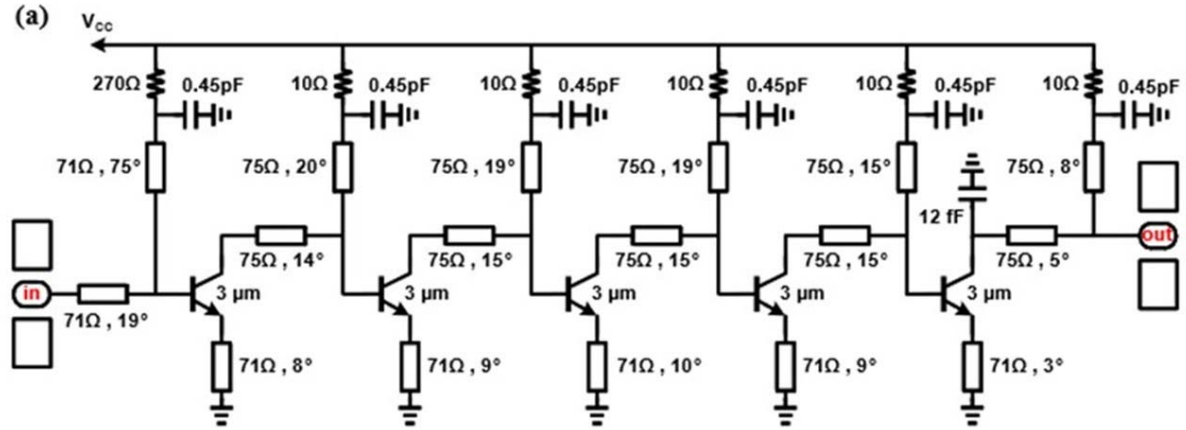


~5.5-6 dB LNA noise @ 200 GHz



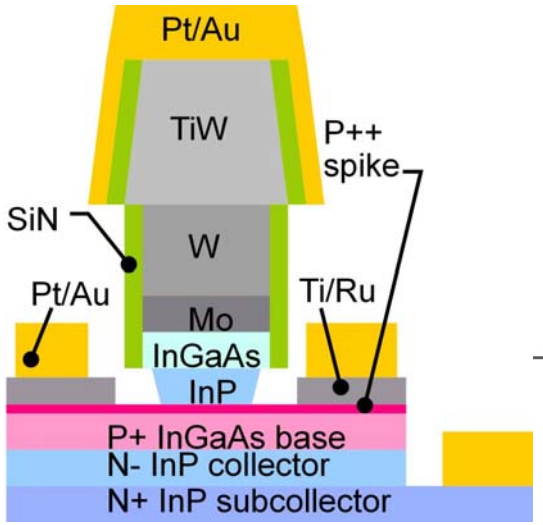
4.9-5.2 dB minimum transistor $F_{cascade}$

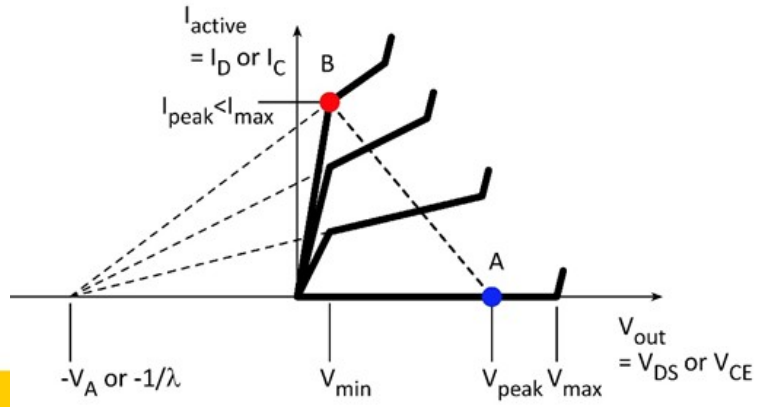


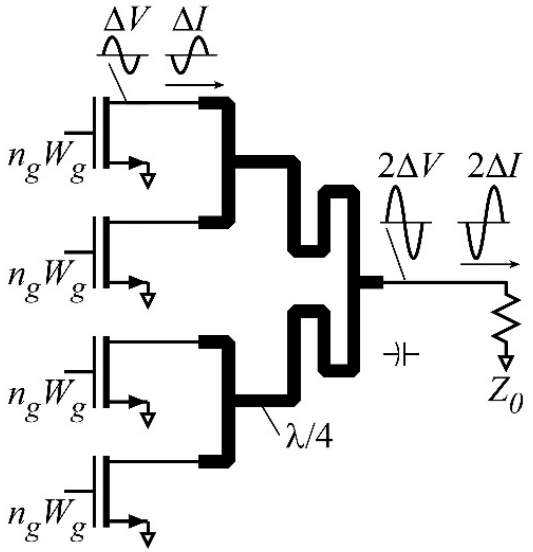


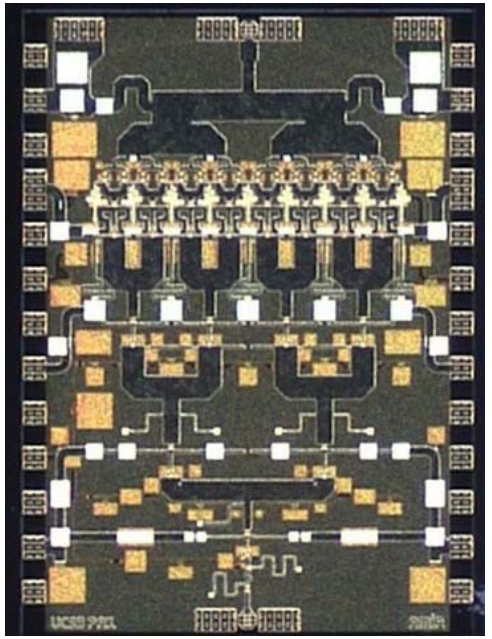
$F_{LNA,\ cascade}$ ~ F_{LNA} +0.15 dB=5.6-6.1 dB given that G_{LNA}=15 dB

100-300 GHz Power Amplifiers









100-300 GHz Power Amplifiers

Power amplifier performance limited by transistor: PAE invariance

Design: pick topologies to minimize passive element loss.

Corporate combining is compact and low-loss

Series techniques at best moderately helpful (may be more compact)

Transistors: more mA/μm→ fewer fingers

less parasitics, better transistor performance.

smaller footprint, better circuit performance

Transistors need high V_{br} and high mA/μm

if not, layout problems

if not, either can't use full V_{br} or can't benefit from f_{max}.

Better transistors make better power amplifiers

End

R_{ce}, R_{ds} can't be part of power transistor model

Transistor output characteristics look like the upper plot, not like the lower plot.

→ model cannot include R_{DS} or R_{CE}