D-Band Adaptively Biased 16-Way-Combined Half-Watt Power Amplifier in 250-nm InP HBT

Amirreza Alizadeh, *Member, IEEE*, Utku Soylu, *Graduate Student Member, IEEE*, Navneet Sharma, Gary Xu, *Member, IEEE*, and Mark J. W. Rodwell, *Fellow, IEEE*

***Abstract*— We present a *D*-band power amplifier (PA), implemented in Teledyne (TSC)-250-nm indium phosphide (InP) technology, that produces record 27.2-dBm output power and 14.9% associated power-added efficiency (PAE) at 150 GHz. The measured saturated output power and PAE exceed 26 dBm and 12.5% over 126–150 GHz. The output stage power combines sixteen common-base (CB) cells, each having a total emitter length of 24 μm. Each power cell is independently biased by an adaptive bias network (ABN) that prevents thermal runaway and increases bias currents with increased RF power to delay the gain compression. The PA occupies 3 mm^2 of the die area. To the authors' knowledge, this work achieves the highest output power among *D*-band PAs implemented in any technology.**

***Index Terms*— Adaptive bias network (ABN), analog predistortion, *D*-band, indium phosphide (InP) heterojunction bipolar transistor (HBT), power amplifiers (PAs), thermal compensation.**

I. Introduction

THE large available unlicensed bandwidth at a waveguide *D*-band (110–170 GHz) makes it an attractive candidate for several applications, including high-resolution radars, spectroscopy, and broadband communication systems. Considering high atmospheric attenuation and high λ^2/R^2 path losses at the *D*-band, the communication range is heavily dependent on the ability of the user to generate RF power by power amplifiers (PAs). Nonetheless, because active devices have a poorer efficiency at the *D*-band than at sub-100-GHz frequencies, larger RF power directly translates to higher dissipated dc power and hence excessive heat in the system, posing reliability issues and performance degradation.

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Amirreza Alizadeh was with the Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA 93117 USA. He is now with Keysight Technologies, Santa Rosa, CA 95403 USA (e-mail: alizadeh_amirreza@yahoo.com).

Utku Soylu was with the Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA 93117 USA. He is now with IBM Research Center, Yorktown Heights, NY 10598 USA.

Navneet Sharma and Gary Xu are with Samsung Research America, Plano, TX 75023 USA.

Mark J. W. Rodwell is with the Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA 93117 USA.

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Overheating in PAs can cause multiple issues, including reduced performance, shortened lifespan, mechanical stress, and even complete failure and device destruction. While heat buildup can be reduced by employing heat sinks, fans, or other cooling mechanisms, the PA should be designed to maximize the power added efficiency (PAE) for a given output power (P_{out}) level. This strategy reduces dc power dissipation and dispersed heat. Still, it is not enough to ensure the reliable operation of the PA, unless the designer optimizes the PA layout to prevent thermal runaway, current hogging, and electromigration.

In the *D*-band, *n*-way-combined bulk and SOI CMOS PAs, due to the low breakdown voltage of the transistors, are yet to exceed the 20-dBm barrier [1], [2], [3], [4]. GaN HEMTs offer superior power density below 100 GHz, but their efficiency drops above 100 GHz [5], [6], [7]. The benchmark result for GaN PAs has been presented in [7], reporting P_{out} of 100 mW with 10.6% PAE at 132 GHz. SiGe HBT PAs have shown better performance compared to their counterparts in CMOS and GaN HEMTs [8], [9], [10], [11], showcasing record 22.4-dBm P_{out} and 16.1% PAE at 130 GHz [10], [11]. Indium phosphide (InP) heterojunction bipolar transistor (HBT) has a higher breakdown voltage and superior f_{max} compared to SiGe HBT [12] and thus has been more popular for implementing *D*-band PAs [13], [14], [15], [16]. Among the *D*-band InP PAs reported in the literature, [17] has achieved the highest output power of 24 dBm with 7% PAE at 140 GHz. On the other hand, [18] has reported a two-stage PA, demonstrating P_{out} of 19.2 dBm and PAE of 30.4% at 138 GHz.

This work is the extension of [19] and describes the design procedure for a 16-way-combined *D*-band PA in the Teledyne 250-nm InP HBT process (TSC250). Each RF transistor in the PA is biased by a separate adaptive bias network (ABN), located next to each RF transistor. The ABN adjusts the bias current of the RF transistor as a function of the input RF power and therefore reduces gain compression. The ABN also senses the temperature at the proximity of the RF transistor and compensates for the thermal-induced current changes, preventing thermal runaway and providing electrothermal stability. This enables the implementation of a PA that produces a record 27.2-dBm output power with 14.9% associated PAE at 150 GHz. The measured saturated output power (P_{sat}) exceeds 26 dBm over 126–150 GHz. To the authors' knowledge, the PA presented in this work

achieves the highest reported output power among *D*-band PAs implemented in any technology.

The rest of this article is structured as follows. In Section II, we discuss device selection and layout. Section III explains the ABN function. Circuit design is covered in Section IV. The measurement results are provided in Section V, and finally, Section VI offers a summary of this article.

II. Device Selection and Layout in TSC250

Teledyne's 250-nm InP HBT technology provides transistors with a nominal collector-emitter breakdown voltage (BVCEO) of 4.5 V and emitter lengths (L_E) varying from 3 to 12 μm. Since the foundry transistor model includes interconnect parasitics up to the METAL1 (M1) layer, stacked vias are required to bring the reference planes to the top metal layer (M4), which is the layer used for realizing most of the microstrip transmission lines (TLs) in the matching networks.

With M4 reference planes, a 6-μm device in the common-emitter (CE) configuration, when biased at $V_{CE} = 2.5$ V and quiescent collector current density (J_{CQ}) of 0.83 mA/μm, generates a P_{out} of 10.3 dBm at 150 GHz with 5.3-dB gain and 40% PAE at the 2-dB compression point. f_{max} of this device is 525 GHz. At the same tone frequency and under the same bias conditions, a 12-μm CE stage provides P_{out} of 13.2 dBm at the 2-dB compression point, but with an inferior PAE of 33.6% and a gain of 4.1 dB due to its much lower f_{max} of 400 GHz. Simulations of the 8- and 10-μm devices also showed reduced gain and PAE compared to the 6-μm device. The 3-, 4-, and 5-μm transistors have a higher f_{max} than the 6-μm device when the reference plane is at M1. However, with M4 reference planes, stacked-via parasitic effects limit the f_{max} of these devices to ≈525 GHz, leaving no improvement over the performance of the 6-μm transistor. Therefore, the 6-μm device offers the best compromise between gain, P_{out}, and PAE and is used in the last stage of the PA where higher PAE is critical for reducing heat and improving the reliability.

The target P_{out} for the PA in this work is 27 dBm at the *D*-band; hence, at least sixty-four unit 6-μm transistors should be power-combined. Thus, we first build a compact four-finger 24-μm device by power-combining four 6-μm devices and then power-combine sixteen of them using a 16-way power combiner to achieve half a watt. Fig. 1 presents the layout of a four-finger 24-μm (4 × 6 μm) transistor in the CE and common-base (CB) topologies, where M1 is the reference ground plane. Interconnects between the four 6-μm fingers in each four-finger transistor were EM-simulated using Keysight RFpro to characterize their parasitic effect.

Fig. 2 shows the maximum available\stable gain (G_{ma}\$G_{ms}$) of a 4 × 6 μm transistor in the CE and CB configurations along with G_{ma}\$G_{ms}$ of a single-finger 6-μm transistor in the CE topology. All three devices were EM-simulated to include the effect of interconnect parasitics up to the top-level metal (M4). In the simulations, J_{CQ} is 0.83 mA/μm and V_{CE} = 2.5 V. For both CE and CB topologies, the 24-μm transistor features an f_{max} of about 468 GHz, which is slightly smaller than the f_{max} of a 6-μm CE device, that is, 525 GHz. Since the

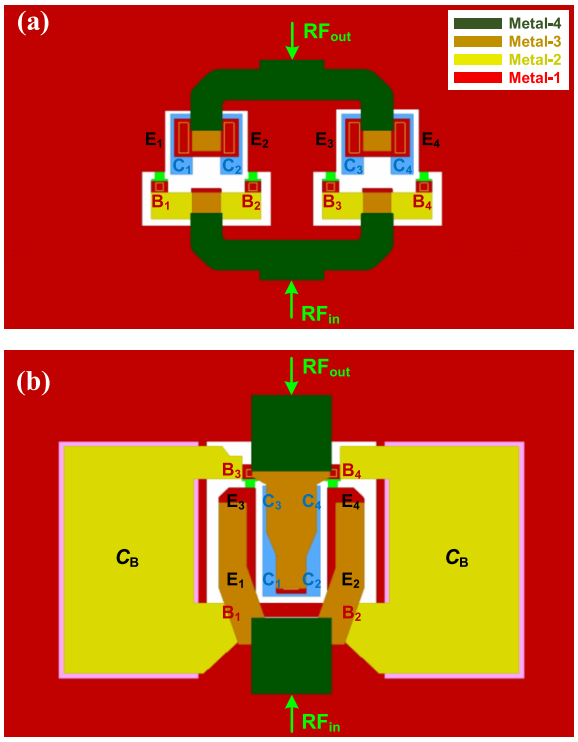

Fig. 1. Layout of a 4 × 6 μm transistor in (a) CE and (b) CB topologies ($C_B \approx 115$ fF).

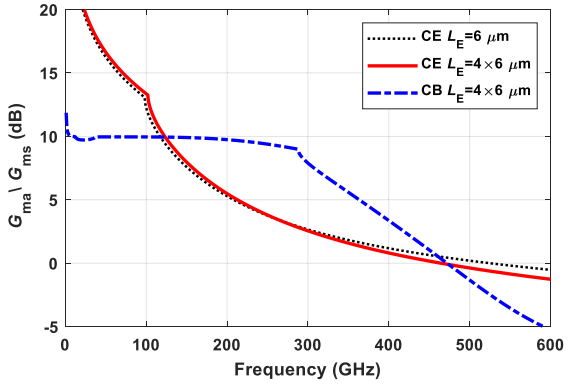

Fig. 2. Maximum available\stable gain (G_{ma}\$G_{ms}$) of the 4 × 6 μm devices of Fig. 1 as well as G_{ma}\$G_{ms}$ of a single-finger 6-μm device in the CE topology. All interconnect parasitics up to top the level metal (M4) were included in the electromagnetic simulations. For all devices, $V_{CC} = 2.5$ V and $J_{CQ} = 0.83$ mA/μm.

CB topology provides a higher G_{ma} than the CE stage around 150 GHz, the PA in this work uses CB structure in all its five stages.

It is worth mentioning that the maximum gain and stability of the CB device are dependent on the value of the degeneration capacitor, C_B, and J_{CQ}. Fig. 3(a) presents the μ-factor versus C_B of a 24-μm CB device at 150 GHz for various J_{CQ} values. As C_B or J_{CQ} increases, the device provides a higher gain, but at the cost of lower μ-factor and potential instability. Our design employs $C_B \leq 115$ fF capacitors, resulting in $\mu \geq 0.99$ for all J_{CQ} values. Fig. 3(b) depicts μ-factor versus frequency of the 24-μm CB device [see Fig. 1(b)] at different bias levels for $C_B = 115$ fF.

The device will achieve unconditionally stability once connected to passive matching networks, which are lossy (≈1.5 dB at 150 GHz) and provide significant out-of-band

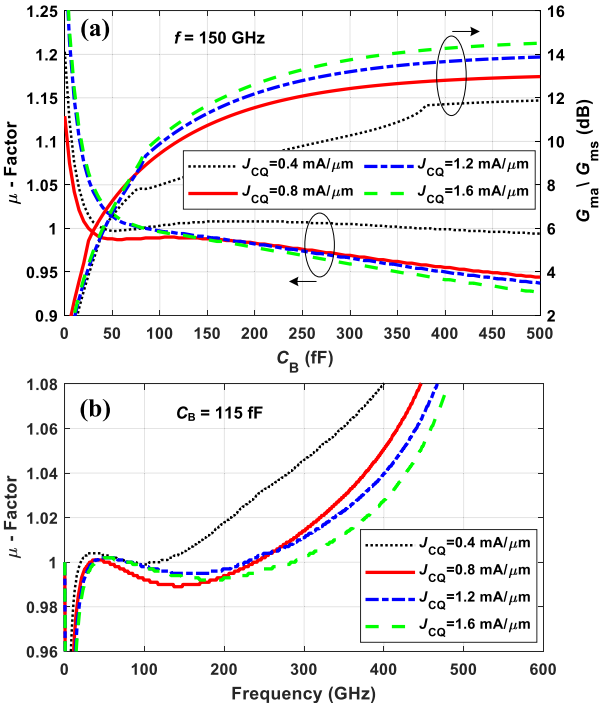

Fig. 3. (a) μ-factor and $G_{\rm ma}\backslash G_{\rm ms}$ versus $C_{\rm B}$ and (b) μ-factor versus frequency of the 4×6 μm CB device shown in Fig. 1(b) for different values of quiescent collector current density ($J_{\rm CQ}$). Simulations employ $V_{\rm CC} = 2.5$ V for (a) and (b) $C_{\rm B} = 115$ fF.

attenuation due to the short-circuit stubs implemented in them. This will ensure stability at sub-10-GHz frequencies, where the μ-factor is less than unity.

III. Adaptive Bias Network

A. Operation Mechanism

The PA in this work targets a combination of high PAE and high $P_{\rm sat}$, and therefore ABNs operate the transistors in deep Class-A and -B. Class-B requires a higher input drive and, while offering a higher collector efficiency (η_C), results in a lower PAE at the *D*-band. In Class-A amplifiers, the collector bias current is independent of the output power. This can be achieved by providing, for example, a fixed base bias current through a large bias resistance. In an ideal Class-B amplifier, the time-average collector current is proportional to the rms RF output current and hence proportional to the square root of the output power. Either an ABN must adjust the bias current as a function of RF power or the base–emitter must be biased just above the cutoff voltage. Fixed-$V_{\rm BE}$ bias is prone to electrothermal instability, which leads to transistor destruction. Class-A and -B designs require a variation of collector current with RF power intermediate between Class-A and -B.

Figs. 4 and 5 show the circuit schematic and layout artwork of the ABN, respectively. The RF transistor Q_1 is biased by a current mirror consisting of Q_2, R_1, and R_2, and diode-connected transistors Q_3 and Q_4. Variation in the reference current ($I_{\rm ref}$) from thermal variations in $V_{\rm BE3}$ and $V_{\rm BE4}$ is negligible if the dc voltage across R_3 is large. Assuming $I_{\rm c} = I_{\rm s}\exp(V_{\rm be}/V_t)$ for all transistors, with $V_t = nkT/q$, given

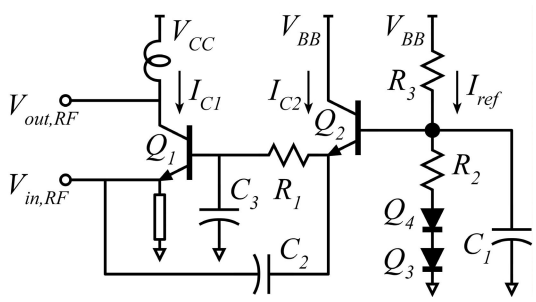

Fig. 4. *D*-band power-transistor gain cell with adaptive dc bias. Q_1 is the RF transistor with $C_3 = 2C_{\rm B}$ providing base capacitive series feedback, while Q_3 and Q_4 are diode-connected transistors.

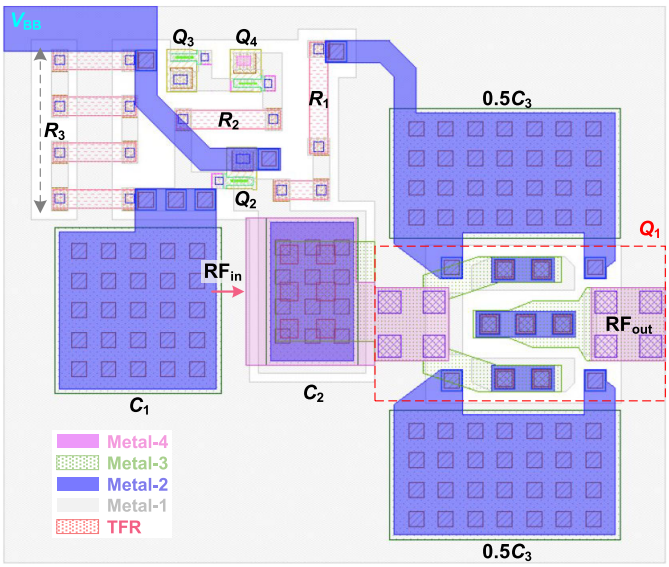

Fig. 5. Layout artwork of the circuit shown in Fig. 4 where the 4×6 μm RF transistor (Q_1) is biased by the ABN.

no RF drive

$$\left(\frac{nkT}{q}\right)\ln\left(\frac{I_{C1}^2 I_{S3} I_{S4}}{\beta I_{\rm ref}^2 I_{S1} I_{S2}}\right) = I_{\rm ref}R_2 - \frac{1}{\beta}I_{C1}R_1. \quad (1)$$

Setting $I_{S1}/\gamma = I_{S2} = I_{S3} = I_{S4}$, where $\gamma = I_{C1}^2/\beta I_{\rm ref}^2$, gives

$$\frac{I_{C1}}{I_{\rm ref}} = \beta\frac{R_2}{R_1} \quad (2)$$

a temperature-independent design.

An ideal diode, biased at a constant dc current and driven by an RF voltage $v_p\cos(\omega t)$ generates a dc bias voltage shift of $\delta V_{\rm diode} \approx -v_p^2/4V_t$ to leading order. In the ABN of Fig. 4, unlike [20], both the RF transistor Q_1 and the reference transistor Q_2 are driven by the RF voltage, and both produce $\delta V_{\rm BE} \approx -v_p^2/4v_t$ shifts upon RF drive. Neglecting transistor RF parasitics, I_{C1} varies approximately as

$$I_{C1} \approx I_{\rm ref}\frac{\beta R_2}{R_1} + \frac{2\left(v_p^2/4V_t\right)}{R_1/\beta + 2V_t/I_{C1}}. \quad (3)$$

I_{C1} has a fixed component and a component varying in proportion to the RF power. Given that $R_1/\beta \gg 2V_t/I_{C1}$, reducing R_1 increases the rate of variation of I_{C1} with RF power. If C_2 was removed so that only Q_1 produced RF rectification, R_1 would have to be smaller for given desired variation of I_{C1}. This is important for the electrothermal

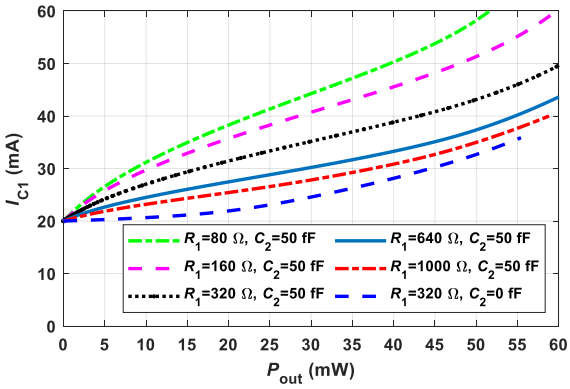

Fig. 6. Variation of I_{C1} versus P_{out} for a 24-μm transistor biased at quiescent collector current density of $J_{CQ} \approx 0.83$ mA/μm. The device is presented with the optimal load and source impedances for all cases to deliver the maximum PAE at 150 GHz.

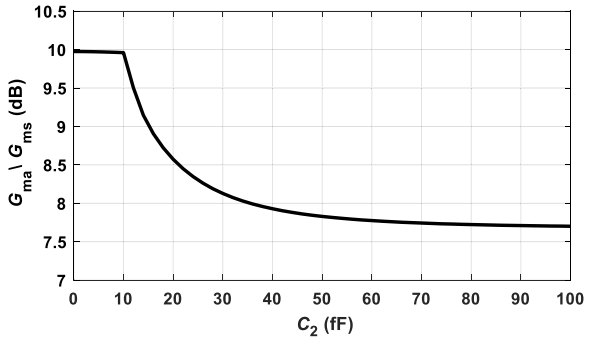

Fig. 7. $G_{ma}\backslash G_{ms}$ variance of a 4 × 6 μm transistor, operating as Q_1 in Fig. 4, as a function of C_2 at 150 GHz. For this simulation, C_B was set to 115 fF, J_{CQ} was 0.83 mA/μm, and R_1 was 500 Ω.

design since a lower R_1 degrades the electrothermal stability (Section III-B).

To illustrate the point, suppose Q_1 in Fig. 4 is a device with a total emitter length (L_E) of 24 μm, biased at $J_{CQ} = 0.83$ mA/μm (i.e., $I_{CQ1} = 20$ mA), and terminated to optimal load and source impedances to maximize the PAE. Fig. 6 presents the collector current of Q_1 (I_{C1}) at 150 GHz versus P_{out} for $R_1 = 320$ Ω and no C_1, and for $C_2 = 50$ fF and different values of R_1. For $R_1 = 320$ Ω, the ABN with $C_2 = 50$ fF features a higher I_{C1} sensitivity to P_{out} compared to the ABN with no C_2 (i.e., $C_2 = 0$ fF). In addition, as R_1 decreases, the ABN becomes more sensitive to P_{out} variations, which is also predicted by (3).

B. Thermal Stability

The ABN of Fig. 4 will be stable against electrothermal runaway if $\beta_T < 1$, where [21]

$$\beta_T \approx \left(\frac{-\partial V_{BE}}{\partial T}\right)\left(\frac{V_{CE1}\theta_{ja1}}{R_1/\beta + R_{E1} + 2V_t/I_{C1}}\right). \quad (4)$$

In the above equation, $\partial V_{BE}/\partial T = -0.88$ mV/K [22], $V_{CE1} = 2.5$ V is the collector–emitter bias voltage, $R_{E1} \approx 0.25$ Ω is the parasitic emitter resistance of Q_1, and $\theta_{ja} \approx 0.58$ K/mW [23] is the thermal resistance of Q_1 (for $L_E = 24$ μm). Electrothermal stability is poorest when I_{C1} is large (i.e., P_{out} is high) hence when V_T/I_{C1} is negligible. Thus, for $\beta \approx 27$ of the HBT transistors in the technology, (4) stipulates $R_1 \geq 27.5$ Ω to avoid thermal runaway. Increasing R_1 would provide a larger margin for process variations, but would reduce the variation of I_{C1}. In summary, the largest I_{C1}-versus-P_{out} variation is achieved for the minimum R_1 set by (4), stipulating $R_1 \geq 27.5$ Ω for $\beta_T < 1$ and $R_1 \geq 62$ Ω for $\beta_T \leq 0.5$.

If the RF transistor Q_1 of Fig. 4 has multiple emitter fingers, the resistor R_1 will not suppress electrothermal instability in the current distribution between fingers. Electrothermal simulations are necessary to evaluate the appropriate value of R_1 in multifinger transistors. If the PDK lacks an electrothermal model, it is advisable to select a larger R_1 value (at least twice the theoretical minimum) to provide a safety margin for heat coupling and related effects. In [24], separate dc bias resistances, isolated from the RF signal path, are provided for each finger in a four-finger HBT power cell. This further enhances electrothermal stability.

C. Loading Effect of the ABN

In the proposed ABN of Fig. 4, R_1 and C_2 load the base and emitter nodes of the RF transistor Q_1. Given that R_1 loads the base node of the RF transistor and does not lie directly in the signal path, it has a negligible effect on $G_{ma}\backslash G_{ms}$. Conversely, C_2 directly impacts the input RF signal of the CB transistor, leading to a decrease in $G_{ma}\backslash G_{ms}$. Fig. 7 shows $G_{ma}\backslash G_{ms}$, at 150 GHz, of a 4 × 6 μm transistor (operating as Q_1 in Fig. 4) as a function of C_2 for $J_{CQ1} \approx 0.83$ mA/μm, $R_1 = 500$ Ω, and $C_B = 0.5C_3 = 115$ fF, as an example. Increasing C_2, while resulting in a larger I_{C1} sensitivity versus P_{out} variation (Fig. 6), adversely affects the gain and hence PAE of the device. This will be further discussed in Section III-D.

D. ABN's Impact on Large-Signal Performance

As previously discussed, the ABN modulates the RF transistor's collector current based on the P_{out} level and therefore significantly impacts the device's large-signal performance. Fig. 8 illustrates the power sweep simulations for a 4 × 6 μm device in CB configuration with $C_B = 115$ fF, operating at a quiescent collector current (I_{CQ}) of 20 mA (i.e., $J_{CQ} \approx 0.83$ mA/μm). The simulation results depict two sample cases of biasing: one using a 500-Ω fixed resistor and the other using the ABN of Fig. 4 with $R_1 = 282$ Ω and $C_2 = 20$ fF. The design without ABN has a peak PAE of 37% with associated P_{out} of 15.5 dBm at its 2.3-dB output compression point. Conversely, in the design with ABN, since the collector current adapts to P_{out}, the gain compression occurs more gradually, achieving a peak PAE of 33.6% and $P_{out} = 16.9$ dBm at 0.84-dB compression. It is important to note that the design with fixed-resistor biasing achieves the same P_{out} at 4.3 dB compression with 30.7% PAE.

The ABN also leads to gain expansion, as shown in Fig. 8(b). The extent of gain expansion can be controlled by the value of C_2 for a given R_1 and C_3 (Section III-E). Moreover, the gain expansion directly translates to phase expansion, particularly at low P_{out} levels, and therefore should be carefully controlled to achieve a low AMPM. For this,

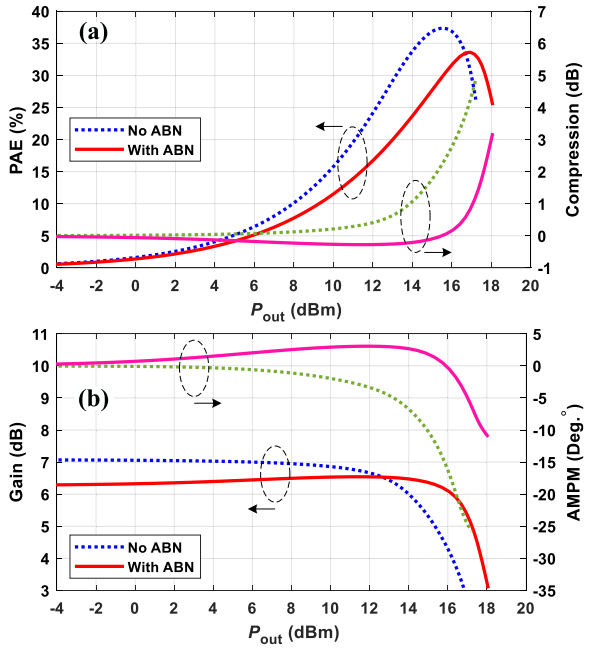

Fig. 8. Simulated results at 150 GHz showing (a) PAE and compression level and (b) gain and AM–PM as functions of P_{out} for a 24-μm transistor in a CB configuration with $C_B = 115$ fF. The transistor is biased at a quiescent collector current of 20 mA (i.e., $J_{CQ1} \approx 0.83$ mA/μm) using either a fixed 500-Ω resistor in its base (without ABN) or the ABN from Fig. 4, which has $R_1 = 282$ Ω and $C_2 = 20$ fF.

C_2 is adjusted to ensure the gain expansion remains below 0.5 dB, as indicated by the negative compression in Fig. 8(a), and to maintain AMPM $\leq 3°$ during power back-off. It is worthwhile to mention that the design with ABN exhibits an improved AMPM response at high P_{out} levels ($P_{out} \geq 12$ dBm) in Fig. 8(b).

E. Optimal C_2 Selection

We have learned so far that R_1 and C_2 control the sensitivity of I_{C1} versus P_{out}. We also know from Fig. 6 that R_1 should be minimized to achieve the highest sensitivity; otherwise, one needs to use a larger C_2, which is often not desired as it reduces $G_{ma} \backslash G_{ms}$ (Fig. 7). However, thermal stability constraints set the lower limit for R_1 (Section III-B), leaving C_2 as the sole adjustable ABN design parameter for optimizing the RF performance.

Fig. 9 illustrates the simulated P_{out}, PAE, and AMPM, versus gain compression level, for a 24-μm CB transistor operating at 150 GHz. The transistor utilizes $C_B = 115$ fF and is biased at $J_{CQ1} \approx 0.83$ mA/μm using the ABN of Fig. 4, which incorporates $R_1 = 282$ Ω and different values of C_2. As C_2 increases, the device achieves a higher P_{out} at a specific compression level (e.g., 1 dB). Nonetheless, there exists an optimal C_2 that maximizes PAE for a given compression level. For example, while $C_2 = 10$ fF is the optimal choice for 1.5 dB compression, the peak PAE at 0.75 dB compression is achieved for $C_2 = 20$ fF. Higher C_2 values maximize the PAE at power levels associated with gain expansion (i.e., negative compression in figures). It should be noted that gain expansion and AMPM increase as C_2 becomes larger. We employ $C_2 = 20$ fF for the final-stage transistors in our PA, as it provides the best combination of PAE (≈33%) and P_{out} (≈17 dBm) at 1 dB gain compression, without causing significant gain expansion (≤0.25 dB) and AMPM degradation at power backoff (≤3°).

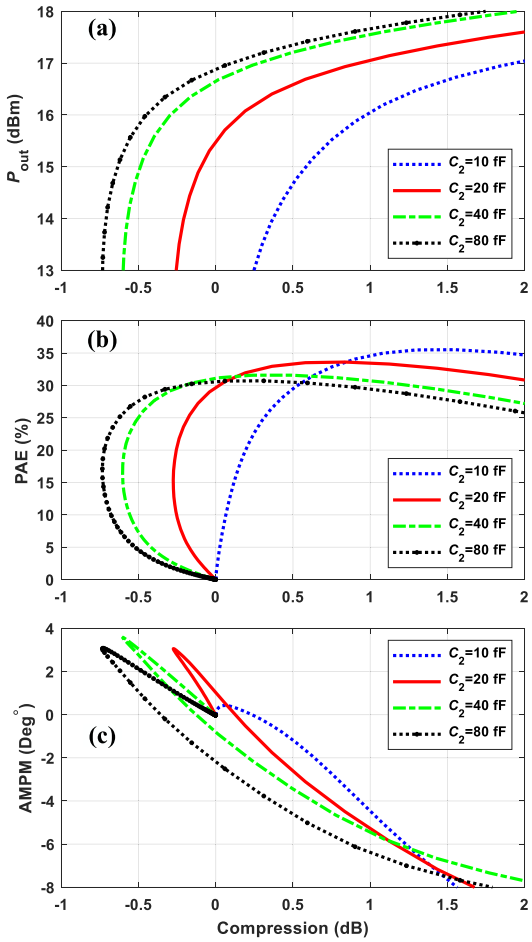

Fig. 9. Simulated results at 150 GHz showing (a) P_{out}, (b) PAE, and (c) AMPM as functions of gain compression level for a 24-μm transistor in a CB configuration with $C_B = 115$ fF. The transistor is biased at a quiescent collector current of 20 mA (i.e., $J_{CQ1} \approx 0.83$ mA/μm) using the ABN from Fig. 4, which has $R_1 = 282$ Ω and $C_2 = 20$, 40, 60, and 80 fF.

IV. Circuit Design

Fig. 10 shows the IC block diagram of the designed PA in Teledyne's 250-nm InP HBT process. The design target of the PA was to achieve ≥20-dB small-signal gain, ≥27-dBm output power, ≥15-dB input return loss (RL), and highest possible PAE over 120–160-GHz bandwidth. We also aimed to restrict the gain expansion to 1 dB. In the gain-budget analysis of the PA, it was considered that every matching network, that is, the input matching network (IMN), interstage matching networks (ISMNs), and the output matching network (OMN), exhibits a dissipative loss ranging from 1.5 to 2 dB. Additionally, based on the gain results shown in Fig. 8(b), we have estimated a gain of ≈6 dB for each amplifying stage.

Given the design goals and the assumptions above, the PA is designed with five stages, employing the commonly used 2:1 staging ratio for the first four stages. Due to the more complex layout of the ISMN45, a staging ratio of 1.5:1 was selected for the transistors in the final two stages of the PA. Consequently, and as previously mentioned, the output (5th) stage utilizes sixteen 24-μm (4 × 6 μm) transistors, configured in the CB

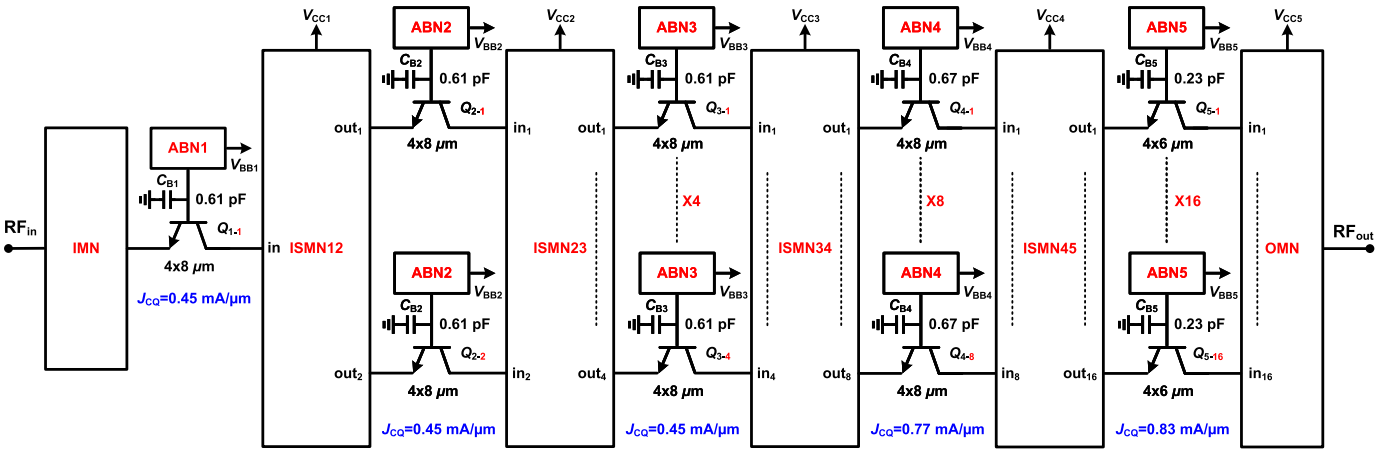

Fig. 10. Architecture of the designed five-stage PA. The first, second, third, fourth, and fifth stages employ 1, 2, 4, 8, and 16 transistors, respectively. Each four-finger transistor in the PA is biased using a dedicated ABN. Transistors in all stages operate in a capacitively degenerated CB configuration.

mode, to achieve an output power exceeding 500 mW. The fourth, third, second, and first stages employ 8, 4, 2, and 1 transistors, respectively, all with an emitter periphery of 32 μm (4 × 8 μm), and they all operate in the CB mode with capacitive feedback. Each four-finger transistor in the PA is biased by a separate ABN to prevent electrothermal instability. The circuit design details are provided below.

A. Degeneration Capacitor (C_B)

All thirty-one transistors in the PA (Fig. 10) operate in the capacitively degenerated CB topology, where the base degeneration capacitor reduces the stage gain, both by shunt-series feedback via the voltage-divider between C_{cb} and C_B, and by increased input impedance of the CB stage. As shown in [25], with a fixed bias, a reduction in C_B increases the base impedance. This effect permits a greater voltage swing at the transistor base, thereby enhancing the output power.

This increase in P_{sat} with reduced C_B can be more clearly understood by considering the effect of embedding a transistor in a lossless passive network (Fig. 11). Under dc bias (not shown), the drive power and load impedance are varied in simulations [see Fig. 11(a)] finding the values necessary to obtain the optimum transistor PAE [26]; this is a load–pull (LP) simulation. With this specific optimum load $Z_{L,opt}$ and input power $P_{in} = -P_1 = -\Re[V_1 I_1^*]$, the rms ac input and output phasor voltages (V_1, V_2) and currents (I_1, I_2) are then recorded, both for the fundamental frequency and any relevant harmonics. The transistor is then embedded in a lossless passive four-port, as shown in Fig. 11(b).

We require that the transistor terminal currents and voltages (I_1, I_2, V_1, V_2) be the same when the transistor is embedded in the lossless four-port [see Fig. 11(b)] as when the transistor is operating under the LP conditions that provide optimum PAE [see Fig. 11(a)]. The port-3 and -4 currents and voltages, both at the fundamental frequency and at any relevant harmonics, necessary to accomplish this are given by

$$[I_3, I_4, V_3, V_4]^T = [m_{ij}][I_1, I_2, V_1, V_2]^T \tag{5}$$

where the mixed four-port parameters $[m_{ij}]$ can be calculated from the admittance parameters $[Y_{ij}]$.

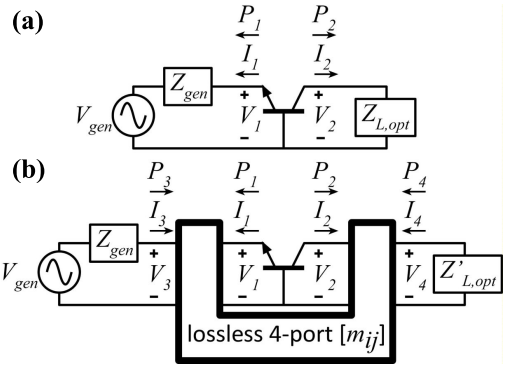

Fig. 11. Invariance of added power (P_{out}-P_{in}) and of PAE, given appropriate load impedance and input power, assuming passive lossless embedding. (a) Transistor operating under LP conditions, providing optimum PAE. (b) Transistor operating with identical terminal voltages and currents while embedded in a lossless four-port $[m_{ij}]$. dc bias networks are not shown.

For Fig. 11(a) and (b), the transistor input power, output power, and added power are

$$P_{in,t} = -P_1 = -\Re\left[V_1 I_1^*\right] \tag{6a}$$

$$P_{out,t} = P_2 = \Re\left[V_2 I_2^*\right] \tag{6b}$$

$$P_{added,t} = P_{out,t} - P_{in,t}. \tag{6c}$$

The PAE of the transistor is

$$\mathrm{PAE}_t = \frac{P_{added,t}}{P_{DC}} \tag{7}$$

where P_{dc} is the dc power dissipation.

The output power, input power, and PAE of the embedded transistor are

$$P_{out,emb} = -P_4 = -\Re\left[V_4 I_4^*\right] \tag{8a}$$

$$P_{in,emb} = P_3 = \Re\left[V_3 I_3^*\right] \tag{8b}$$

$$\mathrm{PAE}_{emb} = P_{added,emb}/P_{dc}. \tag{8c}$$

Note that, without loss of generality, we have selected port-3 and 4 such that $P_3 > 0$ and $P_4 < 0$; if neither are positive, the embedded transistor is an oscillator. Since the four-port is lossless and passive

$$P_1 + P_2 + P_3 + P_4 = 0 \tag{9}$$

and therefore,

$$P_{\text{out,emb}} - P_{\text{in,emb}} = P_{\text{added,emb}} = P_{\text{out},t} - P_{\text{in},t} = P_{\text{added},t}. \quad (10)$$

From (7), (8c), and (10), it can be concluded that

$$\text{PAE}_{\text{emb}} = \text{PAE}_t. \quad (11)$$

In summary, with appropriate input power and external load impedance, Z'_{load}, the transistor with lossless passive embedding has the same added power and the same PAE as that of the transistor without embedding.

Given the above derivations, the output power at peak PAE can be reformulated as

$$P_{\text{out,emb}} = \frac{G}{G-1} P_{\text{added},t} \quad (12)$$

where $G = P_{\text{out,emb}}/P_{\text{in,emb}}$ is the power gain of the stage. Because P_{added} is invariant with lossless passive embedding, $P_{\text{out,emb}}$ increases if the embedding decreases G. The increased P_{out} is directly due to increased P_{in}, as a consequence of reduced gain with constant $P_{\text{out}} - P_{\text{in}}$.

Fig. 12 illustrates the PAE and gain as functions of P_{out} for a 24-μm transistor at 150 GHz, functioning in the CB mode with $C_{\text{B}} = 25$, 50, and 100 fF. The device is biased at $J_{\text{CQ1}} \approx 0.83$ mA/μm using the ABN of Fig. 4. The ABN employs $R_1 = 282\ \Omega$, and its C_2 is adjusted to realize a gain expansion of less than 0.5 dB and AMPM $\leq 3°$ for each C_{B}. Consistent with the above discussion, a device with a smaller C_{B} exhibits lower gain and higher P_{out} at its 1-dB compression point (shown by circle markers in Fig. 12). The observed decrease in PAE with reduced C_{B} in Fig. 12 is due to RF dissipation in R_1; the embedding network is not completely lossless. Adding an inductance in series with R_1 would reduce this degradation in PAE. Furthermore, since we have adjusted the ABN for each C_{B} value to limit the gain expansion, the PAE is also influenced by the ABN performance. Simulations suggest that $C_{\text{B}} = 115$ fF leads to the highest PAE at the 1-dB compression point. Because we have 16 transistors in the last stage of the PA and heating is critical, we choose $C_{\text{B}} = 115$ fF for the last-stage devices to maximize their PAE and reduce the dissipated power.

The driver stages employ 4×8 μm transistors configured in the CB mode, with capacitances of $C_{B1} = C_{B2} = C_{B3} = 0.61$ pF and $C_{B4} = 0.67$ pF. Due to the inherently lower gain of the 4×8 μm transistors compared to their 4×6 μm counterparts used in the final stage, greater base degeneration capacitor values are implemented to offset the reduced gain.

B. Optimum Bias Point

As discussed earlier, C_{B} and C_2 impact the achievable gain from the device. Thus, the optimum bias point (i.e., J_{CQ}) of the device to maximize the PAE depends on these capacitors and several iterations might be needed to find the optimal combination of C_{B}, C_2, and J_{CQ}. Fig. 13 shows the simulated P_{out}, PAE, and transducer power gain (G_T) of a 24-μm (4×6 μm) CB device (with $C_{\text{B}} = 115$ fF) as a function of the quiescent current density at 1-dB gain compression. The device is biased using the ABN of Fig. 4 where for each case, C_2 was fine-tuned to limit the gain expansion and

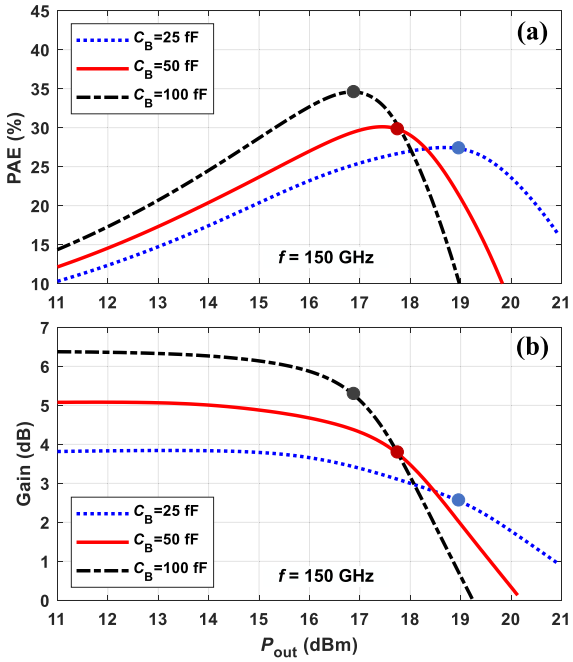

Fig. 12. (a) PAE and (b) gain, versus output power, of a 24-μm transistor in a CB configuration with $C_{\text{B}} = 25$, 50, and 100 fF. The transistor is biased at a quiescent collector current of 20 mA (i.e., $J_{\text{CQ1}} \approx 0.83$ mA/μm) using the ABN from Fig. 4, which has $R_1 = 282\ \Omega$. For each C_{B} value, C_2 is adjusted to realize a gain expansion of less than 0.5 dB and AMPM $\leq 3°$. Markers show the P_{out} levels corresponding to the 1-dB compression point.

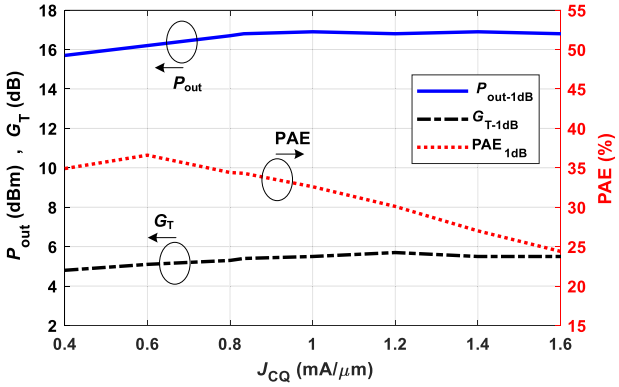

Fig. 13. PAE, P_{out}, and transducer power gain of a 24-μm CB device (with $C_{\text{B}} = 115$ fF) at 1-dB compression point versus the quiescent current density. The device was biased using the ABN of Fig. 4 where for each bias point, C_2 was adjusted to limit the gain expansion and AMPM to 0.5 dB and 3°, respectively, at power back-off. The simulation frequency is 150 GHz.

AMPM to 0.5 dB and 3°, respectively, at power back-off. The highest possible PAE of 36.6% is achieved when J_{CQ} is 0.6 mA/μm, along with a P_{out} of 16.2 dBm and a gain of 5.1 dB. Nevertheless, we chose to set the transistor bias at $J_{\text{CQ}} = 0.83$ mA/μm (i.e., $I_{\text{CQ}} \approx 20$ mA) to obtain a higher P_{out} of 16.8 dBm and a greater gain of 5.4 dB, albeit with a slightly reduced PAE of 34.3%. The transistors in the first four stages of the PA are biased at lower current densities to reduce the total dc power of the PA and improve the PAE.

C. Output Matching Network

To design the matching circuits, recursive LP and source–pull (SP) simulations were conducted for the 4×6 μm and 4×8 μm transistors utilized in the PA. Each transistor was biased using its own ABN during

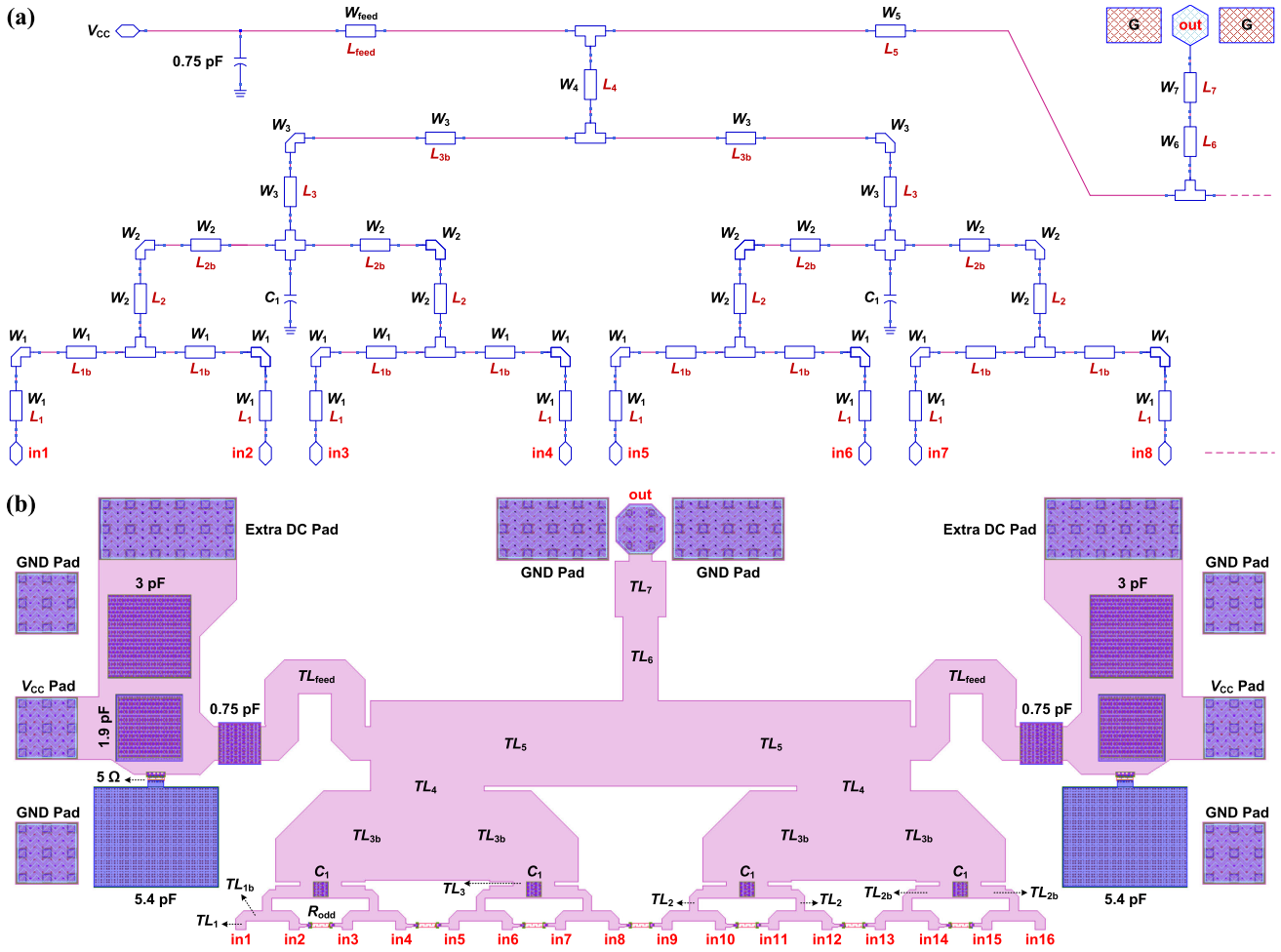

Fig. 14. (a) Half-cell schematic and (b) full layout of the designed OMN, which also serves as a 16-to-1 power combiner.

the simulations, and the source-plane impedance (Z_{SP}) was configured as the conjugate of the large-signal input impedance ($Z_{in}^{\star}$). Once the optimal large-signal load-line impedance (Z_{LP}) and input impedance of the transistors were identified across the 120–160-GHz frequency range, matching networks were crafted to present Z_{LP} and $Z_{in}^{\star}$ to each transistor at its respective load and source planes at each frequency within the bandwidth. Every matching network was EM-simulated using the FEM engine in Keysight ADS and its layout drawing was optimized in multiple steps to minimize the reflection coefficients (≤ -15 dB) and insertion loss when terminated to the conjugate of the impedances that it should present at its input and output ports.

The OMN should combine the output powers of sixteen transistors in the last stage of the PA, and when terminated to 50 Ω at its output port, it should present Z_{LP5} at all its input ports over 120–160 GHz. The half-cell schematic and full layout of the OMN is shown in Fig. 14, and the TL dimensions are given in Table I. We use the design procedure explained in [24] to find the optimal OMN topology. To suppress odd-mode oscillations, 50-Ω resistors, denoted by R_{odd} in Fig. 14(b), were employed between the adjacent input ports of the OMN. Due to the high dc current of the transistors in the last stage of the PA (i.e., ≥500 mA), extra wire-bondable wide dc pads were also incorporated into the OMN. Bypassing

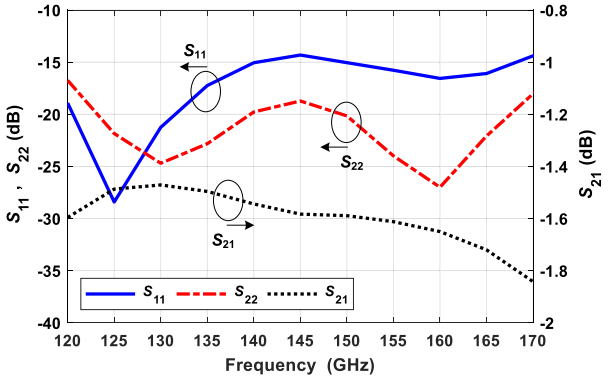

Fig. 15. Large-signal insertion loss and reflection coefficients of the OMN. The reference impedance at each input port is the complex conjugate of the LP impedance ($Z_{LP5}^{\star}$) over 120–170 GHz. The output port is terminated to 50 Ω.

capacitors and damping *RC* networks bypass the feed line and kill supply oscillations.

Fig. 15 shows the insertion loss of the OMN when all its input ports are tied together, and $Z_{LP5}^{\star}/16$ and 50-Ω terminations are presented at its input and output ports, respectively. By using $Z_{LP5}^{\star}/16$ as the port impedance, S_{21} in the graph represents both attenuation of the OMN and loss in P_{sat} due to any difference between the actual load impedance

TABLE I
COMPONENT VALUES IN THE OMNS

	TL_1	TL_{1b}	TL_2	TL_{2b}	TL_3	TL_{3b}	TL_4	TL_5	TL_6	TL_7	TL_{feed}
W (μm)	10	10	11	15	50	110	135	100	45	60	40
L (μm)	12	20	15	30	5	7	6	300	100	70	330

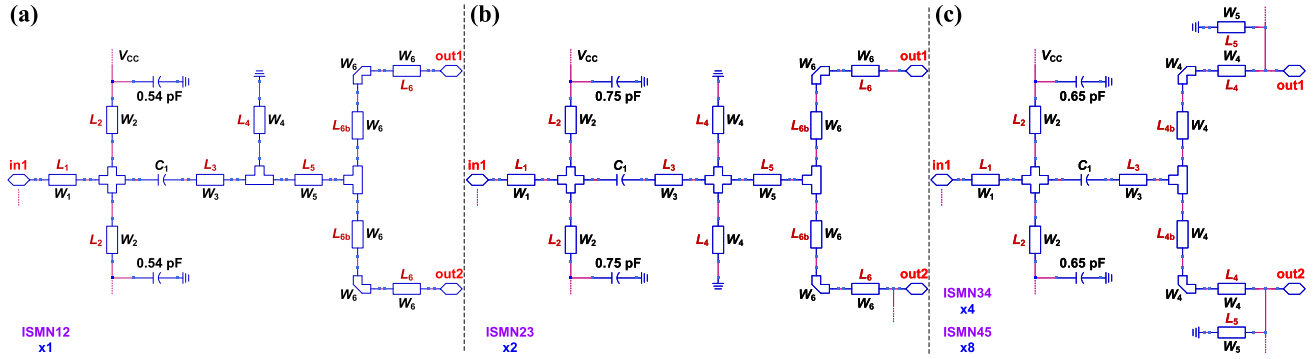

Fig. 16. Circuit schematics of the interstage matching networks (ISMNs). (a) ISMN12. (b) Core cell of ISMN23. (c) Core cell of ISMN34 and ISMN45.

presented to the transistors and the load-line impedance for optimum P_{sat}.

The OMN exhibits an average dissipative loss of 1.6 dB and negligible mismatch loss across the 120–170-GHz frequency range because the large-signal S_{11} and S_{22} are less than -15 dB. We could achieve a reduced OMN loss of 1.3 dB by employing a smaller RF pad with less parasitic. However, the smaller pad did not fulfill the customer's requirements for wire bonding and packaging.

D. Interstage Matching Networks

Fig. 16 presents the circuit topologies for the core cells of the ISMNs, and Table II presents the TL dimensions used in every ISMN. Each core cell consists of a 2:1 power splitter and is replicated 1, 2, 4, and 8 times in ISMN12, ISMN23, ISMN34, and ISMN45, respectively. Fig. 17 shows the layout artwork for ISMN12, ISMN45, and the core cells of ISMN12 and ISMN23. Each ISMN core cell should contain two short-circuit stubs, separated by a coupling capacitor (C_1), to provide dc paths for the collector and emitter currents. For instance, TL_2 stubs in Fig. 17(b) pass the collector currents, whereas TL_5 stubs carry the emitter currents to ground. Because the designed ISMNs do not ensure port-to-port isolation, we have employed odd-mode resistors in ISMNs to secure the odd-mode stability of the PA.

The large-signal insertion loss and reflection coefficients of the designed ISMNs are illustrated in Fig. 18. In simulations over 120–170 GHz, the reference impedance (Z_{Ref}) at each input port of $ISMN_{ij}$ is the complex conjugate of the large-signal load-line impedance of each transistor used in stage i of the PA ($Z^{\star}_{LP\text{-}i}$). Meanwhile, Z_{Ref} at each output port of $ISMN_{ij}$ is $Z^{\star}_{in\text{-}j}$, where $Z_{in\text{-}j}$ represents the large-signal input impedance of each transistor in stage j of the PA. The ISMNs exhibit an insertion loss ranging from 1.3 to 2.3 dB, with their loss characteristics tailored to ensure a flat S_{21} response for the five-stage PA. Owing to the complexity of the layout, ISMN45 experiences the highest loss among the ISMNs. ISMN45 incorporates a high-pass loss response to counterbalance the higher gain of the transistors at the lower end of the operating frequency range. To provide V_{BB} to each ABN, the bias lines must traverse the RF circuits, necessitating efforts to minimize crosstalk with the RF circuits. We have conducted simulations of the ISMNs and bias lines in combination and implemented necessary refinements to enhance the performance.

TABLE II
COMPONENT VALUES IN THE INTERSTAGE MATCHING NETWORKS

Circuit	ISMN12	ISMN23	ISMN34	ISMN45
TL_1	W=5 μm L=30 μm	W=10 μm L=45 μm	W=10 μm L=30 μm	W=13 μm L=43 μm
TL_2	W=6 μm L=140 μm	W=10 μm L=120 μm	W=9 μm L=90 μm	W=15 μm L=175 μm
TL_3	W=25 μm L=80 μm	W=55 μm L=95 μm	W=40 μm L=90 μm	W=23 μm L=13 μm
TL_4	W=9 μm L=200 μm	W=5 μm L=170 μm	W=80 μm L=100 μm	W=27 μm L=15 μm
TL_{4b}	Not Used	Not Used	W=80 μm L=5 μm	W=27 μm L=7 μm
TL_5	W=25 μm L=10 μm	W=55 μm L=50 μm	W=10 μm L=450 μm	W=5 μm L=320 μm
TL_6	W=70 μm L=10 μm	W=80 μm L=90 μm	Not Used	Not Used
TL_{6b}	W=70 μm L=220 μm	W=80 μm L=60 μm	Not Used	Not Used

E. Input Matching Network

The circuit schematic and layout of the IMN are demonstrated in Fig. 19. The IMN should present $Z^{\star}_{in1}$ to the transistor used in the first stage of the PA, and it is matched to 50 Ω at its input port. The input GSG pad is absorbed into the IMN, and two shunt stubs (TL_2 and TL_4) provide a dc path for the emitter current. The 200-Ω resistor to ground is to improve the stability. The insertion loss and reflection coefficients of the IMN are presented in Fig. 20. The average IMN loss is about 1.4 dB over 120–170 GHz, and the reflection coefficients are better than -15 dB.

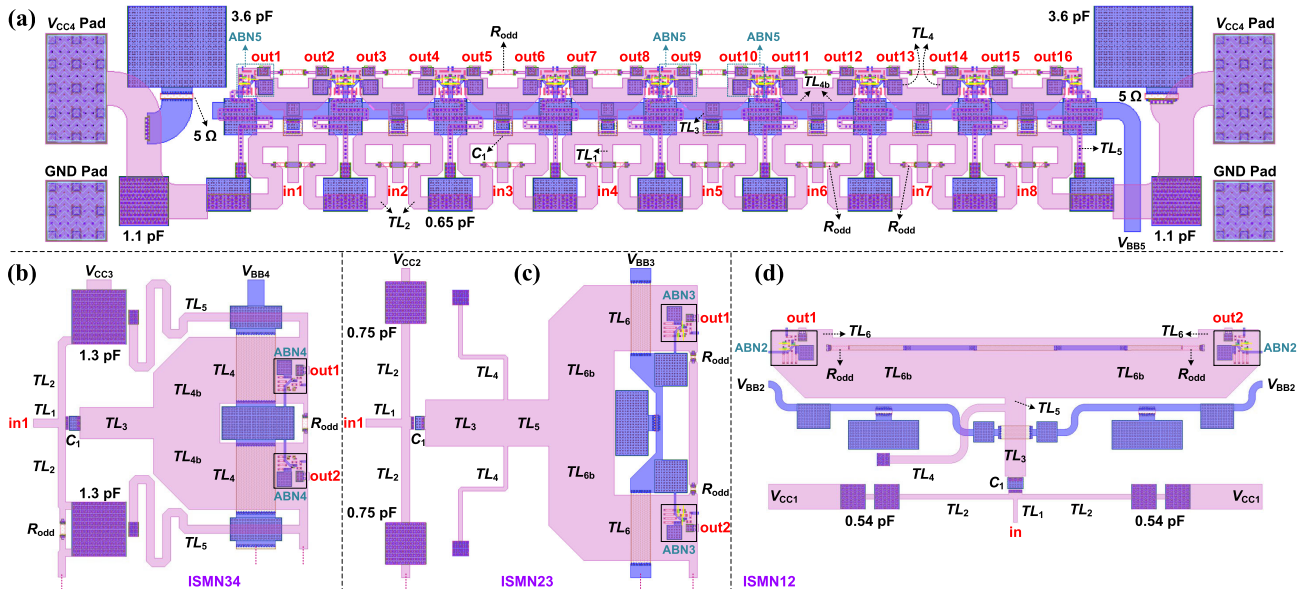

Fig. 17. Artworks of interstage matching networks (ISMNs). (a) ISMN45. (b) Core cell of ISMN34. (c) Core cell of ISMN23. (d) ISMN12. Core cells of ISMN34 and ISMN23 are used in the PA four and two times, respectively.

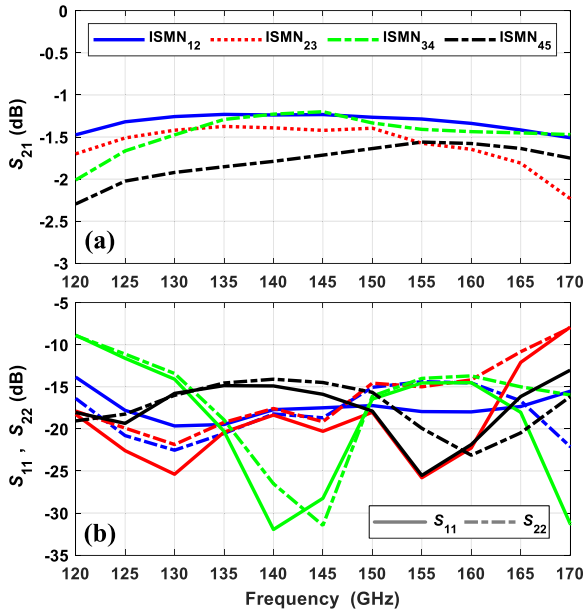

Fig. 18. Large-signal (a) insertion loss and (b) reflection coefficients of the ISMNs. Reference impedance at each input port of ISMN_{ij} is the complex conjugate of the large-signal load-line impedance of each transistor used in stage i of the PA ($Z^{\star}_{\text{LP-i}}$) over 120–170 GHz. The reference impedance at each output port of ISMN_{ij} is $Z^{\star}_{\text{in-j}}$, where $Z_{\text{in-j}}$ represents the large-signal input impedance of each transistor in stage j of the PA.

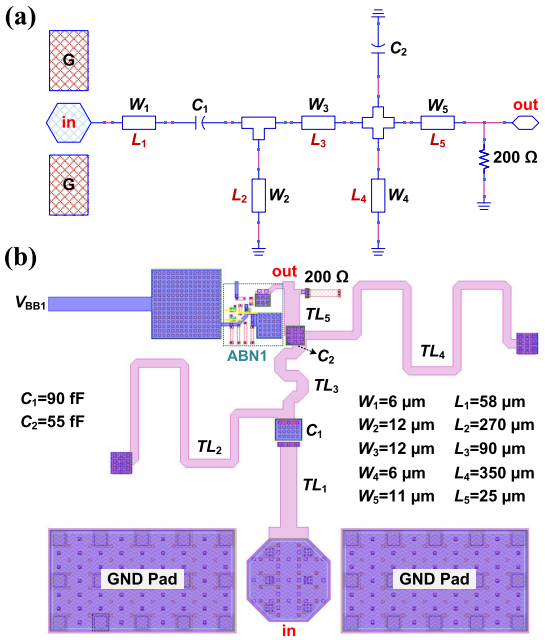

Fig. 19. (a) Circuit schematic and (b) layout of the IMN.

V. Measurements

The designed PA produces approximately 500-mW output power over its operation bandwidth, and considering an average PAE of 15%, it dissipates ≥2.8 W as heat. To handle this, the PA die was bonded to a copper heat sink using a material with 29 $\text{W}/(\text{m}\cdot\text{K})$ thermal conductivity.

On-wafer S-parameter characterization was performed using VDI 110–170-GHz VNA extenders (VNAX:6.5) with a Keysight PNA (N5225A). S-parameter calibration was performed using CS-5 GGB substrate and verified using on-chip multiline through-reflect-line (TRL) calibration standards with RF pads that matched the tested PA.

For power measurements, a synthesizer and 12:1 frequency multiplier (VDI AMC-333) generated the input signal, which passed through a directional coupler and a 140–220-GHz GGB wafer probe, whose waveguide cutoff is 116 GHz. The coupler −20-dB port, connected to a harmonic mixer and spectrum analyzer, monitored the input power; before IC testing, this P_{in} monitor was calibrated against a VDI/Erickson power-meter. The IC output was contacted using a second, identical probe.

Connecting the meter directly to the output probe overloads the meter (200-mW limit). As a high-power attenuator, a 40-cm waveguide was placed between the output probe and the power-meter after first measuring its loss. Six

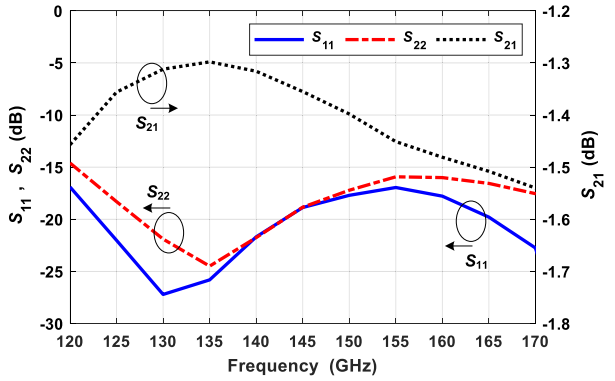

Fig. 20. Insertion loss and reflection coefficients of the IMN. Reference impedance at the output port is the complex conjugate of the input impedance of the transistor (Z^{*}_{in1}) over 120–170-GHz bandwidth. The input port is terminated to 50 Ω.

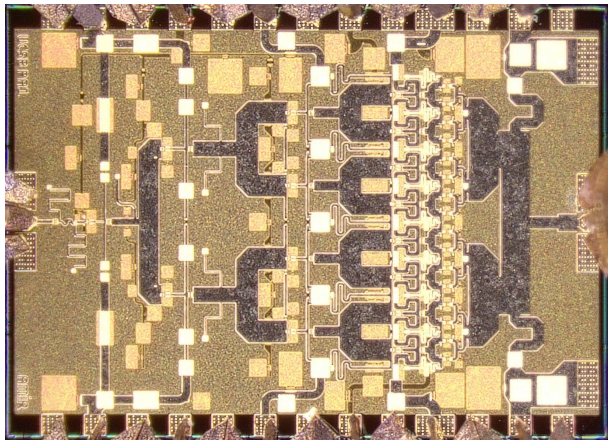

Fig. 21. Photograph of the PA fabricated in Teledyne 250-nm InP HBT process. The die is 2 × 1.5 mm.

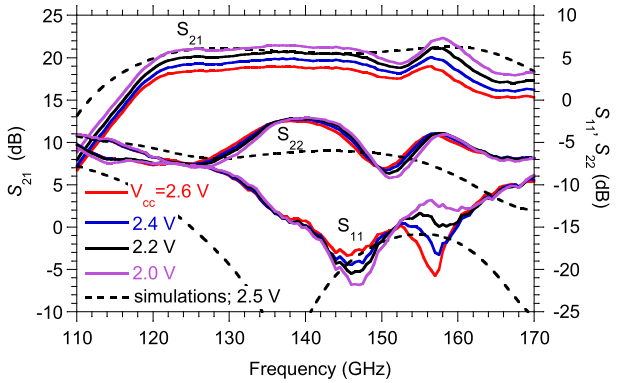

Fig. 22. Simulated and measured *S*-parameters of the PA from Wafer-1 (the low-speed wafer) for $V_{\text{BB1}} = V_{\text{BB2}} = V_{\text{BB3}} = 2.65$ V and $V_{\text{BB4}} = V_{\text{BB5}} = 2.5$ V. The measurements were done by Samsung for different values of V_{CC}, where $V_{\text{CC1}} = V_{\text{CC2}} = V_{\text{CC3}} = V_{\text{CC4}} = V_{\text{CC5}} = V_{\text{CC}}$.

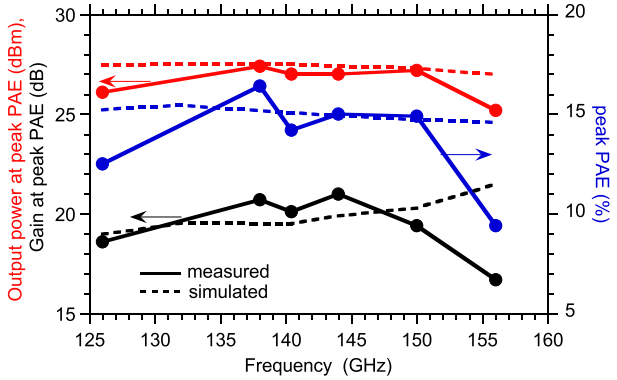

Fig. 23. Maximum PAE, with the associated gain and P_{out} versus frequency. PAs from the high-β wafer (Wafer-2) were measured under $V_{\text{BB1}} = V_{\text{BB2}} = V_{\text{BB3}} = 2.7$ V, $V_{\text{BB4}} = 2.6$ V, $V_{\text{BB5}} = 2.65$ V, $V_{\text{CC1}} = V_{\text{CC2}} = V_{\text{CC3}} = V_{\text{CC4}} = 2.7$ V, and $V_{\text{CC5}} = 2.6$ V.

measurements of the waveguide loss showed 0.33-dB reproducibility (σ). Probe loss (3.07, 2.85, 3.02, 2.51, 2.24, and 2.51 dB per probe at 126, 138, 140.4, 144, 150, and 156 GHz) was estimated by measuring the attenuation of the two probes connected by a 100-μm CPW line (0.08 dB simulated loss). The probe loss measurement reproducibility σ was <0.07 dB. All on-wafer *D*-band power measurements without vector-corrected calibration have $\sigma \approx 1$ dB uncertainty in the measurement of P_{out}; in this high-power measurement, the output attenuator correction introduces an additional 0.33-dB reproducibility (σ).

Fig. 21 shows the die photograph of the implemented PA in Teledyne's 250-nm InP HBT process. Chip dimensions are 2 × 1.5 mm. Bias voltages were supplied via dc probe cards, and *D*-band GGB wafer probes were used for RF performance characterization. The performances of the PAs from two different wafers, Wafer-1 and Wafer-2, were measured. The transistors in Wafer-1 have a lower β than the ones in Wafer-2. As a result, the PAs from Wafer-1 exhibit slightly lower gain and P_{out} compared to the PAs from Wafer-2 under identical bias conditions.

The measured *S*-parameters of the PA from Wafer-1 are presented in Fig. 22 for $V_{\text{BB1}} = V_{\text{BB2}} = V_{\text{BB3}} = 2.65$ V, $V_{\text{BB4}} = V_{\text{BB5}} = 2.5$ V, and different V_{CC} values. In these tests, all PA stages were set to the same collector voltage, meaning $V_{\text{CC1}} = V_{\text{CC2}} = V_{\text{CC3}} = V_{\text{CC4}} = V_{\text{CC5}} = V_{\text{CC}}$ (Fig. 10). The simulated *S*-parameters are also depicted for $V_{\text{CC}} = 2.5$ V. Given that Wafer-1 is a lower-speed wafer, the observed S_{21} is 2–3 dB below the simulated values, equating to a 0.4–0.6 dB lesser gain per stage. For $V_{\text{CC}} = 2.4$ V, the 3-dB bandwidth of S_{21} is measured to be 43.6 GHz (spanning 118.8–162.4 GHz), reflecting a fractional bandwidth of 31% around 140.6 GHz. Overall, the measured data closely aligns with the simulated results. The gain fluctuation in the 150–160-GHz range may be attributed to calibration errors or moving issues.

Fig. 23 shows the highest PAE of a PA from Wafer-2 (the high-speed wafer) plotted against frequency, along with the corresponding gain and P_{out}. The PA was bias at $V_{\text{BB1}} = V_{\text{BB2}} = V_{\text{BB3}} = 2.7$ V, $V_{\text{BB4}} = 2.6$ V, $V_{\text{BB5}} = 2.65$ V, $V_{\text{CC1}} = V_{\text{CC2}} = V_{\text{CC3}} = V_{\text{CC4}} = 2.7$ V, and $V_{\text{CC5}} = 2.6$ V. The maximum PAE recorded is 16.4%, observed at 138 GHz, with a related output power of 27.4 dBm and 21 dB gain. The measured P_{out} exceeds 27 dBm in the 138–150-GHz range and 26 dBm over the 126–150-GHz range.

Fig. 24 shows the simulated and measured PAE, P_{out}, and gain versus P_{in} at 150 GHz. The bias voltages are the same as the ones in the caption of Fig. 23. Because the 2.24-dB probe loss correction at 150 GHz is smaller than at other measurement frequencies, we choose 150 GHz to present power-sweep curves. For an input power of 8 dBm, the recorded output power (P_{out}), PAE, and gain of the PA from Wafer-2 (the high-speed wafer) are 27.2 dBm, 14.9%,

TABLE III

SUMMARY OF THE STATE-OF-THE-ART INTEGRATED PAS WITH >100-MW SATURATED OUTPUT POWER AT THE *D*-BAND

Publication[◇] [Reference]	Technology (node)	V_{DD} (V)	P_{out} (dBm)	PAE (%)	Gain[†] (dB)	Frequency (GHz)	BW (%)	Area (mm^2)	$P^{‡}_{den}$ (W/mm^2)
MWTL-2021 [9]	SiGe HBT 90-nm	3.25/4	17.6-21.9	4.9-12	12	110-145	27.4	1.7	0.09
ISSCC-2022 [10]	SiGe HBT 130-nm	4	22-22.7	16-18.7	15-16	107-135	23.1	1.11	0.17
TMTT-2019 [5]	GaN HEMT 100-nm	15	21-26.4	3-11.5	21-26.4	110-140	24	7.5	0.06
EuMIC-2022 [6]	GaN HEMT 40-nm	12	23.5	7.9	6	136	NA	4.25	0.05
MWTL-2024 [7]	GaN HEMT 64-nm	12	20	10.6	2.5	132	NA	NA	2*
IMS-2019 [17]	InP HBT 250-nm	2.5	23.2-24	5.8-7	14-16	110-150	30.8	1.89	0.13
IMS-2019 [17]	InP HBT 250-nm	2.5	20.3-21.3	6.8-8.9	13-15	55-135	84.2	1.19	0.12
MWTL-2019 [13]	InP HBT 250-nm	2.5	21-21.8	8.2-10.5	15-17.5	115-150	26.4	0.75	0.2
IMS-2020 [14]	InP HBT 250-nm	2.5	18.9-20.5	14.3-20.8	12.3-15.9	125-150	18.2	0.69	0.16
EuMIC-2021 [15]	InP HBT 250-nm	2.5	22.3-23	15-17.8	13-16.5	127-151	17.3	1.34	0.15
MWTL-2022 [16]	InP HBT 250-nm	2.5	20.2-21	12.5-16.2	16-18	150-180	18.2	0.77	0.16
This Work	InP HBT 250-nm	2.6	26-27.4	13-16.4	19-21	126-152	18.7	3	0.18

[◇]Spec values for other works were extracted from their text or otherwise estimated from the plots.
[†]Gain at power saturation. [‡]Power density. *P_{out} per active device area.

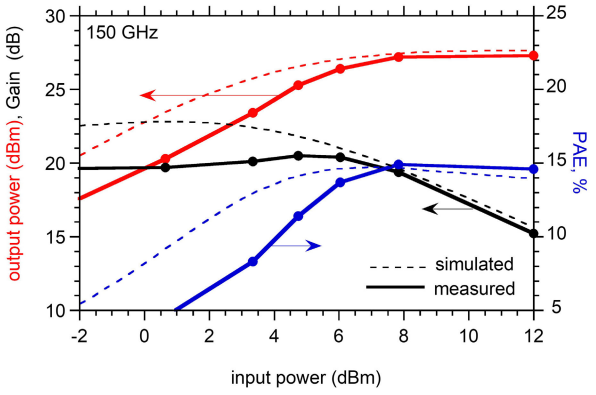

Fig. 24. Simulated and measured PAE, P_{out}, and gain of the PA form Wafer-2 (i.e., the high-β wafer) versus P_{in} at 150 GHz. The PA was biased at $V_{BB1} = V_{BB2} = V_{BB3} = 2.7$ V, $V_{BB4} = 2.6$ V, $V_{BB5} = 2.65$ V, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = 2.7$ V, and $V_{CC5} = 2.6$ V.

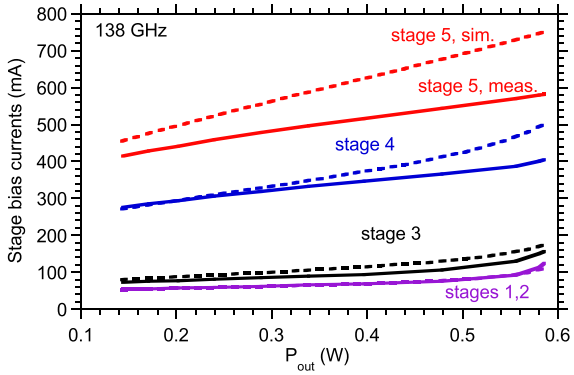

Fig. 25. Measured and simulated collector current of each PA stage versus P_{out} at 138 GHz. A PA from the high-β wafer (Wafer-2) was characterized under $V_{BB1} = V_{BB2} = V_{BB3} = 2.7$ V, $V_{BB4} = 2.6$ V, $V_{BB5} = 2.65$ V, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = 2.7$ V, and $V_{CC5} = 2.6$ V.

and 19.2 dB, respectively. The measured gain-versus-P_{in} curve shows approximately 0.95 dB of gain expansion. This observed gain expansion is larger than the 0.5 dB predicted by the simulations, which might be due to simulation inaccuracies or variations in the process. At 150 GHz, the gain of the PA compresses by 1-dB for $P_{in} = 9$ dBm. At this drive level, PAE and gain are 14.9% and 18.6 dB, respectively, whereas $P_{out} = 27.2$ dBm.

Fig. 25 depicts the simulated and measured collector bias currents of the PA from the high-β wafer at 138 GHz, where the PA exhibits the highest PAE and P_{out}. The bias voltages are identical to those mentioned in the caption of Fig. 23. Consistent with the results illustrated in Fig. 6 and the simulations of PA collector currents at supply rails (I_{CC}), the measurements demonstrate the anticipated linear relationship of I_{CC} with P_{out}; the difference between simulation and measurement could stem from model inaccuracies or process variations.

It is worth mentioning that, based on Samsung's measurements, PAs from Wafer-1 (low-β) wafer, though having a lower gain and PAE compared to those from the high-β wafer, have consistently shown an average output power of 25 from 126 GHz to 160 GHz, indicating a broader bandwidth for the low-β samples. Table III compares the present and prior results for *D*-band PAs. The presented PA in this work establishes a new record for output power of the *D*-band PAs in any technology. In addition, its power density ($P_{den} = P_{out}$/Area) is among the best, only second to the newly published 132-GHz GaN PA [7], which has reported the output power per active device area.

VI. Conclusion

A five-stage *D*-band PA, in a 250-nm InP HBT technology, operating on a 2.6-V supply, with peak 27.2-dBm output power and 14.9% associated PAE is presented. The measured saturated output power exceeds 26 dBm over 126–150 GHz. Multiple transistors are power combined at each PA stage to increase the output power, where all active cells employ a CB topology with capacitive base degeneration. Each transistor is biased using an ABN, which adjusts the bias point based on the input RF power. The ABN also acts as an analog predistorter and engineers the P_{in}–P_{out} curve. The PA occupies 2×1.5 mm^2 die area, including pads, and consumes 3.47-W dc power at peak PAE.

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Amirreza Alizadeh (Member, IEEE) received the Ph.D. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2017.

From 2018 to 2019, he was an Assistant Professor at the Department of Electrical Engineering, AmirKabir University of Technology (Tehran Polytechnic), Tehran. From 2019 to 2021, he held a postdoctoral research position at the School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ, USA, where he lectured on various topics on full-duplex radios and phase noise in injection-locked VCOs. From 2021 to 2023, he was a Staff Scientist with the Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA, USA, working on developing 210- and 280-GHz communication links. He is currently a Research and Development IC Design Engineer with Keysight Technologies, Santa Rosa, CA, USA. His research interests include RF and mm-wave integrated circuits and systems, mm-wave antennas in package, and mm-wave module design and packaging.

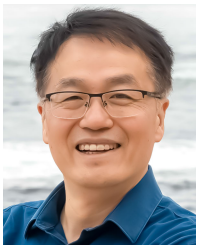
Utku Soylu (Graduate Student Member, IEEE) received the B.S. degree in electrical and electronics engineering from Boğaziçi University, Istanbul, Turkey, in 2018, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California at Santa Barbara, Santa Barbara, CA, USA, in 2019 and 2023, respectively.

He is currently a Research Scientist with the Cryogenic Control Hardware and Systems Group, IBM T. J. Watson Research Center, Yorktown Heights, NY, USA. His research interests include circuit, module, and system design for 200–300-GHz wireless communication links, and cryo-CMOS circuit design for quantum computers.

Dr. Soylu received the Analog Devices Inc. Outstanding Student Designer Award in 2022 and the UCSB ECE Department Herb Kroemer Dissertation Fellowship in Spring 2023. He currently serves as a TPC member of BCICTS.

Navneet Sharma received the B.E. degree in electronics and communication from Delhi University, New Delhi, India, in 2004, the M.S. degree in electrical engineering (EE) from NCSU, Raleigh, NC, USA, in 2008, and the Ph.D. degree in EE from UT Dallas, Richardson, TX, USA, in 2016.

From 2005 to 2007, he was an Analog Design Engineer at Freescale Inc., Gachibowli, India. He is currently with Samsung Research America, Plano, TX, USA, developing next-generation communication and consumer products. His research interests include circuits and systems at millimeter-wave and terahertz.



Gary Xu (Member, IEEE) received the B.S. degree from Tsinghua University, Beijing, China, in 1996, and the M.S. degree in electrical engineering from Rice University, Houston, TX, USA, in 1999.

He is currently a Vice President with Samsung Research America, Plano, TX, USA, leading beyond 5G and 6G wireless system design and technology development. His team has been working on massive MIMO, mmWave, and advanced duplexing systems. In 2015, he led the world's first Full Dimension MIMO (FD-MIMO/massive MIMO) prototype development and successfully demonstrated its commercial feasibility. Before joining Samsung, he worked as a wireless system engineer at Nokia and then Texas Instruments.

Mark J. W. Rodwell (Fellow, IEEE) received the Ph.D. degree from Stanford University, Stanford, CA, USA, in 1988.

He holds the Doluca Family Endowed Chair in Electrical and Computer Engineering with the University of California at Santa Barbara (UCSB), Santa Barbara, CA, USA, and directs the SRC/DARPA ComSenTer Wireless Research Center. His research group develops high-frequency transistors, ICs, and communication systems.

Dr. Rodwell was a recipient of the 1997 IEEE Microwave Prize, the 1998 European Microwave Conference Microwave Prize, the 2009 IEEE IPRM Conference Award, the 2010 IEEE Sarnoff Award, the 2012 Marconi Prize Paper Award, and the 2022 SIA/SRC University Research Award. Since 2024, he has been serving as an IEEE-MTT-S Distinguished Microwave Lecturer.