Antenna-Integrated and PA-Embedded Glass Substrates for D-Band InP Power Amplifier Modules

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***Abstract*—This article presents an innovative antenna-in-package (AiP) solution designed for 140-GHz indium phosphide (InP) power amplifier (PA) front-end modules. In this design, InP PAs are strategically embedded at the center of a glass substrate (AGC EN-A1) sandwiched by low-loss dielectric layers (ABF-GL102) on both sides. This arrangement facilitates ultrashort die-to-package interconnects through 20-μm dielectric vias, achieving a remarkably low simulated loss of 0.2–0.3 dB at 140 GHz and an impressive $S11/S22$ of less than −15 dB across a wide frequency range from 110 to 170 GHz. We conducted a thorough evaluation of various PA designs with two-stage and three-stage amplifying circuits embedded within this package. The findings reveal that the embedded InP PAs deliver consistent small signal gains of 11.1 dB for the two-stage and 15.8 dB for the three-stage PAs at 140 GHz, comparable with their bare die performance and other existing packaging technologies. A key feature of this design is the integration of a 5-μm-thick copper heat spreader on the PA backside, which significantly enhances thermal management. In addition, the design accommodates the seamless integration of a 1 × 8 microstrip patch antenna array. Directly connected to the PA output, this array achieves maximum broadside gains of 12.9, 25.3, and 29.7 dB for the standalone antenna, and the PA-antenna modules with two-stage and three-stage PAs at 139 GHz, respectively, over a 3-dB bandwidth of 5 GHz (136–141 GHz). Moreover, the radiation pattern of the PA-antenna module has been meticulously characterized, showcasing a 13° 3-dB *E*-plane beamwidth and 64° 3-dB *H*-plane beamwidth from the broadside. With its superior electrical and thermal performance, scalability, and cost-effectiveness, this package presents a promising solution for developing D-band beamforming arrays in next-generation communication systems.**

***Index Terms*—Antenna in package (AiP), D band, die embedding, die-to-package interconnect, glass package, indium phosphide (InP), microvia.**

I. Introduction

THE rapid advancement in high-data-rate media platforms and real-time systems has significantly increased the demand for wireless communication bandwidth to process and stream complex data instantly [1]. While the industry continues to enhance 5G technologies, researchers are shifting their focus toward the next generation of wireless communication, 6G, exploring higher spectrum bandwidths [2]. The D band (110–170 GHz) is particularly promising, due to its ample frequency bandwidth [3] making it a leading candidate for 6G wireless communication systems [4].

To overcome the high path loss at frequencies above 100 GHz, RF front-end (RFFE) modules must meet higher performance requirements. Efficient generation, transmission, and radiation of RF power are crucial to enhance long-range performance. Various IC technologies such as silicon germanium (SiGe) [5], [6], III–V [7], [8], and CMOS [9], [10] are being investigated for active devices to address these challenges in the D band. For passive components, integration methods, such as antenna-on-chip (AoC) [11] and antenna-in-package (AiP) [12], are widely used to incorporate antennas directly into RFFE modules. However, increasing frequency introduces greater parasitics, complicating the integration of active and passive devices. Amidst these diverse technologies, heterogeneous integration emerges as a potent approach to effectively combine the advantages of each technology. As demonstrated in [12], an eight-channel tile module (8 × 8 antenna array) utilizing CMOS frequency upconversion IC and indium phosphide (InP) HBT power amplifier (PA) IC is presented. However, traditional packaging, with its assembly complexities, limits electrical performance and the level of integration, which can be further enhanced by employing more advanced packaging

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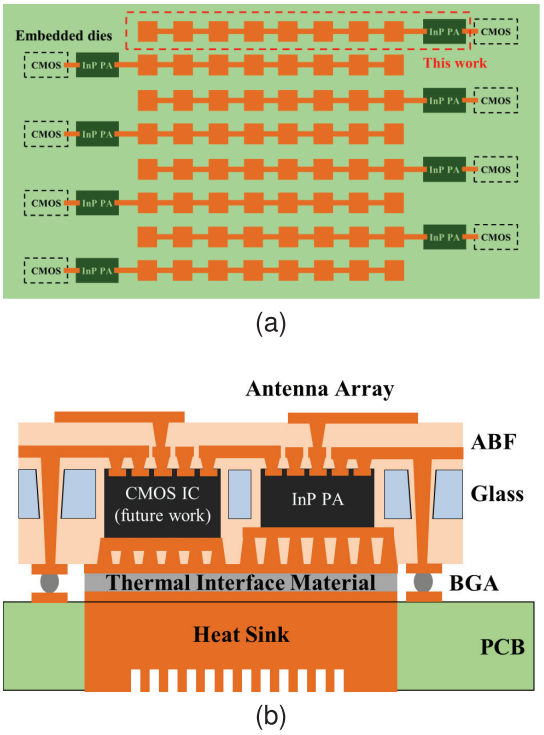

Fig. 1. (a) Top view of an eight-channel tile module with CMOS IC and InP PA embedded in the glass substrate. (b) Cross-sectional view of the die-embedded glass substrate.

approaches. The concept of building equivalent 8×8 modules utilizing an advanced die-embedded glass substrate is shown in Fig. 1(a). In this article, we demonstrate one of the PA-antenna channels using this novel packaging technology. This approach enhances electrical performance and eliminates additional assembly steps by embedding the PA directly into the substrate during fabrication.

The development of advanced packaging technology has been playing an important role in the field of high-performance computing [13], providing valuable insights for the evolution of RF packaging [14] in the aspects, such as minimizing interconnect loss and managing heat efficiently. However, adaptations are necessary to meet specific RF requirements, especially for antenna integration. Challenges also intensify at higher frequencies. At 140 GHz, the electrical performance degrades due to increased parasitic effects and restricted interconnect bandwidth. This degradation can negate some advantages of operating at these higher frequencies. Furthermore, integrating large-scale antenna arrays becomes problematic when space is limited, necessitating more sophisticated designs for antenna integration and die arrangement to achieve scalable modules. In addition, high-power PAs at these frequencies tend to produce more heat as power-added efficiency (PAE) declines, underscoring the need for effective thermal management within the packaging. Finally, cost-effectiveness is nonnegligible when choosing substrate materials that can support extensive antenna arrays at a reasonable cost for RF applications.

State-of-the-art RFIC packaging solutions for D-band modules include wire-bonding [12], flip-chip [15], and embedded wafer-level ball grid array (eWLB) packages [16]. As mentioned earlier, these packaging methods must have the ability to support integrated antennas and thermal management for the chips. Typically, the top side of the package is used for antenna patches, while the bottom facilitates electrical and thermal connections to the PCB. In the wire-bonding case, on-die pads are connected to on-package antennas via gold wires, and the die's backside is attached to the package with thermal interface material to dissipate heat. This method benefits from a simple assembly and effective thermal management, but it suffers from significant interconnect losses due to the wires. Flip-chip and eWLB options offer better electrical performance compared to wire bonding. However, managing heat in high-power PAs can be challenging with these methods due to the complexities involved in assembling heat spreaders.

Besides various integration methods, the cutting-edge substrates for D-band RF packaging also encompass a range of materials, including low-temperature co-fired ceramic (LTCC) [12], organic substrates [17], and glass substrates [15]. LTCC stands out for its excellent electrical performance due to its low-Dk and -Df characteristics [18]. In addition, its high thermal conductivity and low coefficients of thermal expansion (CTE) contribute to its popularity in RF packaging applications. However, LTCC's drawbacks include relatively large feature sizes, limited substrate sizes, and higher costs from the fabrication process. Organic substrates, on the other hand, offer favorable electrical properties and finer feature sizes, making them a prevalent choice for packaging substrates, including in D-band applications. Nonetheless, the thermal–mechanical reliability of organic substrates can be compromised due to their higher CTE and lower modulus [14]. Emerging as a promising alternative, glass substrates exhibit impressive electrical and thermal–mechanical performance. Moreover, their capability to support larger panel sizes at a reduced cost adds to their appeal. Glass-based packages have showcased significant potential in D-band RF applications [19], indicating a promising future for this technology.

Within the realm of integration technologies and substrate materials, we have been leveraging the synergies between die embedding and glass substrates to pioneer advanced solutions for D-band module packaging. The proposed module is shown in Fig. 1. In the proposed packaging concept, low-power CMOS ICs, high-power III–V PAs, and passive antenna arrays are integrated into the glass package. This proposed package contains the key elements of a D-band RFFE module as in [12]. Within the module, a pivotal interconnect in the RFFE module lies in linking PA and antenna. Departing from conventional methods like wire bonding or flip-chip, we can significantly minimize interconnect length by embedding the PA directly beneath the antenna patches, which is presented in the following sections. Previous work has showcased the feasibility of this approach and offered preliminary characterization results using passive transmission dies. By embedding PA at the substrate's center, we unlock the potential to utilize the substrate's backside for heat spreader deposition, effectively shortening the heat path from PA to onboard heat sink. With separate heat spreader and heat sink availability, the thermal crosstalk can be eliminated among different channels.

Moreover, employing low-loss dielectric layers laminated on the glass substrate ensures optimal electrical performance and thermal–mechanical reliability, facilitating scalability into larger arrays. Besides the integration of the PA-antenna module shown in this article, low-power CMOS ICs can be integrated into the package to further extend the functionality of the proposed module, which represents future work. The process compatibility for CMOS dies is demonstrated in [20] and [21], in which Si passive dies are embedded and characterized. Several other key components including the micro-via, patch antenna, and heat spreader have been demonstrated in the previous work as well [20], [22], [23].

Building upon this foundation, our recent work [24] involved embedding a 140 GHz InP PA (without antennas), marking the first functional demonstration of the PA package using glass embedding technology. The PA utilizes Teledyne's 250 nm InP HBT technology [25] and the design is similar to [8]. As a reference, PA in [8] consumes 0.52-W dc power with a size of 0.69 mm^2, leading to a heat density of 0.75 W/mm^2. The demonstration in [24] indicates the ability of die-embedded glass substrate to handle high frequency and high power PA. In this article, we extend our work by integrating the PA and antenna array with low-loss interconnects. We present the characterization of the PA-antenna module, providing unprecedented insights into the module-level performance of die-embedded glass packaging at 140 GHz.

The rest of this article is organized as follows. Section II discusses the package design, fabrication process, and fabrication results to show the technological feasibility, presenting a detailed implementation process for this novel package. Then, in Section III, following the substrate properties and design rules in the previous section, the electrical designs regarding the PA-antenna modules are presented. The measurements of the embedded PA and the PA-antenna module are also presented in this section, showcasing the performance of this technology. Section IV offers a comparison of state-of-the-art D-band RFFE modules and their packaging technologies, providing a comprehensive evaluation of the advantages and disadvantages of our approach. Finally, Section V concludes this article with a summary and final remarks.

II. Package Design and Process Development

In this section, we meticulously outline the methodology employed in utilizing a die-embedded glass substrate for 140-GHz InP PA packaging. We delve into the material properties, substrate stack-up, and the complete fabrication process flow. Furthermore, we showcase the outcomes of the package fabrication, which affirm the exceptional quality of die-embedded glass substrate fabrication process.

A. Package Stack-Up

As introduced earlier, the InP PA is embedded within the glass substrate. The top side of the substrate accommodates the antenna, and the bottom side handles thermal management. We employ an AGC EN-A1 glass substrate as core material for embedding, sandwiched with Ajinomoto Build-up Film (ABF)

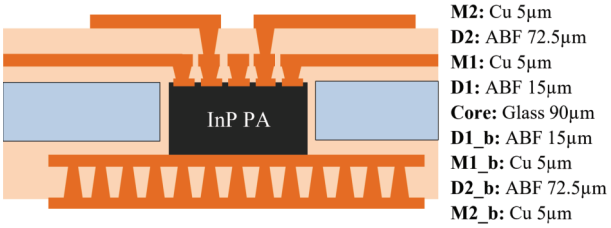

Fig. 2. Die-embedded glass substrate stack-up.

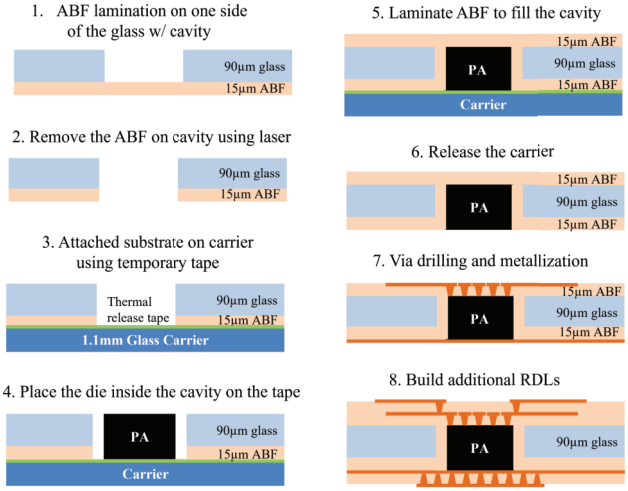

Fig. 3. Fabrication process flow of the die-embedded glass substrate.

GL102 (Dk = 3.3 and Df = 0.0044 at 5.8 GHz) on both sides, to facilitate low-loss interconnects. The electrical properties of package materials have been characterized in the D band in [26]. The embedding of InP PA involves creating through cavities in the glass substrate, allowing access to both sides of the PA. Fig. 2 displays the stack-up of the die-embedding package, centering the PA die within the glass substrate with the on-die pads oriented upward. The initial ABF layer (D1) above the glass cavity serves to fill gaps and encapsulate the die. The thicknesses of each layer are detailed in Fig. 2. Subsequently, metal layers are deposited on the substrate, and connections between the die and the package are achieved via blind/buried vias in the dielectric layers. The Cu heat spreader (M1_b) is applied to the PA's bottom side without the use of thermal interface materials. To adapt the PA package for microstrip antenna integration, an additional ABF layer (D2) is laminated on each side. The patch antenna connects through blind vias in D2, while thermal vias draw heat away from the heat spreader in the M1_b layer.

B. Process Flow

The process flow for the die-embedded package is shown in Fig. 3. A significant advantage of this die embedding process is its dual-integration capability: it utilizes the top side redistribution layer (RDL) for interconnects and antenna, while exposing the bottom side for thermal management. The preliminary process using Si dummy dies has been examined in [20]. In this work, we optimized the RDL process and

added a heat spreader process to accommodate active InP dies, providing a complete process for functional demonstration. Meanwhile, as an extension of the work done in [24], the methods shown in this work further simplify the process steps, create a shorter thermal path, and more importantly, demonstrate the antenna integration process with the active InP dies.

The process begins by forming a substrate comprising a glass core and a 15-μm ABF dielectric layer (D1_b) with through cavities. This is achieved by laminating the 15-μm ABF onto a precavitied glass core and then removing excess ABF via laser ablation (steps 1 and 2). Alternatively, cavities can be drilled through both the ABF and glass. Once the substrate is prepared, the ABF side is attached to a carrier using temporary thermal release tapes (step 3). The die is then placed face-up in the cavity's center using a die placement tool (step 4) and encapsulated by laminating another 15-μm ABF layer (D1) over it (step 5), which also fills the gaps between the embedded die and substrate.

Following encapsulation, the carrier is removed (step 6), leaving the die embedded with its bottom fully exposed for effective heat extraction via a Cu heat spreader (M1_b) added in subsequent layers. RDL construction on the top involves drilling blind vias with a laser and metallizing these vias—and the bottom heat spreader—using standard semiadditive processes (SAP) [27]. This completes the package for the InP PA with two metal layers, featuring ultrashort vias for PA-package interconnects and a Cu-coated backside for enhanced thermal management (step 7).

The two-metal layer package as step 7 successfully incorporates PA into the glass substrates. To enhance its capabilities to support the microstrip antenna array, additional RDL layers can be added to the PA-embedded glass substrate. We laminate 72.5-μm ABF layers (D2 and D2_b) on both sides. The second RDL is built using SAP as well. On the bottom side, to facilitate heat transfer from the initial heat spreader (M1_b) to the outer layer (M2_b), options include thermal vias and thermal interface materials. In this work, thermal vias are utilized as a demonstrative example as heat density has already been reduced in M1_b. The additional steps are depicted as step 8.

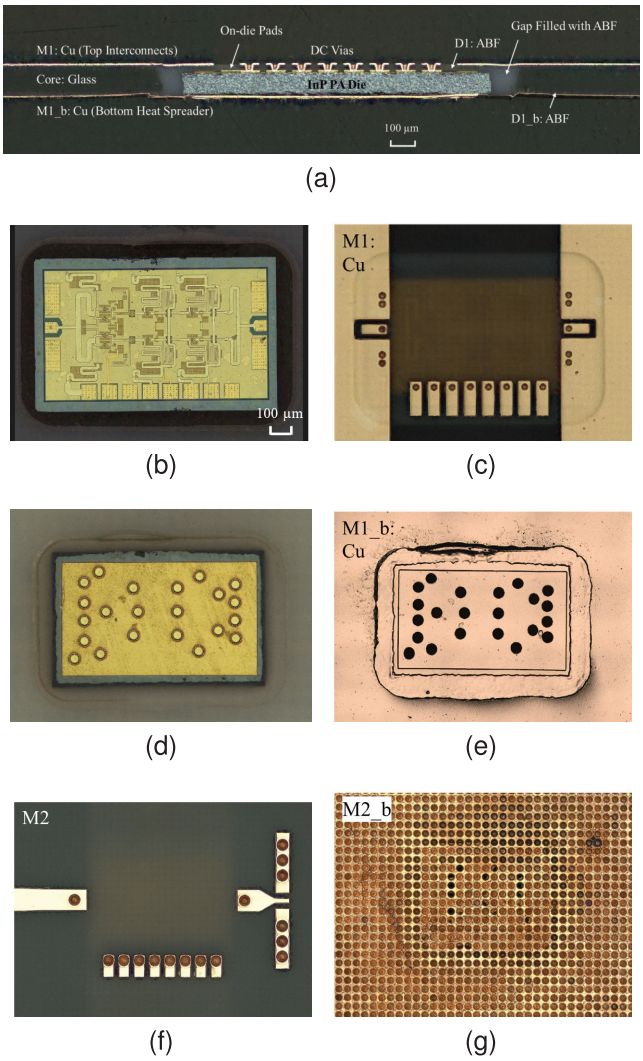

Fig. 4. Fabrication results of the die-embedded substrate. (a) Cross section of the die-embedded glass substrate. (b) PA die placed into the premade glass cavities. (c) Interconnects on the top metal layer (M1) of the substrate. (d) Backside of the embedded PA die being exposed. (e) Backside of the embedded PA die with electroplated Cu heat spreading layer (M1_b). (f) Second metal layer (M2) on the top. (g) Bottom layer M2_b and Cu-plated thermal vias in D2_b for heat spreading.

C. Fabrication Results

This section presents the fabrication results, demonstrating that the PA package meets the earlier specified requirements. Fig. 4(a) displays a cross section of the two-metal layer PA-embedded glass substrate, highlighting the vias that connect the on-die pads to the on-package pads, as well as the bottom heat spreader. The gap between the embedded die and the glass substrate is completely filled by ABF, which ensures good reliability. It is to be noted that due to the thickness difference between the embedded die and the top surface of the substrate, the actual thickness of D1 is 20 μm on top of the die, which is also reflected in the modeling in the following sections.

The top and bottom views of the internal fabrication steps are also presented. Fig. 4(b) shows the InP PAs placed inside the cavity. In Fig. 4(c), we show the placed die with ABF layer (D1) laminated on top. The on-die metal pads are still visible so the alignment of via drilling can be done on the pads to mitigate the die-shift from the placement. The top metal layer (M1) with RF and dc pads is shown in Fig. 4(c). On the bottom, the backside of the die is directly exposed as shown in Fig. 4(d). This enables the full usage of the backside for heat spreading. Fig. 4(e) shows the electroplated Cu heat spreader (M1_b) on the bottom. Fig. 4(f) shows the second metal layer (M2) including the PA input, PA-antenna transition, and the dc pads. Fig. 4(g) shows the bottom layer M2_b and Cu-plated thermal vias in D2_b to dissipate the heat from the inner heat spreading layer (M1_b).

The fabrication results confirm the viability of using dielectric blind vias to accommodate finer feature sizes (20 μm). Moreover, by integrating the PA directly into the substrate, this method eliminates the need for an additional die assembly process. Encapsulating the die within the substrate not only

streamlines production but also enhances the die's protection, significantly improving reliability.

In summary, this section presents the substrate stack-up design, the fabrication process flow, and the fabrication results of the die-embedded substrate. This technology shows significant advancements in realizing die-to-package interconnects and thermal management to address electrical and thermal challenges for 140-GHz PA modules compared to traditional packaging methods such as wire-bonding or flip-chip. The following section will provide electrical characterization to further demonstrate the performance of this technology.

III. Electrical Design and Characterization

The electrical characterization includes package loss extraction and PA-antenna module characterization. The interconnect is designed to match the input/output impedance of the InP PA (50 Ω) and realize wide bandwidth. The package loss is then extracted by comparing the PA small signal gain before/after packaging. The integrated on-package antenna array is also characterized to demonstrate the availability for building large antenna arrays for beamforming.

A. Interconnect Design

We design the die-to-package interconnect utilizing microvias. The size of these microvias is determined by the aspect ratio and the dielectric thickness. Specifically, in our design, the innermost ABF layers (D1 and D1_b) are 15-μm thickness. Due to the difference in thickness between the embedded die and the glass core, the via thickness is around 20 μm since ABF can flow and fill the thickness difference. Consequently, we utilize vias with a depth of 20 μm and diameter of 25 μm in our simulations. To facilitate the connection of the ground–signal–ground (GSG) pads on the PA, we optimize the placement of signal and ground vias using the High Frequency Structure Simulator (HFSS) to minimize interface reflections. The dimensions, layout, and simulation ports of the PA-package transition are depicted in Fig. 5(a).

An additional ABF layer is introduced to support a microstrip antenna, thereby enhancing the interconnect from the on-die GSG pads to the antenna's microstrip feeding line. This layer is laminated on the top of the first on-package metal layer, which acts as the ground for the microstrip structure. The second ABF layer has a thickness of 72.5 μm to improve the bandwidth of antenna, and features vias of the 72.5-μm diameter. The transition model and simulation ports to the microstrip are detailed in Fig. 5(b).

The simulation results for the die-to-package transitions are illustrated in Fig. 5(c) and (d). Both transitions exhibit excellent matching between the on-die pads and the on-package transmission lines, with a $S11/S22$ less than −15 dB across the frequency range of 110–170 GHz. The transition involving a single metal layer on the top side (CPW case) incurs a loss of 0.2 dB at 140 GHz, indicating superior electrical performance compared to other die-to-package interconnects. With two-metal layers on the top side (microstrip case), even if the matching condition improves ($S11/S22 <$ −20 dB from 110–170 GHz), the insertion loss increases to 0.3 dB atthe insertion loss increases to 0.3 dB at 140 GHz due to one additional dielectric layers.

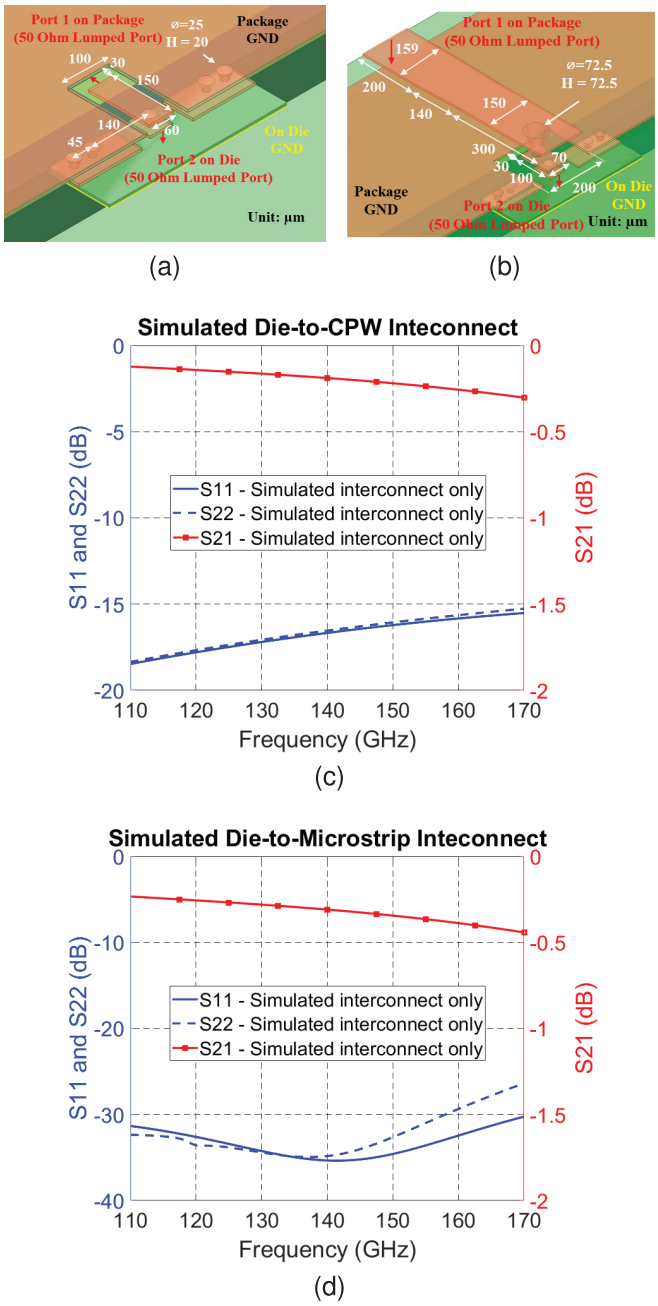

Fig. 5. Design and simulation results of the interconnects. (a) On-die GSG pad to on-package CPW interconnect. (b) On-die GSG pad to on-package microstrip interconnect. (c) Simulation results of die-to-CPW interconnect. (d) Simulation results of die-to-microstrip interconnect.

B. PA Performance

The performance of PAs is assessed both before and after packaging. This study explores two 140-GHz InP PA configurations, featuring two-stage and three-stage amplification circuits, respectively. The details of the three-stage PA design, simulation, and measurement results are presented in [8]. Given that the packaging involves only passive components, small-signal gain measurements are enough for package performance characterization. By analyzing the small signal gains of PAs before and after packaging, we can determine the gain discrepancy and estimate packaging losses. Due to

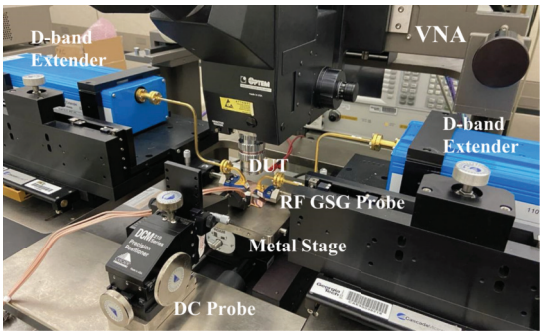

Fig. 6. Two-port setup of PA small signal gain measurement.

considerable heat generation, effective thermal management is essential during these measurements. Accordingly, the measurement setup utilized is depicted in Fig. 6. The measurements of the bare/packaged PAs are done in parallel (not the same PA) due to the handling difficulties for the singulated bare PAs during the measurement. For the bare PA, given its small size, it is attached to a thin Si wafer (200 μm) using Ag-paste for ease of handling during measurements. Therefore, it cannot be reused for packaging. This wafer is then vacuum-sealed onto the metal chuck to facilitate thermal management. The packaged PAs utilize one metal layer on top to support the CPW, as shown in Fig. 5(a). The PA-embedded substrate is vacuum sealed onto the metal chuck of the probe station, which acts as a heat sink to promote efficient contact and heat dissipation. For the measurement equipment, the small signal gain measurement is conducted by Agilent Vector Network Analyzer (E8361C) with D-band frequency extenders (V06VNA2). Two GSG RF probes with 75-μm pitches (Cascade Infinity 170-S-GSG-75-BT) are used for the RF input and output. The dc bias signal, we use GGB multicontact wedge with decoupling capacitors on the probes.

The small signal S-parameter measurement results is shown in Fig. 7(a) and (b). We use the same dc bias condition for three-stage PAs as in [8] for S-parameter measurement. For two-stage PAs, the bias condition of the first stage stays the same, while the second stage I_{CC2} increases to 60 mA. As for the matching at the PA input/output, the bare PAs and packaged PAs show similar levels of matching conditions ($S11/S22$). This indicates that package does not introduce additional mismatch at the input/output and the package-to-die interconnects have low parasitics and realized wide band matching as the simulation results in the previous subsection. As for the small signal gain results, the embedded InP PAs deliver small signal gains of 11.1 dB for the two-stage and 15.8 dB for the three-stage PAs at 140 GHz, comparable with the bare die performance of 12.9 dB for two-stage bare PA and 18.4 dB for three-stage bare PA. The gain difference extraction is shown in Fig. 7(c). This figure shows gain differences of 1.8 and 2.6 dB for two-stage and two-stage cases, respectively. It should be noted that the gain difference includes both input and output interconnects. Therefore, the loss per interconnect is only half of the gain difference, which are 0.9 and 1.3 dB per interconnect. Moreover, since we use different PAs for before and after packaging measurement, performance variation of the die itself might also affect the extracted difference. Nevertheless, such performance is still comparable to the wire bonding or flip-chip interconnects and can be further improved by a more optimized chip-package co-design process.

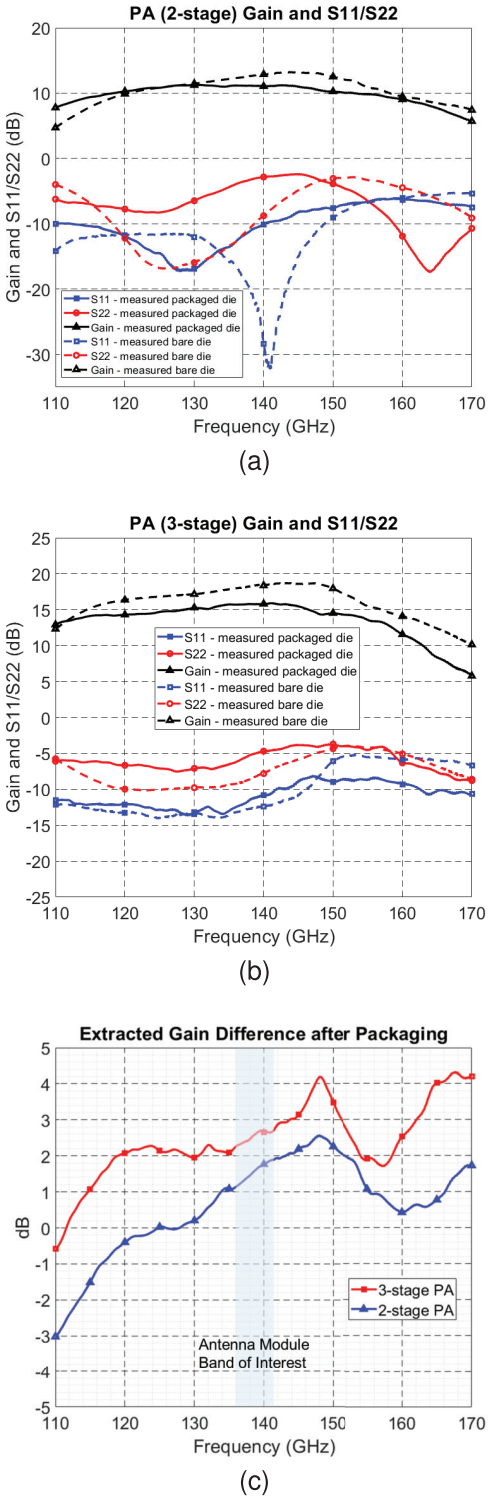

Fig. 7. (a) Measurement results of bare PAs and packaged PAs. (a) Two-stage PA before and after packaging. (b) Three-stage PA before and after packaging. (c) Extracted gain difference after packaging.

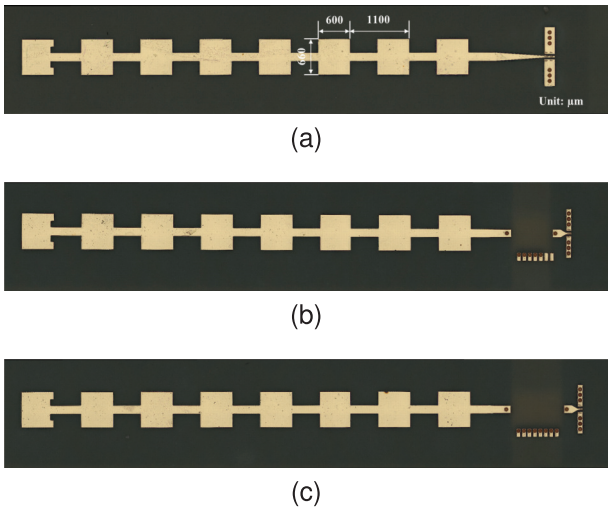

Fig. 8. Antenna modules with (a) no PA connected, (b) two-stage PA connected, and (c) three-stage PA connected.

C. Antenna Module Measurement

In this article, we introduce the capabilities of the die-embedded glass substrate through the presentation of D-band PA-antenna module measurements for the first time. A 1×8 series-fed patch antenna array, similar to the one described in [20], is utilized on the glass substrate to form a single-channel array in [12] within the PA-antenna module. The series-fed antenna array is designed and optimized using the methods in [22], [28], and [29]. The microstrip interconnects as Fig. 5(b) are used for the PA to antenna interconnect. Therefore, both the PA output and the antenna input are matched to 50 Ω, ensuring optimized impedance matching. In the PA-antenna module characterization, we examine three cases which include an antenna without PA, an antenna module with two-stage PA, and an antenna module with three-stage PA. The pictures of the antenna modules are shown in Fig. 8(a)–(c).

The measurements encompass both broadside gain and radiation pattern assessments. The broadside gain measurement evaluates the overall realized gain of the PA-antenna module in comparison to the standalone antenna. Meanwhile, the radiation pattern measurement assesses how minimally the module impacts the antenna's pattern while maintaining a comparable radiation angle.

The setup for the broadside gain measurement is depicted in Fig. 9. Based on the two-port PA measurement configuration described earlier, a fixed horn antenna with a known gain is connected to one port, while the antenna module is fed through the same probe used for the PA measurement at the other port. The horn antenna is aligned to face the broadside of the patch antenna at a far-field distance. The distance between the patch antenna and horn antenna is around 14 mm, exceeding the far-field distance requirement as calculated in [30], which has a similar setup. The Friis transmission equation is utilized to derive the gain of the antenna. The calibration process of a similar setup is described in [30]. The measurement results for the antenna alone, as well as the antenna combined with two-stage and three-stage PAs, are presented in Fig. 10(a). The $S11$

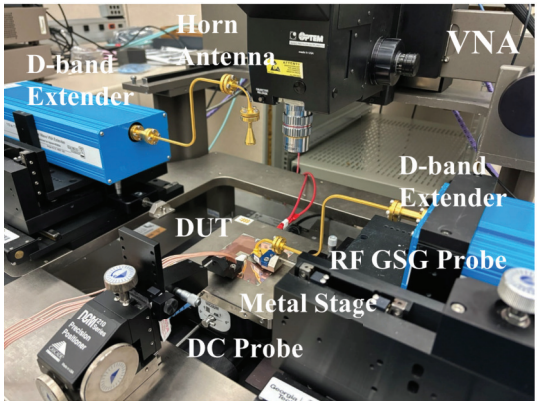

Fig. 9. Broadside gain measurement of antenna modules.

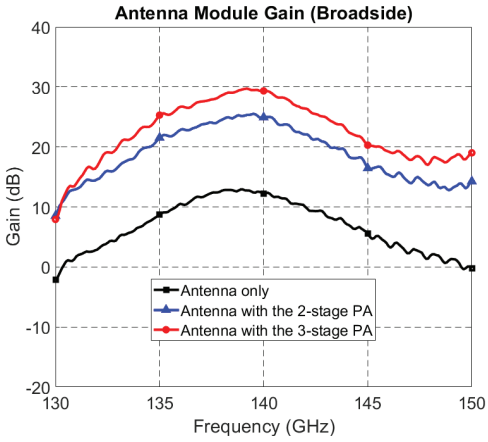

Fig. 10. Gain and $S11$ measurement results of the antenna. (a) Broadside gain of the standalone antenna, antenna modules with two-stage and three-stage PAs. (b) $S11$ of the standalone antenna, antenna modules with two-stage and three-stage PAs.

measurement results for all three configurations indicate $S11$ values below −10 dB at the antenna and PA inputs within the bandwidth, confirming efficient signal delivery to the antenna modules. The broadside gain results reveal maximum gains of 12.9 dB for the antenna without PA, 25.3 dB with a two-stage

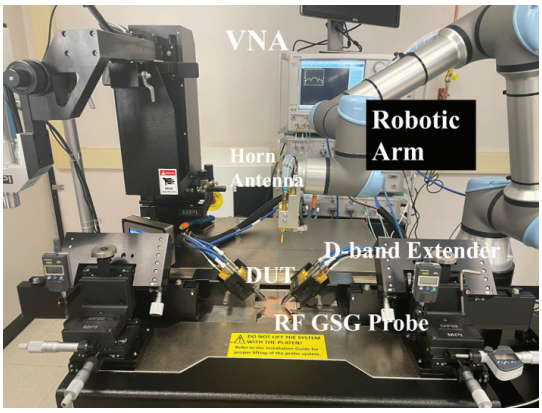

Fig. 11. Radiation pattern measurement of antenna modules.

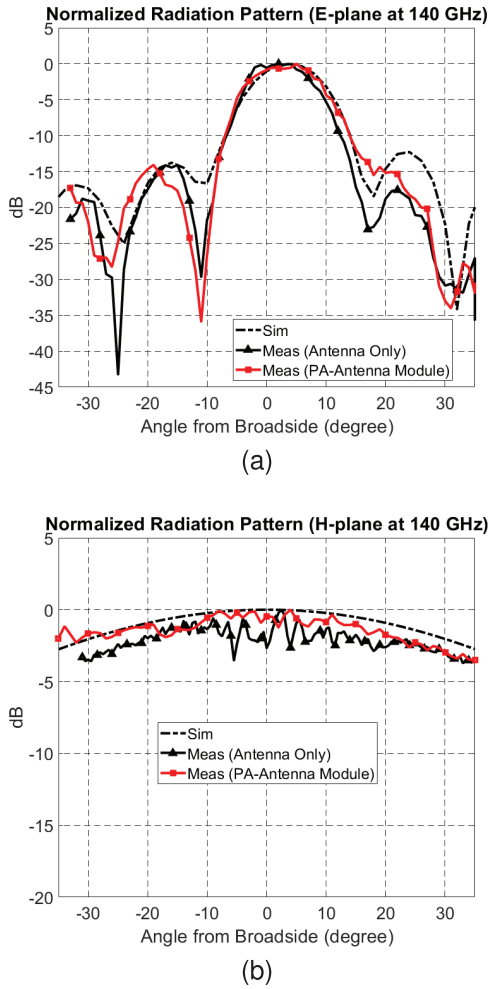

Fig. 12. Simulation and measurement results of the normalized radiation pattern of antenna modules. (a) *E*-plane at 140 GHz. (b) *H*-plane at 140 GHz.

PA, and 29.7 dB with a three-stage PA. The 3-dB bandwidth of antenna modules is from 136–141 GHz. These results also show comparable bandwidth and transmission frequency responses, suggesting that the wideband on-package interconnect between PA and antenna presented in Section III-A is not a limiting factor for the module's performance. A formula based on cascade network *S*-parameter [31] shows the $S21$ of PA-antenna module in (1). By realizing good matching between PA and package, we improve the $S21$ and reduce $S22$ of the packaged PA; therefore, we improve the $S21$ of the overall module

$$S21_{module} = \frac{S21_{PA}S21_{antenna}}{1 - S22_{PA}S11_{antenna}}. \quad (1)$$

Radiation pattern measurements are also conducted to assess the antenna modules. We evaluated the radiation patterns of a 1×8 microstrip patch antenna, both alone and combined with a two-stage PA, to compare their performances. The setup for these measurements is illustrated in Fig. 11. The antenna module inputs are fed through a D-band probe, while a horn antenna, mounted on a rotating arm, captures the radiated signals. This horn antenna connects to a frequency extender. Measurements are made by conducting two-port tests at various angles, and the results for the *E*-plane and *H*-plane are displayed in Fig. 12(a) and (b), respectively. The antenna achieved *E*-plane and *H*-plane 3-dB beamwidth of 13° and 64°, respectively. In addition, the radiation pattern of the antenna module integrated with the two-stage PA maintained a consistent pattern similar to the standalone antenna array. In the antenna measurement setups of Figs. 9 and 11, although absorbers are not present to suppress multipath interference, reflections from metal objects in the test system are partially suppressed by the directivity of the receiving horn antenna. Evidence of only small multipath interference in these measurements is shown in Fig. 10(a), where only a small frequency ripple is observed, and in Fig. 12(a), where the measurements conform closely with simulations except at large angles from broadside. The deviation in the patterns of Fig. 12(a) at large angles from the broadside may be due to reflections from the test apparatus. These results demonstrate that integrating the PA with the antenna module does not degrade antenna radiation performance. Leveraging the superior electrical properties of the die-embedded glass substrate, this technology holds significant promise for using this single 1×8 antenna array to develop large-scale beamforming arrays for 6G applications.

In summary, our study provides a detailed electrical design and performance evaluation of a die-embedded glass substrate based on the D-band InP PA package and antenna module. Our functional demonstration highlights that this innovative packaging technology successfully accommodates advanced D-band RFIC technologies, enabling the realization of fully functional modules, and successfully improving the matching at the PA-package interface. This work contributes valuable knowledge to both the fields of RFFE modules and advanced packaging, paving the way for the advancement of state-of-the-art D-band RF modules.

IV. Comparison

We have validated the performance of the die-embedded glass substrate through the characterization of both PA and combined PA-antenna module. This section presents a detailed comparison, as shown in Table I, which highlights the advancements of this packaging technology over state-of-the-art D-band modules/packages. Our comparative analysis encompasses the realization methods, electrical performance, and thermal management. Notably, accurate extraction of the

TABLE I
COMPARISON AMONG PACKAGED D-BAND RFFE MODULES

	[32] TMTT 2024	[33] TMTT 2023	[34] TMTT 2024	[35] ISSCC 2022	[12] TMTT 2023	**This work**
Package Material	PCB (Astra)	PCB (Megtron)	PCB	Glass Substrate	LTCC	**Glass Core & ABF**
RFIC Technology	45nm RFSOI CMOS	55nm SiGe BiCMOS	45nm RFSOI CMOS	130nm SiGe BiCMOS	22FD-SOI CMOS + InP HBT	**InP HBT**
RFIC Assembly	Flip-chip	Flip-chip	Flip-chip	Flip-chip	Flip-chip (CMOS) + Wirebonding (InP)	**Substrate Embedding (No Assembly)**
Antenna Integration	Patch antenna on PCB + Flat lens (PCB)	Patch antenna on PCB	Patch antenna on PCB	Patch antenna on glass	1×8 microstrip patch antenna on LTCC	**1×8 microstrip patch antenna on glass**
Antenna/Module Performance	25 dBi gain of patch antenna + flat lens	14 dBi measured gain of 16-element antenna array	44 dB of TX array (8×8) EIRP gain	30.3 dBi simulated gain of 16×16 antenna array	36 dB measured single sideband conversion gain of CMOS upconversion IC + InP PA + 1×8 patch antenna module	**29.7 dB measured gain of InP PA + 1×8 patch antenna module**
System/module size	80 mm × 57 mm for overall area	6.25 mm × 6.25 mm for antenna array	N/A	34 mm × 43 mm for entire glass interposer	12 mm × 33 mm for LTCC carrier	**11 mm × 1.1 mm area for PA + 1×8 patch antenna**
Thermal Management	N/A	Thermal interface material	External thermal pad	Heat sink (details not shown)	Silver-filled epoxy	**Direct electro-plated Cu layer**
Package Interconnect Loss	2 dB (Sim)	0.3 dB for bumps	N/A	N/A	2.6 dB (Sim)	**0.2 - 0.3 dB (Sim) & 0.9 - 1.3 dB (Meas)**
Package Bandwidth (PA only w/o antenna)	N/A	N/A	N/A	N/A	10 GHz (Sim)	**60 GHz (Sim)**

exact package loss is relatively difficult in the system. Therefore, some of the packaging losses are estimated by simulation. Key advantages of the die-embedded glass substrate include the following.

1) The capability for ultrashort on-package interconnects with well-controlled geometries, which enhance electrical performance and offer substantial optimization opportunities.
2) An integrated heat spreader that effectively minimizes thermal resistance between the PA and the onboard heatsink, ensuring robust thermal management.
3) The use of a glass substrate with a tailor-adjustable coefficient of thermal expansion (CTE) facilitates the realization of large-scale systems, improving both reliability and cost-effectiveness.

These features position our technology as a superior choice for next-generation systems, underscoring its potential in high-performance applications.

V. CONCLUSION

This article has presented a novel AiP solution designed for 140-GHz InP PA modules. The innovative design involves embedding InP PAs within a glass substrate (AGC EN-A1), surrounded by low-loss dielectric layers (ABF-GL102). This configuration facilitated ultrashort die-to-package interconnects using 20-μm dielectric vias, achieving 0.2–0.3-dB simulated loss at 140 GHz and a less than −15-dB $S11/S22$ from 110 to 170 GHz. Thermal management was enhanced by integrating a 5-μm-thick copper heat spreader on the PA backside. Our comprehensive evaluation of various PA designs within this package demonstrated that the embedded InP PAs achieved small signal gains of 11.1 dB for two-stage and 15.8 dB for three-stage configurations at 140 GHz. In addition, the package supports the integration of a 1×8 microstrip patch antenna array directly connected to the PA output, which provided maximum broadside gains of 12.9, 25.3, and 29.7 dB for the antenna, two-stage, and three-stage PA-antenna modules, respectively. The antenna's radiation pattern featured 13° 3-dB E-plane beamwidth and 64° 3-dB H-plane beamwidth from the broadside. With its novel implementation, superior electrical and thermal performance, along with scalability and cost-effectiveness, this package offers a compelling solution for developing D-band beamforming arrays in next-generation communication systems.

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