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Single-stage G-band HBT Amplifier with 6.3 dB Gain at 175 GHz

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***Abstract* — We report a single-stage tuned amplifier that exhibits a peak small signal gain of 6.3 dB at 175 GHz. The amplifier was designed in a transferred-substrate InP-based HBT technology that has exhibited record values of extrapolated f_{max}. The gain-per-stage of the amplifier is amongst the highest reported in any transistor technology in this frequency band.**

I. Introduction

Submicron device scaling has made transistor-based electronics in the 140-220 GHz (G-band) frequency range realizable. Applications at these frequencies include: remote atmospheric sensing, wideband communication systems, and automotive radar. Multi-stage G-band amplifiers with large small-signal gains have been reported in InP-based HEMT technologies, where electron beam lithography was used to define submicron gate lengths. State-of-the-art HEMT results include: a 3-stage amplifier with 30 dB gain at 140 GHz [1], a 3-stage amplifier with 12-15 dB gain from 160-190 GHz [2], and a 6-stage amplifier with 20 ± 6 dB from 150-215 GHz [3].

In [4], we reported the first tuned HBT amplifier in the 140-220 GHz band. The single-stage amplifier exhibited a peak gain of 3.0 dB at 185 GHz. In this work, improved device performance has resulted in an amplifier with better than twice the gain. The gain-per-stage of the present result is amongst the highest reported from any transistor technology in this frequency band.

InGaAs/InAlAs transferred-substrate HBTs have demonstrated record extrapolated RF figures of merit, $f_\tau > 295$ GHz and $f_{max} > 1$ THz [5,6], when emitter and collectors are scaled to submicron dimensions. Previous amplifiers designed in this technology have included: an 80 GHz traveling-wave amplifier with 11.5 dB mid-band gain [7], Darlington and f_τ-doubler resistive feedback amplifiers with 18 dB gain and > 50 GHz bandwidth and 8.2 dB gain and 80 GHz bandwidth, respecitvely [7], and tuned W-band power amplifiers delivering 10 dBm at 78 GHz [9]. Here, we demonstrate the potential for an ultra-low parasitic HBT technology to compete with HEMTs in submillimeter wave tuned-circuit applications.

II. Transferred-Substrate HBT Technology

By providing access to both sides of the device epitaxy, the transferred-substrate process allows for scaling of both the emitter and collector stripe widths. Using this novel processing technique, the collector-base capacitance (C_{cb}) is determined by the area of the collector contact, and not by the area of the base mesa as in a traditional mesa HBT. High values of transistor power-gain cutoff frequency (f_{max}) can be obtained by aggressively scaling the emitter and collector widths to submicron dimensions.

A. Growth and Fabrication

Details of the transferred-substrate process and device layer structure can be found in [10]. A brief overview of the technology will be provided here.

The HBT layer structure has a single InAlAs/InGaAs heterojunction and is grown by molecular beam epitaxy on a semi-insulating InP substrate. A 40 nm base layer is p+ Be doped at 5×10^{19} cm^{-3}, and includes approximately 50 meV of compositional grading to reduce base transit time. In this work, the InGaAs collector was 300 nm thick.

Prior to substrate transfer, the HBT fabrication process is similar to that of a traditional mesa-HBT. Technology features include: self-aligned base contacts, polymide device passivation, two levels of metal interconnects, MIM capacitors, and NiCr resistors.

After the definition of the final interconnect layer, a spin-on-polymer, benzocyclobutene (ε_r=2.7), is spun onto the wafer and serves as the microstrip transmission line dielectric. Vias are dry-etched in the BCB, and the BCB is simultaneously etched back to a final thickness of 5 μm. A gold ground plane is electroplated on the BCB surface. The InP wafer is then mechanically bonded to a GaAs carrier wafer with the ground plane at the GaAs wafer surface. A selective HCl etch removes the InP substrate revealing the collector epitaxy. Collector contacts can then be defined over the devices. In this work, electron beam lithography was used to define the emitter and collector stripes. A cross-section of the transferred-substrate technology is shown in Fig. 1.

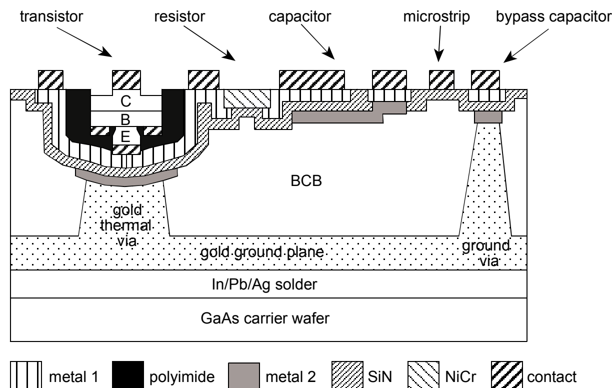

Fig. 1. Schematic cross-section of transferred-substrate HBT process.

B. Device Results

The transistor used in the amplifier design had an emitter junction area of 0.4 μm x 6 μm, and a collector stripe of 0.7 μm x 6.4 μm. Devices of that geometry have typical DC small signal current gains, β, of 20, and common-emitter breakdown voltages, BV_{CEO}, of 1.5 V at a current density of 10^5 A/cm^2.

Fig. 2 shows the unilateral power gain (U), the maximum stable gain (MSG), and the short circuit current gain (h_{21}) for a transistor measured from 6-45 GHz and 140-220 GHz. The device was biased at I_c = 4.8 mA, and V_{ce} = 1.2 V. The bias conditions are identical to those used in the measured amplifier.

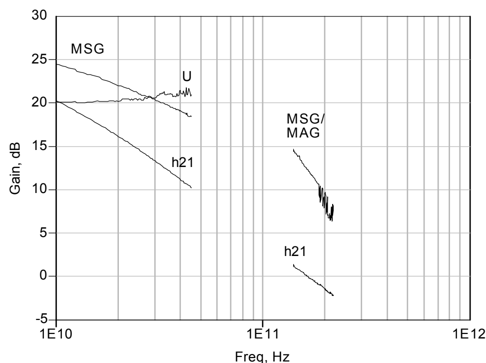

Fig. 2. HBT current gain (H21), maximum stable power gain (MSG) and unilateral power gain (U), measured in the DC-45 GHz and 140-220 GHz bands.

The unilateral power gain is not plotted in the 140-220 GHz band. The measurement of U at these frequencies is extremely sensitive to small measurement variations, and measurements in this band showed large spurious variations. Extrapolating at 20 dB/decade from the low frequency measurement of U, predicts an f_{max} ~ 500 GHz; however, this estimate may be low since U does not appear to be rolling off at 45 GHz. The current-gain cutoff frequency (f_T) of the device was measured to be 165 GHz.

Devices with improved on-wafer calibration structures have since been fabricated. Power gain measurements of these devices in the 140-220 GHz band show more consistent behaviour, and confirm the high available gain from the devices in this band. These results will be reported at a later date.

III. AMPLIFIER DESIGN

The amplifier employed a simple common-emitter topology. Shunt-stub tuning at the input and output of the device was used to conjugately match the transistor at the intended design frequency of 200 GHz. A shunt resistor at the output was used to ensure low frequency stability, and a quarter-wave line to a radial stub capacitor bypassed the resistor at the design frequency. Bias T's built into the on-wafer probes provided DC bias to the input and output of the amplifier. A chip photograph of the fabricated amplifier is shown in Fig. 3.

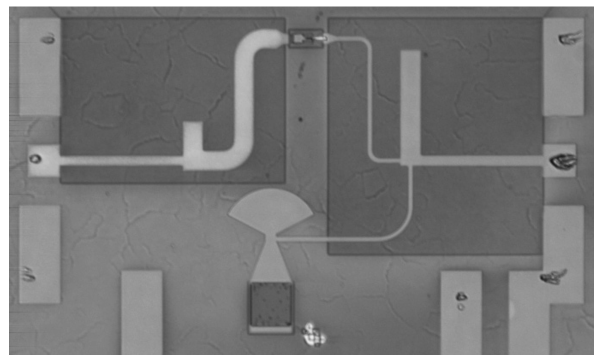

Fig. 3. Chip photograph of fabricated amplifier. Dimensions 690 μm x 350 μm.

The amplifier was designed using a hybrid-pi transistor model developed from an earlier generation e-beam lithography device [5]. The model was developed from on-wafer S-parameter measurements from 1 to 50 GHz and 75 to 110 GHz and extrapolated to the design frequency.

The circuit was designed using Agilent's Advanced Design System software. A planar electromagnetic simulator was used to model the resistor/radial stub network and any microstrip discontinuities in the circuit. Standard microstrip CAD models were used to model the remaining transmission lines in the circuit.

A test structure of the input and output matching networks cascaded together without an active device was included on-wafer to verify the accuracy of the passive element models. The measured and modeled S-parameters of this test structure are shown in Fig. 4.

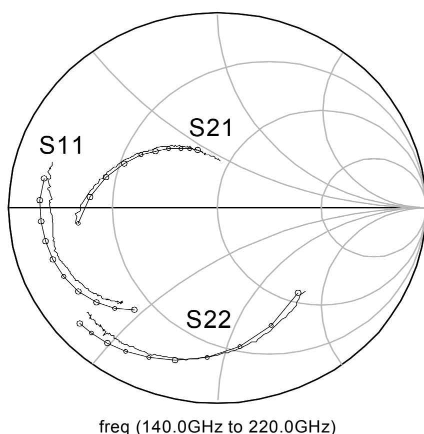

Fig. 4. Measured (solid) and modeled (circle) S-parameters of matching network test structure.

The good agreement between the measured and modeled results verifies the passive element design. The accuracy of the microstrip models at such high frequencies is attributed in part to the thin BCB dielectric substrate provided in the transferred substrate process. The thickness of the substrate (5 µm) was selected to provide a low inductance wiring environment for densely packed mixed-signal IC applications. Additionally, the thin dielectric improves thermal heat-sinking and provides low inductance access to the backside ground plane. For high frequency tuned-circuit applications, it was found that these advantages are mitigated by the high resistive losses incurred in the transmission line matching networks. Simulation of the circuit with lossless transmission lines resulted in a 2.0 dB increase in the gain.

IV. Results

The amplifier was measured on-wafer from 140-220 GHz. The measurements were made using an HP8510C Vector Network Analyzer (VNA) with Oleson Microwave Labs Millimeter Wave VNA Extensions. The test set extensions are connected to GGB Industries coplanar wafer probes via a short length of WR-5 waveguide. The waveguide has enough flexibility to allow the probes sufficient range of motion (>2mm) for on-wafer testing. The device and amplifier measurements were calibrated on-wafer using Thru-Reflect-Line calibration standards.

Fig. 5 shows the measured gain, and input and output return loss of the amplifier. The bias conditions for the transistor were V_{CE} = 1.2 V, and I_C = 4.8 mA. The amplifier was found to have a peak gain of 6.3 dB at 175 GHz, with a gain of better than 3 dB from 140 to 190 GHz. Both the input and output return loss were better than 10 dB at 175 GHz.

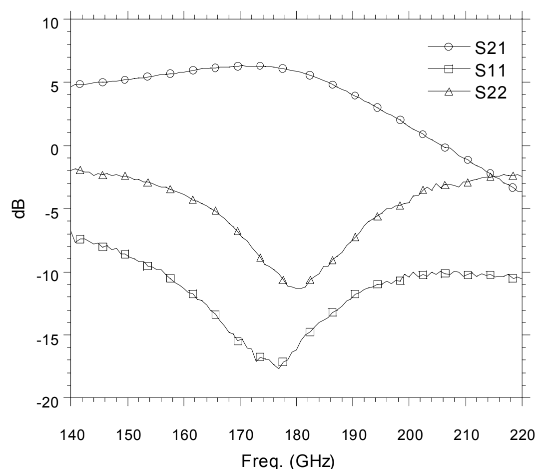

Fig. 5. Measured S-parameters of single-stage amplifier.

Simulations of the amplifier using the hybrid-pi transistor model predicted a peak gain of 6.5 dB at 200 GHz. The downward shift in the peak gain has been attributed to the transistor model used for the design. While measurements of a matching network test structure showed good agreement with the passive element models, S-parameter measurements of individual transistors in the 140-220 GHz band showed poor agreement with the hybrid-pi model used to design the amplifier. When the measured transistor S-parameters were used in circuit simulations in place of the model, the simulations showed close agreement with the measured amplifier results. Fig. 6 shows the measured gain of the amplifier and the results from circuit simulations using measured transistor S-parameters.

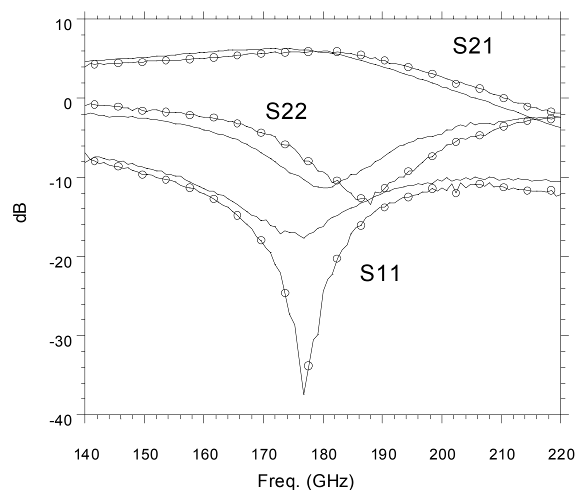

Fig. 6. S-parameters of measured amplifier (solid line) and simulated amplifier using measured transistor S-parameter model (circles).

The measured device S-parameters did show good agreement with the hybrid-pi transistor model at lower frequencies. To develop the model, transistors were measured at a variety of bias conditions in the DC-50 GHz and 75-110 GHz bands. The measured Y-parameters are analyzed to extract the bias dependent parameters, such as the transconductance, and base and collector transit times, and the bias indepent terms, such as the extrinsic emitter resistance. The values of the extracted parameters are found be consistent with those expected from the physical properties of the device.

A hybrid-pi model thus derived from 6-45 GHz measurements of a device on the current wafer showed poor agreement with the measured S-parameters of the same device in the 140-220 GHz band. The measured and modeled S11 and S22 of this device in both bands are shown in Fig. 7. The poor agreement in the higher frequency band points to a weakness in extending the simple hybrid-pi model to these frequencies. At the time of this writing, the source of the discrepancies had not been determined.

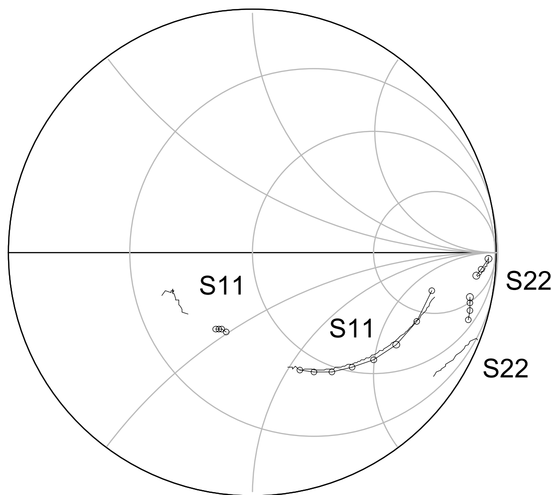

Fig. 7. S-parameters of device measurements (solid lines) and simulations of hybrid-pi model (circles) from 6-45 GHz and 140-220 GHz.

Developing an accurate device model is necessary to better understand transistor operation at these and higher operating frequencies. However, measured device S-parameters may be used for future submillimenter wave circuit designs, provided device dimensions are selected from the current library of measured transistors. Using this approach, multi-stage amplifiers are currently being developed.

V. CONCLUSIONS

We have presented a single-stage HBT tuned amplifier in an ultra-low parasitic transferred-substrate HBT technology. The amplifier exhibited a peak gain of 6.3 dB at 175 GHz. Future submillimter wave ICs being deveoloped in the transferred-substrate technology inculde oscillators and multi-stage amplifiers.

ACKNOWLEDGEMENT

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REFERENCES

[1] C. Pobanz, M. Matloubian, M. Lui, H.-C. Sun, M. Case, C.M. Ngo, P. Janke, T. Gaier, and L. Samoska, "A high gain D-band InP HEMT amplifier," *IEEE Journal of Solid State Circuits*, vol. 34, no. 9, September 1999.

[2] R. Lai, M. Barsky, R. Groundbacher, P.H. Liu, T.P. Chin, M. Nishimoto, R. Elmajarian, R. Rodriguez, L. Tran, A. Gutierrez, A. Oki, and D. Streit, "InP HEMT amplifier development for G-band (140-220 GHz) applications," *Proceedings 2000 International Electron Devices Meeting,* Dec., San Francisco, CA.

[3] S. Weinreb, T. Gaier, R. Lai, M. Barsky, Y. C. Leong, and L. Samoska, "High-gain 120-215-GHz MMIC amplifier with integral waveguide transitions," *IEEE Microwave and Guided Wave Lett.*, vol. 9, no. 7, July 1999.

[4] M. Urteaga, D. Scott, T. Mathew, S. Krishnan, Y. Wei and M. Rodwell, "185 GHz Monolithic Amplifier in InGaAs/InAlAs Transferred-Substrate HBT Technology," *Proceedings 2001 IEEE MTT-S,* May, Pheonix, AZ.

[5] Q. Lee, S. C. Martin, D. Mensa, R. P. Smith, J. Guthrie, S. Jaganathan, Y. Betser, T. Mathew, S. Krishan, L. Samoska, ans M. Rodwell, "Submicron transferred-substrate heterojunction bipolar transistors with greater than 1 THz f_{max}," *Proceedings 1999 IEEE Device Research Conference,* June, Santa Barbara, CA.

[6] Y. Betser, D. Scott, D. Mensa, S. Jaganathan, T. Mathew and M. Rodwell, "InAlAs/InGaAs HBTs with Simultaneously High values of Ft and Fmax for mixed analog/digital applications" *IEEE Elect Dev. Lett*, vol. 22, No 2, Feb. 2001.

[7] S. Krishnan, S. Jaganathan, T. Mathew, Y. Wei, M. Rodwell, "Broadband HBT amplifiers", *Proceedings, IEEE Cornell Conference on High Speed Electronics,* June 2000.

[8] J. Guthrie, M. Urteaga, D. Scott, D. Mensa, T. Mathew, Q. Lee, S. Krishnan, S. Jaganathan, Y. Betser and M. Rodwell, "HBT MMIC 75GHz and 78GHz power amplifiers," *Proceedings 12th Intl. Conf. On Indium Phosphide and Related Materials,* May 2000.

[10] M. Rodwell, Q. Lee, D. Mensa, J. Guthrie, Y. Betser, S.C. Martin, R.P. Smith, S. Jaganathan, T. Mathew, P. Krishnan, C. Serhan, and S. Long, "Transferred-Substrate Heterojunction Bipolar Transistor Integrated Circuit Technology," *Proceedings 1999 Indium Phosphide and Related Materials Conference,* May.

2001 GaAs IC Symposium, Baltimore, Maryland, October 21-24.